

## 2.5V or 3.3V, 200MHz, 11 Output Zero Delay Buffer

### Features

- Output frequency range: 16.67MHz to 200MHz
- Input frequency range: 16.67MHz to 200MHz
- 2.5V or 3.3V operation
- Split 2.5V/3.3V outputs
- $\pm 2\%$  max Output duty cycle variation
- 11 Clock outputs: Drive up to 22 clock lines
- LVCMOS reference clock input
- 125-pS max output-output skew
- PLL bypass mode
- Spread Aware™
- Output enable/disable
- Pin compatible with MPC9352 and MPC952
- Industrial temperature range:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- 32-Pin 1.0mm TQFP & LQFP Packages

### Functional Description

The PCS5I9352 is a low voltage high performance 200MHz PLL-based zero delay buffer designed for high speed clock distribution applications.

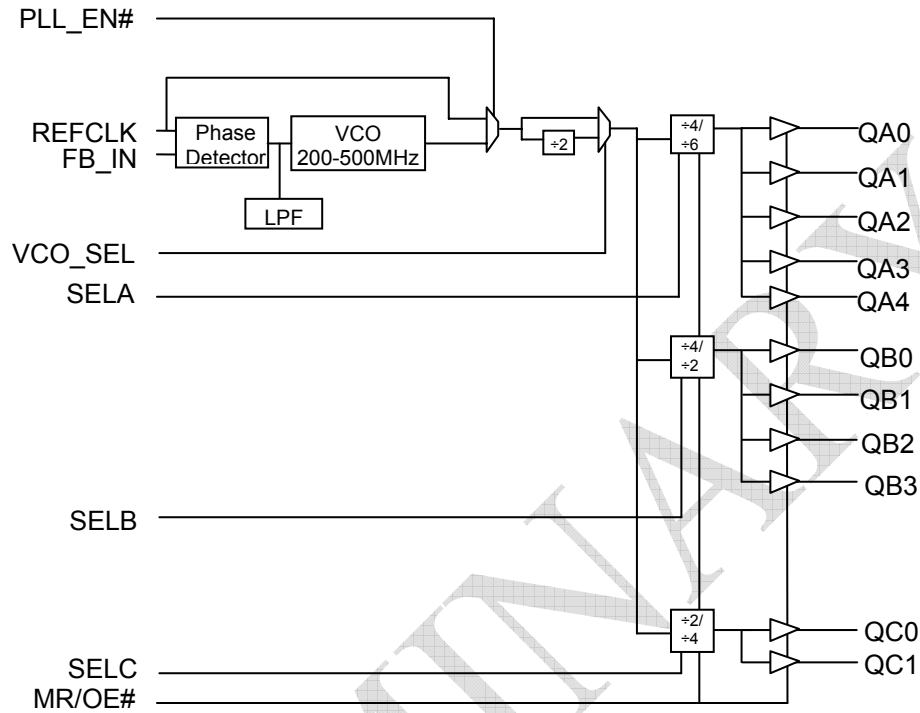
The PCS5I9352 features an LVCMOS reference clock input and provides 11 outputs partitioned in 3 banks of 5, 4, and 2 outputs. Bank A divides the VCO output by 4 or 6 while Bank B divides by 4 and 2 and Bank C divides by 2 and 4 per SEL(A:C) settings, see Table 2. These dividers allow output to input ratios of 3:1, 2:1, 3:2, 1:1, 2:3, 1:2, and 1:3. Each LVCMOS compatible output can drive 50 $\Omega$  series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces giving the device an effective fanout of 1:22.

The PLL is ensured stable given that the VCO is configured to run between 200MHz to 500MHz. This allows a wide range of output frequencies from 16.67MHz to 200MHz. For normal operation, the external feedback input, FB\_IN, is connected to one of the outputs. The internal VCO is running at multiples of the input reference clock set by the feedback divider, see Table 1.

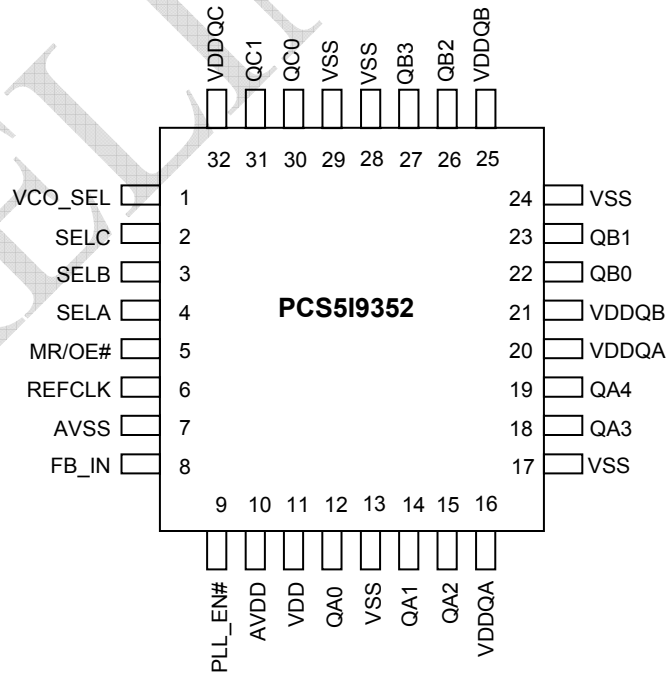
When PLL\_EN# is HIGH, PLL is bypassed and the reference clock directly feeds the output dividers. This mode is fully static and the minimum input clock frequency specification does not apply.

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Block Diagram



Pin Configuration



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Pin Configuration<sup>1</sup>

Pin	Name	I/O	Type	Description
6	REFCLK	I, PD	LVC MOS	Reference clock input.
12, 14, 15, 18, 19	QA(0:4)	O	LVC MOS	Clock output bank A.
22, 23, 26, 27	QB(0:3)	O	LVC MOS	Clock output bank B.
30, 31	QC(0,1)	O	LVC MOS	Clock output bank C.
8	FB_IN	I, PD	LVC MOS	<b>Feedback clock input.</b> Connect to an output for normal operation. This input should be at the same voltage rail as input reference clock. See <i>Table 1</i> .
1	VCO_SEL	I, PD	LVC MOS	<b>VCO divider select input.</b> See <i>Table 2</i> .
5	MR/OE#	I, PD	LVC MOS	<b>Master reset/output enable/disable input.</b> See <i>Table 2</i> .
9	PLL_EN#	I, PD	LVC MOS	<b>PLL enable/disable input.</b> See <i>Table 2</i> .
2, 3, 4	SEL(A:C)	I, PD	LVC MOS	<b>Frequency select input, Bank (A:C).</b> See <i>Table 2</i> .
16, 20	VDDQA	Supply	VDD	<b>2.5V or 3.3V power supply for bank A output clocks.</b> <sup>2,3</sup>
21, 25	VDDQB	Supply	VDD	<b>2.5V or 3.3V power supply for bank B output clocks.</b> <sup>2,3</sup>
32	VDDQC	Supply	VDD	<b>2.5V or 3.3V power supply for bank C output clocks.</b> <sup>2,3</sup>
10	AVDD	Supply	VDD	<b>2.5V or 3.3V power supply for PLL.</b> <sup>2,3</sup>
11	VDD	Supply	VDD	<b>2.5V or 3.3V power supply for core and inputs.</b> <sup>2,3</sup>
7	AVSS	Supply	Ground	<b>Analog ground.</b>
13, 17, 24, 28, 29	VSS	Supply	Ground	<b>Common ground.</b>

Note: 1. PD = Internal pull-down.

2. A 0.1µF bypass capacitor should be placed as close as possible to each positive power pin (<0.2"). If these bypass capacitors are not close to the pins their high frequency filtering characteristics will be cancelled by the lead inductance of the traces.

3. AVDD and VDD pins must be connected to a power supply level that is at least equal or higher than that of VDDQB, VDDQC, and VDDQD output supply pins.

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Table 1: Frequency Table

VCO_SEL	Feedback Output Divider	VCO	Input Frequency Range (AVDD = 3.3V)	Input Frequency Range (AVDD = 2.5V)
0	÷2	Input Clock * 2	100MHz to 200MHz	100MHz to 200MHz
0	÷4	Input Clock * 4	50MHz to 125MHz	50MHz to 100MHz
0	÷6	Input Clock * 6	33.33MHz to 83.33MHz	33.33MHz to 66.67MHz
1	÷2	Input Clock * 4	50MHz to 125MHz	50MHz to 100MHz
1	÷4	Input Clock * 8	25MHz to 62.5MHz	25MHz to 50MHz
1	÷6	Input Clock * 12	16.67MHz to 41.67MHz	16.67MHz to 33.33MHz

Table 2: Function Table

Control	Default	0	1
VCO_SEL	0	VCO	VCO ÷ 2
PLL_EN#	0	PLL enabled. The VCO output connects to the output dividers	Bypass mode, PLL disabled. The input clock connects to the output dividers
MR/OE#	0	Outputs enabled	Outputs disabled (three-state), VCO running at its minimum frequency
SELA	0	QA = VCO÷4	QA = VCO÷6
SELB	0	QB = VCO ÷4	QB = VCO÷2
SELC	0	QC = VCO÷2	QC = VCO÷4

Absolute Maximum Ratings

Parameter	Description	Condition	Min	Max	Unit
VDD	DC Supply Voltage		-0.3	5.5	V
VDD	DC Operating Voltage	Functional	2.375	3.465	V
VIN	DC Input Voltage	Relative to Vss	-0.3	VDD+ 0.3	V
VOUT	DC Output Voltage	Relative to Vss	-0.3	VDD+ 0.3	V
VTT	Output termination Voltage			VDD ÷2	V
LU	Latch Up Immunity	Functional	200		mA
RPS	Power Supply Ripple	Ripple Frequency < 100 kHz		150	mVp-p
Ts	Temperature, Storage	Non Functional	-65	+150	°C
TA	Temperature, Operating Ambient	Functional	-40	+85	°C
TJ	Temperature, Junction	Functional		155	°C
ØJC	Dissipation, Junction to Case	Functional		42	°C/W
ØJA	Dissipation, Junction to Ambient	Functional		105	°C/W
ESDH	ESD Protection (Human Body Model)		2000		Volts
FIT	Failure in Time	Manufacturing test		10	ppm

Note: These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

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**DC Electrical Specifications** ( $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ )

Parameter	Description	Condition	Min	Typ	Max	Unit
V <sub>IL</sub>	Input Voltage, Low	LVC MOS			0.7	V
V <sub>IH</sub>	Input Voltage, High	LVC MOS	1.7		V <sub>DD</sub> + 0.3	V
V <sub>OL</sub>	Output Voltage, Low <sup>1</sup>	I <sub>OL</sub> = 15 mA			0.6	V
V <sub>OH</sub>	Output Voltage, High <sup>1</sup>	I <sub>OH</sub> = -15 mA	1.8			V
I <sub>IL</sub>	Input Current, Low	V <sub>IL</sub> = V <sub>SS</sub>			-10	μA
I <sub>IH</sub>	Input Current, High <sup>2</sup>	V <sub>IL</sub> = V <sub>DD</sub>			100	μA
I <sub>DDA</sub>	PLL Supply Current	AV <sub>DD</sub> only		5	10	mA
I <sub>DDQ</sub>	Quiescent Supply Current	All V <sub>DD</sub> pins except AV <sub>DD</sub>		3	5	mA
I <sub>DD</sub>	Dynamic Supply Current			170		mA
C <sub>IN</sub>	Input Pin Capacitance			4		pF
Z <sub>OUT</sub>	Output Impedance			17 - 20		Ω

Note: 1. Driving one 50Ω parallel terminated transmission line to a termination voltage of V<sub>TT</sub>. Alternatively, each output drives up to two 50Ω series terminated transmission lines.

2. Inputs have pull-down resistors that affect the input current.

**DC Electrical Specifications** ( $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ )

Parameter	Description	Condition	Min	Typ	Max	Unit
V <sub>IL</sub>	Input Voltage, Low	LVC MOS			0.8	V
V <sub>IH</sub>	Input Voltage, High	LVC MOS	2.0		V <sub>DD</sub> + 0.3	V
V <sub>OL</sub>	Output Voltage, Low <sup>1</sup>	I <sub>OL</sub> = 24 mA			0.55	V
		I <sub>OL</sub> = 12 mA			0.30	
V <sub>OH</sub>	Output Voltage, High <sup>1</sup>	I <sub>OH</sub> = -24 mA	2.4			V
I <sub>IL</sub>	Input Current, Low	V <sub>IL</sub> = V <sub>SS</sub>			-10	μA
I <sub>IH</sub>	Input Current, High <sup>2</sup>	V <sub>IL</sub> = V <sub>DD</sub>			100	μA
I <sub>DDA</sub>	PLL Supply Current	AV <sub>DD</sub> only		5	10	mA
I <sub>DDQ</sub>	Quiescent Supply Current	All V <sub>DD</sub> pins except AV <sub>DD</sub>		3	5	mA
I <sub>DD</sub>	Dynamic Supply Current			240		mA
C <sub>IN</sub>	Input Pin Capacitance			4		pF
Z <sub>OUT</sub>	Output Impedance			14 - 17		Ω

Note: 1. Driving one 50Ω parallel terminated transmission line to a termination voltage of V<sub>TT</sub>. Alternatively, each output drives up to two 50Ω series terminated transmission lines.

2. Inputs have pull-down resistors that affect the input current.

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AC Electrical Specifications ( $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ )<sup>1</sup>

Parameter	Description	Condition	Min	Typ	Max	Unit
f <sub>VCO</sub>	VCO Frequency		200		400	MHz
f <sub>in</sub>	Input Frequency	÷2 Feedback	100		200	MHz
		÷4 Feedback	50		100	
		÷6 Feedback	33.33		66.67	
		÷8 Feedback	25		50	
		÷12 Feedback	16.67		33.33	
		Bypass mode (PLL_EN# = 1)	0		200	
f <sub>refDC</sub>	Input Duty Cycle		25		75	%
t <sub>r</sub> , t <sub>f</sub>	TCLK Input Rise/FallTime	0.7V to 1.7V			1.0	nS
f <sub>MAX</sub>	Maximum Output Frequency	÷2 Output	100		200	MHz
		÷4 Output	50		100	
		÷6 Output	33.33		66.67	
		÷8 Output	25		50	
		÷12 Output	16.67		33.33	
DC	Output Duty Cycle	f <sub>MAX</sub> < 100MHz	47		53	%
		f <sub>MAX</sub> > 100MHz	44		56	
t <sub>r</sub> , t <sub>f</sub>	Output Rise/Fall times	0.6V to 1.8V	0.1		1.0	nS
t <sub>(φ)</sub>	Propagation Delay (static phase offset)	TCLK to FB_IN, same VDD, does not include jitter	-100		100	pS
t <sub>sk(O)</sub>	Output-to-Output Skew	Skew within Bank			125	pS
t <sub>sk(B)</sub>	Bank-to-Bank Skew	Banks at same voltage, same frequency			175	pS
		Banks at same voltage, different frequency			225	
t <sub>PLZ, HZ</sub>	Output Disable Time				8	nS
t <sub>PZL, ZH</sub>	Output Enable Time				10	nS
BW	PLL Closed Loop Bandwidth (-3dB)	÷2 Feedback		2		MHz
		÷4 Feedback		1 - 1.5		
		÷6 Feedback		0.6		
		÷8 Feedback		0.75		
		÷12 Feedback		0.5		
t <sub>JIT(CC)</sub>	Cycle-to-Cycle Jitter	Same frequency			100	pS
		Multiple frequencies			300	
t <sub>JIT(PER)</sub>	Period Jitter	Same frequency			100	pS
		Multiple frequencies			150	
t <sub>JIT(φ)</sub>	I/O Phase Jitter	VCO < 300MHz		150		pS
		VCO > 300MHz		100		
t <sub>LOCK</sub>	Maximum PLL Lock Time				1	mS

Note: 1. AC characteristics apply for parallel output termination of 50Ω to V<sub>TT</sub>. Parameters are guaranteed by characterization and are not 100% tested.

**AC Electrical Specifications** ( $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )<sup>1</sup>

Parameter	Description	Condition	Min	Typ	Max	Unit
f <sub>VCO</sub>	VCO Frequency		200		500	MHz
f <sub>in</sub>	Input Frequency	÷2 Feedback	100		200	MHz
		÷4 Feedback	50		125	
		÷6 Feedback	33.33		83.33	
		÷8 Feedback	25		62.5	
		÷12 Feedback	16.67		41.67	
		Bypass mode (PLL_EN# = 1)	0		200	
f <sub>refDC</sub>	Input Duty Cycle		25		75	%
t <sub>r</sub> , t <sub>f</sub>	TCLK Input Rise/FallTime	0.8V to 2.0V			1.0	nS
f <sub>MAX</sub>	Maximum Output Frequency	÷2 Output	100		200	MHz
		÷4 Output	50		125	
		÷6 Output	33.33		83.33	
		÷8 Output	25		62.5	
		÷12 Output	16.67		41.67	
DC	Output Duty Cycle	f <sub>MAX</sub> < 100MHz	48		52	%
		f <sub>MAX</sub> > 100MHz	44		56	
t <sub>r</sub> , t <sub>f</sub>	Output Rise/Fall times	0.55V to 2.4V	0.1		1.0	nS
t <sub>(φ)</sub>	Propagation Delay (static phase offset)	TCLK to FB_IN, same V <sub>DD</sub> , does not include jitter	-100		200	pS
t <sub>sk(O)</sub>	Output-to-Output Skew	Skew within each Bank			125	pS
t <sub>sk(B)</sub>	Bank-to-Bank Skew	Banks at same voltage, same frequency			175	pS
		Banks at same voltage, different frequency			235	
		Banks at different voltage			425	
t <sub>PLZ, HZ</sub>	Output Disable Time				8	nS
t <sub>PZL, ZH</sub>	Output Enable Time				10	nS
BW	PLL Closed Loop Bandwidth (-3dB)	÷2 Feedback		2		MHz
		÷4 Feedback		1 - 1.5		
		÷6 Feedback		0.6		
		÷8 Feedback		0.75		
		÷12 Feedback		0.5		
t <sub>JIT(CC)</sub>	Cycle-to-Cycle Jitter	Same frequency			100	pS
		Multiple frequencies			275	
t <sub>JIT(PER)</sub>	Period Jitter	Same frequency			100	pS
		Multiple frequencies			150	
t <sub>JIT(φ)</sub>	I/O Phase Jitter	VCO < 300MHz		150		pS
		VCO > 300MHz		100		
t <sub>LOCK</sub>	Maximum PLL Lock Time				1	mS

Note:1.AC characteristics apply for parallel output termination of 50Ω to V<sub>TT</sub>. Parameters are guaranteed by characterization and are not 100% tested.

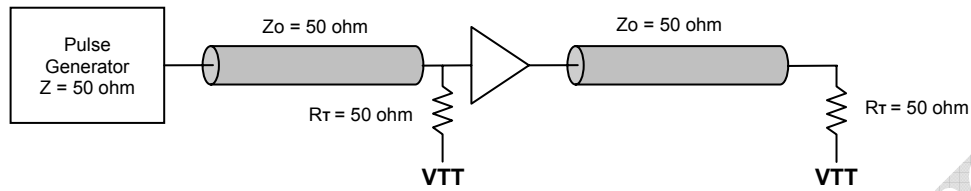


Figure 1. AC Test Reference for VDD = 3.3V / 2.5V

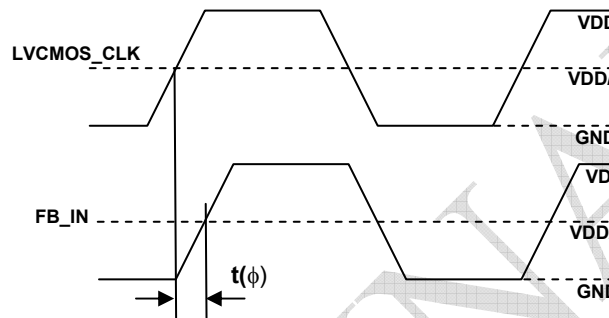


Figure 2. LVC MOS Propagation Delay  $t(\phi)$ , Static Phase Offset

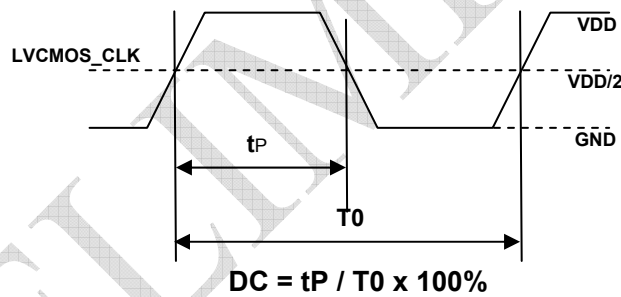


Figure 3. Output Duty Cycle (DC)

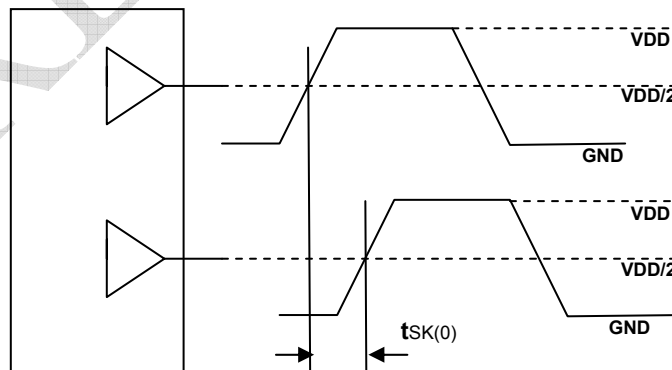
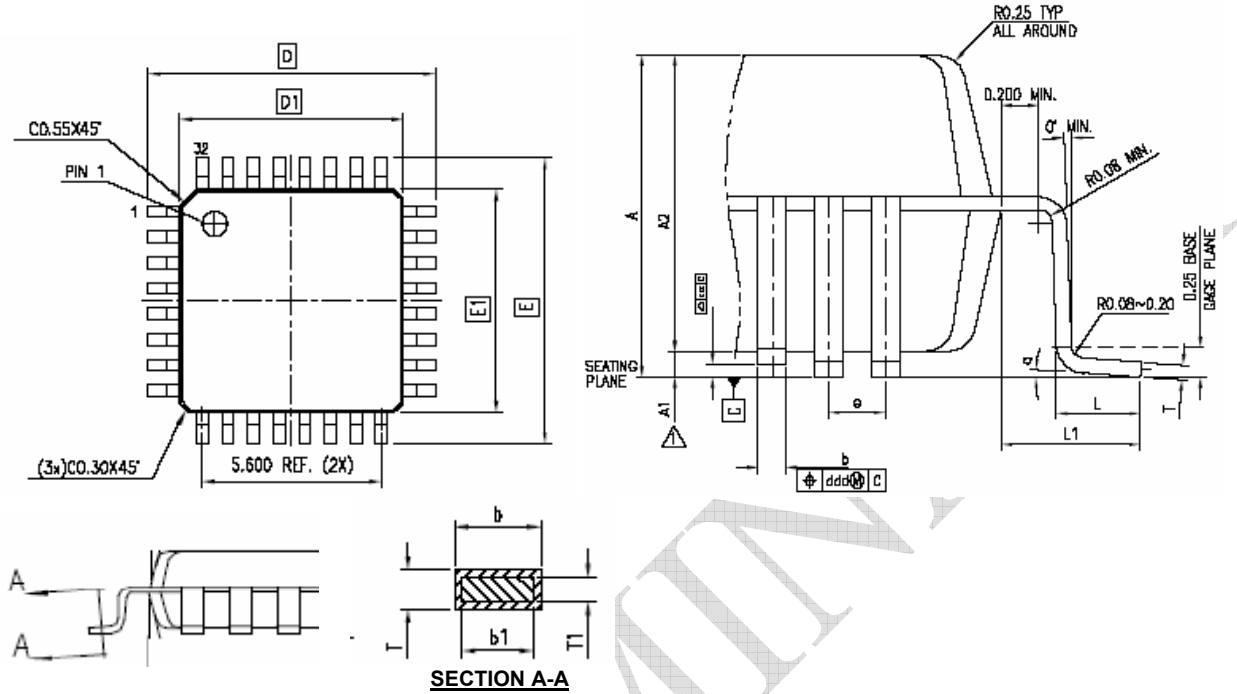


Figure 4. Output-to-Output Skew ,  $tsK(0)$



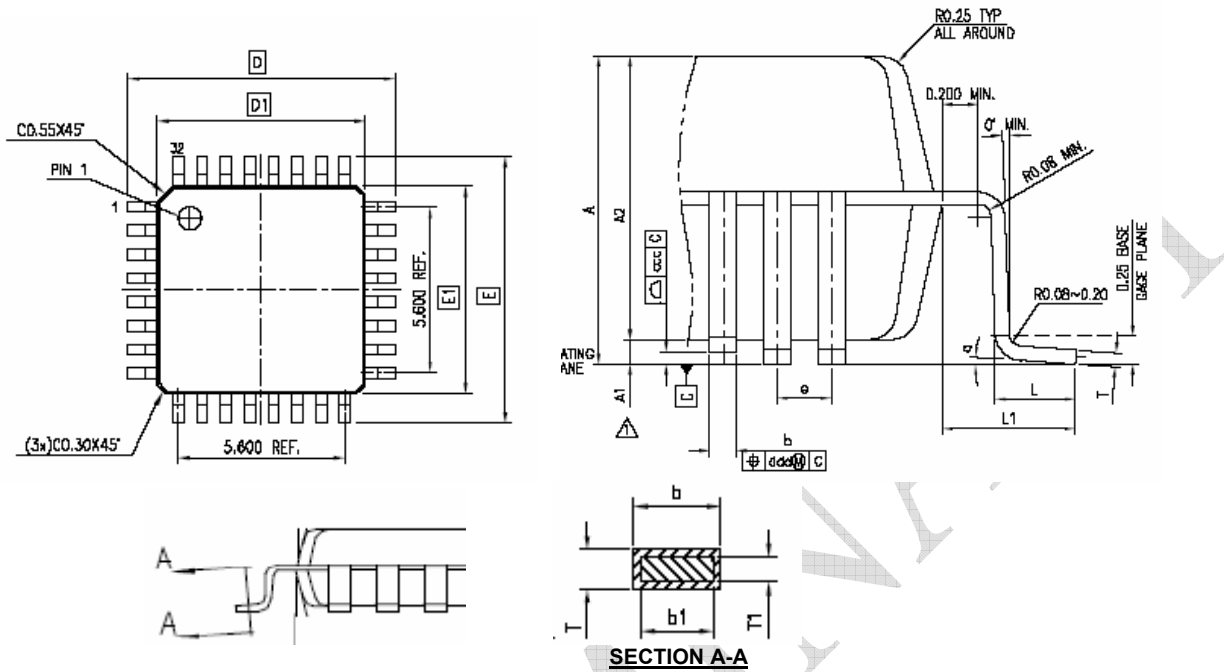
Package Diagram

32-lead TQFP Package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	....	0.0472	...	1.2
A1	0.0020	0.0059	0.05	0.15
A2	0.0374	0.0413	0.95	1.05
D	0.3465	0.3622	8.8	9.2
D1	0.2717	0.2795	6.9	7.1
E	0.3465	0.3622	8.8	9.2
E1	0.2717	0.2795	6.9	7.1
L	0.0177	0.0295	0.45	0.75
L1	0.03937 REF		1.00 REF	
T	0.0035	0.0079	0.09	0.2
T1	0.0038	0.0062	0.097	0.157
b	0.0118	0.0177	0.30	0.45
b1	0.0118	0.0157	0.30	0.40
R0	0.0031	0.0079	0.08	0.2
a	0°	7°	0°	7°
e	0.031 BASE		0.8 BASE	

32-lead LQFP Package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	....	0.0630	...	1.6
A1	0.0020	0.0059	0.05	0.15
A2	0.0531	0.0571	1.35	1.45
D	0.3465	0.3622	8.8	9.2
D1	0.2717	0.2795	6.9	7.1
E	0.3465	0.3622	8.8	9.2
E1	0.2717	0.2795	6.9	7.1
L	0.0177	0.0295	0.45	0.75
L1	0.03937 REF		1.00 REF	
T	0.0035	0.0079	0.09	0.2
T1	0.0038	0.0062	0.097	0.157
b	0.0118	0.0177	0.30	0.45
b1	0.0118	0.0157	0.30	0.40
R0	0.0031	0.0079	0.08	0.20
e	0.031 BASE		0.8 BASE	
a	0°	7°	0°	7°

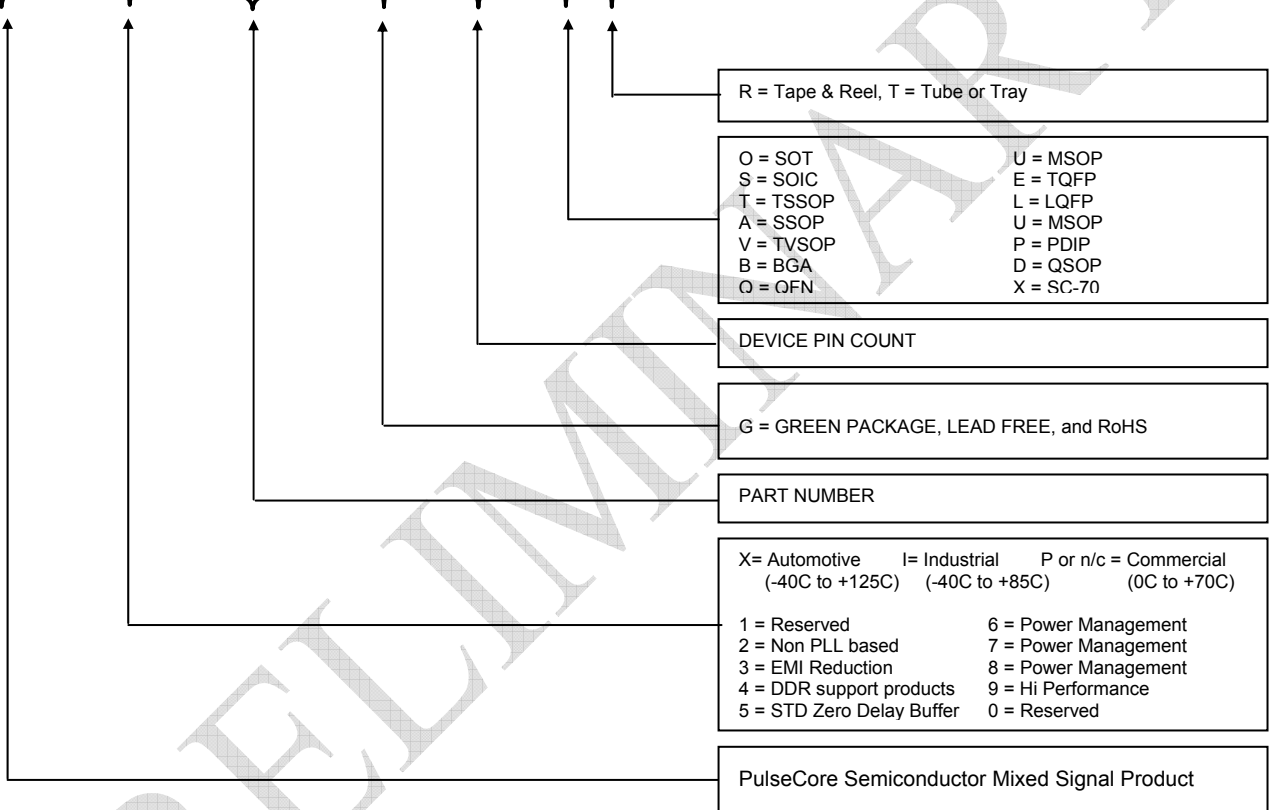
rev 0.3

**Ordering Information**

Part Number	Marking	Package Type	Temperature
PCS5I9352G-32-ET	PCS5I9352G	32-pin TQFP, Green	Industrial
PCS5I9352G-32-LT	PCS5I9352G	32-pin LQFP –Tape and Reel, Green	Industrial

**Device Ordering Information**

PCS 5 I 9 3 5 2 G - 3 2 - L T



Licensed under US patent #5,488,627, #6,646,463 and #5,631,920.



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Preliminary Information  
Part Number: PCS5I9352  
Document Version: 0.3

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003

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