PAS6311LT CMOS VGA DIGITAL IMAGE SESNSOR

General Description

The PAS6311LT is a highly integrated CMOS active-pixel image sensor that has a VGA resolution of 648H x 488V. It embedded the new FinePixel™ sensor technology to perform the excellent image quality. The PAS6311LT outputs 10-bit RGB raw data through a parallel data bus. It is available in 24-pin CSP.

The PAS6311LT can be programmed to set the exposure time for different luminance condition via I2C™ serial control bus. By programming the internal register set, it performs on-chip frame rate adjustment, offset correction DAC and programmable gain control.

Features

- VGA(640x480) resolution, ~1/6" Lens.
- Bayer RGB color filter array.
- 10-bits parallel RGB raw data output.
- On-Chip 10-bits pipeline A/D converter.
- On-Chip programmable gain amplifier
  - 3-bits front gain amplifier.
  - 7-bits color gain amplifier.
  - 7-bits global gain amplifier.
- Digital gain stage.
- Continuous variable frame time.
- Continuous variable exposure time.
- I2C™ interface.
- Flash light timing
- 1.8V~3.3V I/O voltage
- <15mA power dissipation (30fps / 2.5v).
- 10uA low power-down dissipation.
- Window-of-Interest (WOI).
- Sub-sampling.
- Defect compensation.
- Lens shading compensation.
- Companding
- Automatic background compensation
- Critical register table backward compatible with PAS6302
- Ball to ball compatible with PAS6302CS

Key Specification

Supply voltage	Analog	2.5V
	Core	1.8V
	I/O	1.8V ~ 3.3V
Resolution		640 (H) x 480 (V)
Array Diagonal		2.91mm (~1/6" Optic)
Pixel Size		3.6 μ m x 3.6 μ m
Max. Frame Rate		~30 fps @ 0.3Mega
Max. System Clock		Up to 48MHz
Max. Pixel Clock		Up to 12MHz
Color Filter		RGB Bayer Pattern
Exposure Time		~ Frame time to Line time
Scan Mode		Progressive
Sensitivity		1.3V/(Lux*Sec)
S/N Ratio		41dB
Dark Current		12mV/sec at 60℃
Chief Ray Angle		22 ~ 25 degree
Package Type		24-ball CSP

PixArt Imaging Inc.

E-mail: fae_service@pixart.com.tw

1. Pin Assignment

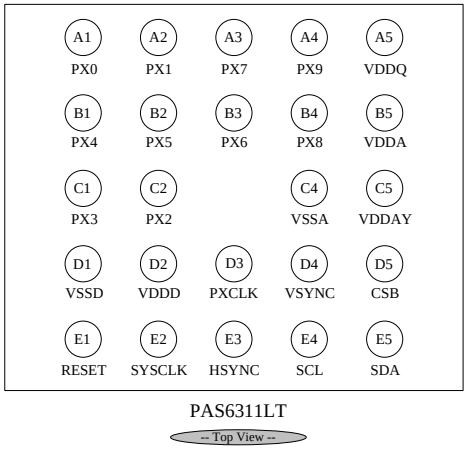


Figure 1.1 Shows the PAS6311LT pin diagram

Pin No.	Name	Type	Description
C4	VSSA	GND	Analog ground.
B5	VDDA	PWR	Analog VDD, 2.5V.
D5	CSB	IN	Power Down (chip power down if high).
C5	VDDAY	IN	Internal voltage reference.
D2	VDDD	PWR	Digital core VDD, 1.8V.
D4	VSYNC	OUT	Vertical synchronization signal.
E3	HSYNC	OUT	Horizontal synchronization signal.
D3	PXCLK	OUT	Pixel clock output.
A5	VDDQ	PWR	I/O VDD, 1.8V ~ 3.3V.
E2	SYSCLK	IN	Master clock input.
E1	RESET	IN	Resets all registers to default (chip reset if high .)
D1	VSSD	GND	Digital ground.
A4	PX9	OUT	Digital data out.
B4	PX8	OUT	Digital data out.
A3	PX7	OUT	Digital data out.
B3	PX6	OUT	Digital data out.
B2	PX5	OUT	Digital data out.
B1	PX4	OUT	Digital data out.
C1	PX3	OUT	Digital data out.
C2	PX2	OUT	Digital data out.
A2	PX1	OUT	Digital data out.
A1	PX0	OUT	Digital data out.
E4	SCL	IN	I2C clock.
E5	SDA	I/O	I2C data. Internal pull high resister is 10KΩ.

PixArt Imaging Inc.

E-mail: fae_service@pixart.com.tw

2. Sensor Array Format & Output Timing

2.1. Physical Sensor Array Format

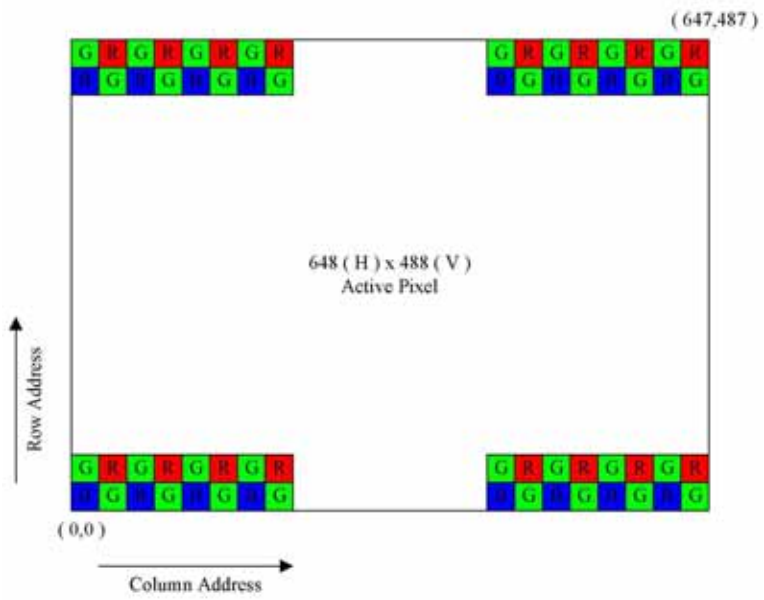


Figure 2.1 Physical Sensor Array Format

2.2. Output Timing

VGA mode (648 x 488) pixel readout:

H_Start[9:0] = 0, V_Start[8:0] = 0, H_Size[9:0] = 647, V_Size[8:0]= 487,

LPF[13:0] = 508, Nov_Size[7:0]= 136,

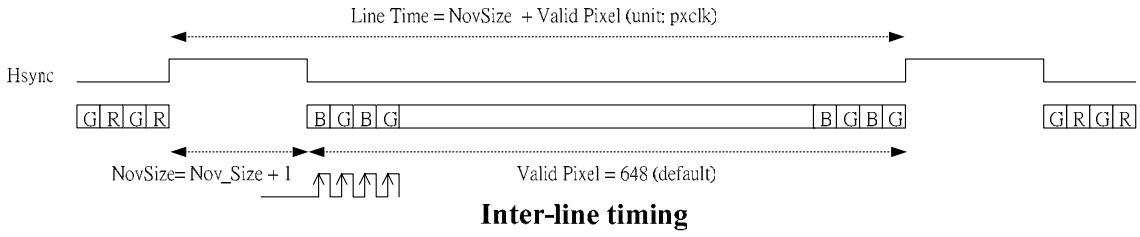


Figure 2.2 Inter-line timing

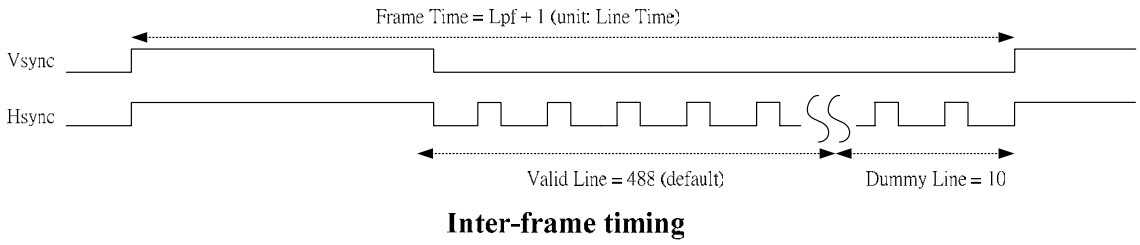


Figure 2.3 Inter-frame timing

PixArt Imaging Inc.

E-mail: fae_service@pixart.com.tw

3. Block Diagram & Function Description

3.1. Block Diagram

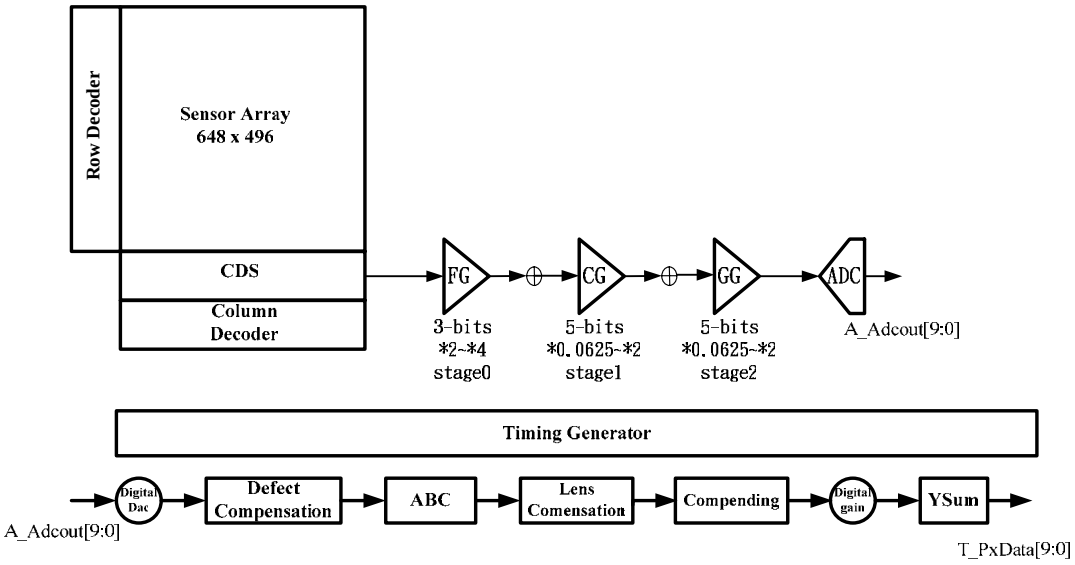


Figure 3.1 Shows the PAS6311LT sensor block diagram

The PAS6311LT is a 1/6" CMOS imaging sensor with 640 (H) x 480 (V) physical pixels. The active region of sensor array is 648 (H) x 488 (V). The sensor array is cover with Bayer pattern color filters and μ-lens. The first pixel location (0,0) is programmable in 2 direction (X and Y) and the default value is at the left-down side of sensor array.

After a programmable exposure time, the image is sampled first with CDS (Correlated Double Sampling) block to improve S/N ration and reduce fixed pattern noise.

Three analog gain stages are implemented before signal transferred by the 10-bits A/D converter. The front gain stage (FG) can be programmed to fit the saturation level of sensor to the full-range input of ADC. The programmable color gain stage (CG) is used to balance the luminance response difference between B/G/R. The global gain stage (GG) is programmed to adapt the gain to the image luminance.

The fine gained signal will be digitized by the on-chip 10-bits A/D converter. After the image data has been digitized, further alteration to the signal can be applied before the data is output.

3.2. Defect Compensation

The defect compensation block can detect the possible defective pixels and replace it with average output of like-colored pixels on either side of defective pixel. It's no limitation on the capability of defective number. This function is also enabled or disabled by user.

3.3. Companding Curves

The companding function is used to simulate the gamma curve and do non-linear transformation before outputting data. There are 8 curves selected by setting register Compand_Sel as shown in Figure 3.2 and this function is also enabled or disabled by user.

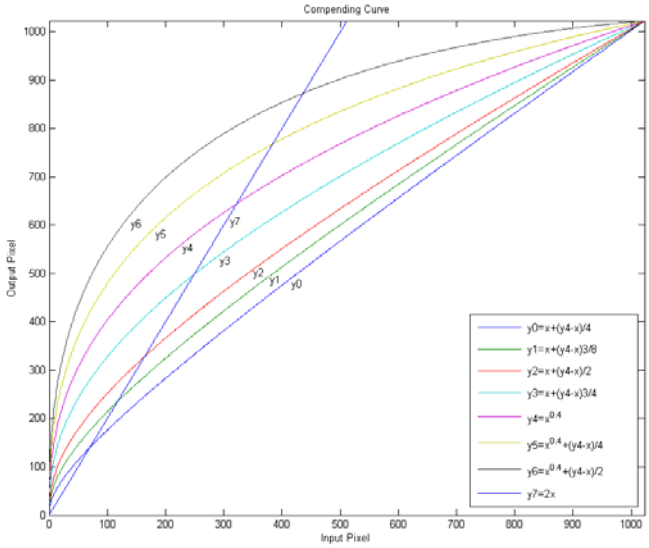


Figure 3.2 Companding curves program by Compand_EnH and Compand_Sel

3.4. Power Down Mode

The PAS6311LT can enter power-down mode by setting register "SW_PwrDn" or by enabling CSB pin. PAS6311LT supports two power-down modes :

- Software Power Down : Setting register "SW_PwrDn" = 0x01 could have power-down effect upon all the internal block except I2C™.
- Hardware Power Down : Pulling CSB pin to high could have power-down effect upon the whole chip. The chip will go into standby state.

3.5. Reset Mode

The PAS6311LT can be reset by setting register "SW_Reset" or by enabling Reset pin. PAS6311LT supports two reset modes :

- Software Reset : Set register "SW_Reset" = 0x01 to reset all the I2C™ registers. It resets the register value only and non-whole chip.
- HardwareReset : Pull Reset pin to high to reset the whole chip.

3.6. Automatic Background Compensation (ABC)

By setting register "ABC_en" = 0x01, PAS6311LT can do the black-level calibration automatically. The purpose of this function supports user to set Dac value by hardware self-calculation to make dark like real dark.

PixArt Imaging Inc.

E-mail: fae_service@pixart.com.tw

3.7. Window-of-Interest (WOI)

Users could be allowed to define window size as well as window location in PAS6311LT. The location of window can be set anywhere in the pixel array. Window size and window location is defined by register “H_Start”, “V_Start”, “V_Size” and “H_Size”. “H_Start” and “V_Satrt” define the starting column and starting row of the window. “H_Size” and “V_Size” define the width and depth of the window.

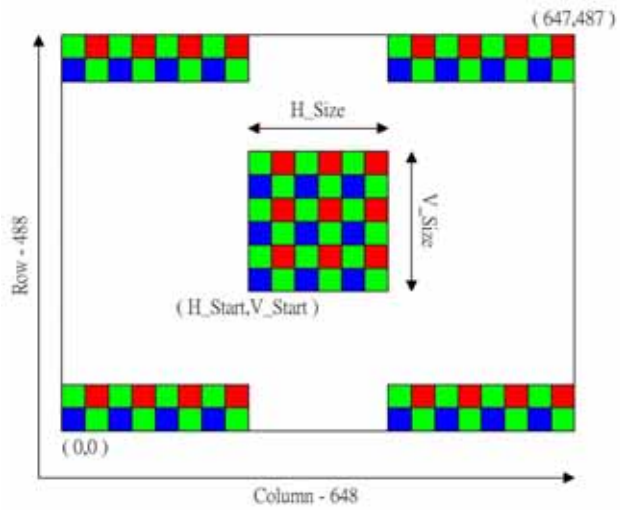


Figure 3.3

3.7.1. Output timing of WOI

Hardware windowing QVGA (320x240) pixels readout :

H_Start[9:0] = 0, V_Start[8:0] = 0, H_Size[9:0] = 319, V_Size[8:0]= 239,

Nov_Size [7:0] = 136,

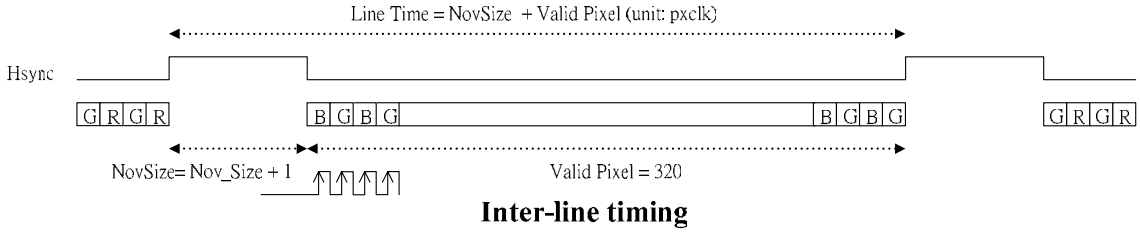


Figure 3.4 Inter-line timing of W.O.I

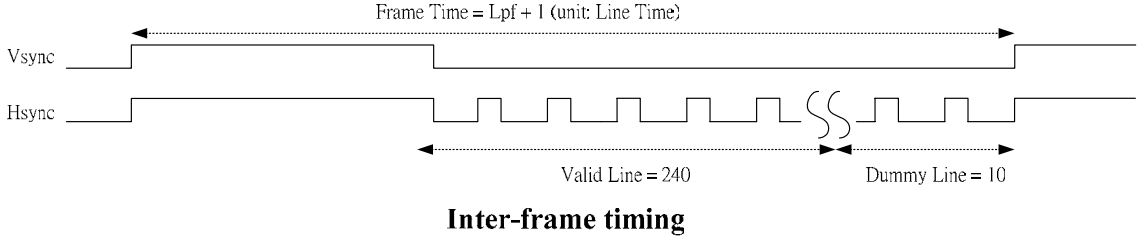


Figure 3.5 Inter-frame timing of W.O.I

PixArt Imaging Inc.

E-mail: fae_service@pixart.com.tw

3.8. Sub-Sampling

PAS6311LT can be programmed to output image in QVGA and QQVGA size. For QVGA sub-sampling mode, both vertical and horizontal pixels are divided by 2; For QQVGA sub-sampling mode, both vertical and horizontal pixels are divided by 4. By programming Skip_Analog and Skip_Digital, the maximum sub-sampling rate is 1/64 (Skip_Analog + Skip_Digital).

3.8.1. Skip_Analog

Analog sub-sampling to (1/2) * VGA size readout :

H_Start[9:0] = 0, V_Start[8:0] = 0, H_Size[9:0] = 647, V_Size[8:0]= 487,

Nov_Size[7:0] = 136, Skip_Analog = 1 (sub-sampling 1/2)

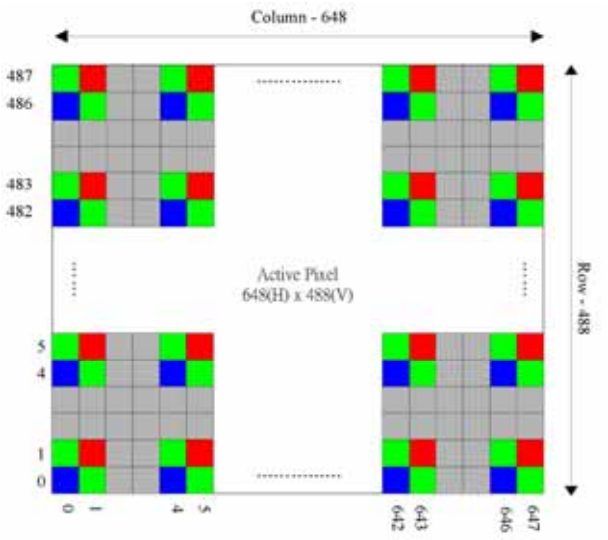


Figure 3.6

Valid pixels = (H_Size + 1) / Skip_Analog = (647 + 1) / 2 = 324

Valid lines = (V_Siez + 1) / Skip_Analog = (487 + 1) / 2 = 244

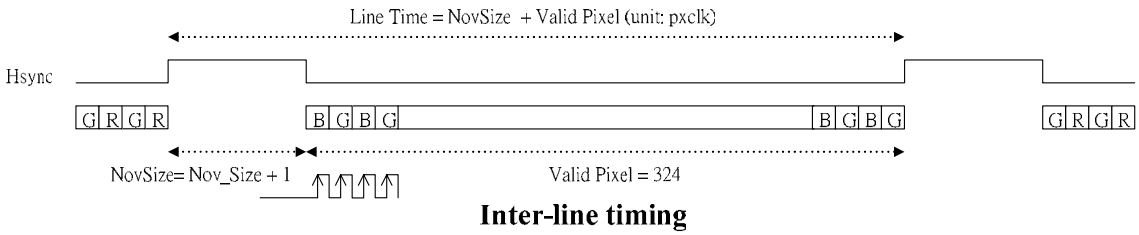


Figure 3.7 Inter-line timing of Skip_Analog = 1

PixArt Imaging Inc.

E-mail: fae_service@pixart.com.tw

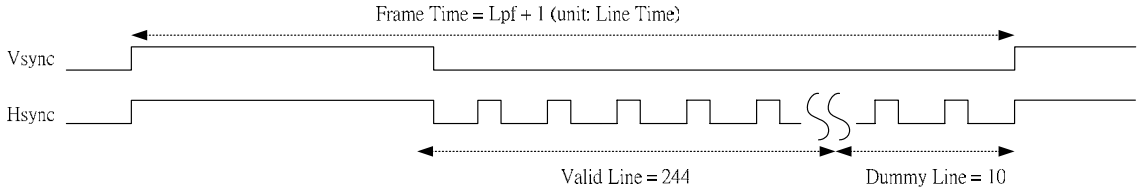


Figure 3.8 Inter-frame timing of Skip_Analog = 1

3.8.2. Skip_Digital

Digital sub-sampling to (1/2) * VGA size readout :

H_Start[9:0] = 0, V_Start[8:0] = 0, H_Size[9:0] = 647, V_Size[8:0]= 487,

Nov_Size [7:0] = 136, Skip_Digital = 1

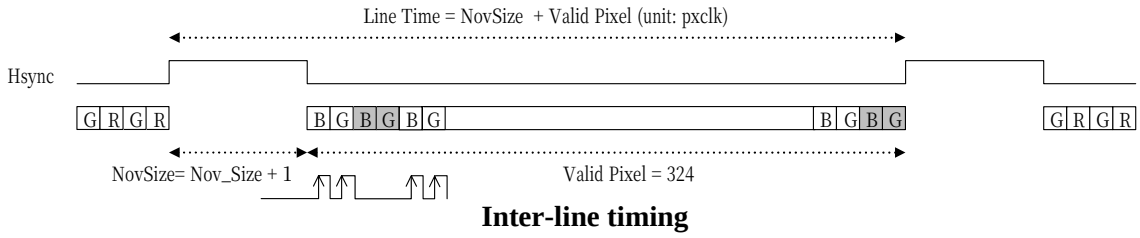


Figure 3.9 Inter-line timing of Skip_Digital = 1

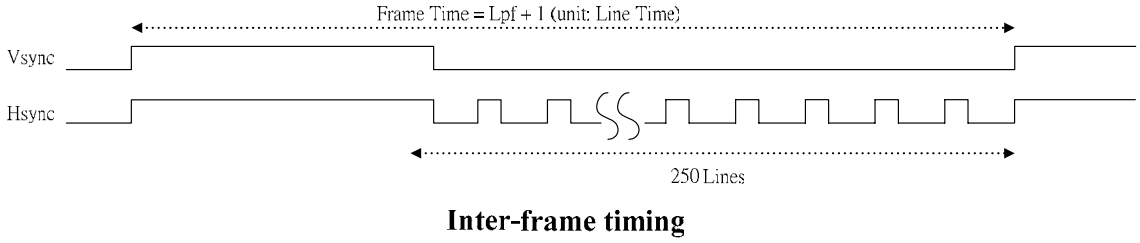


Figure 3.10 Inter-frame timing of Skip_Digital = 1

PixArt Imaging Inc.

E-mail: fae_service@pixart.com.tw

4. I2C™ Bus

PAS6311LT supports I2C bus transfer protocol and acts as slave device. The 7-bits unique slave address is “1000000” and supports receiving / transmitting speed as maximum 400KHz.

4.1. I2C Bus Overview

- Only two wires SDA (serial data) and SCL (serial clock) carry information between the devices connected to the I2C bus. Normally both SDA and SCL lines are open collector structure and pulled high by external pull-up resistors.
- Only the master can initiates a transfer (start), generates clock signals, and terminates a transfer (stop).
- Start and stop condition : A high to low transition of the SDA line while SCL is high defines a start condition. A low to high transition of the SDA line while SCL is high defines a stop condition. Please refer to Figure 4.1.
- Valid data : The data on the SDA line must be stable during the high period of the SCL clock. Within each byte, MSB is always transferred first. Read / Write control bit is the LSB of the first byte. Please refer to Figure 4.2.
- Both the master and slave can transmit and receive data from the bus.
- Acknowledge : The receiving device should pull down the SDA line during high period of the SCL clock line when a complete byte was transferred by transmitter. In the case of a master received data from a slave, the master does not generate an acknowledgment on the last byte to indicate the end of a master read cycle.

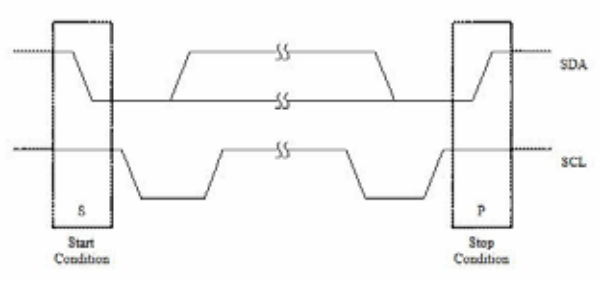


Figure 4.1 Start and Stop conditions

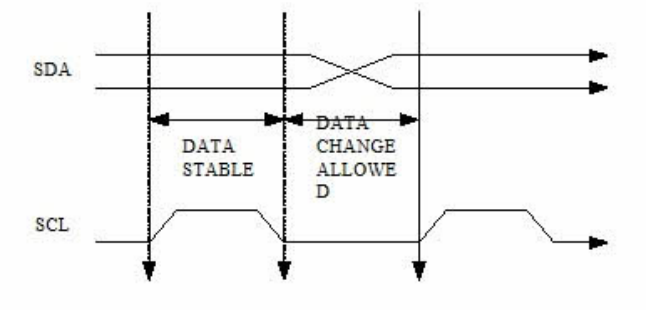
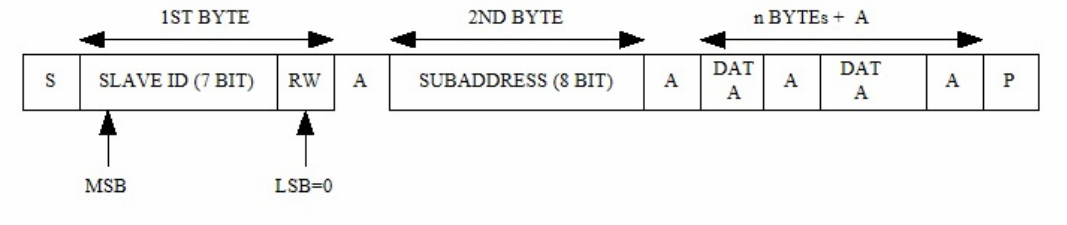


Figure 4.2 Valid Data

4.2. Data Transfer Format

4.2.1. Master transmits data to salve (write cycle)

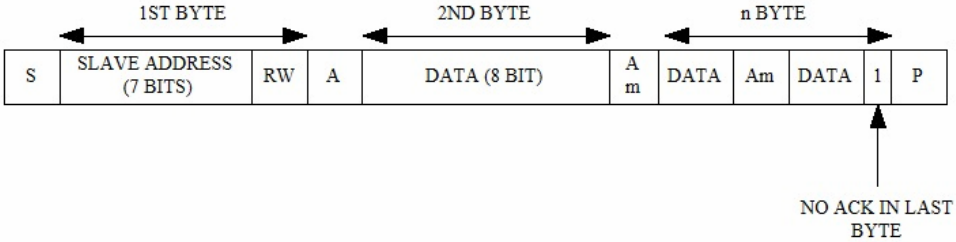
- S : Start.
- A : Acknowledge by salve.
- P : Stop.
- RW : The LSB of 1ST byte to decide whether current cycle is read or write cycle. RW = 1 – Read cycle, RW = 0 – Write cycle.
- SUBADDRESS : The address values of PAS6311LT internal control registers. (Please refer to PAS6311LT register description)



During write cycle, the master generates start condition and then places the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After slave (PAS6311LT) issues acknowledgment, the master places 2nd byte (Sub Address) data on SDA line. Again follow the PAS6311LT acknowledgment, the master places the 8 bits data on SDA line and transmit to PAS6311LT control register (address was assigned by 2nd byte). After PAS6311LT issue acknowledgment, the master can generate a stop condition to end of this write cycle. In the condition of multi-byte write, the PAS6311LT sub-address is automatically increment after each DATA byte transferred. The data and A cycles is repeat until last byte write. Every control registers value inside PAS6311LT can be programming via this way.

4.2.2. Slave transmits data to master (read cycle)

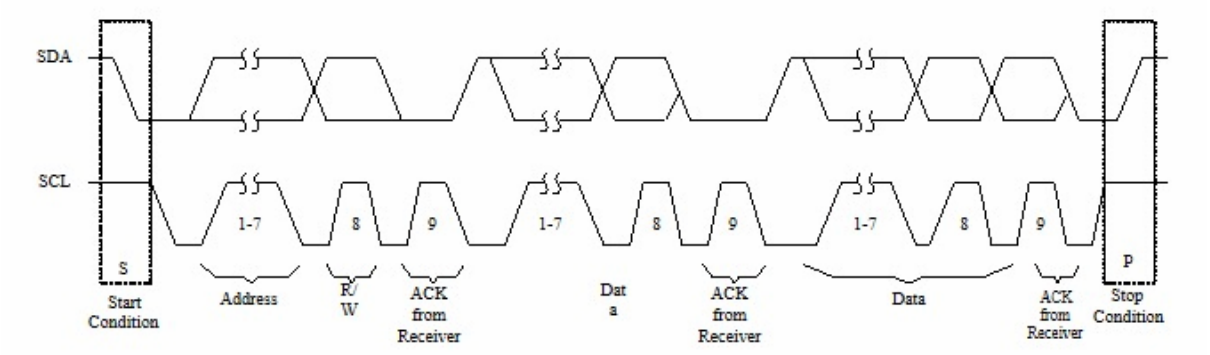
- The sub-address was taken from previous write cycle.
- The sub-address is automatically increment after each byte read.
- Am : Acknowledge by master.
- Note there is no acknowledgment from master after last byte read.



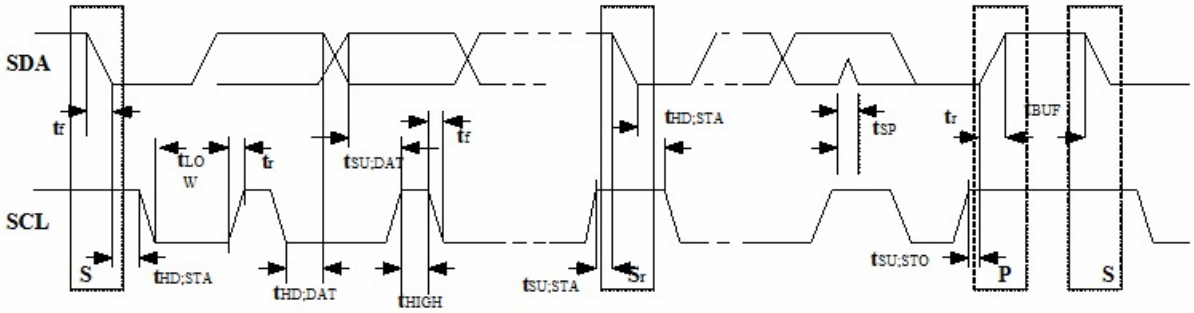
PixArt Imaging Inc.

E-mail: fae_service@pixart.com.tw

During read cycle, the master generates start condition and then place the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After issue acknowledgment, 8 bits DATA was also placed on SDA line by PAS6311LT. The 8 bits data was read from PAS6311LT internal control register that address was assigned by previous write cycle. Follow the master acknowledgment, the PAS6311LT place the next 8 bits data (address is increment automatically) on SDA line and then transmit to master serially. The DATA and Am cycles is repeat until the last byte read. After last byte read, Am is no longer generated by master but instead by keep SDA line high. The slave (PAS6311LT) must releases SDA line to master to generate STOP condition.



4.3. I2C™ Bus Timing



4.4. I2C™ Bus Timing Specification

Parameter	Symbol	Standard Mode		Unit
		Min.	Max	
SCL clock frequency.	f_{scl}	10	400	KHz
Hold time (repeated) Start condition. After this period, the first clock pulse is generated.	$t_{HD:STA}$	4.0	-	μs
Low period of the SCL clock.	t_{LOW}	4.7	-	μs
High period of the SCL clock.	t_{HIGH}	0.75	-	μs
Set-up time for a repeated START condition.	$t_{SU;STA}$	4.7	-	μs

Data hold time. For I2C-bus device.	$t_{HD;DAT}$	0	3.45	μs
Data set-up time.	$t_{SU;DAT}$	250	-	ns
Rise time of both SDA and SCL signals.	t_r	30	N.D.	ns (notel)
Fall time of both SDA and SCL signals.	t_f	30	N.D.	ns (notel)
Set-up time for STOP condition.	$t_{SU;STO}$	4.0	-	μs
Bus free time between a STOP and START.	t_{BUF}	4.7	-	μs
Capacitive load for each bus line.	C_b	1	15	pF
Noise margin at LOW level for each connected device. (Including hysteresis)	V_{nL}	0.1 VDD	-	V
Noise margin at HIGH level for each connected device. (including hysteresis)	V_{nH}	0.2 VDD	-	V

Note : It depends on the “high” period time of SCL.

PixArt Imaging Inc.

E-mail: fae_service@pixart.com.tw

5. Specifications

Absolute Maximum Ratings

Ambient Storage Temperature		-40℃ to +125℃
Supply Voltage (with respect to ground)	V_{DDD}	3.0V
	V_{DDA}	4.5V
	V_{DDQ}	4.5V
All Input / Output Voltage (with respect to ground)		-0.3V to VDDQ+0.5V
Lead temperature, Surface-mount process		245℃
ESD rating, Human Body model		2000V

DC Electrical Characteristics (0℃ < T_A < 70℃)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Type : POWER					
V_{DDA}	DC supply voltage – Analog	2.45	2.5	2.8	V
V_{DDD}	DC supply voltage – Digital	1.7	1.8	1.98	V
V_{DDQ}	DC supply voltage – I/O	1.7	-	3.3	V
I_{DD}	Operating Current (~ 30fps / 2.5v)		15		mA
I_{PWDN}	Power Down Current (see Note[a])		10	20	μA
Type : IN & I/O Reset and System Clock(input clock)					
V_{IH}	Input Voltage HIGH	VDDQ * 0.7			V
V_{IL}	Input Voltage LOW			VDDQ * 0.3	V
Type : OUT & I/O for PX0~9, SDA, H/VSYNC and PXCLK(output clock)					
V_{OH}	Output Voltage HIGH (see Note[b])	VDDQ * 0.9			V
V_{OL}	Output Voltage LOW			VDDQ * 0.1	V

Note[a] : V_{DDA} = 2.5V, V_{DDQ} = 2.8V

Note[b] : For SDA, the minimum V_{OH} is VDDQ * 0.75

AC Operating Condition (0℃ < T_A < 70℃)

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{sysclk}	System clock frequency	10	24	48	MHz
t_{sysclk_dc}	System clock duty cycle	45	50	55	%

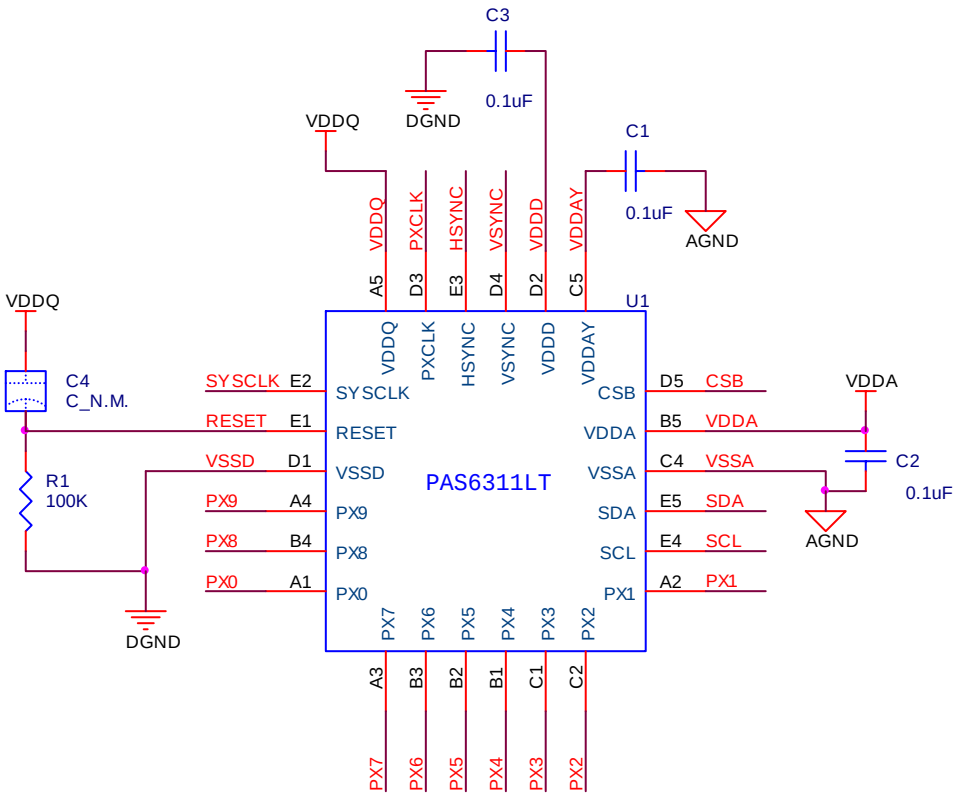
Sensor Characteristics

Parameter	Typ.	Unit
Sensitivity	1.3	V/(Lux*sec)
Signal to Noise Ratio	41	dB
Dynamic Range	52	dB

PixArt Imaging Inc.

E-mail: fae_service@pixart.com.tw

6. Reference Circuit Schematic

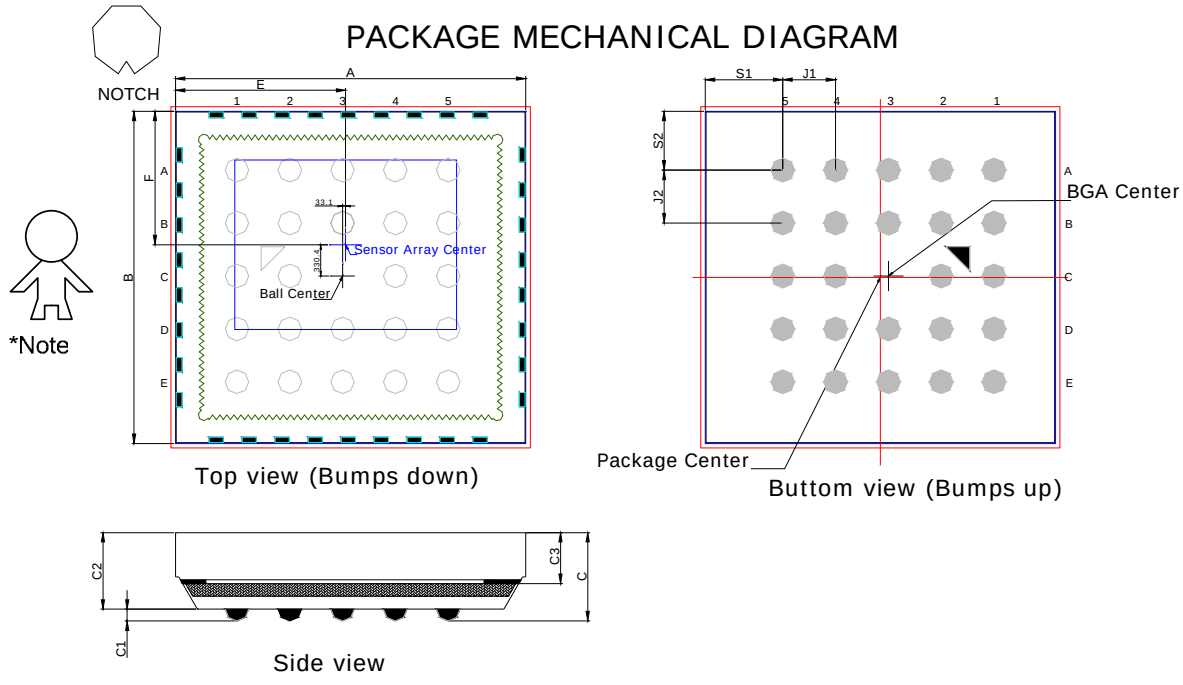


PixArt Imaging Inc.

E-mail: fae_service@pixart.com.tw

7. Package Information

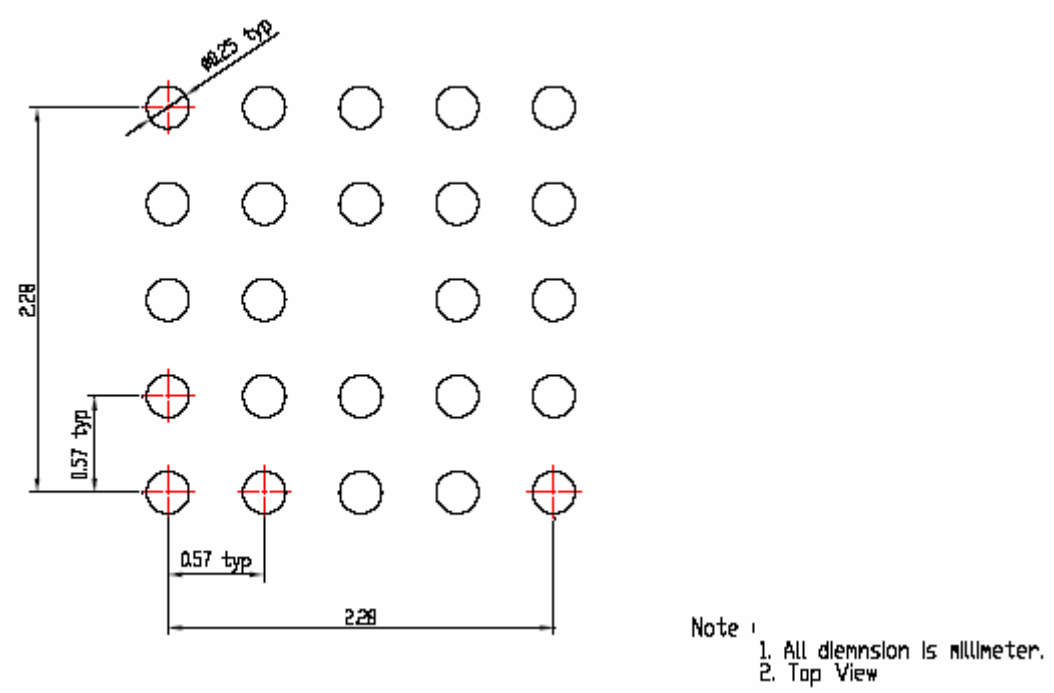
	Symbol	Nominal	Min.	Max.
		μm		
Package Body Dimension X	**A**	3715	3690	3740
Package Body Dimension Y	**B**	3515	3490	3540
Package Height	**C**	955	895	1015
Ball Height	**C1**	130	100	160
Package Body Thickness	**C2**	825	780	870
Glass Thickness	**C3**	545	525	565
Ball Diameter	**D**	250	220	280
Total Pin Count	**N**	24		
Pin Count X axis	**N1**	5		
Pin Count Y axis	**N2**	5		
Pins Pitch X axis	**J1**	570		
Pins Pitch Y axis	**J2**	570		
Edge to Pin Center Distance along X	**S1**	803	773	833
Edge to Pin Center Distance along Y	**S2**	603	573	633
Edge to Optical Center Distance along X	**E**	1806	1781	1831
Edge to Optical Center Distance along Y	**F**	1412	1387	1437



*Note:

The formation of image is the result formed by package Top view(A1 : left-up) and general Lens(invert and mirror the image).

Recommended Layout PCB



PixArt Imaging Inc.

E-mail: fae_service@pixart.com.tw

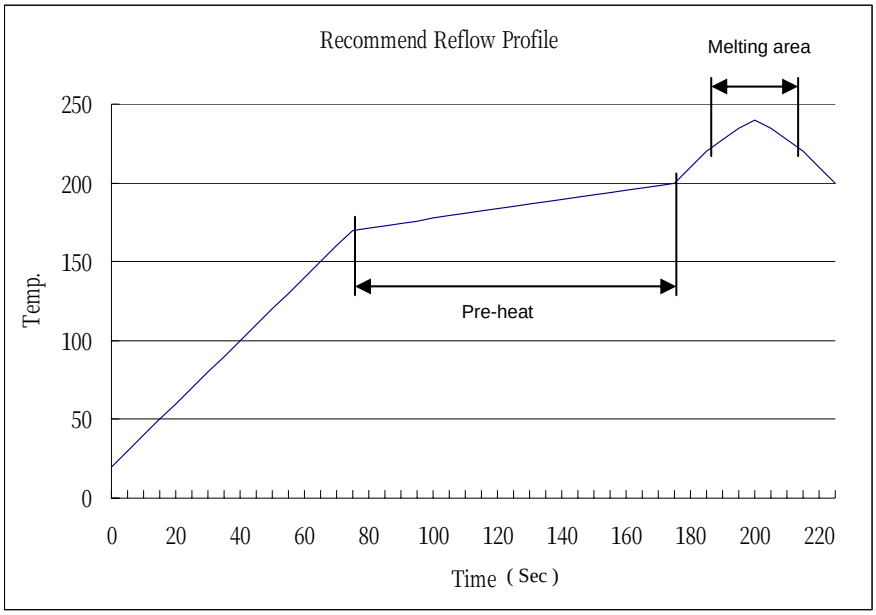
Recommended Condition For Infrared Reflow

Carefully observe the mounting conditions, recommended temperature profile when

Mounting infrared reflows is show in the figure below.

After mounting on the mother board, it must be dispense epoxy in side of the CSP package.

⊙ Reflow Profile



Recommend Pb-free solder paste vender & type : 1. Almit LFM-48W TM-HP

2. Senju M705-GRN360-K

Programming rate	Pre-heat	Melting area
1.5~2.5 °C/sec	170~200°C 90 +/- 30 sec	>220°C 30~50sec with peak temperature 230~245°C

⊙ Dispense Epoxy