IP5306CX8

Integrated differential microphone filter with ESD protection to IEC 61000-4-2 level 4

Rev. 01 — 12 February 2010 Product data sheet

1. Product profile

1.1 General description

The IP5306CX8 is a dual-channel RC low-pass filter array which is designed to provide filtering of undesired RF signals. In addition, the IP5306CX8 incorporates diodes to provide protection to downstream components from ElectroStatic Discharge (ESD) voltages as high as ±15 kV contact according the IEC 61000-4-2 model, far exceeding standard level 4.

IP5306CX8 is fabricated using monolithic silicon technology and integrates five resistors, several diodes and four high density capacitors in a single Wafer-Level Chip-Scale Package (WLCSP). These features make the IP5306CX8 ideal for use in applications requiring the utmost in miniaturization such as mobile phone handsets, cordless telephones and personal digital devices.

1.2 Features and benefits

- Pb-free, RoHS compliant and free of halogen and antimony (Dark Green compliant)
- Integrated differential microphone RC filter with high density capacitors [2 × (0.8 nF + 1.5 nF)] and biasing resistor network
- Integrated ESD protection withstanding ±15 kV contact discharge, far exceeding IEC 61000-4-2 level 4
- WLCSP with 0.4 mm pitch

1.3 Applications

- Differential microphones in mobile phones and other portable electronics

2. Pinning information

2.1 Pinning

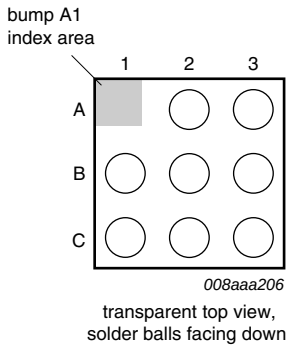


Fig 1. Pin configuration IP5306CX8

2.2 Pin description

Table 1. Pinning

Pin	Description
A1	not connected (missing ball)
A2	filter channel feedthrough (e.g. hookup)
A3	microphone biasing supply pin
B1	filter channel 1 external 15 kV microphone connection
B2	ground
B3	filter channel 1 internal 2 kV microphone amplifier/Analog-to-Digital Converter (ADC) input connection
C1	filter channel 2 external 15 kV microphone connection
C2	ground
C3	filter channel 2 internal 2 kV microphone amplifier/ADC input connection

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
IP5306CX8	WLCSP8	wafer level chip-size package; 8 bumps; 1.19 × 1.19 × 0.61 mm	IP5306CX8

4. Functional diagram

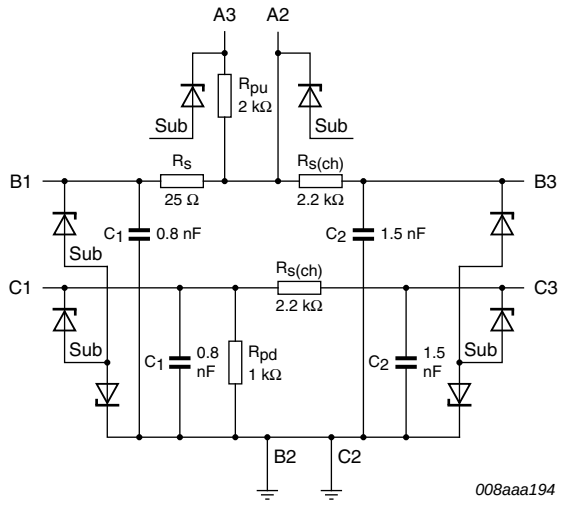


Fig 2. Schematic diagram IP5306CX8

5. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_I	input voltage			−0.5	+4.5	V
V_{ESD}	electrostatic discharge voltage	pins B1 and C1 to ground				
		contact discharge	[1]	−15	+15	kV
		air discharge	[1]	−15	+15	kV
		IEC 61000-4-2 level 4; pins B1 and C1 to ground				
		contact discharge		−8	+8	kV
		air discharge		−15	+15	kV
		IEC 61000-4-2 level 1; pins A2, A3, B3 and C3 to ground				
		contact discharge		−2	+2	kV
		air discharge		−2	+2	kV
P_{ch}	channel power dissipation	continuous power		-	30	mW
P_{tot}	total power dissipation	continuous power		-	60	mW
T_{stg}	storage temperature			−55	+150	°C
$T_{reflow(peak)}$	peak reflow temperature	10 s maximum		-	260	°C
T_{amb}	ambient temperature			−35	+85	°C

[1] Device is qualified with 1000 pulses of ±15 kV contact discharges each, according to the IEC61000-4-2 model and far exceeds the specified level 4 (8 kV contact discharge).

6. Characteristics

Table 4. Channel characteristics

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{pu}	pull-up resistance	biasing	1.9	2.0	2.1	kΩ
R_{pd}	pull-down resistance	biasing	0.8	1.0	1.2	kΩ
$R_{s(ch)}$	channel series resistance		1.76	2.20	2.64	kΩ
R_s	series resistance		20	25	30	Ω
C_1	capacitance 1	high density; $V_{bias(DC)}$ = 0 V; f = 100 kHz	-	0.8	1.0	nF
C_2	capacitance 2		1.0	1.5	-	nF
C_d	diode capacitance	$V_{bias(DC)}$ = 0 V; f = 100 kHz [1]				
		connected to 15 kV ESD pins	-	11.5	-	pF
		connected to 2 kV ESD pins	-	3	-	pF
V_{BR}	breakdown voltage	positive direction; I_{test} = 1 mA	14	16.5	-	V
		negative direction; I_{test} = −1 mA	-	−16.5	−14	V
I_{LR}	reverse leakage current	per channel; V_I = 5.0 V	-	-	100	nA
		per channel; V_I = −5.0 V	−100	-	-	nA

[1] Guaranteed by design.

7. Application information

7.1 Application diagram

A typical application diagram showing IP5306CX8 connected between a microphone and the baseband ADC input pins is depicted in Figure 3. The 2 kV ESD compliant pins (A2, A3, B3 and C3) are connected to the baseband interface side while the two 15 kV ESD compliant pins (B1 and C1) are connected to the microphone.

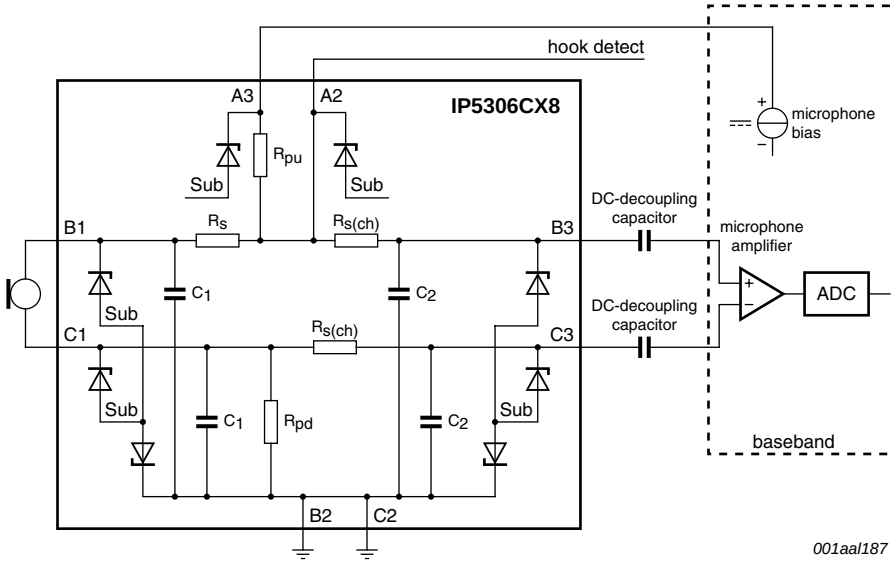


Fig 3. Typical application diagram of IP5306CX8

7.2 Insertion loss

The insertion loss measurement configuration of a typical 50 Ω NetWork Analyzer (NWA) system for evaluation of the IP5306CX8 is shown in Figure 4.

The insertion loss of both microphone channels at frequencies up to 6 GHz is displayed in Figure 5. Pin A3 (microphone biasing supply pin) is shorted to ground, pin A2 (filter channel feedthrough) is left floating (n.c.).

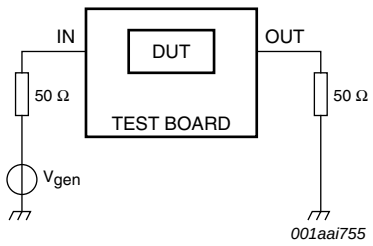
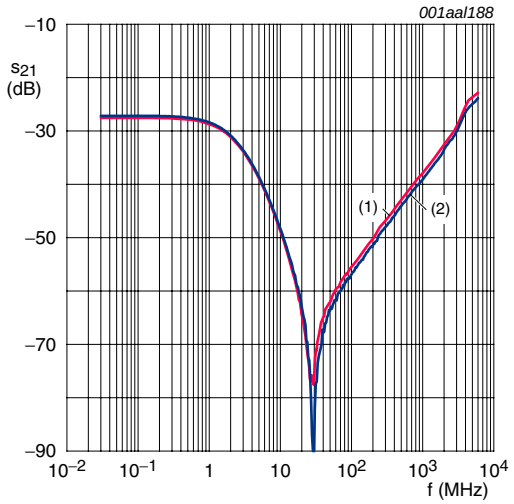


Fig 4. Frequency response measurement configuration



(1) Channel 1 (pins B1 and B3).

(2) Channel 2 (pins C1 and C3).

Fig 5. Measured insertion loss magnitudes

7.3 Crosstalk

The crosstalk measurement configuration of a typical 50 Ω NWA system for evaluation of the IP5306CX8 is shown in Figure 6.

The measured crosstalk within the IP5306CX8 in a 50 Ω NWA system from one channel to the other channel is shown in Figure 7. Pin A3 (microphone biasing supply pin) is shorted to ground, pin A2 (filter channel feedthrough) is left floating (n.c.).

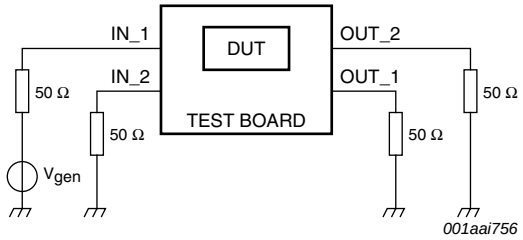
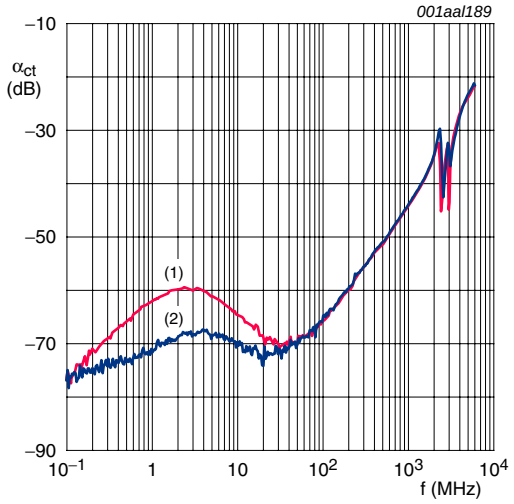


Fig 6. Crosstalk measurement configuration



(1) Channel 1 to channel 2 (pins B1 and C3).

(2) Channel 2 to channel 1 (pins C1 and B3).

Fig 7. Measured crosstalk between adjacent channels

7.4 Voltage dependency of high density capacitors

The high density capacitors integrated in IP5306CX8 show a voltage dependency similar to some higher value discrete ceramic capacitors.

When used in an average mobile application, the typical voltage swing across the capacitance will be in the range of −0.5 V to +4 V. In this event, the capacitor values change proportional to the bias voltage as depicted in Figure 8.

The measurement is performed several times, starting at the 'starting point' at 0 V, increasing to 4 V (arrow 1), decreasing to −0.5 V (following arrow 2) and back to +4 V (arrow 3).

When measuring the capacitance over voltage for voltage swings of e.g. −20 V to +20 V, a hysteresis in the capacitance over $V_{bias(DC)}$ can be observed (see Figure 9), which is inherent to the integration process for the high density capacitors in this product.

Again, the measurement starts at 'starting point', following arrow 1 up to $V_{bias(DC)}$ = 20 V, from there along arrow 2 down to $V_{bias(DC)}$ = −20 V and back via arrow 3 and arrow 4.

Values of C_1 and C_2 specified in Table 4 are based on measurements at the starting point.

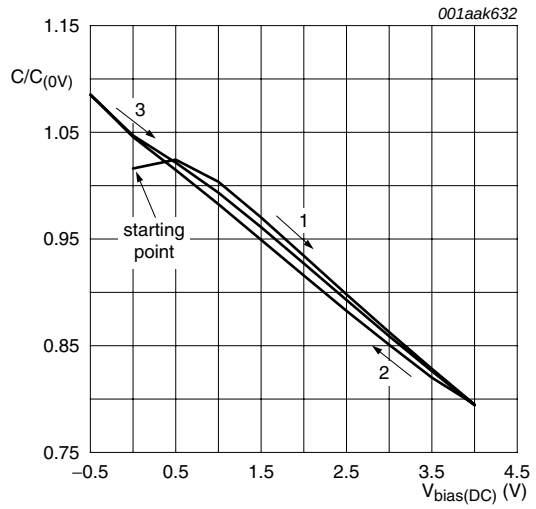


Fig 8. Relative capacitance $C/C_{(0V)}$ of high density capacitors for $-0.5\ V \leq V_{bias(DC)} \leq +4\ V$

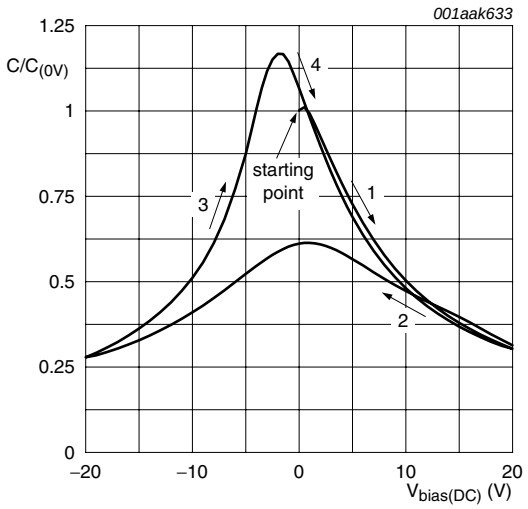


Fig 9. Relative capacitance $C/C_{(0V)}$ of high density capacitors for $-20\ V \leq V_{bias(DC)} \leq +20\ V$

8. Package outline

WLCSP8: wafer level chip-size package; 8 bumps (3 x 3 - A1)

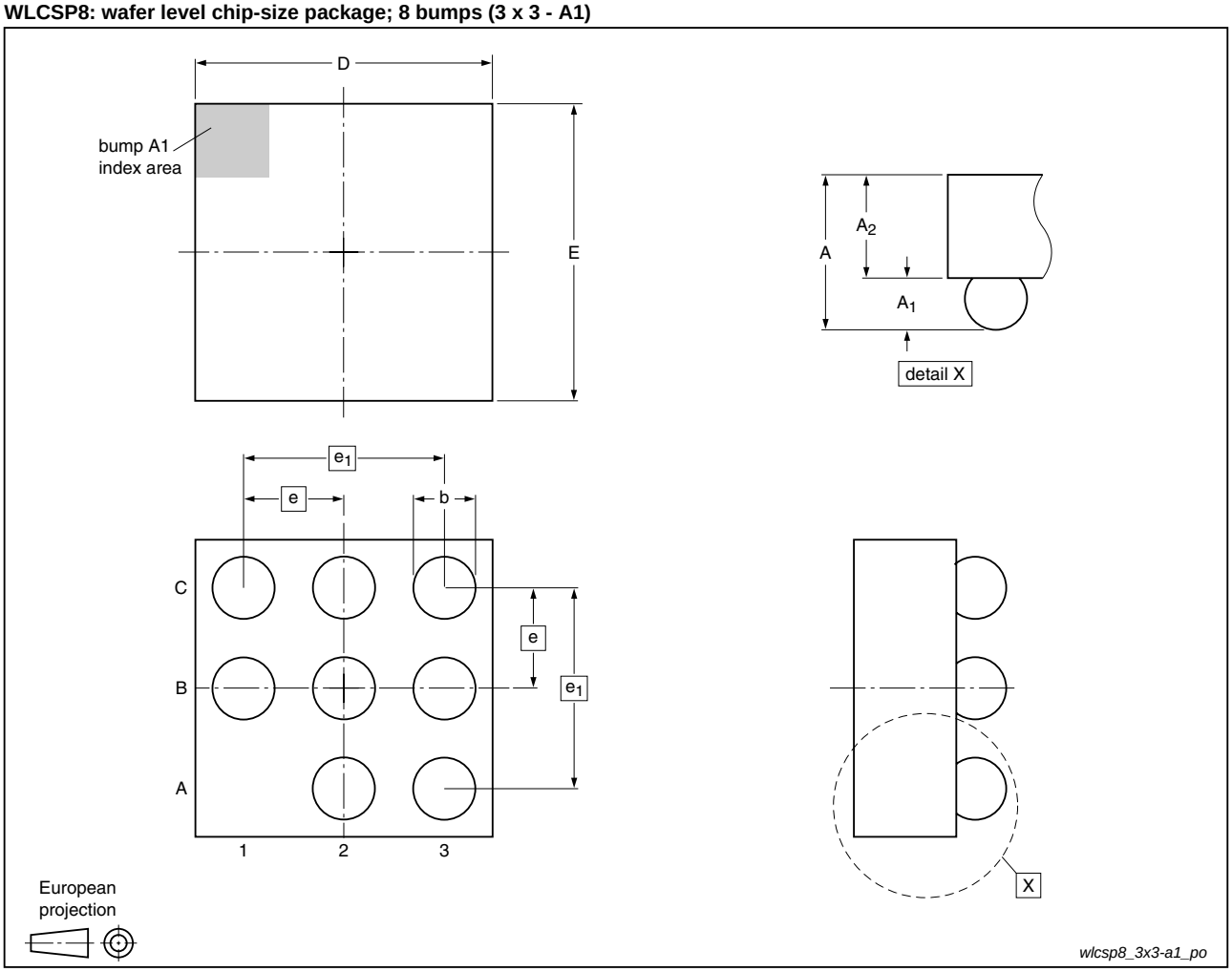


Fig 10. Package outline IP5306CX8 (WLCSP8)

Table 5. Dimensions for Figure 10

Symbol	Min	Typ	Max	Unit
A	0.56	0.61	0.66	mm
A_1	0.18	0.20	0.22	mm
A_2	0.38	0.41	0.44	mm
b	0.21	0.26	0.31	mm
D	1.14	1.19	1.24	mm
E	1.14	1.19	1.24	mm
e	-	0.4	-	mm
e_1	-	0.8	-	mm

9. Soldering of WLCSP packages

9.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note *AN10439 "Wafer Level Chip Scale Package"* and in application note *AN10365 "Surface mount reflow soldering description"*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

9.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

9.3 Reflow soldering

Key characteristics in reflow soldering are:

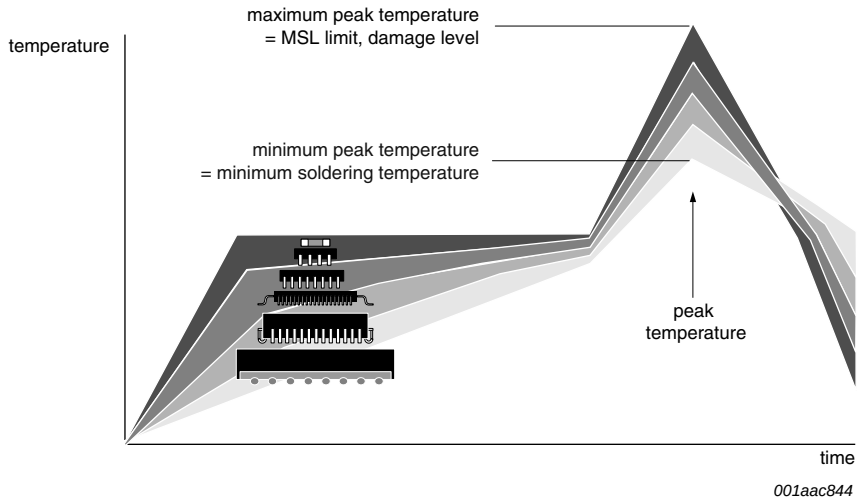
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 11) than a PbSn process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 6.

Table 6. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 11.



MSL: Moisture Sensitivity Level

Fig 11. Temperature profiles for large and small components

For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

9.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

9.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

9.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 "Surface mount reflow soldering description"*.

9.3.4 Cleaning

Cleaning can be done after reflow soldering.

10. Abbreviations

Table 7. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
DUT	Device Under Test
ESD	ElectroStatic Discharge
NWA	NetWork Analyzer
RoHS	Restriction of Hazardous Substances
WLCSP	Wafer-Level Chip-Scale Package

11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP5306CX8_1	20100212	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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