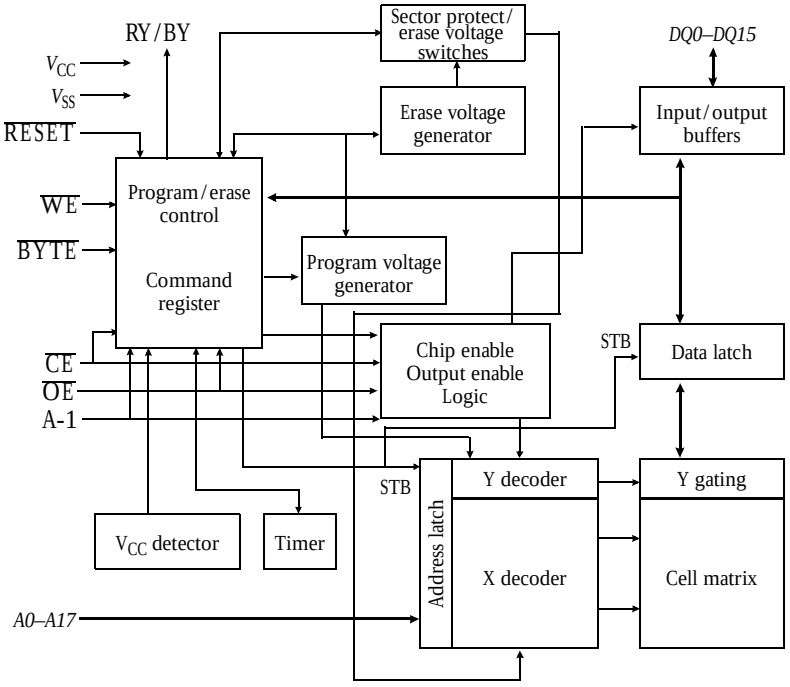
# 3V 512K x 8/256K × 16 CMOS Flash EEPROM

## Features

- Organization: 512Kx8/256Kx16
- Sector architecture
  - One 16K; two 8K; one 32K; and seven 64K byte sectors
  - One 8K; two 4K; one 16K; and seven 32K word sectors
  - Boot code sector architecture—T (top) or B (bottom)
  - Erase any combination of sectors or full chip
- Single 2.7-3.6V power supply for read/write operations
- Sector protection
- High speed 70/80/90/120 ns address access time
- Automated on-chip programming algorithm
  - Automatically programs/verifies data at specified address
- Automated on-chip erase algorithm
  - Automatically preprograms/erases chip or specified sectors
- Hardware $\overline{\text{RESET}}$ pin
  - Resets internal state machine to read mode
- Low power consumption
  - 200 nA typical automatic sleep mode current
  - 200 nA typical standby current
  - 10 mA typical read current
- JEDEC standard software, packages and pinouts
  - 48-pin TSOP
  - 44-pin SO; availability TBD
- Detection of program/erase cycle completion
  - DQ7 $\overline{\text{DATA}}$ polling
  - DQ6 toggle bit
  - DQ2 toggle bit
  - RY/$\overline{\text{BY}}$ output
- Erase suspend/resume
  - Supports reading data from or programming data to a sector not being erased
- Low $V_{CC}$ write lock-out below 1.5V
- 10 year data retention at 150C
- 100,000 write/erase cycle endurance

## Logic block diagram

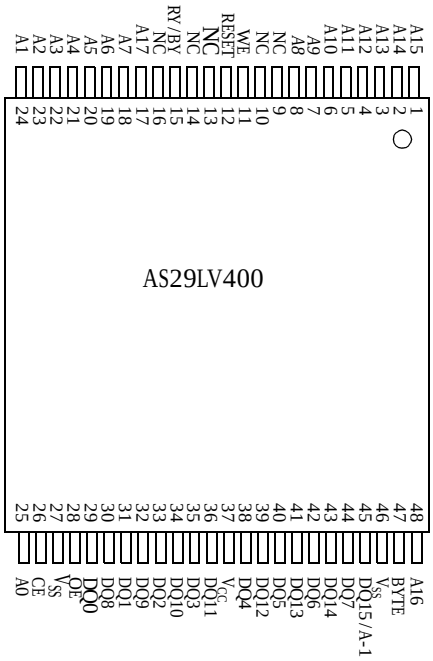



## Selection guide

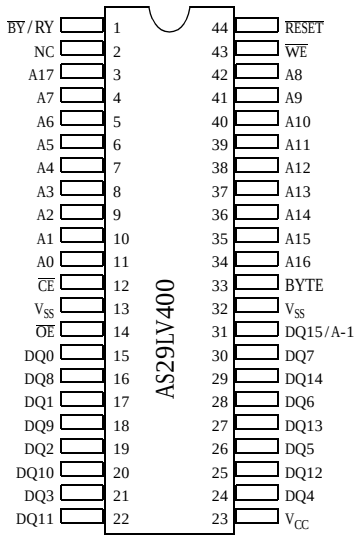
| | | 29LV400-70 | 29LV400-80 | 29LV400-90 | 29LV400-120 | Unit |
|---|---|---|---|---|---|---|
| Maximum access time | $t_{AA}$ | 70 | 80 | 90 | 120 | ns |
| Maximum chip enable access time | $t_{CE}$ | 70 | 80 | 90 | 120 | ns |
| Maximum output enable access time | $t_{OE}$ | 30 | 30 | 35 | 50 | ns |

## Pin assignments:

48-pin TSOP




44-pin SO (availability TBD)



## Functional description

The AS29LV400 is an 4 megabit, 3.0 volt Flash memory organized as 512Kbyte of 8 bits/256Kbytes of 16 bits each. For flexible Erase and Program capability, the 4 megabits of data is divided into eleven sectors: one 16K, two 8K, one 32K, and seven 64k byte sectors; or one 8K, two 4K, one 16K, and seven 32K word sectors. The ×8 data appears on DQ0–DQ7; the ×16 data appears on DQ0–DQ15. The AS29LV400 is offered in JEDEC standard 48-pin TSOP and 44-pin SO. This device is designed to be programmed and erased with a single 3.0V $V_{CC}$ supply. The device can also be reprogrammed in standard EPROM programmers.

The AS29LV400 offers access times of 70/80/90/120 ns, allowing 0-wait state operation of high speed microprocessors. To eliminate bus contention the device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$), and output enable ($\overline{OE}$) controls. Word mode (×16 output) is selected by $\overline{BYTE}$ = high. Byte mode (×8 output) is selected by $\overline{BYTE}$ = low.

The AS29LV400 is fully compatible with the JEDEC single power supply Flash standard. The device uses standard microprocessor write timings to send Write commands to the register. An internal state-machine uses register contents to control the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the Programming and Erase operations. Data is read in the same manner as other Flash or EPROM devices. Use the Program command sequence to invoke the on-chip programming algorithm that automatically times the program pulse widths, and verifies proper cell margin. Use the Erase command sequence to invoke the automated on-chip erase algorithm that preprograms the sector when it is not already programmed before executing the erase operation. The Erase command also times the erase pulse widths and verifies the proper cell margins.

Boot sector architecture enables the system to boot from either the top (AS29LV400T) or the bottom (AS29LV400B) sector. Sector erase architecture allows specified sectors of memory to be erased and reprogrammed without altering data in other sectors. A sector typically erases and verifies within 1.0 seconds. Hardware sector protection disables both the Program and the Erase operations in all, or any combination of the eleven sectors. The device provides true background erase with Erase Suspend, which puts erase operations on hold to either read data from, or program data to, a sector that is not being erased. The Chip Erase command will automatically erase all unprotected sectors.

When shipped from the factory, AS29LV400 is fully erased (all bits = 1). The programming operation sets bits to 0. Data is programmed into the array one byte at a time in any sequence and across sector boundaries. A sector must be erased to change bits from 0 to 1. Erase returns all bytes in a sector to the erased state (all bits = 1). Each sector is erased individually with no effect on other sectors.

The device features a single 3.0V power supply operation for Read, Write, and Erase functions. Internally generated and regulated voltages are provided for the Program and Erase operations. A low $V_{CC}$ detector automatically inhibits write operations during power transtitions. The RY/$\overline{BY}$ pin, $\overline{DATA}$ polling of DQ7, or toggle bit (DQ6) may be used to detect the end of the program or to erase operations. The device automatically resets to the Read mode after the Program or Erase operations are completed. DQ2 indicates which sectors are being erased.

The AS29LV400 resists accidental erasure or spurious programming signals resulting from power transitions. The Control register architecture permits alteration of memory contents only when successful completion of specific command sequences has occured. During power up, the device is set to Read mode with all Program/Erase commands disabled if $V_{CC}$ is less than $V_{LKO}$ (lockout voltage). The command registers are not affected by noise pulses of less than 5 ns on $\overline{OE}$, $\overline{CE}$, or $\overline{WE}$. To initiate Write commands, $\overline{CE}$ and $\overline{WE}$ must be a logical zero and $\overline{OE}$ a logical 1.

When the device's hardware $\overline{RESET}$ pin is driven low, any Program/Erase operation in progress is terminated and the internal state machine is reset to Read mode. If the $\overline{RESET}$ pin is tied to the system reset circuitry and a system reset occurs during an automated on-chip Program/Erase algorithm, the operating data in the address locations may become corrupted and require rewriting. Resetting the device enables the system's microprocessor to read boot-up firmware from the Flash memory.

The AS29LV400 uses Fowler-Nordheim tunnelling to electrically erase all bits within a sector simultaneously. Bytes are programmed one at a time using the EPROM programming mechanism of hot electron injection.

## Operating modes

| Mode | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | A0 | A1 | A6 | A9 | $\overline{RESET}$ | DQ |
|---|---|---|---|---|---|---|---|---|---|
| ID read MFR code | L | L | H | L | L | L | $V_{ID}$ | H | Code |
| ID read device code | L | L | H | H | L | L | $V_{ID}$ | H | Code |
| Read | L | L | H | A0 | A1 | A6 | A9 | H | $D_{OUT}$ |
| Standby | H | X | X | X | X | X | X | H | High Z |
| Output disable | L | H | H | X | X | X | X | H | High Z |
| Write | L | H | L | A0 | A1 | A6 | A9 | H | $D_{IN}$ |
| Enable sector protect | L | $V_{ID}$ | Pulse/L | L | H | L | $V_{ID}$ | H | X |
| Sector unprotect | L | $V_{ID}$ | Pulse/L | L | H | H | $V_{ID}$ | H | X |
| Temporary sector unprotect | X | X | X | X | X | X | X | $V_{ID}$ | X |
| Verify sector protect† | L | L | H | L | H | L | $V_{ID}$ | H | Code |
| Verify sector unprotect† | L | L | H | L | H | H | $V_{ID}$ | H | Code |
| Hardware Reset | X | X | X | X | X | X | X | L | High Z |

L = Low ($<V_{IL}$) = logic 0; H = High ($>V_{IH}$) = logic 1; $V_{ID}$ = 10.0 ± 1.0V; X = don't care.
In ×16 mode, BYTE = $V_{IH}$. In ×8 mode, BYTE = $V_{IL}$ with DQ8-DQ14 in high Z and DQ15 = A-1.
†Verification of sector protect/unprotect during A9 = $V_{ID}$.

## Mode definitions

| Item | Description |
|---|---|
| ID MFR code, device code | Selected by A9 = $V_{ID}$(9.5V–10.5V), $\overline{CE}$ = $\overline{OE}$ = A1 = A6 = L, enabling outputs. When A0 is low ($V_{IL}$) the output data = 52h, a unique Mfr. code for Alliance Semiconductor Flash products. When A0 is high ($V_{IH}$), $D_{OUT}$ represents the device code for the AS29LV400. |
| Read mode | Selected with $\overline{CE}$ = $\overline{OE}$ = L, $\overline{WE}$ = H. Data is valid in $t_{ACC}$ time after addresses are stable, $t_{CE}$ after $\overline{CE}$ is low and $t_{OE}$ after $\overline{OE}$ is low. |
| Standby | Selected with $\overline{CE}$ = H. Part is powered down, and $I_{CC}$ reduced to <1.0 µA when $\overline{CE}$ = $V_{CC}$ ± 0.3V = $\overline{RESET}$. If activated during an automated on-chip algorithm, the device completes the operation before entering standby. |
| Output disable | Part remains powered up; but outputs disabled with $\overline{OE}$ pulled high. |
| Write | Selected with $\overline{CE}$ = $\overline{WE}$ = L, $\overline{OE}$ = H. Accomplish all Flash erasure and programming through the command register. Contents of command register serve as inputs to the internal state machine. Address latching occurs on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs later. Data latching occurs on the rising edge $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Filters on $\overline{WE}$ prevent spurious noise events from appearing as write commands. |
| Enable sector protect | Hardware protection circuitry implemented with external programming equipment causes the device to disable program and erase operations for specified sectors. For in-system sector protection, refer to Sector protect algorithm on page 12. |
| Sector unprotect | Disables sector protection for all sectors using external programming equipment. All sectors must be protected prior to sector unprotection. For in-system sector unprotection, refer to Sector unprotect algorithm on page 12. |
| Verify sector protect/ unprotect | Verifies write protection for sector. Sectors are protected from program/erase operations on commercial programming equipment. Determine if sector protection exists in a system by writing the ID read command sequence and reading location XXX02h, where address bits A12–17 select the defined sector addresses. A logical 1 on DQ0 indicates a protected sector; a logical 0 indicates an unprotected sector. |
| Temporary sector unprotect | Temporarily disables sector protection for in-system data changes to protected sectors. Apply +10V to $\overline{RESET}$ to activate temporary sector unprotect mode. During temporary sector unprotect mode, program protected sectors by selecting the appropriate sector address. All protected sectors revert to protected state on removal of +10V from $\overline{RESET}$. |
| $\overline{RESET}$ | Resets the interal state machine to read mode. If device is programming or erasing when $\overline{RESET}$ = L, data may be corrupted. |
| Deep power down | Hold $\overline{RESET}$ low to enter deep power down mode (<1 µA). Recovery time to start of first read cycle is 50ns. |
| Automatic sleep mode | Enabled automatically when addresses remain stable for 300ns. Typical current draw is 1 µA. Existing data is available to the system during this mode. If an address is changed, automatic sleep mode is disabled and new data is returned within standard access times. |

## Flexible sector architecture

| Sector | Bottom boot sector architecture (AS29LV400B) | | | Top boot sector architecture (AS29LV400T) | | |
|---|---|---|---|---|---|---|
| | ×8 | ×16 | Size (Kbytes) | ×8 | ×16 | Size (Kbytes) |
| 0 | 00000h–03FFFh | 00000h–01FFFh | 16 | 00000h–0FFFFh | 00000h–07FFFh | 64 |
| 1 | 04000h–05FFFh | 02000h–02FFFh | 8 | 10000h–1FFFFh | 08000h–0FFFFh | 64 |
| 2 | 06000h–07FFFh | 03000h–03FFFh | 8 | 20000h–2FFFFh | 10000h–17FFFh | 64 |
| 3 | 08000h–0FFFFh | 04000h–07FFFh | 32 | 30000h–3FFFFh | 18000h–1FFFFh | 64 |
| 4 | 10000h–1FFFFh | 08000h–0FFFFh | 64 | 40000h–4FFFFh | 20000h–27FFFh | 64 |
| 5 | 20000h–2FFFFh | 10000h–17FFFh | 64 | 50000h–5FFFFh | 28000h–2FFFFh | 64 |
| 6 | 30000h–3FFFFh | 18000h–1FFFFh | 64 | 60000h–6FFFFh | 30000h–37FFFh | 64 |
| 7 | 40000h–4FFFFh | 20000h–27FFFh | 64 | 70000h–77FFFh | 38000h–3BFFFh | 32 |
| 8 | 50000h–5FFFFh | 28000h–2FFFFh | 64 | 78000h–79FFFh | 3C000h–3CFFFh | 8 |
| 9 | 60000h–6FFFFh | 30000h–37FFFh | 64 | 7A000h–7BFFFh | 3D000h–3DFFFh | 8 |
| 10 | 70000h–7FFFFh | 38000h–3FFFFh | 64 | 7C000h–7FFFFh | 3E000h–3FFFFh | 16 |

In word mode, there are one 8K word, two 4K word, one 16K word, and seven 32K word sectors. Address range is A17–A-1 if $\overline{BYTE}$ = $V_{IL}$; address range is A17–A0 if $\overline{BYTE}$ = $V_{IH}$.

## ID Sector address table

| Sector | Bottom boot sector address (AS29LV400B) | | | | | | Top boot sector address (AS29LV400T) | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | A17 | A16 | A15 | A14 | A13 | A12 | A17 | A16 | A15 | A14 | A13 | A12 |
| 0 | 0 | 0 | 0 | 0 | 0 | X | 0 | 0 | 0 | X | X | X |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | X | X | X |
| 2 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | X | X | X |
| 3 | 0 | 0 | 0 | 1 | X | X | 0 | 1 | 1 | X | X | X |
| 4 | 0 | 0 | 1 | X | X | X | 1 | 0 | 0 | X | X | X |
| 5 | 0 | 1 | 0 | X | X | X | 1 | 0 | 1 | X | X | X |
| 6 | 0 | 1 | 1 | X | X | X | 1 | 1 | 0 | X | X | X |
| 7 | 1 | 0 | 0 | X | X | X | 1 | 1 | 1 | 0 | X | X |
| 8 | 1 | 0 | 1 | X | X | X | 1 | 1 | 1 | 1 | 0 | 0 |
| 9 | 1 | 1 | 0 | X | X | X | 1 | 1 | 1 | 1 | 0 | 1 |
| 10 | 1 | 1 | 1 | X | X | X | 1 | 1 | 1 | 1 | 1 | X |

## READ codes

| Mode | | A17–A12 | A6 | A1 | A0 | Code |
|---|---|---|---|---|---|---|
| MFR code (Alliance Semiconductor) | | X | L | L | L | 52h |
| Device code | ×8 T boot | X | L | L | H | B9h |
| | ×8 B boot | X | L | L | H | BAh |
| | ×16 T boot | X | L | L | H | 22B9h |
| | ×16 B boot | X | L | L | H | 22BAh |
| Sector protection | | Sector address | L | H | L | 01h protected<br>00h unprotected |

Key: L =Low (<$V_{IL}$); H = High (>$V_{IH}$); X =Don't care

## Command format

| Command sequence | | Required bus write cycles | 1st bus cycle | | 2nd bus cycle | | 3rd bus cycle | | 4th bus cycle | | 5th bus cycle | | 6th bus cycle | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Address | Data | Address | Data | Address | Data | Address | Data | Address | Data | Address | Data |
| Reset/Read | | 1 | XXXh | F0h | Read Address | Read Data | | | | | | | | |
| Reset/ Read | ×16 | 3 | 555h | AAh | 2AAh | 55h | 555h | F0h | Read Address | Read Data | | | | |
| | ×8 | | AAAh | | 555h | | AAAh | | | | | | | |
| Autoselect ID Read | ×16 | 3 | 555h | AAh | 2AAh | 55h | 555h | 90h | 01h Device code | 22B9h (T) 22BAh (B) | | | | |
| | ×8 | | AAAh | | 555h | | AAAh | | 02h Device code | B9h(T) BAh(B) | | | | |
| | ×16 | | 555h | AAh | 2AAh | 55h | 555h | 90h | 00h MFR code | 0052h | | | | |
| | ×8 | | AAAh | | 555h | | AAAh | | | 52h | | | | |
| | ×16 | | 555h | AAh | 2AAh | 55h | 555h | 90h | XXX02h Sector protection | 0001h = protected 0000h = unprotected | | | | |
| | ×8 | | AAAh | | 555h | | AAAh | | XXX04h Sector protection | 0001h=protected 0000h=unprotected | | | | |
| Program | ×16 | 4 | 555h | AAh | 2AAh | 55h | 555h | A0h | Program Address | Program Data | | | | |
| | ×8 | | AAAh | | 555h | | AAAh | | | | | | | |
| Unlock bypass | ×16 | 3 | 555 | AAh | 2AA | 55h | 555 | 20h | | | | | | |
| | ×8 | | AAA | | 555 | | AAA | | | | | | | |
| Unlock bypass program | | 2 | XXX | A0h | Program address | Program data | | | | | | | | |
| Unlock bypass reset | | 2 | XXX | 90h | XXX | 00h | | | | | | | | |
| Chip Erase | ×16 | 6 | 555h | AAh | 2AAh | 55h | 555h | 80h | 555h | AAh | 2AAh | 55h | 555h | 10h |
| | ×8 | | AAAh | | 555h | | AAAh | | AAAh | | 555h | | AAAh | |
| Sector Erase | ×16 | 6 | 555h | AAh | 2AAh | 55h | 555h | 80h | 555h | AAh | 2AAh | 55h | Sector Address | 30h |
| | ×8 | | AAAh | | 555h | | AAAh | | AAAh | | 555h | | | |
| Sector Erase Suspend | | 1 | XXXh | B0h | | | | | | | | | | |
| Sector Erase Resume | | 1 | XXXh | 30h | | | | | | | | | | |

1 Bus operations defined in "Mode definitions," on page 3.

2 Reading from and programming to non-erasing sectors allowed in Erase Suspend mode.

3 Address bits A11-A17 = X = Don't Care for all address commands except where Program Address and Sector Address are required.

4 Data bits DQ15-DQ8 are don't care for unlock and command cycles.

5 The Unlock Bypass command must be initiated before the Unlock Bypass Program command.

6 The Unlock Bypass Reset command returns the device to reading array data when it is in the unlock bypass mode.

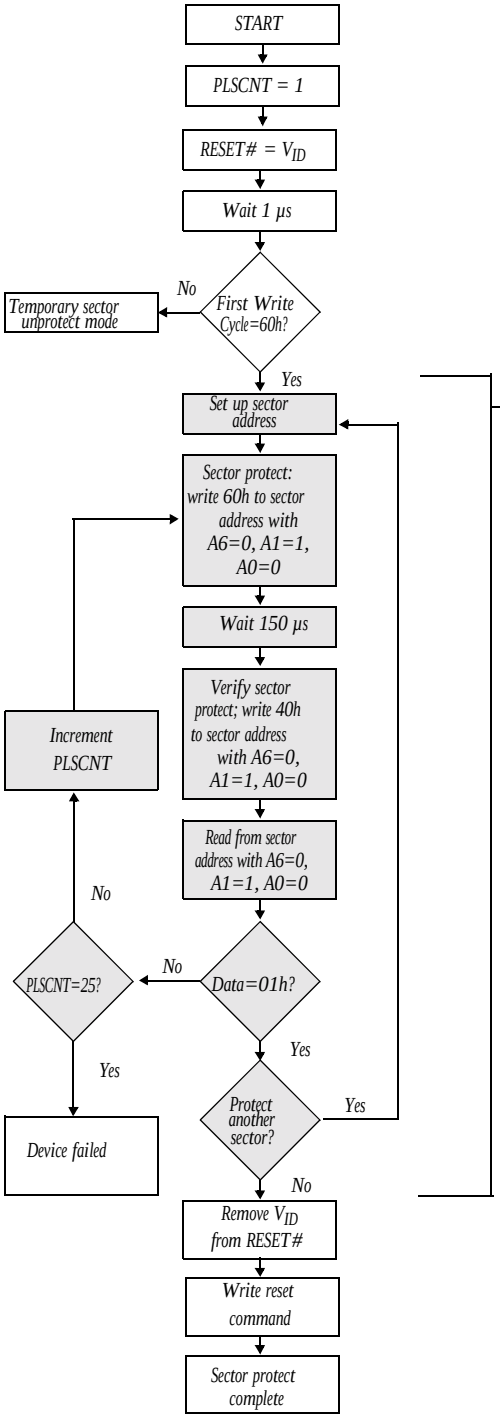
## Command definitions

| Item | Description |
|---|---|
| Reset/Read | Initiate read or reset operations by writing the Read/Reset command sequence into the command register. This allows the microprocessor to retrieve data from the memory. Device remains in read mode until command register contents are altered.<br><br>Device automatically powers up in read/reset state. This feature allows only reads, therefore ensuring no spurious memory content alterations during power up. |
| ID Read | AS29LV400 provides manufacturer and device codes in two ways. External PROM programmers typically access the device codes by driving +10V on A9. AS29LV400 also contains an ID Read command to read the device code with only +3V, since multiplexing +10V on address lines is generally undesirable.<br><br>Initiate device ID read by writing the ID Read command sequence into the command register. Follow with a read sequence from address XXX00h to return MFR code. Follow ID Read command sequence with a read sequence from address XXX01h to return device code.<br><br>To verify write protect status on sectors, read address XXX02h. Sector addresses A17–A12 produce a 1 on DQ0 for protected sector and a 0 for unprotected sector.<br><br>Exit from ID read mode with Read/Reset command sequence. |
| Hardware Reset | Holding $\overline{\text{RESET}}$ low for 500 ns resets the device, terminating any operation in progress; data handled in the operation is corrupted. The internal state machine resets 20 µs after $\overline{\text{RESET}}$ is driven low. RY/$\overline{\text{BY}}$ remains low until internal state machine resets. After $\overline{\text{RESET}}$ is set high, there is a delay of 50 ns for the device to permit read operations. |
| Byte/word Programming | Programming the AS29LV400 is a four bus cycle operation performed on a byte-by-byte or word-by-word basis. Two unlock write cycles precede the Program Setup command and program data write cycle. Upon execution of the program command, no additional CPU controls or timings are necessary. Addresses are latched on the falling edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever is last; data is latched on the rising edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever is first. The AS29LV400's automated on-chip program algorithm provides adequate internally-generated programming pulses and verifies the programmed cell margin.<br><br>Check programming status by sampling data on the RY/$\overline{\text{BY}}$ pin, or either the $\overline{\text{DATA}}$ polling (DQ7) or toggle bit (DQ6) at the program address location. The programming operation is complete if DQ7 returns equivalent data, if DQ6 = no toggle, or if RY/$\overline{\text{BY}}$ pin = high.<br><br>The AS29LV400 ignores commands written during programming. A hardware reset occurring during programming may corrupt the data at the programmed location.<br><br>AS29LV400 allows programming in any sequence, across any sector boundary. Changing data from 0 to 1 requires an erase operation. Attempting to program data 0 to 1 results in either DQ5 = 1 (exceeded programming time limits); reading this data after a read/reset operation returns a 0. When programming time limit is exceeded, DQ5 reads high, and DQ6 continues to toggle. In this state, a Reset command returns the device to read mode. |

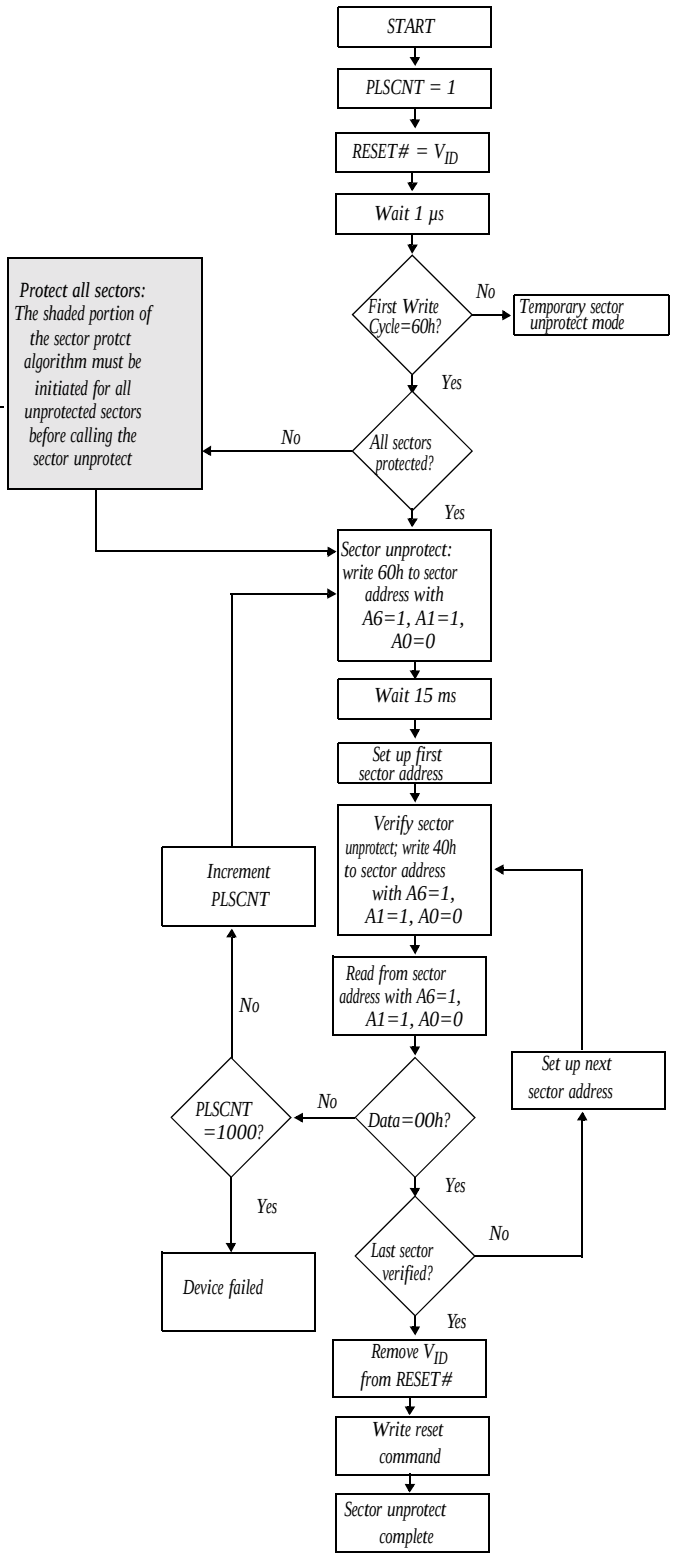
| Item | Description |
|---|---|
| Unlock Bypass Command Sequence | The unlock bypass feature increases the speed at which the system programs bytes or words to the device because it bypasses the first two unlock cycles of the standard program command sequence.<br><br>To initiate the unlock bypass command sequence, two unlock cycles must be written, then followed by a third cycle which has the unlock bypass command, 20h.<br><br>The device then begins the unlock bypass mode. In order to program in this mode, a two cycle unlock bypass program sequence is required. The first cycle has the unlock bypass program command, A0h. It is followed by a second cycle which has the program address and data. To program additional data, the same sequence must be followed.<br><br>The unlock bypass mode has two valid commands, the Unlock Bypass Program command and the Unlock Bypass Reset command. The only way the system can exit the unlock bypass mode is by issuing the unlock bypass reset command sequence. This sequence involves two cycles. The first cycle contains the data, 90h. The second cycle contains the data 00h. Addresses are don't care for both cycles. The device then returns to reading array data. |
| Chip Erase | Chip erase requires six bus cycles: two unlock write cycles; a setup command, two additional unlock write cycles; and finally the Chip Erase command.<br><br>Chip erase does not require logical 0s to be written prior to erasure. When the automated on-chip erase algorithm is invoked with the Chip Erase command sequence, AS29LV400 automatically programs and verifies the entire memory array for an all-zero pattern prior to erase. The 29LV400 returns to read mode upon completion of chip erase unless DQ5 is set high as a result of exceeding time limit. |
| Sector Erase | Sector erase requires six bus cycles: two unlock write cycles, a setup command, two additional unlock write cycles, and finally the Sector Erase command. Identify the sector to be erased by addressing any location in the sector. The address is latched on the falling edge of $\overline{WE}$; the command, 30h is latched on the rising edge of $\overline{WE}$. The sector erase operation begins after a sector erase time-out.<br><br>To erase multiple sectors, write the Sector Erase command to each of the addresses of sectors to erase after following the six bus cycle operation above. Timing between writes of additional sectors must be less than the erase time-out period, or the AS29LV400 ignores the command and erasure begins. During the time-out period any falling edge of $\overline{WE}$ resets the time-out. Any command (other than Sector Erase or Erase Suspend) during time-out period resets the AS29LV400 to read mode, and the device ignores the sector erase command string. Erase such ignored sectors by restarting the Sector Erase command on the ignored sectors.<br><br>The entire array need not be written with 0s prior to erasure. AS29LV400 writes 0s to the entire sector prior to electrical erase; writing of 0s affects only selected sectors, leaving non-selected sectors unaffected. AS29LV400 requires no CPU control or timing signals during sector erase operations.<br><br>Automatic sector erase begins after sector erase time-out from the last rising edge of $\overline{WE}$ from the sector erase command stream and ends when the $\overline{DATA}$ polling (DQ7) is logical 1. $\overline{DATA}$ polling address must be performed on addresses that fall within the sectors being erased. AS29LV400 returns to read mode after sector erase unless DQ5 is set high by exceeding the time limit. |

| Item | Description |
|---|---|
| Erase Suspend | Erase Suspend allows interruption of sector erase operations to read data from or program data to a sector not being erased. Erase suspend applies only during sector erase operations, including the time-out period. Writing an Erase Suspend command during sector erase time-out results in immediate termination of the time-out period and suspension of erase operation.<br><br>AS29LV400 ignores any commands during erase suspend other than Read/Reset, Program or Erase Resume commands. Writing the Erase Resume Command continues erase operations. Addresses are Don't Care when writing Erase Suspend or Erase Resume commands.<br><br>AS29LV400 takes 0.2–15 µs to suspend erase operations after receiving Erase Suspend command. To determine completion of erase suspend, either check DQ6 after selecting an address of a sector not being erased, or poll RY/$\overline{BY}$. Check DQ2 in conjunction with DQ6 to determine if a sector is being erased. AS29LV400 ignores redundant writes of Erase Suspend.<br><br>While in erase-suspend mode, AS29LV400 allows reading data (erase-suspend-read mode) from or programming data (erase-suspend-program mode) to any sector not undergoing sector erase; these operations are treated as standard read or standard programming mode. AS29LV400 defaults to erase-suspend-read mode while an erase operation has been suspended.<br><br>Write the Resume command 30h to continue operation of sector erase. AS29LV400 ignores redundant writes of the Resume command. AS29LV400 permits multiple suspend/resume operations during sector erase. |
| Sector Protect | When attempting to write to a protected sector, $\overline{DATA}$ polling and Toggle Bit 1 (DQ6) are activated for about <1 µs. When attempting to erase a protected sector, $\overline{DATA}$ polling and Toggle Bit 1 (DQ6) are activated for about <5 µs. In both cases, the device returns to read mode without altering the specified sectors. |
| Ready/Busy | RY/$\overline{BY}$ indicates whether an automated on-chip algorithm is in progress (RY/$\overline{BY}$ = low) or completed (RY/$\overline{BY}$ = high). The device does not accept Program/Erase commands when RY/$\overline{BY}$ = low. RY/$\overline{BY}$= high when device is in erase suspend mode. RY/$\overline{BY}$ = high when device exceeds time limit, indicating that a program or erase operation has failed. RY/$\overline{BY}$ is an open drain output, enabling multiple RY/$\overline{BY}$ pins to be tied in parallel with a pull up resistor to $V_{CC}$. |

## Sector protect algorithm




## Sector unprotect algorithm



## Status operations

| | |
|---|---|
| $\overline{\text{DATA}}$ polling (DQ7) | Only active during automated on-chip algorithms or sector erase time outs. DQ7 reflects complement of data last written when read during the automated on-chip program algorithm (0 during erase algorithm); reflects true data when read after completion of an automated on-chip program algorithm (1 after completion of erase agorithm). |
| Toggle bit 1 (DQ6) | Active during automated on-chip algorithms or sector erase time outs. DQ6 toggles when $\overline{\text{CE}}$ or $\overline{\text{OE}}$ toggles, or an Erase Resume command is invoked. DQ6 is valid after the rising edge of the fourth pulse of $\overline{\text{WE}}$ during programming; after the rising edge of the sixth $\overline{\text{WE}}$ pulse during chip erase; after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse for sector erase. For protected sectors, DQ6 toggles for <1 µs during program mode writes, and <5 µs during erase (if all selected sectors are protected). |
| Exceeding time limit (DQ5) | Indicates unsuccessful completion of program/erase operation (DQ5 = 1). $\overline{\text{DATA}}$ polling remains active. If DQ5 = 1 during chip erase, all or some sectors are defective; during byte programming or sector erase, the sector is defective (in this case, reset the device and execute a program or erase command sequence to continue working with functional sectors). Attempting to program 0 to 1 will set DQ5 = 1. |
| Sector erase timer (DQ3) | Checks whether sector erase timer window is open. If DQ3 = 1, erase is in progress; no commands will be accepted. If DQ3 = 0, the device will accept sector erase commands. Check DQ3 before and after each Sector Erase command to verify that the command was accepted. |
| Toggle bit 2 (DQ2) | During sector erase, DQ2 toggles with $\overline{\text{OE}}$ or $\overline{\text{CE}}$ only during an attempt to read a sector being erased. During chip erase, DQ2 toggles with $\overline{\text{OE}}$ or $\overline{\text{CE}}$ for all addresses. If DQ5 = 1, DQ2 toggles only at sector addresses where failure occurred, and will not toggle at other sector addresses. Use DQ2 in conjunction with DQ6 to determine whether device is in auto erase or erase suspend mode. |

## Write operation status

| | Status | DQ7 | DQ6 | DQ5 | DQ3 | DQ2 | RY/$\overline{\text{BY}}$ |
|---|---|---|---|---|---|---|---|
| Standard mode | Auto programming | $\overline{\text{DQ}}$7 | Toggle | 0 | N/A | No toggle | 0 |
| | Program/erase in auto erase | 0 | Toggle | 0 | 1 | Toggle† | 0 |
| Erase suspend mode | Read erasing sector | 1 | No toggle | 0 | N/A | Toggle | 1 |
| | Read non-erasing sector | Data | Data | Data | Data | Data | 1 |
| | Program in erase suspend | $\overline{\text{DQ}}$7 | Toggle | 0 | N/A | Toggle† | 0 |
| Exceeded time limits | Auto programming (byte) | $\overline{\text{DQ}}$7 | Toggle | 1 | N/A | No toggle | 1 |
| | Program/erase in auto erase | 0 | Toggle | 1 | N/A | Toggle† | 1 |
| | Program in erase suspend (non-erase suspended sector) | $\overline{\text{DQ}}$7 | Toggle | 1 | N/A | No toggle | 1 |

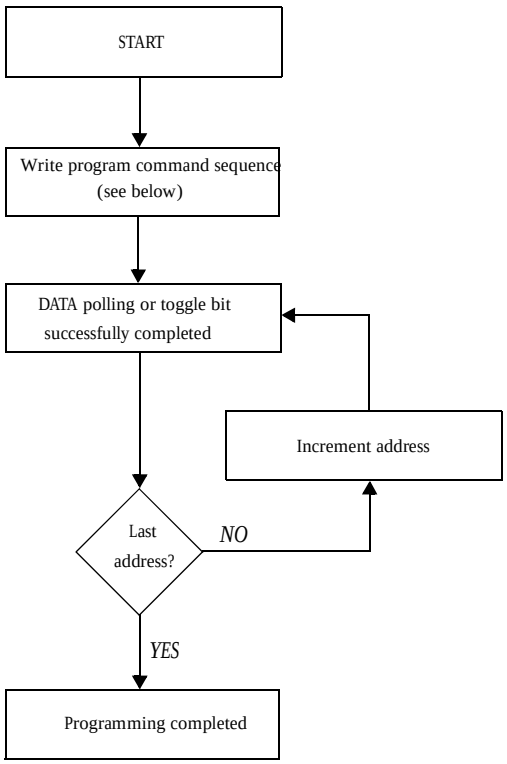
DQ2 toggles when an erase-suspended sector is read repeatedly.

DQ6 toggles when any address is read repeatedly.

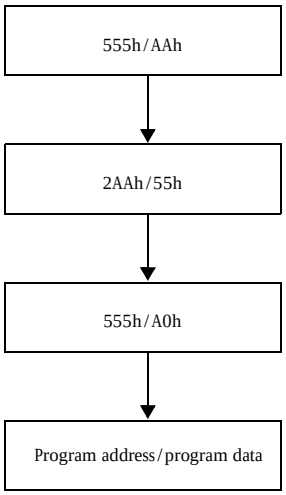
DQ2 = 1 if byte address being programmed is read during erase-suspend program mode.

†DQ2 toggles when the read address applied points to a sector which is undergoing erase, suspended erase, or a failure to erase.

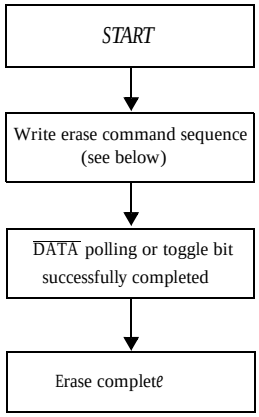
## Automated on-chip programming algorithm



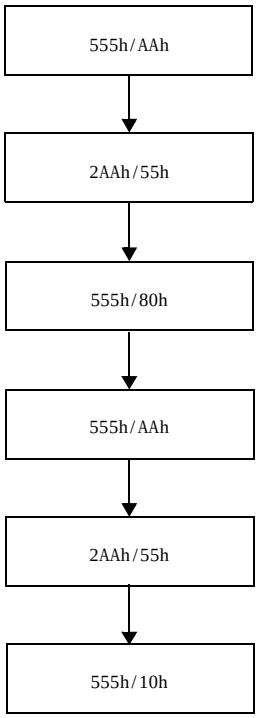

Program command sequence
×16 mode (address/data):



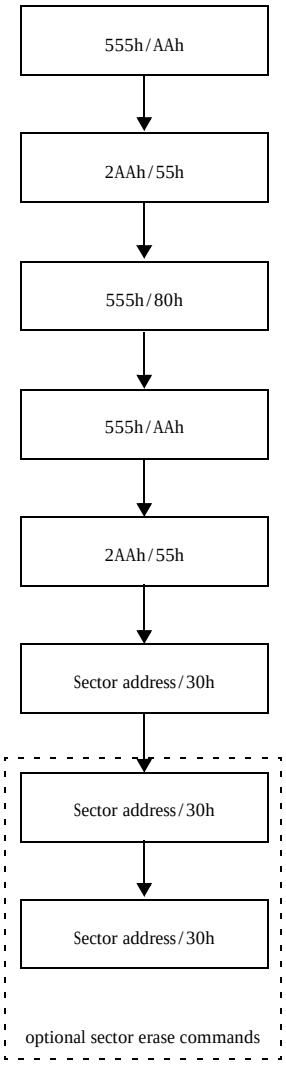

## Automated on-chip erase algorithm




Chip erase command sequence
×16 mode (address/data):

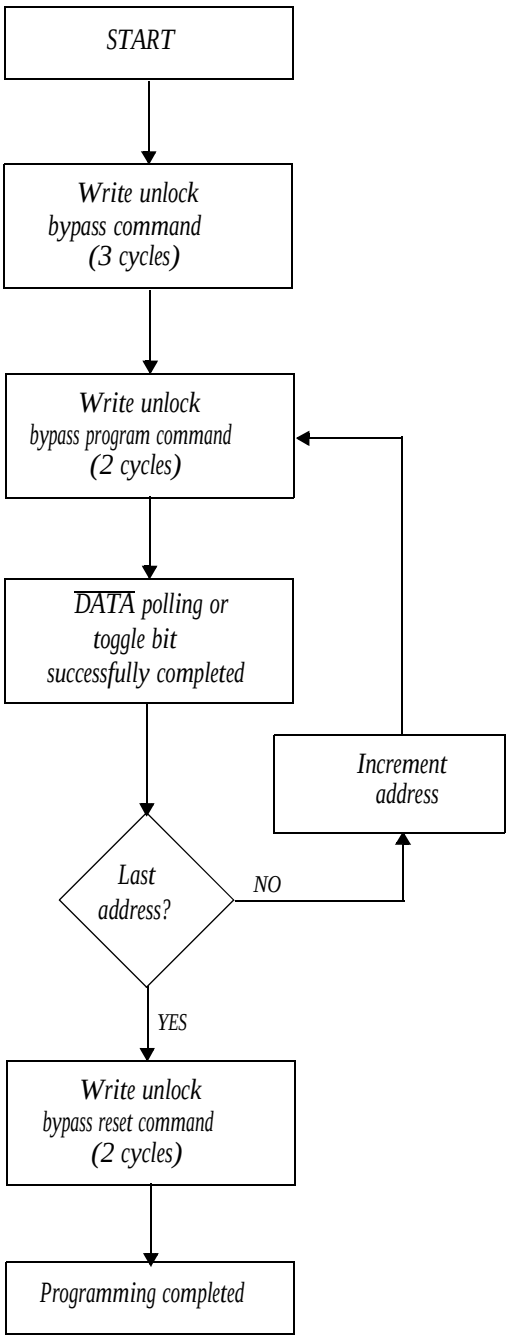



Individual sector/multiple sector erase command sequence
×16 mode (address/data):

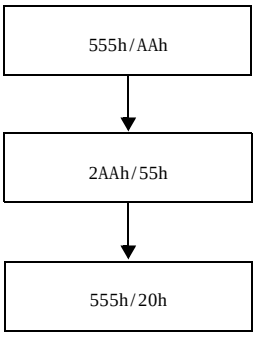



† The system software should check the status of DQ3 prior to and following each subsequent sector erase command to ensure command completion. The device may not have accepted the command if DQ3 is high on second status check.

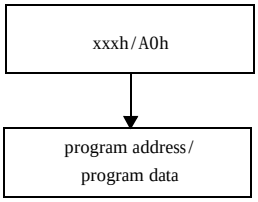
## Programming using unlock bypass command



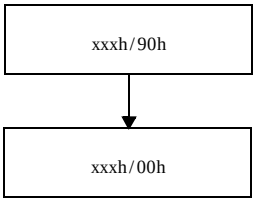

Unlock bypass command sequence
x16 mode (address/data)



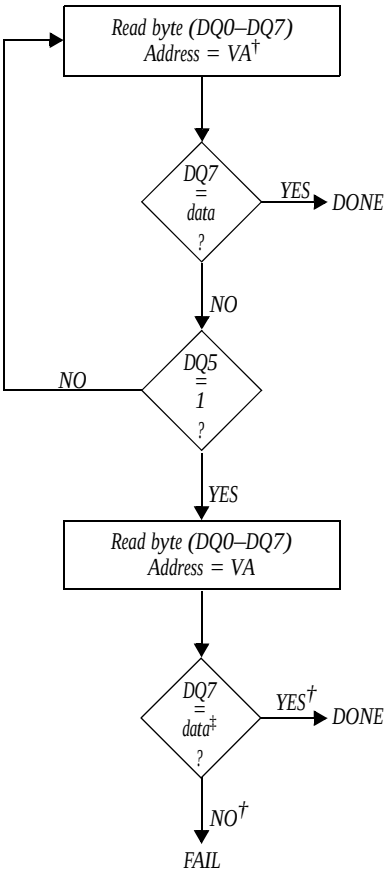

Unlock bypass program command sequence
x16 mode (address/data)




Unlock bypass reset command sequence
x16 mode (address/data)



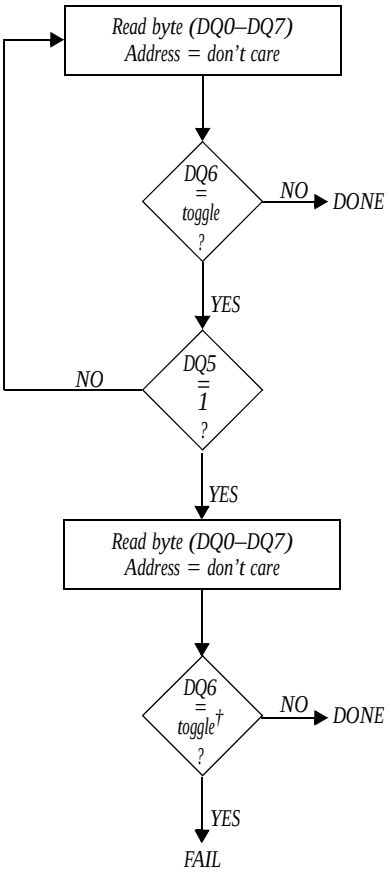
## Data polling algorithm




† VA = Byte address for programming. VA = any of the sector addresses within the sector being erased during Sector Erase. VA = valid address equals any non-protected sector group address during Chip Erase.

‡ DQ7 rechecked even if DQ5 = 1 because DQ5 and DQ7 may not change simultaneously.

## Toggle bit algorithm




†DQ6 rechecked even if DQ5 = 1 because DQ6 may stop toggling when DQ5 changes to 1.

## DC electrical characteristics

$V_{CC}$ = 2.7–3.6V

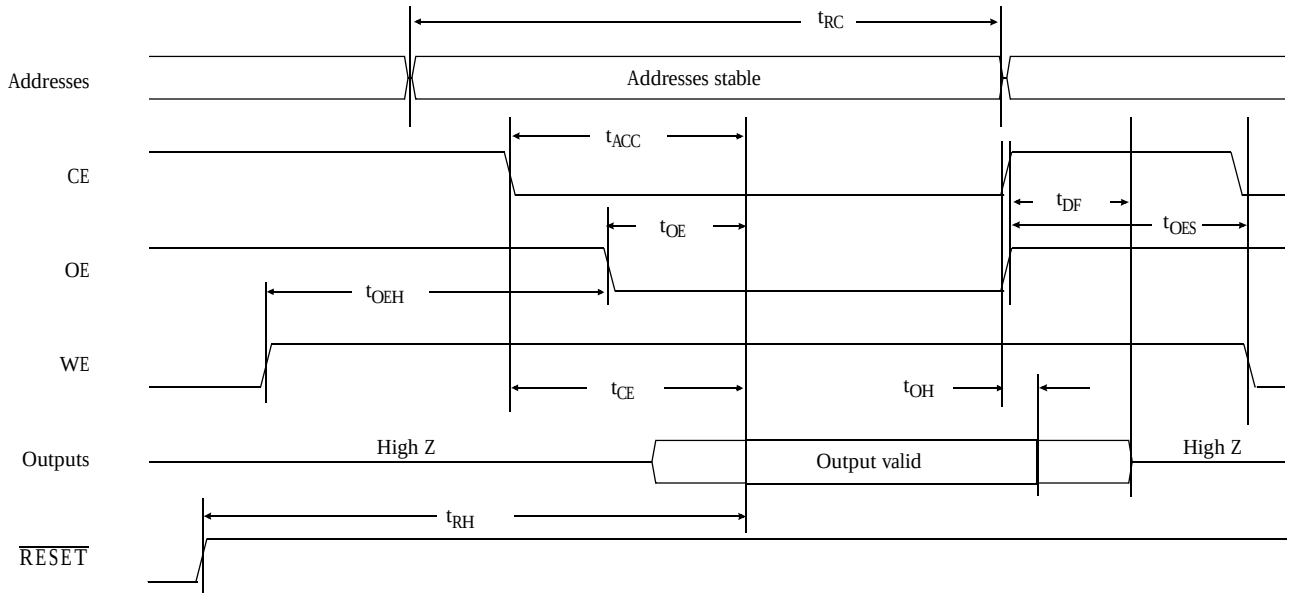
| Parameter | Symbol | Test conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| Input load current | $I_{LI}$ | $V_{IN} = V_{SS}$ to $V_{CC}$, $V_{CC} = V_{CC\ MAX}$ | - | ±1 | µA |
| A9 Input load current | $I_{LIT}$ | $V_{CC} = V_{CC\ MAX}$, A9 = 10V | | 35 | µA |
| Output leakage current | $I_{LO}$ | $V_{OUT} = V_{SS}$ to $V_{CC}$, $V_{CC} = V_{CC\ MAX}$ | - | ±1 | µA |
| Active current, read @ 5MHz | $I_{CC1}$ | $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ | - | 20 | mA |
| Active current, program/erase | $I_{CC2}$ | $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ | - | 100 | mA |
| Automatic sleep mode* | $I_{CC3}$ | $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$; $V_{IL}$= 0.3V, $V_{IH} = V_{CC}$ - 0.3V | - | 5 | µA |
| Standby current | $I_{SB}$ | $\overline{CE} = V_{CC}$ - 0.3V, $\overline{RESET} = V_{CC}$ - .3V | - | 5 | µA |
| Deep power down current[3] | $I_{PD}$ | $\overline{RESET}$ = 0.3V | - | 5 | µA |
| Input low voltage | $V_{IL}$ | | -0.5 | 0.8 | V |
| Input high voltage | $V_{IH}$ | | 0.7×$V_{CC}$ | $V_{CC}$ + 0.3 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 4.0mA, $V_{CC} = V_{CC\ MIN}$ | - | 0.45 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = -2.0 mA, $V_{CC} = V_{CC\ MIN}$ | 0.85×$V_{CC}$ | - | V |
| Low VCC lock out voltage | $V_{LKO}$ | | 1.5 | - | V |
| Input HV select voltage | $V_{ID}$ | | 9 | 11 | V |

* Automatic sleep mode enables the deep power down mode when addresses are stable for 150 ns. Typical sleep mode current is 200 nA.

## AC parameters — read cycle

| JEDEC Symbol | Std Symbol | Parameter | -70 Min | -70 Max | -80 Min | -80 Max | -90 Min | -90 Max | -120 Min | -120 Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{AVAV}$ | $t_{RC}$ | Read cycle time | 70 | | 80 | - | 90 | - | 120 | - | ns |
| $t_{AVQV}$ | $t_{ACC}$ | Address to output delay | - | 70 | - | 80 | - | 90 | - | 120 | ns |
| $t_{ELQV}$ | $t_{CE}$ | Chip enable to output | - | 70 | - | 80 | - | 90 | - | 120 | ns |
| $t_{GLQV}$ | $t_{OE}$ | Output enable to output | - | 30 | - | 30 | - | 35 | - | 50 | ns |
| | $t_{OES}$ | Output enable setup time | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| $t_{EHQZ}$ | $t_{DF}$ | Chip enable to output High Z | - | 20 | - | 20 | - | 30 | - | 30 | ns |
| $t_{GHQZ}$ | $t_{DF}$ | Output enable to output High Z | - | 20 | - | 20 | - | 30 | - | 30 | ns |
| $t_{AXQX}$ | $t_{OH}$ | Output hold time from addresses, first occurrence of $\overline{CE}$ or $\overline{OE}$ | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| | $t_{OEH}$ | Output enable hold time: Read | 10 | - | 10 | - | 10 | - | 10 | - | ns |
| | | Output enable hold time: Toggle and data polling | 10 | - | 10 | - | 10 | - | 10 | - | ns |
| $t_{PHQV}$ | $t_{RH}$ | $\overline{RESET}$ high to output delay | - | 50 | - | 50 | - | 50 | - | 50 | ns |
| | $t_{READY}$ | $\overline{RESET}$ pin low to read mode | - | 10 | - | 10 | - | 10 | - | 10 | µs |
| | $t_{RP}$ | $\overline{RESET}$ pulse | 500 | | 500 | - | 500 | - | 500 | - | ns |

## Read waveform



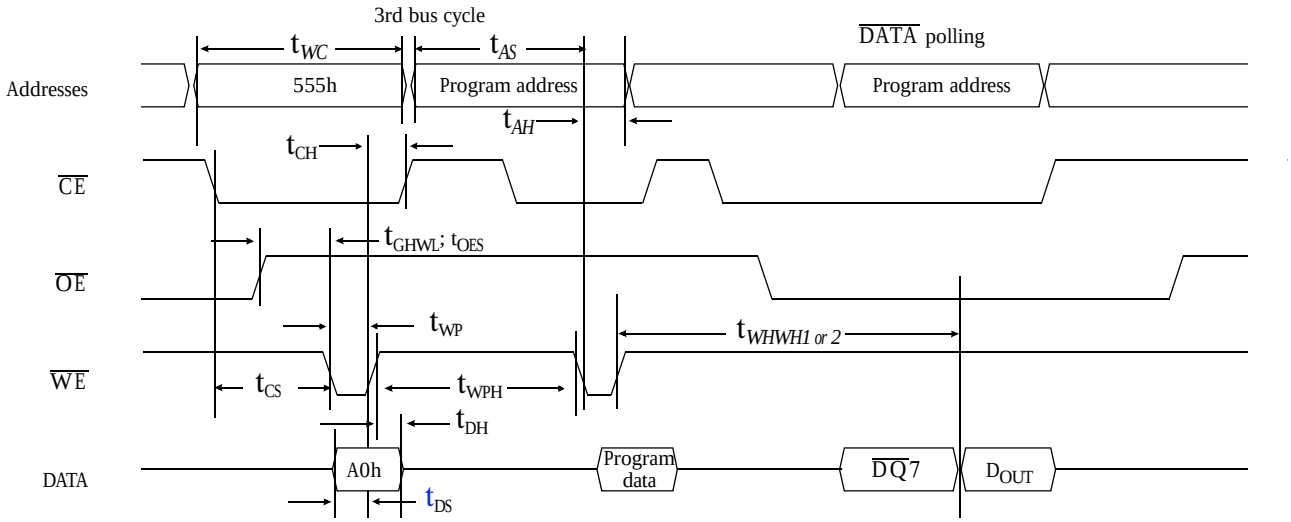
## AC parameters — write cycle

$\overline{WE}$ controlled

| JEDEC Symbol | Std Symbol | Parameter | -70 Min | -70 Max | -80 Min | -80 Max | -90 Min | -90 Max | -120 Min | -120 Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{AVAV}$ | $t_{WC}$ | Write cycle time | 70 | - | 80 | - | 90 | - | 120 | - | ns |
| $t_{AVWL}$ | $t_{AS}$ | Address setup time | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| $t_{WLAX}$ | $t_{AH}$ | Address hold time | 45 | - | 45 | - | 45 | - | 50 | - | ns |
| $t_{DVWH}$ | $t_{DS}$ | Data setup time | 35 | - | 35 | - | 45 | - | 50 | - | ns |
| $t_{WHDX}$ | $t_{DH}$ | Data hold time | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| $t_{GHWL}$ | $t_{GHWL}$ | Read recover time before write | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| $t_{ELWL}$ | $t_{CS}$ | $\overline{CE}$ setup time | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| $t_{WHEH}$ | $t_{CH}$ | $\overline{CE}$ hold time | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| $t_{WLWH}$ | $t_{WP}$ | Write pulse width | 35 | - | 35 | - | 35 | - | 50 | - | ns |
| $t_{WHWL}$ | $t_{WPH}$ | Write pulse width high | 30 | - | 30 | - | 30 | - | 30 | - | ns |

## Write waveform

$\overline{WE}$ controlled



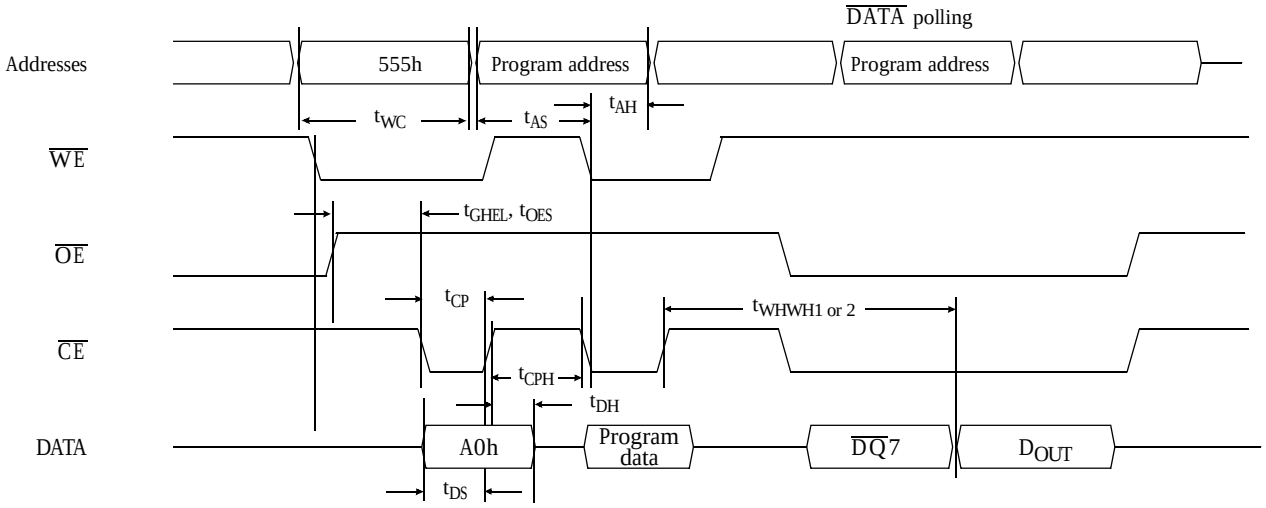
## AC parameters — write cycle 2

$\overline{CE}$ controlled

| JEDEC Symbol | Std Symbol | Parameter | -70 Min | -70 Max | -80 Min | -80 Max | -90 Min | -90 Max | -120 Min | -120 Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{AVAV}$ | $t_{WC}$ | Write cycle time | 70 | - | 80 | - | 90 | - | 120 | - | ns |
| $t_{AVEL}$ | $t_{AS}$ | Address setup time | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| $t_{ELAX}$ | $t_{AH}$ | Address hold time | 45 | - | 45 | - | 45 | - | 50 | - | ns |
| $t_{DVEH}$ | $t_{DS}$ | Data setup time | 35 | - | 35 | - | 45 | - | 50 | - | ns |
| $t_{EHDX}$ | $t_{DH}$ | Data hold time | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| $t_{GHEL}$ | $t_{GHEL}$ | Read recover time before write | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| $t_{WLEL}$ | $t_{WS}$ | $\overline{WE}$ setup time | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| $t_{EHWH}$ | $t_{WH}$ | $\overline{WE}$ hold time | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| $t_{ELEH}$ | $t_{CP}$ | $\overline{CE}$ pulse width | 35 | - | 35 | - | 35 | - | 50 | - | ns |
| $t_{EHEL}$ | $t_{CPH}$ | $\overline{CE}$ pulse width high | 30 | - | 30 | - | 30 | - | 30 | - | ns |

## Write waveform 2

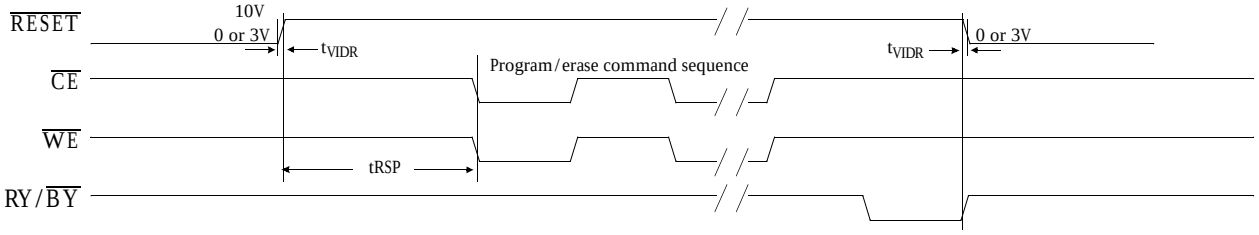
$\overline{CE}$ controlled



## AC parameters — temporary sector unprotect

| JEDEC Symbol | Std Symbol | Parameter | -70 Min | -70 Max | -80 Min | -80 Max | -90 Min | -90 Max | -120 Min | -120 Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | $t_{VIDR}$ | $V_{ID}$ rise and fall time | 500 | - | 500 | - | 500 | - | 500 | - | ns |
| | $t_{RSP}$ | $\overline{RESET}$ setup time for temporary sector unprotect | 4 | - | 4 | - | 4 | - | 4 | - | µs |

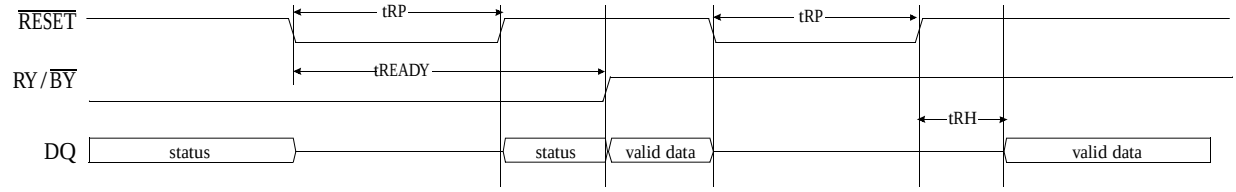
## Temporary sector unprotect waveform




## AC parameters — $\overline{RESET}$

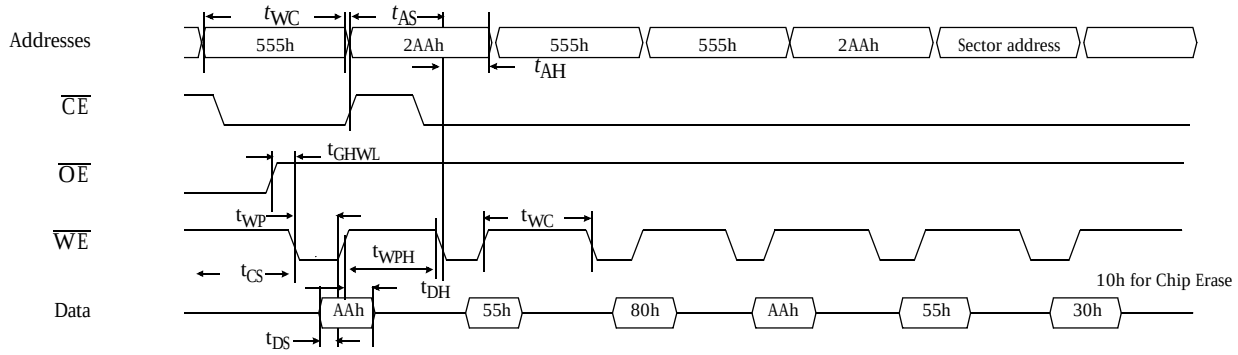
| JEDEC Symbol | Std Symbol | Parameter | -70 Min | -70 Max | -80 Min | -80 Max | -90 Min | -90 Max | -120 Min | -120 Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | $t_{RP}$ | $\overline{RESET}$ pulse | 500 | - | 500 | - | 500 | - | 500 | - | ns |
| | $t_{RH}$ | $\overline{RESET}$ High time before Read | - | 50 | - | 50 | - | 50 | - | 50 | ns |
| | $t_{READY}$ | $\overline{RESET}$ Low to Read mode | - | 10 | - | 10 | - | 10 | - | 10 | µs |

## $\overline{RESET}$ waveform




## Erase waveform

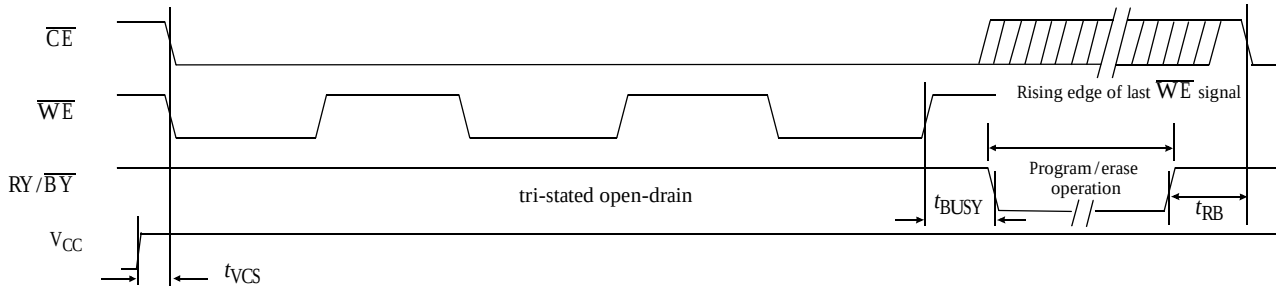
×16 mode



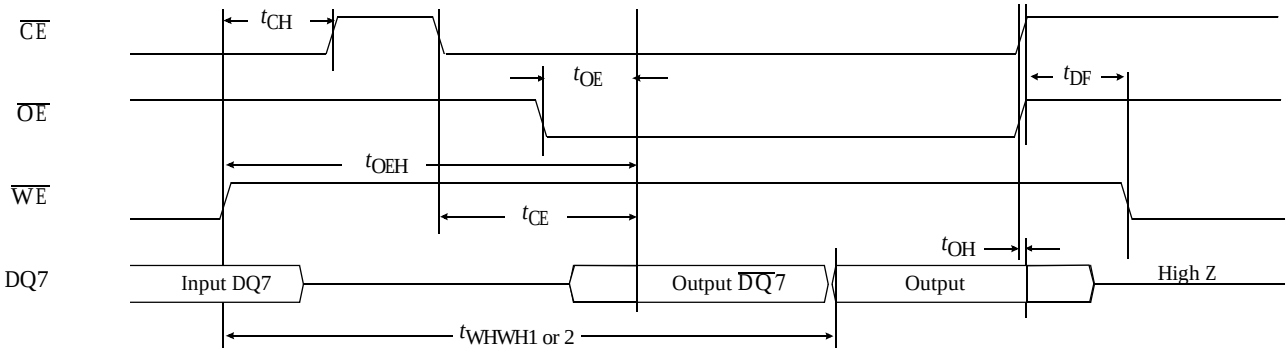
## AC Parameters — READY/BUSY

| JEDEC Symbol | Std Symbol | Parameter | -70 Min | -70 Max | -80 Min | -80 Max | -90 Min | -90 Max | -120 Min | -120 Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| - | $t_{VCS}$ | $V_{CC}$ setup time | 50 | - | 50 | - | 50 | - | 50 | - | µs |
| - | $t_{RB}$ | Recovery time from RY/$\overline{BY}$ | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| - | $t_{BUSY}$ | Program/erase valid to RY/$\overline{BY}$ delay | 90 | - | 90 | - | 90 | - | 90 | - | ns |

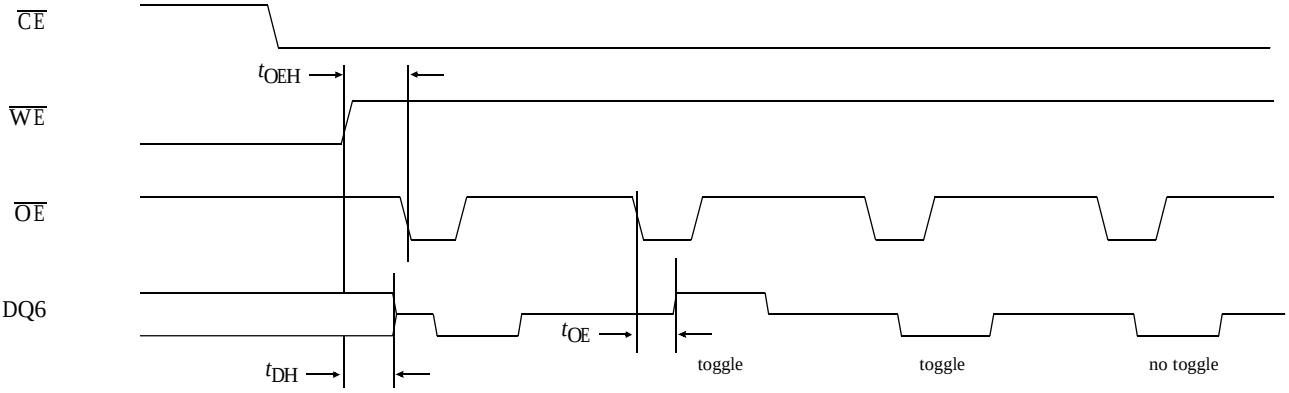
## RY/$\overline{BY}$ waveform




## DATA polling waveform



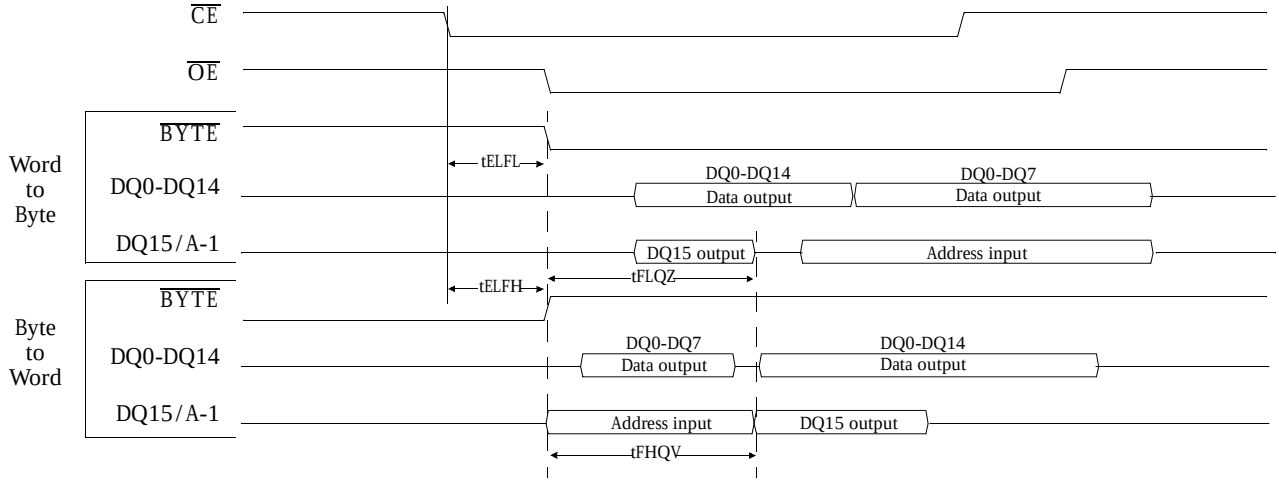

## Toggle bit waveform



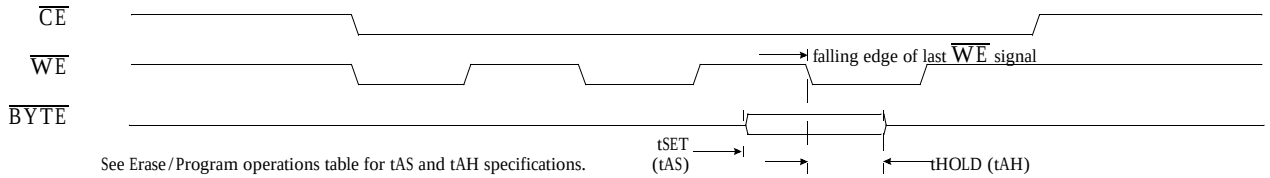
## Word/byte configuration

| JEDEC Symbol | Std Symbol | Parameter | -70 Min | -70 Max | -80 Min | -80 Max | -90 Min | -90 Max | -120 Min | -120 Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| - | $t_{ELFL}/t_{ELFH}$ | $\overline{CE}$ to BYTE switching Low or High | - | 10 | - | 10 | - | 10 | - | 10 | ns |
| - | $t_{FLQZ}$ | $\overline{BYTE}$ switching Low to output High-Z | - | 30 | - | 30 | - | 35 | - | 40 | ns |
| - | $t_{FHQZ}$ | $\overline{BYTE}$ switching High to output Active | 70 | - | 80 | - | 90 | - | 120 | - | ns |

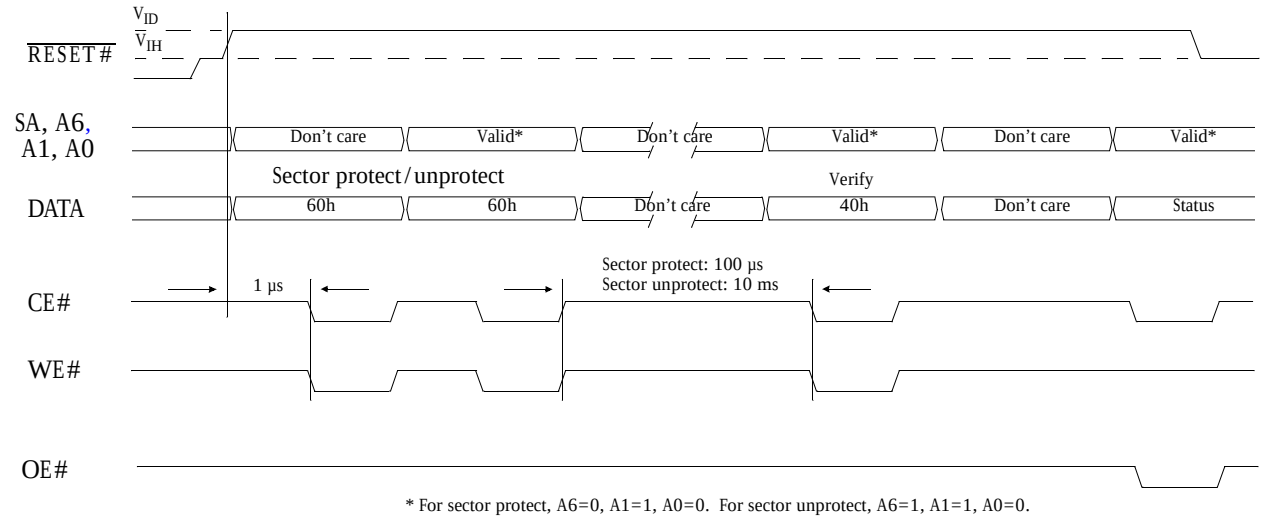
## BYTE read waveform




## $\overline{BYTE}$ write waveform

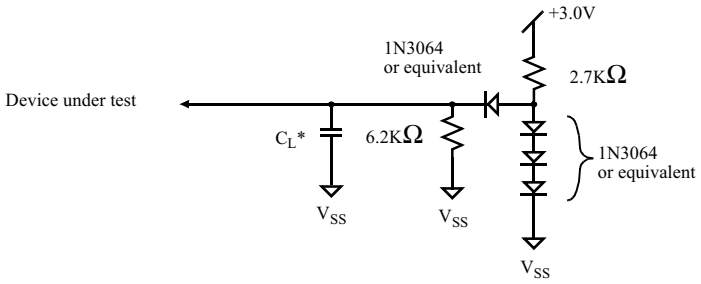



## Sector protect/unprotect




* For sector protect, A6=0, A1=1, A0=0. For sector unprotect, A6=1, A1=1, A0=0.

## AC test conditions




## Test specifications

| Test Condition | -70, -80 | -90, -120 | Unit |
|---|---|---|---|
| Output Load | 1 TTL gate | | |
| Output Load Capacitance $C_L$ (including jig capacitance) | 30 | 100 | pF |
| Input Rise and Fall Times | 5 | | ns |
| Input Pulse Levels | 0.0-3.0 | | V |
| Input timing measurement reference levels | 1.5 | | V |
| Output timing measurement reference levels | 1.5 | | V |

## Erase and programming performance

| Parameter | | Limits Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| Sector erase and verify-1 time (excludes 00h programming prior to erase) | | - | 1.0 | 15 | sec |
| Programming time | Byte | - | 10 | 300 | µs |
| | Word | - | 15 | 360 | µs |
| Chip programming time | | - | 7.2 | 27 | sec |
| Erase/program cycles* | | - | 100,000 | - | cycles |

* Erase/program cycle test is not verified on each shipped unit.

## Latchup tolerance

| Parameter | Min | Max | Unit |
|---|---|---|---|
| Input voltage with respect to $V_{SS}$ on A9, OE, and RESET pin | -1.0 | +12.0 | V |
| Input voltage with respect to $V_{SS}$ on all DQ, address, and control pins | -0.5 | VCC+0.5 | V |
| Current | -100 | +100 | mA |

*Includes all pins except $V_{CC}$. Test conditions: $V_{CC}$ = 3.0V, one pin at a time.*

## Recommended operating conditions

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | +2.7 | +3.6 | V |
| | $V_{SS}$ | 0 | 0 | V |
| Input voltage | $V_{IH}$ | 1.9 | $V_{CC}$ + 0.3 | V |
| | $V_{IL}$ | –0.5 | 0.8 | V |

## Absolute maximum ratings

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input voltage (Input or DQ pin) | $V_{IN}$ | –0.5 | $V_{CC}$+ 0.5 | V |
| Input voltage (A9 pin, $\overline{OE}$, $\overline{RESET}$) | $V_{IN}$ | –0.5 | +12.5 | V |
| Power supply voltage | $V_{CC}$ | -0.5 | +4.0 | V |
| Operating temperature | $T_{OPR}$ | –55 | +125 | °C |
| Storage temperature (plastic) | $T_{STG}$ | –65 | +150 | °C |
| Short circuit output current | $I_{OUT}$ | - | 150 | mA |

Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## TSOP pin capacitance

| Symbol | Parameter | Test setup | Typ | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 | 6 | 7.5 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 | 8.5 | 12 | pF |
| $C_{IN2}$ | Control pin capacitance | $V_{IN}$ = 0 | 8 | 10 | pF |

## SO pin capacitance (availablity TBD)

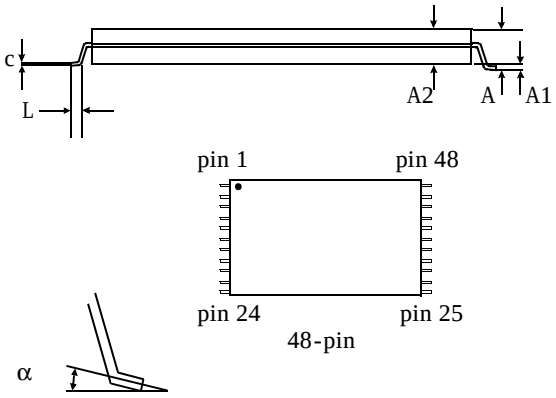
| Symbol | Parameter | Test setup | Typ | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 | 6 | 7.5 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 | 8.5 | 12 | pF |
| $C_{IN2}$ | Control pin capacitance | $V_{IN}$ = 0 | 8 | 10 | pF |

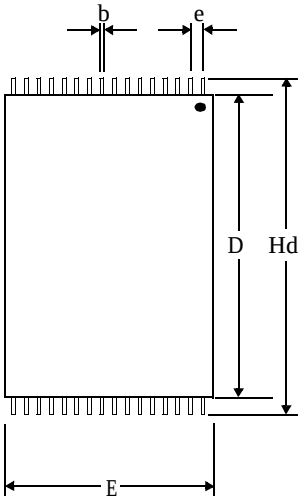
## Data retention

| Parameter | Temp.(°C) | Min | Unit |
|---|---|---|---|
| Minimum pattern data retention time | 150° | 10 | years |
| | 125° | 20 | years |

## Thin Small Outline Package (TSOP-1)

### Package dimensions




| | 48-pin 12×20 | |
|---|---|---|
| | Min | Max |
| A | – | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.95 | 1.05 |
| b | 0.17 | 0.27 |
| c | 0.15 nominal | |
| D | 18.20 | 18.60 |
| e | 0.50 nominal | |
| E | 11.90 | 12.10 |
| Hd | 19.80 | 20.20 |
| L | 0.50 | 0.70 |
| α | 0° | 5° |

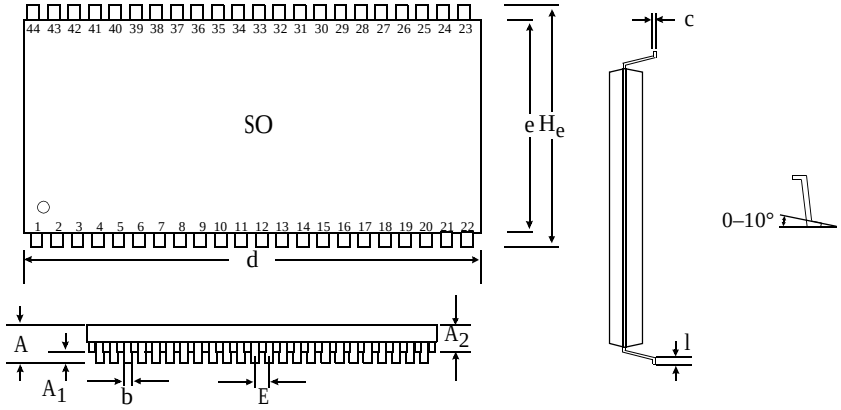
## Small Outline plastic package (SO)

### Package dimensions

JEDEC MO - 175 AA

44-pin SO

| | Min (mm) | Max (mm) |
|---|---|---|
| A | – | 3.1 |
| A1 | 0.05 | – |
| A2 | 2.5 | 2.9 |
| b | 0.25 | 0.45 |
| c | 0.09 | *0.25* |
| d | 28.0 | 28.4 |
| e | 12.4 | 12.8 |
| E | 1.27 (typical) | |
| He | 16.05 (typical) | |
| l | 0.73 | 1.3 |



## AS29LV400 ordering codes

| Package \ Access Time | 70ns(commercial and industrial) | 80ns(commercil and industrial) | 90ns(commercial and industrial) | 120ns(commercial and industrial) |
|---|---|---|---|---|
| TSOP, 12×20 mm, 48-pin<br>Top boot configuration | AS29LV400T-70TC<br>AS29LV400T-70TI | AS29LV400T-80TC<br>AS29LV400T-80TI | AS29LV400T-90TC<br>AS29LV400T-90TI | AS29LV400T-120TC<br>AS29LV400T-120TI |
| TSOP, 12×20 mm, 48-pin<br>Bottom boot configuration | AS29LV400B-70TC<br>AS29LV400B-70TI | AS29LV400B-80TC<br>AS29LV400B-80TI | AS29LV400B-90TC<br>AS29LV400B-90TI | AS29LV400B-120TC<br>AS29LV400B-120TI |
| SO*, 13.3 mm, 44-pin<br>Top boot configuration | AS29LV400T-70SC<br>AS29LV400T-70SI | AS29LV400T-80SC<br>AS29LV400T-80SI | AS29LV400T-90SC<br>AS29LV400T-90SI | AS29LV400T-120SC<br>AS29LV400T-120SI |
| SO, 13.3 mm, 44-pin<br>Bottom boot configuration | AS29LV400B-70SC<br>AS29LV400B-70SI | AS29LV400B-80SC<br>AS29LV400B-80SI | AS29LV400B-90SC<br>AS29LV400B-90SI | AS29LV400B-120SC<br>AS29LV400B-120SI |

* shaded area indicates advanced information - availability of SO package is TBD.

## AS29LV400 part numbering system

| AS29LV | 400 | X | –XXX | X | X | X |
|---|---|---|---|---|---|---|
| 3V Flash EEPROM prefix | Device number | T= Top boot configuration<br>B= Bottom boot configuration | Address access time | Package:<br>S = SO*<br>T = TSOP | Temperature range:<br>C = Commercial: 0°C to 70°C<br>I = Industrial: -40°C to 85°C | Options:<br>B = Burn-in<br>H = High $I_{SB}$ (<1mA)<br>Blank= Standard |