ADC1412D065/080/105/125

**Dual 14-bit ADC 65, 80, 105 or 125 Msps
CMOS or LVDS DDR digital outputs**

1. General description

The ADC1412D is a dual channel 14-bit Analog-to-Digital Converter (ADC) optimized for high dynamic performances and low power consumption at sample rates up to 125 Msps. Pipelined architecture and output error correction ensure the ADC1412D is accurate enough to guarantee zero missing codes over the entire operating range. Supplied from a single 3 V source, it can handle output logic levels from 1.8 V to 3.3 V in CMOS mode, thanks to a separate digital output supply. It supports the LVDS (Low Voltage Differential Signalling) DDR (Double Data Rate) output standard. An integrated SPI (Serial Peripheral Interface) allows the user to easily configure the ADC. The device also includes a programmable gain amplifier with a flexible input voltage range. With excellent dynamic performance from the baseband to input frequencies of 170 MHz or more, the ADC1412D is ideal for use in communications, imaging and medical applications.
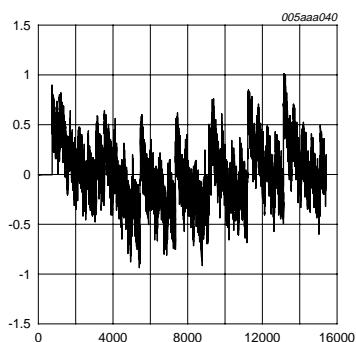

Fig 1. Integral Non-Linearity (INL)
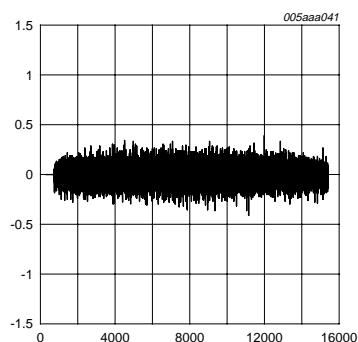
**Fig 2. Differential Non-Linearity (DNL)**
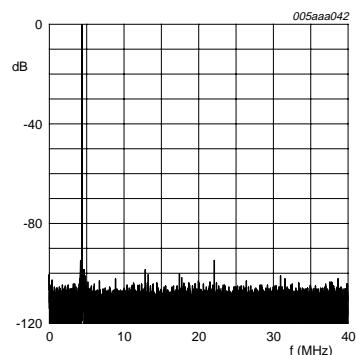
Fig 3. Output spectrum: −1 dBFS, 80 Msps, f_i = 4.43 MHz

2. Features

- SNR, 73 dB
- SFDR, 90 dBc
- Sample rate up to 125 Msps
- Dual-channel14-bit pipelined ADC core
- Single 3 V supply
- Flexible input voltage range: 1 V to 2 V (p-p) with 6 dB programmable fine gain
- CMOS or LVDS DDR digital outputs
- INL ±1 LSB, DNL ±0.5 LSB (typical)
- Input bandwidth, 650 MHz
- Power dissipation, 775 mW at 80 Msps
- SPI Interface
- Duty cycle stabilizer
- Fast OTR detection
- Offset binary, 2's complement, gray code
- Power-down and Sleep modes
- HVQFN64 package

NXP founded by Philips

3.　Applications
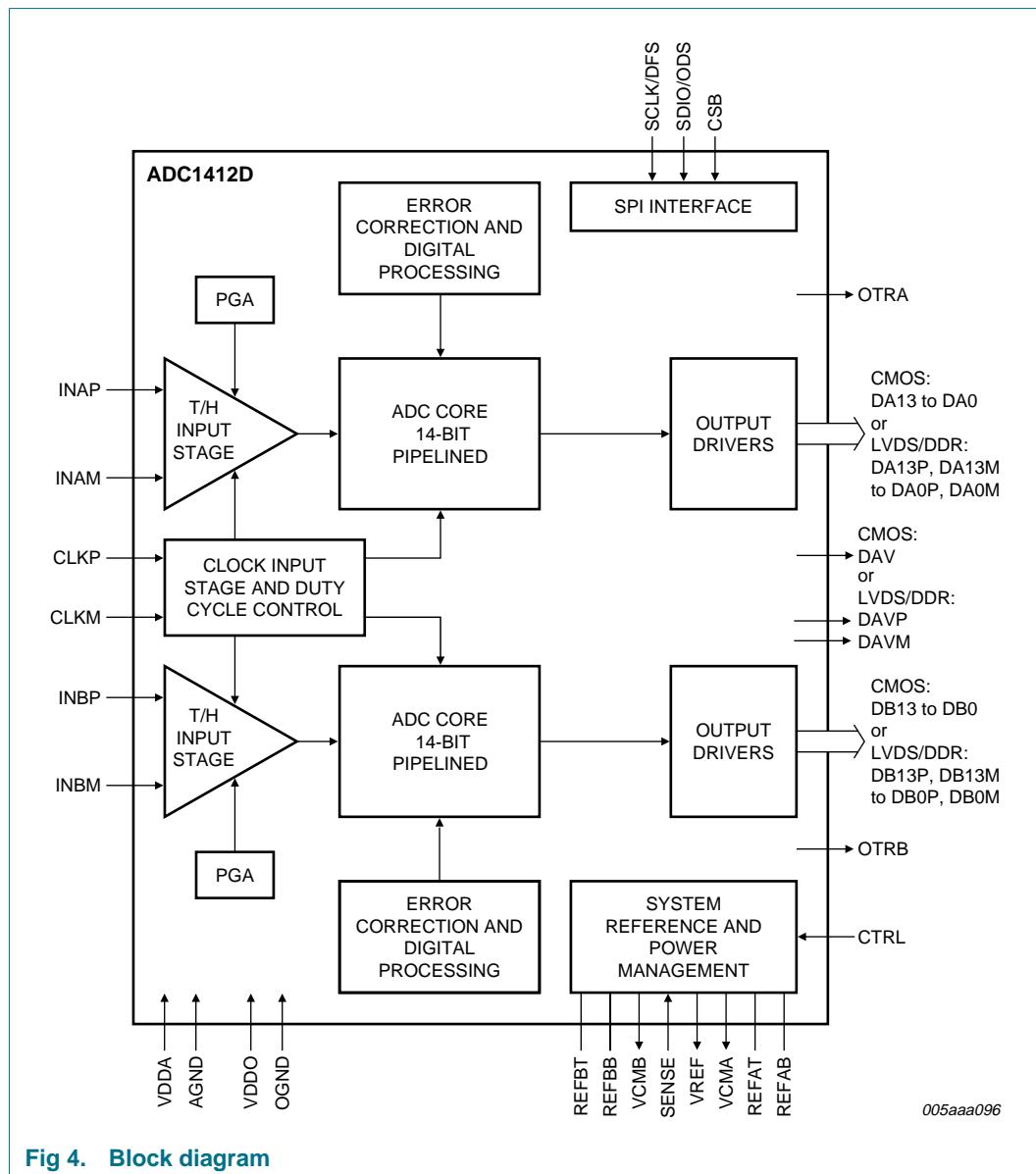
■ Wireless and wired broadband communications

■ Spectral analysis　　　　　　　　　　■ Portable instrumentation

■ Ultrasound equipment　　　　　　　　■ Imaging systems

4.　Ordering information

Table 1.　Ordering information

| Type number	f_s (Msps)	Package		Version
		Name	**Description**	
ADC1412D125HN/C1	125	HVQFN64	plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 x 9 x 0.85 mm	SOT804-3
ADC1412D105HN/C1	105	HVQFN64	plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 x 9 x 0.85 mm	SOT804-3
ADC1412D080HN/C1	80	HVQFN64	plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 x 9 x 0.85 mm	SOT804-3
ADC1412D065HN/C1	65	HVQFN64	plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 x 9 x 0.85 mm	SOT804-3

5. Block diagram

Fig 4.   Block diagram

6. Pinning information

6.1 CMOS outputs selected

6.1.1 Pinning
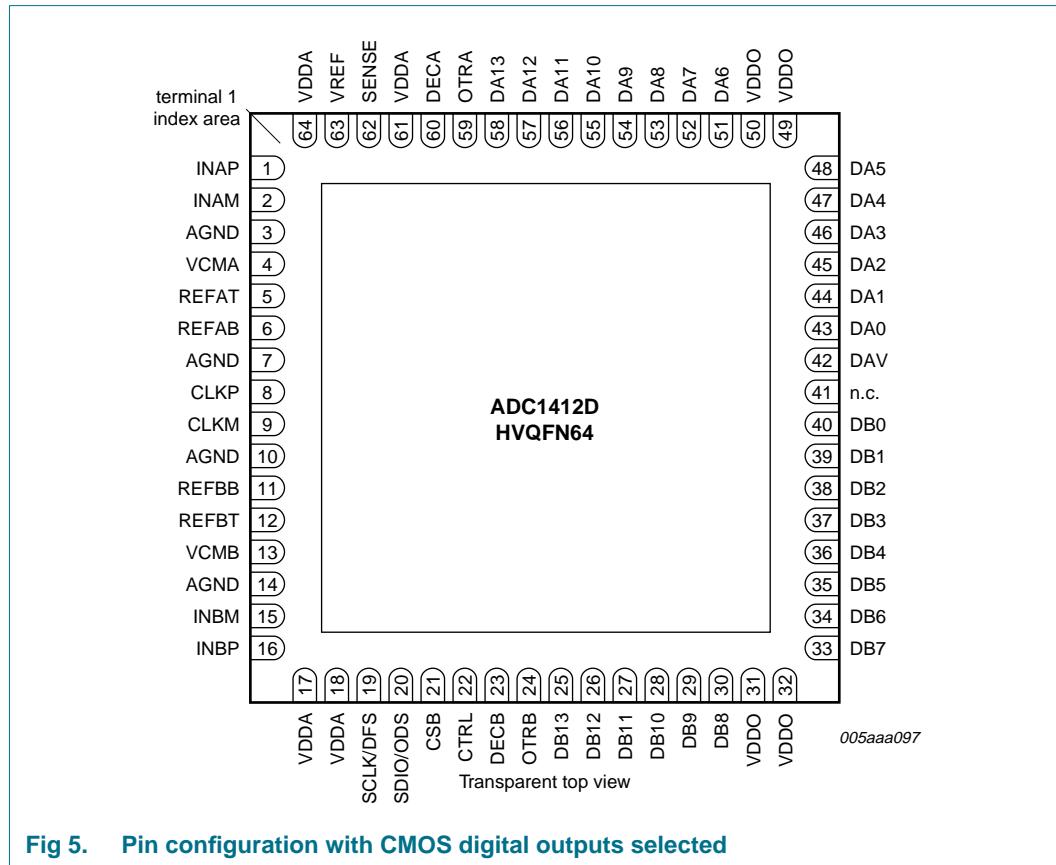
**Fig 5.** Pin configuration with CMOS digital outputs selected

6.1.2 Pin description

Table 2. Pin description (CMOS digital outputs)

Symbol	Pin	Type[1]	Description
INAP	1	I	analog input; channel A
INAM	2	I	complementary analog input; channel A
AGND	3	G	analog ground
VCMA	4	O	common-mode output voltage; channel A
REFAT	5	O	top reference; channel A
REFAB	6	O	bottom reference; channel A
AGND	7	G	analog ground
CLKP	8	I	clock input
CLKM	9	I	complementary clock input
AGND	10	G	analog ground
REFBB	11	O	bottom reference; channel B
REFBT	12	O	top reference; channel B

Table 2. **Pin description (CMOS digital outputs)**

Symbol	Pin	Type[1]	Description
VCMB	13	O	common-mode output voltage; channel B
AGND	14	G	analog ground
INBM	15	I	complementary analog input; channel B
INBP	16	I	analog input; channel B
VDDA	17	P	analog power supply
VDDA	18	P	analog power supply
SCLK/DFS	19	I	SPI clock / data format select
SDIO/ODS	20	I/O	SPI data IO / output data standard
$\overline{\text{CS}}$	21	I	SPI chip select
CTRL	22	I	control mode select
DECB	23	O	regulator decoupling node; channel B
OTRB	24	O	out of range; channel B
DB13	25	O	data output bit 13 (MSB); channel B
DB12	26	O	data output bit 12; channel B
DB11	27	O	data output bit 11; channel B
DB10	28	O	data output bit 10; channel B
DB9	29	O	data output bit 9; channel B
DB8	30	O	data output bit 8; channel B
VDDO	31	P	output power supply
VDDO	32	P	output power supply
DB7	33	O	data output bit 7; channel B
DB6	34	O	data output bit 6; channel B
DB5	35	O	data output bit 5; channel B
DB4	36	O	data output bit 4; channel B
DB3	37	O	data output bit 3; channel B
DB2	38	O	data output bit 2; channel B
DB1	39	O	data output bit 1; channel B
DB0	40	O	data output bit 0 (LSB); channel B
n.c.	41	-	-
DAV	42	O	data valid output clock
DA0	43	O	data output bit 0 (LSB); channel A
DA1	44	O	data output bit 1; channel A
DA2	45	O	data output bit 2; channel A
DA3	46	O	data output bit 3; channel A
DA4	47	O	data output bit 4; channel A
DA5	48	O	data output bit 5; channel A
VDDO	49	P	output power supply
VDDO	50	P	output power supply
DA6	51	O	data output bit 6; channel A
DA7	52	O	data output bit 7; channel A
DA8	53	O	data output bit 8; channel A
DA9	54	O	data output bit 9; channel A
DA10	55	O	data output bit 10; channel A
DA11	56	O	data output bit 11; channel A
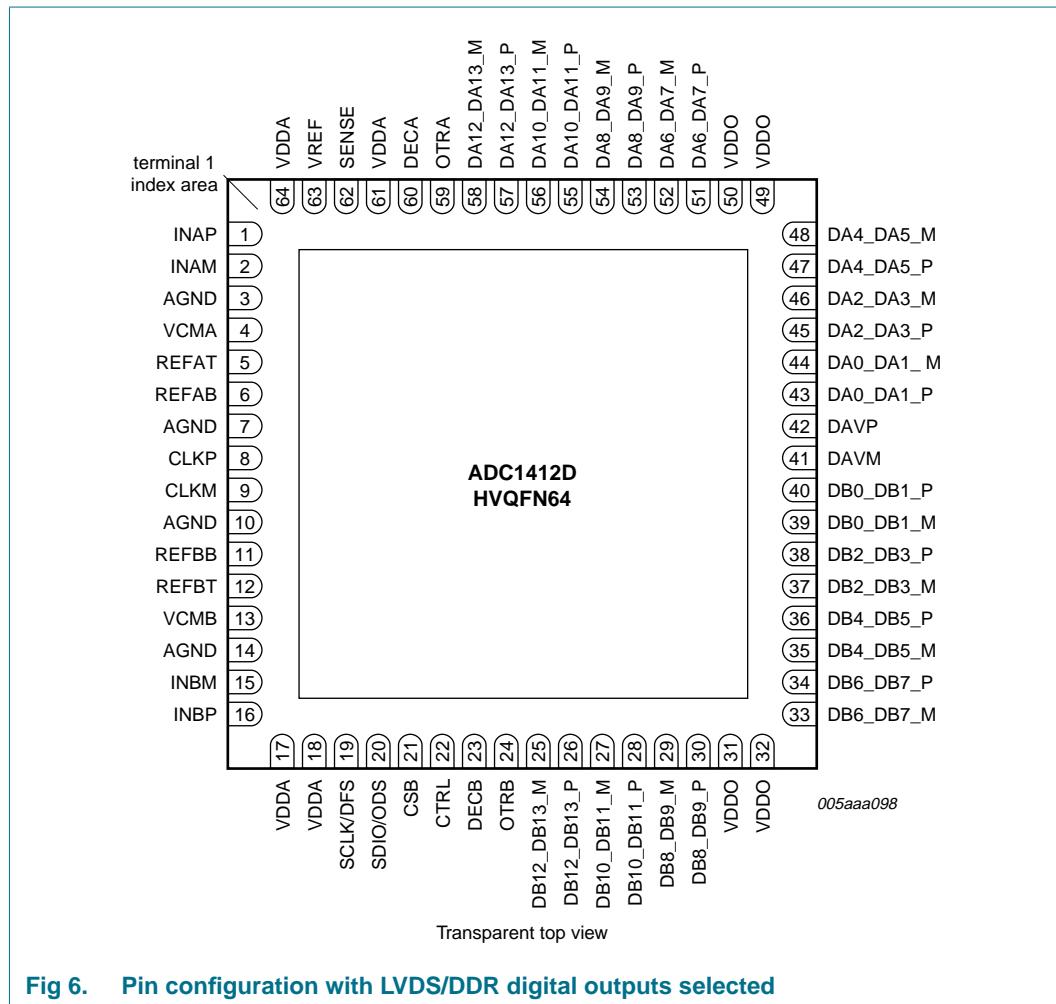
Table 2.   Pin description (CMOS digital outputs)

Symbol	Pin	Type[1]	Description
DA12	57	O	data output bit 12; channel A
DA13	58	O	data output bit 13 (MSB); channel A
OTRA	59	O	out of range; channel A
DECA	60	O	regulator decoupling node; channel A
VDDA	61	P	analog power supply
SENSE	62	I	reference programming pin
VREF	63	I/O	voltage reference input/output
VDDA	64	P	analog power supply

[1]   P: power supply; G: ground; I: input; O: output; I/O: input/output.

## 6.2 LVDS/DDR outputs selected

6.2.1 Pinning

Fig 6.   Pin configuration with LVDS/DDR digital outputs selected

6.2.2 Pin description

Table 3. Pin description (LVDS/DDR) digital outputs)[1]

Symbol	Pin	Type[2]	Description
DB12_DB13_M	25	O	differential output data DB12 and DB13 multiplexed, complement
DB12_DB13_P	26	O	differential output data DB12 and DB13 multiplexed, true
DB10_DB11_M	27	O	differential output data DB10 and DB11 multiplexed, complement
DB10_DB11_P	28	O	differential output data DB10 and DB11 multiplexed, true
DB8_DB9_M	29	O	differential output data DB8 and DB9 multiplexed, complement
DB8_DB9_P	30	O	differential output data DB8 and DB9 multiplexed, true
DB6_DB7_M	33	O	differential output data DB6 and DB7 multiplexed, complement
DB6_DB7_P	34	O	differential output data DB6 and DB7 multiplexed, true
DB4_DB5_M	35	O	differential output data DB4 and DB5 multiplexed, complement
DB4_DB5_P	36	O	differential output data DB4 and DB5 multiplexed, true
DB2_DB3_M	37	O	differential output data DB2 and DB3 multiplexed, complement
DB2_DB3_P	38	O	differential output data DB2 and DB3 multiplexed, true
DB0_DB1_M	39	O	differential output data DB0 and DB1 multiplexed, complement
DB0_DB1_P	40	O	differential output data DB0 and DB1 multiplexed, true
DAVM	41	O	data valid output clock, complement
DAVP	42	O	data valid output clock, true
DA0_DA1_P	43	O	differential output data DA0 and DA1 multiplexed, true
DA0_DA1_M	44	O	differential output data DA0 and DA1 multiplexed, complement
DA2_DA3_P	45	O	differential output data DA2 and DA3 multiplexed, true
DA2_DA3_M	46	O	differential output data DA2 and DA3 multiplexed, complement
DA4_DA5_P	47	O	differential output data DA4 and DA5 multiplexed, true
DA4_DA5_M	48	O	differential output data DA4 and DA5 multiplexed, complement
DA6_DA7_P	51	O	differential output data DA6 and DA7 multiplexed, true
DA6_DA7_M	52	O	differential output data DA6 and DA7 multiplexed, complement
DA8_DA9_P	53	O	differential output data DA8 and DA9 multiplexed, true
DA8_DA9_M	54	O	differential output data DA8 and DA9 multiplexed, complement
DA10_DA11_P	55	O	differential output data DA10 and DA11 multiplexed, true
DA10_DA11_M	56	O	differential output data DA10 and DA11 multiplexed, complement
DA12_DA13_P	57	O	differential output data DA12 and DA13 multiplexed, true
DA12_DA13_M	58	O	differential output data DA12 and DA13 multiplexed, complement

[1] Pins 1 to 24, pin 59 to 64 and pins 31, 32, 49 and 50 are the same for both CMOS and LVDS DDR outputs (see Table 2).

[2] P: power supply; G: ground; I: input; O: output; I/O: input/output.

7. Limiting values

Table 4.   Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDA}	analog supply voltage		<tbd>	<tbd>	V
V_{DDO}	output supply voltage		<tbd>	<tbd>	V
ΔV_{CC}	supply voltage difference	$V_{DDA} - V_{DDO}$	<tbd>	<tbd>	V
T_{stg}	storage temperature		−55	+125	°C
T_{amb}	ambient temperature		−40	+85	°C
T_j	junction temperature		-	<tbd>	°C

8. Thermal characteristics

Table 5.   Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	[1]	<tbd>	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	[1]	<tbd>	K/W

[1]   In compliance with JEDEC test board, in free air.

9. Static characteristics

Table 6.   Static characteristics
Typical values measured at V_{DDA} = 3 V, V_{DDO} = 1.8 V, T_{amb} = 25 °C and C_L = 5 pF; min and max values are across the full temperature range T_{amb} = −40 °C to +85 °C at V_{DDA} = 3 V, V_{DDO} = 1.8 V; $V_{INAP} - V_{INAM}$ = −1 dBFS; $V_{INBP} - V_{INBM}$ = −1 dBFS; internal reference mode; applied to CMOS and LVDS interface; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DDA}	analog supply voltage		2.85	3.0	3.4	V
V_{DDO}	output supply voltage	CMOS mode	1.65	1.8	3.6	V
		LVDS DDR mode	2.85	3.0	3.6	V
I_{DDA}	analog supply current	f_{clk} = 125 Msps; f_i =70 MHz	-	370	-	mA
I_{DDO}	output supply current	CMOS mode; f_{clk} = 125 Msps; f_i =70 MHz	-	40	-	mA
		LVDS DDR mode: f_{clk} = 125 Msps; f_i =70 MHz	-	90	-	mA
P	power dissipation	ADC1412D125	-	1100	-	mW
		ADC1412D105	-	975	-	mW
		ADC1412D080	-	775	-	mW
		ADC1412D065	-	670	-	mW
		Power-down mode	-	<tbd>	-	mW
		Sleep mode	-	<tbd>	-	mW

Table 6.　　**Static characteristics** *…continued*

Typical values measured at V_{DDA} = 3 V, V_{DDO} = 1.8 V, T_{amb} = 25 °C and C_L = 5 pF; min and max values are across the full temperature range T_{amb} = −40 °C to +85 °C at V_{DDA} = 3 V, V_{DDO} = 1.8 V; V_{INAP} − V_{INAM} = −1 dBFS; V_{INBP} − V_{INBM} = −1 dBFS; internal reference mode; applied to CMOS and LVDS interface; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Clock inputs: pins CLKP and CLKM						
AC coupled; LVPECL, LVDS and sine wave						
$V_{i(clk)dif}$	differential clock input voltage	peak-to-peak	0.2	0.8	\<tbd>	V
LVCMOS						
V_I	input voltage		$0.3V_{DDA}$	-	$0.7V_{DDA}$	V
Logic Input: pin CTRL						
V_{IL}	LOW-level input voltage		-	0	-	V
		LOW-medium level	-	$0.3V_{DDA}$	-	V
		medium-HIGH level	-	$0.6V_{DDA}$	-	
V_{IH}	HIGH-level input voltage		-	V_{DDA}	-	V
I_{IL}	LOW-level input current		\<tbd>	-	\<tbd>	μA
I_{IH}	HIGH-level input current		−10	-	+10	μA
Serial Peripheral Interface: pins $\overline{CS}$, SDIO/ODS, SCLK/DFS						
V_{IL}	LOW-level input voltage		0	-	$0.3V_{DDA}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDA}$	-	V_{DDA}	V
I_{IL}	LOW-level input current		−10	-	+10	μA
I_{IH}	HIGH-level input current		−50	-	+50	μA
C_I	input capacitance		-	4	-	pF
Digital Outputs: CMOS mode - pins DA13 to DA0, DB13 to DB0, OTRA, OTRB AND DAV						
Output levels, V_{DDO}=3 V						
V_{OL}	LOW-level output voltage	I_{OL} = \<tbd>	OGND	-	$0.2V_{DDO}$	V
V_{OH}	HIGH-level output voltage	I_{OH} = \<tbd>	$0.8V_{DDO}$	-	V_{DDO}	V
I_{OL}	LOW-level output current	3-state; output level = 0 V	-	\<tbd>	-	μA
I_{OH}	HIGH-level output current	3-state; output level = V_{DDA}	-	\<tbd>	-	μA
C_O	output capacitance	high impedance; $\overline{OE}$ = HIGH	-	3	-	pF
Output levels, V_{DDO}=1.8 V						
V_{OL}	LOW-level output voltage	I_{OL} = \<tbd>	OGND	-	$0.2V_{DDO}$	V
V_{OH}	HIGH-level output voltage	I_{OH} = \<tbd>	$0.8V_{DDO}$	-	V_{DDO}	V
Digital Outputs, LVDS DDR mode - pins DA13P/DA13M to DA0P/DA0M, DB13P/DB13M to DB0P/DBOM, DAVP and DAVM						
Output levels, VDDO = 3 V only, R_L = 100 Ω						
$V_{O(offset)}$	output offset voltage	output buffer current set to 3.5 mA	-	1.2	-	V
$V_{O(dif)}$	differential output voltage	output buffer current set to 3.5 mA	-	350	-	mV
C_O	output capacitance		-	\<tbd>	-	pF
Analog inputs: pins INAP, INAM, INBP and INBM						
I_I	Input current		−5	-	+5	μA
R_I	Input resistance		-	\<tbd>	-	Ω

Table 6. **Static characteristics** *…continued*

Typical values measured at $V_{DDA} = 3$ V, $V_{DDO} = 1.8$ V, $T_{amb} = 25\,°C$ and $C_L = 5$ pF; min and max values are across the full temperature range $T_{amb} = -40\,°C$ to $+85\,°C$ at $V_{DDA} = 3$ V, $V_{DDO} = 1.8$ V; $V_{INAP} - V_{INAM} = -1$ dBFS; $V_{INBP} - V_{INBM} = -1$ dBFS; internal reference mode; applied to CMOS and LVDS interface; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_I	Input capacitance		-	5	-	pF
$V_{I(cm)}$	common-mode input voltage	$V_{INAP} = V_{INAM}$; $V_{INBP} = V_{INBM}$	0.9	1.5	2	V
B_i	input bandwidth		-	600	-	MHz
$V_{I(dif)}$	differential input voltage	peak-to-peak	1	-	2	V
Common mode output voltage: pins VCMA and VCMB						
$V_{O(cm)}$	common-mode output voltage		-	$0.5V_{DDA}$	-	V
$I_{O(cm)}$	common-mode output current		-	<tbd>	-	µA
I/O reference voltage: pin VREF						
V_{VREF}	voltage on pin VREF	output	-	0.5 to 1	-	V
		input	0.5	-	1	V
Accuracy						
INL	integral non-linearity		−5	±1	+5	LSB
DNL	differential non-linearity	guaranteed no missing codes	−0.95	±0.5	+0.95	LSB
E_{offset}	offset error		-	±2	-	mV
E_G	gain error		-	±0.5	-	%FS
$M_{G(CTC)}$	channel-to-channel gain matching		-	<tbd>	-	%
Supply						
PSRR	power supply rejection ratio	100 mV (p-p) on V_{DDA}	-	35	-	dBc

10. Dynamic characteristics

10.1 Dynamic Characteristics

Table 7.   Dynamic characteristics

Typical values measured at V_{DDA} = 3 V, V_{DDO} = 1.8 V, T_{amb} = 25 °C and C_L = 5 pF; min and max values are across the full temperature range T_{amb} = −40 °C to +85 °C at V_{DDA} = 3 V, V_{DDO} = 1.8 V; V_{INAP} − V_{INAM} = −1 dBFS; V_{INBP} − V_{INBM} = −1 dBFS; internal reference mode; applied to CMOS and LVDS interface; unless otherwise specified.

Symbol	Parameter	Conditions	ADC1412D065			ADC1412D080			ADC1412D105			ADC1412D125			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Analog signal processing															
α_{2H}	second harmonic level	f_i = 3 MHz	-	94	-	-	94	-	-	96	-	-	96	-	dBc
		f_i = 30 MHz	-	93	-	-	93	-	-	92	-	-	93	-	dBc
		f_i = 70 MHz	-	90	-	-	91	-	-	91	-	-	91	-	dBc
		f_i = 170 MHz	-	88	-	-	88	-	-	85	-	-	85	-	dBc
α_{3H}	third harmonic level	f_i = 3 MHz	-	92	-	-	93	-	-	91	-	-	90	-	dBc
		f_i = 30 MHz	-	91	-	-	92	-	-	91	-	-	89	-	dBc
		f_i = 70 MHz	-	90	-	-	90	-	-	90	-	-	87	-	dBc
		f_i = 170 MHz	-	88	-	-	87	-	-	88	-	-	87	-	dBc
THD	total harmonic distortion	f_i = 3 MHz	-	88	-	-	88	-	-	87	-	-	87	-	dBc
		f_i = 30 MHz	-	87	-	-	87	-	-	87	-	-	86	-	dBc
		f_i = 70 MHz	-	86	-	-	86	-	-	85	-	-	84	-	dBc
		f_i = 170 MHz	-	83	-	-	83	-	-	82	-	-	82	-	dBc
ENOB	effective number of bits	f_i = 3 MHz	-	11.9	-	-	11.9	-	-	11.8	-	-	11.8	-	bits
		f_i = 30 MHz	-	11.7	-	-	11.7	-	-	11.7	-	-	11.7	-	bits
		f_i = 70 MHz	-	11.6	-	-	11.6	-	-	11.6	-	-	11.6	-	bits
		f_i = 170 MHz	-	11.6	-	-	11.5	-	-	11.5	-	-	11.5	-	bits
SNR	signal-to-noise ratio	f_i = 3 MHz	-	73.2	-	-	73.1	-	-	72.9	-	-	72.5	-	dBFS
		f_i = 30 MHz	-	72.4	-	-	72.3	-	-	72.3	-	-	72.2	-	dBFS
		f_i = 70 MHz	-	71.8	-	-	71.8	-	-	71.7	-	-	71.6	-	dBFS
		f_i = 170 MHz	-	71.3	-	-	71.2	-	-	71.1	-	-	71	-	dBFS
SFDR	spurious-free dynamic range	f_i = 3 MHz	-	91	-	-	91	-	-	90	-	-	90	-	dBc
		f_i = 30 MHz	-	90	-	-	90	-	-	90	-	-	89	-	dBc
		f_i = 70 MHz	-	89	-	-	89	-	-	88	-	-	87	-	dBc
		f_i = 170 MHz	-	86	-	-	86	-	-	85	-	-	85	-	dBc
IMD	Intermodulation distortion	f_i = 3 MHz	-	94	-	-	94	-	-	93	-	-	93	-	dBc
		f_i = 30 MHz	-	93	-	-	93	-	-	93	-	-	92	-	dBc
		f_i = 70 MHz	-	92	-	-	92	-	-	91	-	-	90	-	dBc
		f_i = 170 MHz	-	89	-	-	89	-	-	88	-	-	88	-	dBc
$\alpha_{ct(ch)}$	channel crosstalk	f_i = 70 MHz	-	tbd	-	-	tbd	-	-	tbd	-	-	tbd	-	dB

10.2 Clock and Digital Output Timing

Table 8. **Clock and digital output timing characteristics**
Typical values measured at V_{DDA} = 3 V, V_{DDO} = 1.8 V, T_{amb} = 25 °C and C_L = 5 pF; min and max values are across the full temperature range T_{amb} = −40 °C to +85 °C at V_{DDA} = 3 V, V_{DDO} = 1.8 V ; $V_{INAP} - V_{INAM}$ = −1 dBFS; $V_{INBP} - V_{INBM}$ = −1 dBFS; unless otherwise specified.

Symbol	Parameter	Conditions	ADC1412D065			ADC1412D080			ADC1412D105			ADC1412D125			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Clock timing input: pins CLKP and CLKM															
f_{clk}	clock frequency		20	-	65	60	-	80	60	-	105	60	-	125	MHz
$t_{lat(data)}$	data latency time		-	14	-	-	14	-	-	14	-	-	14	-	clk/cy
δ_{clk}	clock duty cycle	DCS_EN = 1	30	50	70	30	50	70	30	50	70	30	50	70	%
		DCS_EN = 0	45	50	55	45	50	55	45	50	55	45	50	55	%
$t_{d(s)}$	sampling delay time		-	0.8	-	-	0.8	-	-	0.8	-	-	0.8	-	ns
t_{wake}	wake-up time		-	tbd	-	-	tbd	-	-	tbd	-	-	tbd	-	ns
CMOS mode timing: pins DA13 to DA0, DB13 to DB0 and DAV															
t_{PD}	propagation delay	DATA	-	3.9	-	-	3.9	-	-	3.9	-	-	3.9	-	ns
		DAV	-	4.2	-	-	4.2	-	-	4.2	-	-	4.2	-	ns
t_{su}	set-up time		-	7.7	-	-	6.5	-	-	4.7	-	-	4.3	-	ns
t_h	hold time		-	6.7	-	-	5.5	-	-	3.8	-	-	3.5	-	ns
t_r	rise time[1]	DATA	0.5	-	2.4	0.5	-	2.4	0.5	-	2.4	0.5	-	2.4	ns
		DAV	0.5	-	2.4	0.5	-	2.4	0.5	-	2.4	0.5	-	2.4	ns
t_f	fall time[1]	DATA	0.5	-	2.4	0.5	-	2.4	0.5	-	2.4	0.5	-	2.4	ns
LVDS DDR mode timing: pins DA13P/DA13M to DA0P/DA0M, DAVP and DAVM; DB13P/DB13M to DB0P/DB0M															
t_{PD}	propagation delay	DATA		3.9			3.9			3.9			3.9		ns
		DAV		4.2			4.2			4.2			4.2		ns

[1] Measured between 20 % to 80 % of V_{DDO}; rise time measured from −50 mV to +50 mV; fall time measured from +50 mV to −50 mV.

10.3 SPI Timings

Table 9.   **Characteristics**

Typical values measured at V_{DDA} = 3 V, V_{DDO} = 1.8 V, T_{amb} = 25 °C and C_L = 5 pF; min and max values are across the full temperature range T_{amb} = −40 °C to +85 °C at V_{DDA} = 3 V, V_{DDO} = 1.8 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPI timings						
$t_{w(SCLK)}$	SCLK pulse width		40	-	-	ns
$t_{w(SCLKH)}$	SCLK HIGH pulse width		16	-	-	ns
$t_{w(SCLKL)}$	SCLK LOW pulse width		16	-	-	ns
t_{su}	set-up time	data to SCLKH	5	-	-	ns
		$\overline{CS}$ to SCLKH	5	-	-	ns
t_h	hold time	data to SCLKH	2	-	-	ns
		$\overline{CS}$ to SCLKH	2	-	-	ns
$f_{clk(max)}$	maximum clock frequency		-	-	25	MHz

11. Application information

11.1 Device control

The ADC1412D can be controlled via the Serial Peripheral Interface (SPI control mode) or directly via the I/O pins (PIN control mode).

11.1.1 SPI and PIN control modes

The device enters PIN control mode at power-up, and remains in this mode as long as pin $\overline{CS}$ is held HIGH. In PIN control mode, the SPI pins SDIO, $\overline{CS}$ and SCLK are used as static control pins. SPI settings are ignored.

SPI control mode is enabled by forcing pin $\overline{CS}$ LOW. It is not possible to toggle between PIN control and SPI control modes. Once SPI control mode has been enabled, the device will remain in this mode until it is powered down. The transition from PIN control mode to SPI control mode is illustrated in Figure 7.
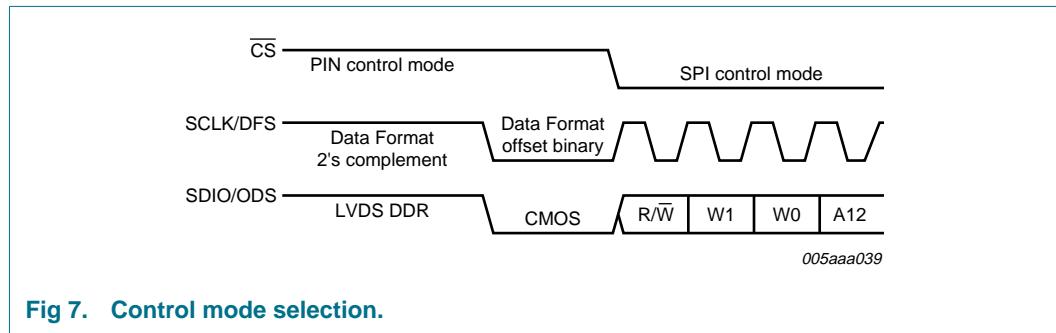
Fig 7. Control mode selection.

When the device enters SPI control mode, the output data standard (CMOS or LVD DDR) is not determined by the state of the relevant SPI control bit (LVDS/CMOS; see Table 22), but by the level on pin SDIO at the instant a transition is triggered by a falling edge on $\overline{CS}$ (SDIO = LOW = CMOS).

11.1.2 Operating mode selection

The active ADC1412D operating mode (Power-up, Power-down or Sleep) can be selected via the SPI interface (see Table 19) or using pins PWD and $\overline{OE}$ in PIN control mode, as described in Table 10.

Table 10. Operating mode selection via pin CTRL

Pin CTRL	Operating mode	Output high-Z
0	Power-down	yes
$0.3V_{DDA}$	Sleep	yes
$0.6V_{DDA}$	Power-up	yes
V_{DDA}	Power-up	no

11.1.3 Selecting the output data standard

The output data standard (CMOS or LVDS DDR) can be selected via the SPI interface (see Table 22) or using pin ODS in PIN control mode. LVDS DDR is selected when ODS is HIGH, otherwise CMOS is selected.

11.1.4 Selecting the output data format

The output data format can be selected via the SPI interface (offset binary, 2's complement or gray code; see Table 22) or using pin DFS in PIN control mode (offset binary or 2's complement). Offset binary is selected when DFS is LOW. When DFS is HIGH, 2's complement is selected.
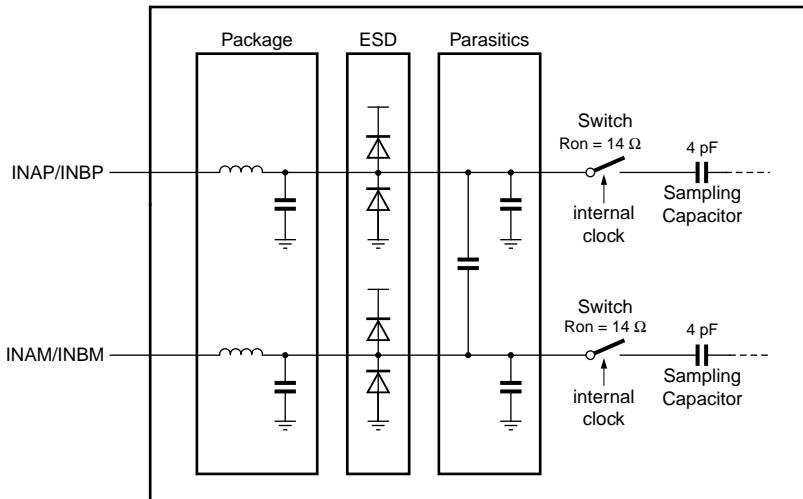
11.2 Analog inputs

11.2.1 Input stage

The analog input of the ADC1412D supports differential or single-ended input drive. Optimal performance is achieved using differential inputs with the common-mode input voltage ($V_{I(cm)}$) on pins INAP, INAM, INBP and INBM set to $0.5V_{DDA}$.

The full scale analog input voltage range is configurable between 1 V (p-p) and 2 V (p-p) via a programmable internal reference (see Section 11.3 and Table 21 further details).

The equivalent circuit of the sample and hold input stage, including ESD protection and circuit and package parasitics, is shown in Figure 8.

005aaa092

Fig 8.   Input sampling circuit

The sample phase occurs when the internal clock (derived from the clock signal on pin CLKP/CLKM) is HIGH. The voltage is then held on the sampling capacitors. When the clock signal goes LOW, the stage enters the hold phase and the voltage information is transmitted to the ADC core.

11.2.2 Anti-kickback circuitry

Anti-kickback circuitry (R-C filter in Figure 9 is needed to counteract the effects of charge injection generated by the sampling capacitance.

The RC filter is also used to filter noise from the signal before it reaches the sampling stage. The value of the capacitor should be chosen to maximize noise attenuation without degrading the settling time excessively.

005aaa093
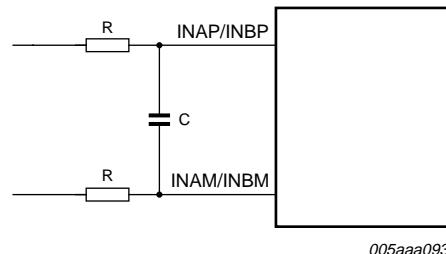
Fig 9.   Anti-kickback circuit

The component values are determined by the input frequency and should be selected so as not to affect the input bandwidth.

Table 11.   RC coupling versus input frequency - recommended values

Input frequency	R	C
3 MHz	25 ohms	12 pF
70 MHz	12 ohms	8 pF
170 MHz	12 ohms	8 pF

11.2.3 Transformer

The configuration of the transformer circuit is determined by the input frequency. The configuration shown in Figure 10 would be suitable for a baseband application.

005aaa094
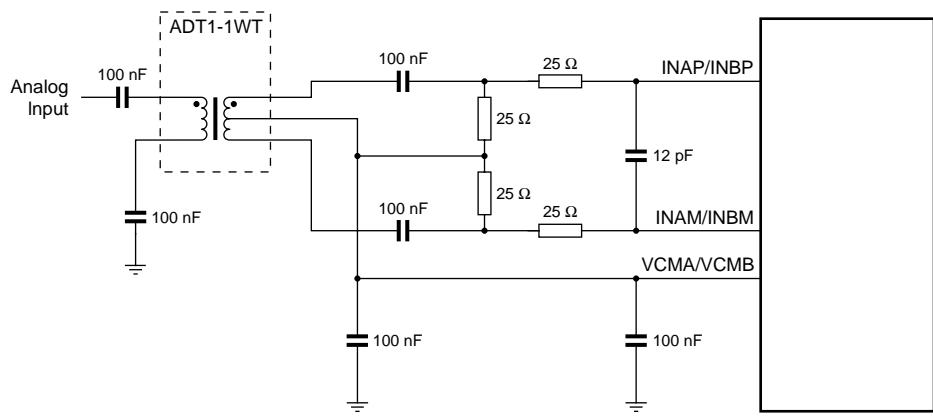
Fig 10. Single transformer configuration suitable for baseband applications

The configuration shown in Figure 11 is recommended for high frequency applications. In both cases, the choice of transformer will be a compromise between cost and performance.
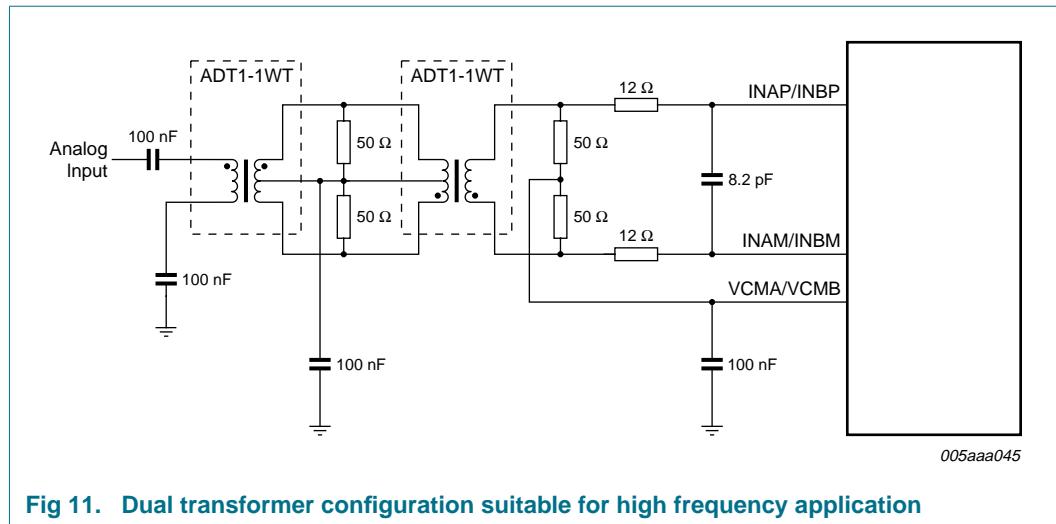
Fig 11. **Dual transformer configuration suitable for high frequency application**

11.3 System reference and power management

11.3.1 Internal/external references

The ADC1412D has a stable and accurate built-in internal reference voltage. This reference voltage can be set internally, externally or via the SPI (programmable in 1 dB steps between 0 dB and −6 dB via control bits INTREF when bit INTREF_EN = 1; see Table 21). The equivalent reference circuit is shown in Figure 12.
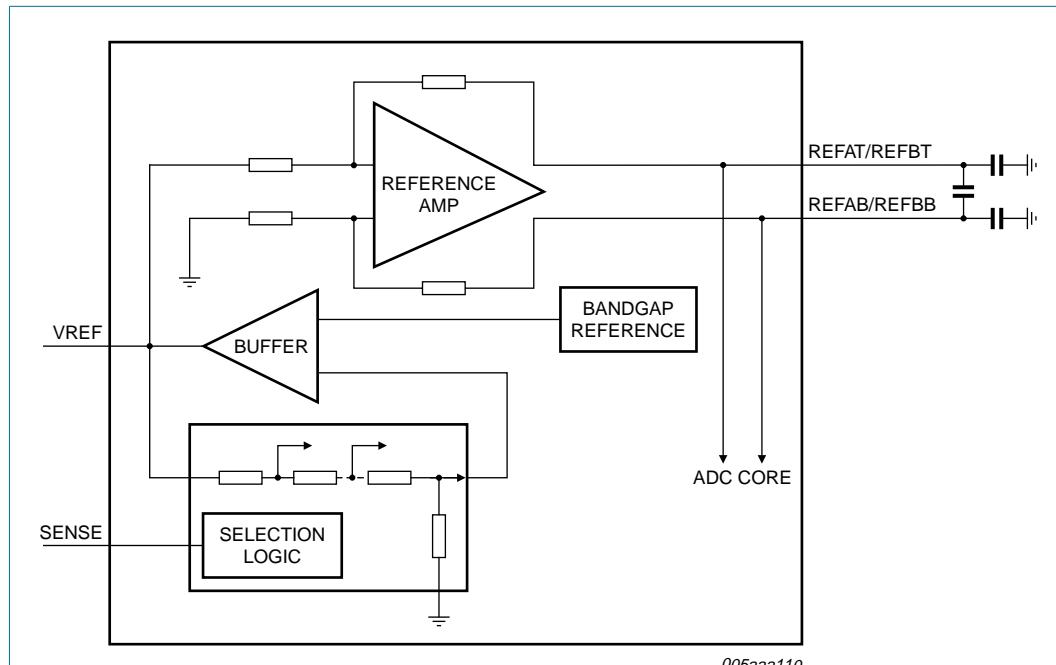
Fig 12. **Single transformer configuration suitable for baseband applications**
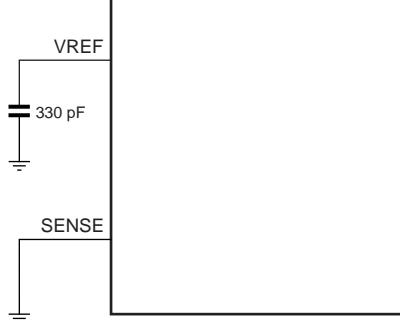
If bit INTREF_EN is set to 0, the reference voltage will be determined either internally or externally as detailed in Table 12.

Table 12.   Reference selection
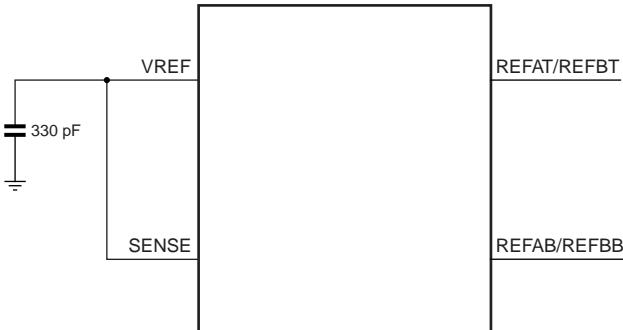
Selection	SPI bit INTREF_EN	SENSE pin	VREF pin	full scale (p-p)
internal	0	AGND	330 pF capacitor to AGND	2 V
internal	0	pin VREF connected to pin SENSE and via a 330 pF capacitor to AGND		1 V
external	0	V_{DDA}	external voltage between 0.5 V and 1 V[1]	1 V to 2 V
internal via SPI	1	pin VREF connected to pin SENSE and via 330 pF capacitor to AGND		1 V to 2 V

[1]   The voltage on pin VREF is doubled internally to generate the internal reference voltage.
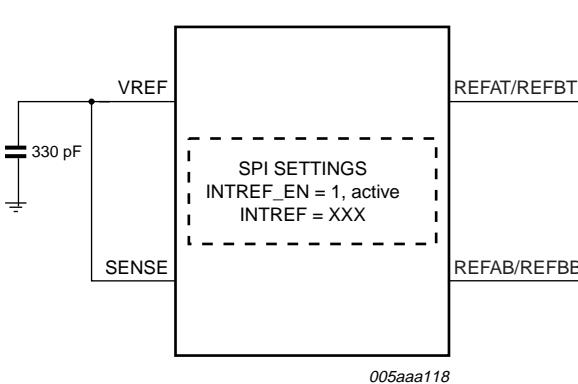
Figure 13 to Figure 16 illustrate how to connect the SENSE and VREF pins to select the required reference voltage source.
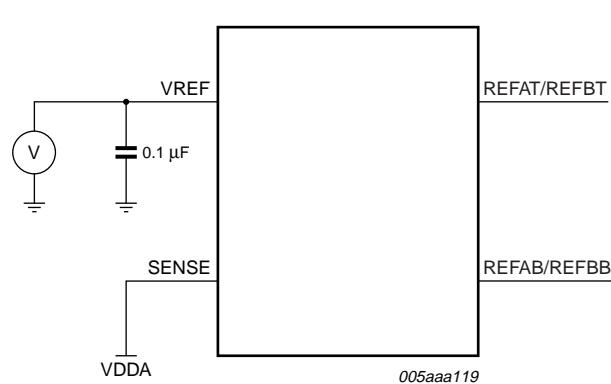
Fig 13. Internal reference, 2 V (p-p) full scale

Fig 14. Internal reference, 1 V (p-p) full scale

Fig 15. Internal reference via SPI, 1 V to 2 V (p-p) full scale

Fig 16. External reference, 1 V to 2 V (p-p) full scale

11.3.2 Gain control

The gain is programmable between 0 dB to −6 dB in 1 dB steps via the SPI (see Table 21). This makes it possible to improve the Spurious-Free Dynamic Range (SFDR) of the ADC1412D. The corresponding full scale input voltage range varies between 2 V (p-p) and 1 V (p-p), as shown in Table 13:

Table 13.   Reference SPI Gain Control

INTREF	Gain	full scale (p-p)
000	0 dB	2 V
001	−1 dB	1.78 V
010	−2 dB	1.59 V
011	−3 dB	1.42 V
100	−4 dB	1.26 V
101	−5 dB	1.12 V
110	−6 dB	1 V
111	reserved	x

11.3.3 Common-mode output voltage ($V_{O(cm)}$)

A 0.1 μF filter capacitor should be connected between pin VCMA/VCMB and ground to ensure a low-noise common-mode output voltage. When AC-coupled, pin VCMA/VCMB can then be used to set the common-mode reference for the analog inputs, for instance via a transformer middle point.
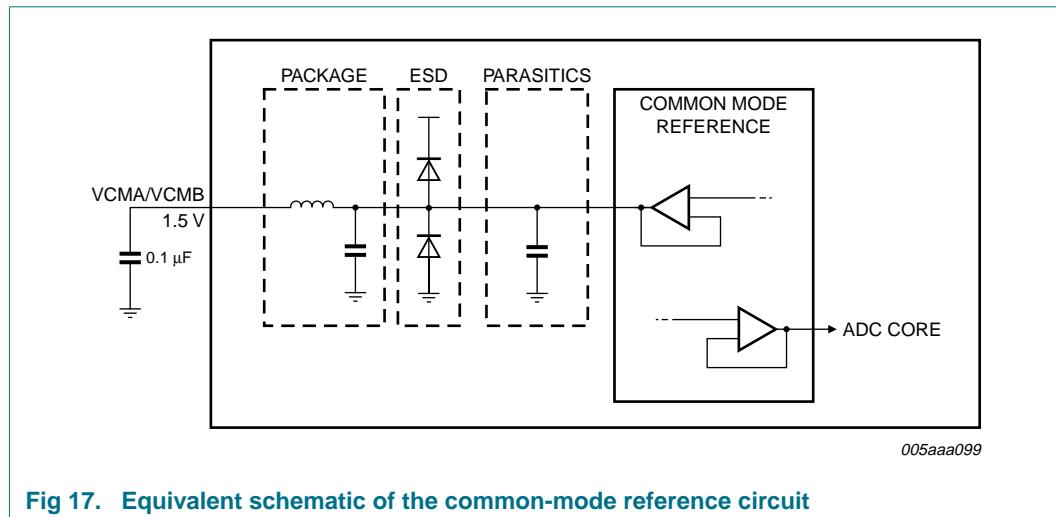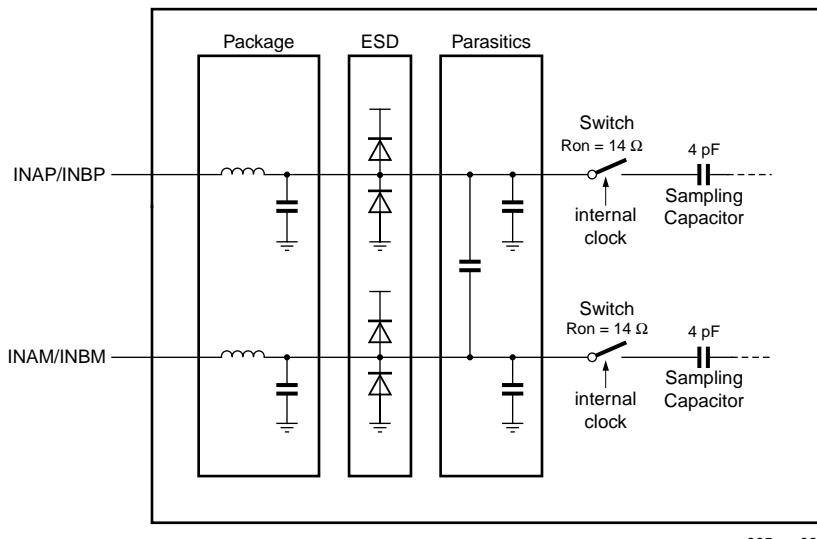
Fig 17. Equivalent schematic of the common-mode reference circuit

11.3.4 Biasing

The common-mode input voltage ($V_{I(cm)}$) on pins INAP/INBP and INAM/INBM should be set externally to $0.5V_{DDA}$ for optimal performance and should always be between 0.9 V and 2 V.

The graph in Figure 18 illustrates how the SFDR and SNR characteristics vary with changes in the common-mode input voltage.
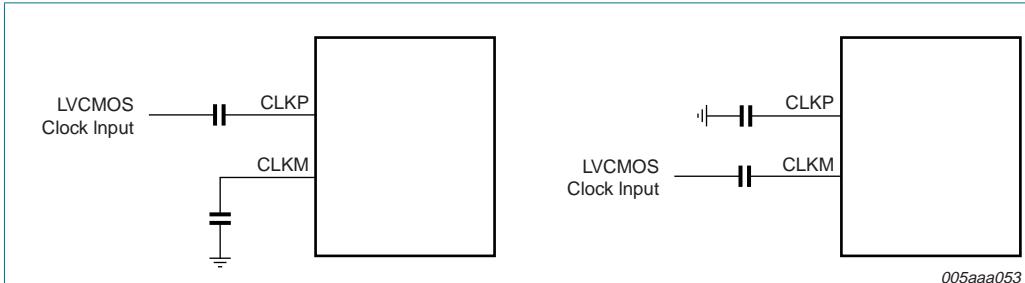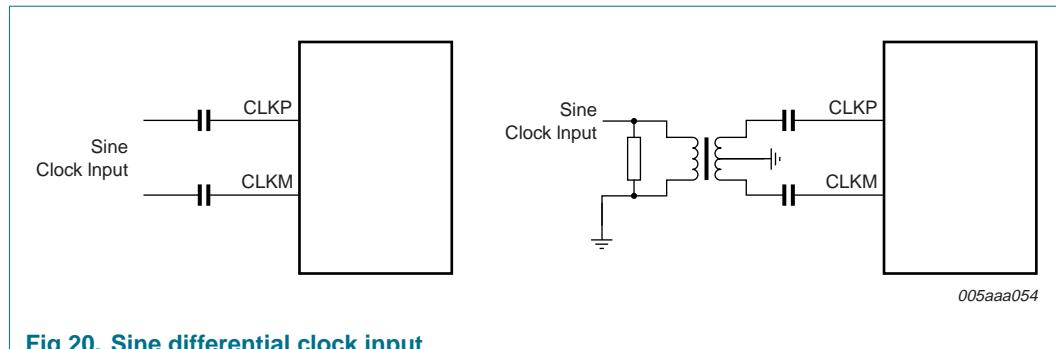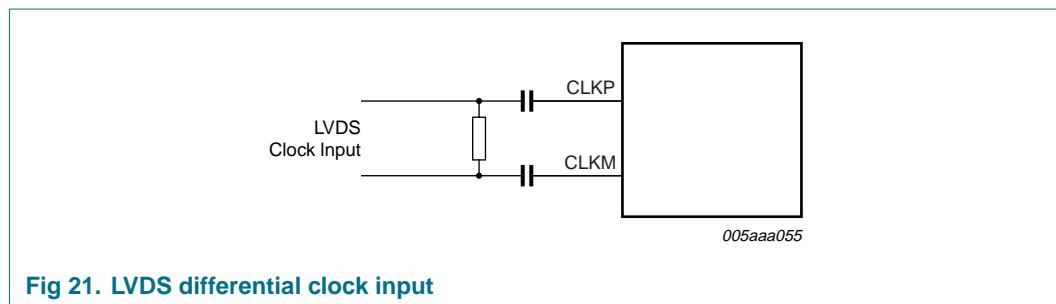
Fig 18. **SFDR and SNR performances versus V$_{I(cm)}$**

11.4 Clock input

11.4.1 Drive modes
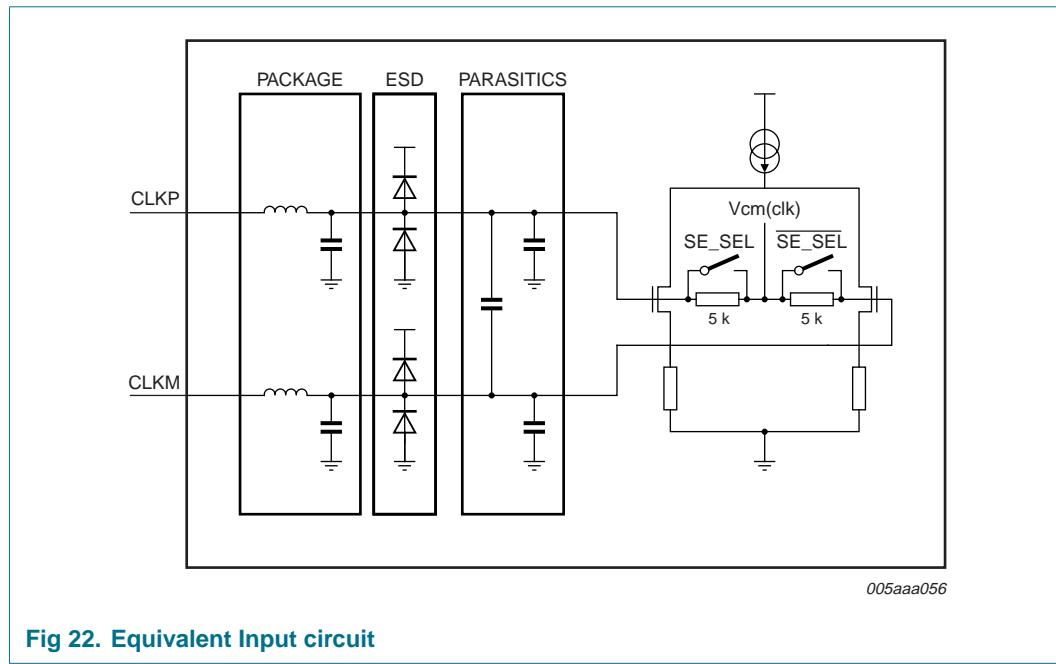
The ADC1412D can be driven differentially (SINE, LVPECL or LVDS) without the performance being affected by the choice of configuration. It can also be driven by a single-ended LVCMOS signal connected to pin CLKP (CLKM should be connected to ground via a capacitor) or CLKM (CLKP should be connected to ground via a capacitor).


Fig 19. LVCMOS Single Ended Clock Input

Fig 20. Sine differential clock input

Fig 21. LVDS differential clock input

11.4.2 Equivalent input circuit

The equivalent circuit of the input clock buffer is shown in Figure 22. The common-mode voltage of the differential input stage is set via internal 5 kΩ resistors.


Fig 22. Equivalent Input circuit

Single-ended or differential clock inputs can be selected via the SPI interface (see Table 20). If single-ended is enabled, the input pin (CLKM or CLKP) is selected via control bit SE_SEL.

If single-ended is implemented without setting SE_SEL to the appropriate value, the unused pin should be connected to ground via a capacitor.

11.4.3 Duty cycle stabilizer

The duty cycle stabilizer can improve the overall performances of the ADC by compensating the duty cycle of the input clock signal. When the duty cycle stabilizer is active (bit DCS_EN = 1; see Table 20), the circuit can handle signals with duty cycles of between 30 % and 70 % (typical). When the duty cycle stabilizer is disabled (DCS_EN = 0), the input clock signal should have a duty cycle of between 45 % and 55 %.

11.4.4 Clock input divider

The ADC1412D contains an input clock divider that divides the incoming clock by a factor of 2 (when bit CLKDIV = 1; see Table 20). This feature allows the user to deliver a higher clock frequency with better jitter performance, leading to a better SNR result once acquisition has been performed.

11.5 Digital outputs

11.5.1 Digital output buffers: CMOS mode

The digital output buffers can be configured as CMOS by setting bit LVDS/CMOS to 0 (see Table 22).

Each digital output has a dedicated output buffer. The equivalent circuit of the CMOS digital output buffer is shown in Figure 23. The buffer is powered by a separate OGND/V$_{DDO}$ to ensure 1.8 V to 3.4 V compatibility and is isolated from the ADC core. Each buffer can be loaded by a maximum of 10 pF.
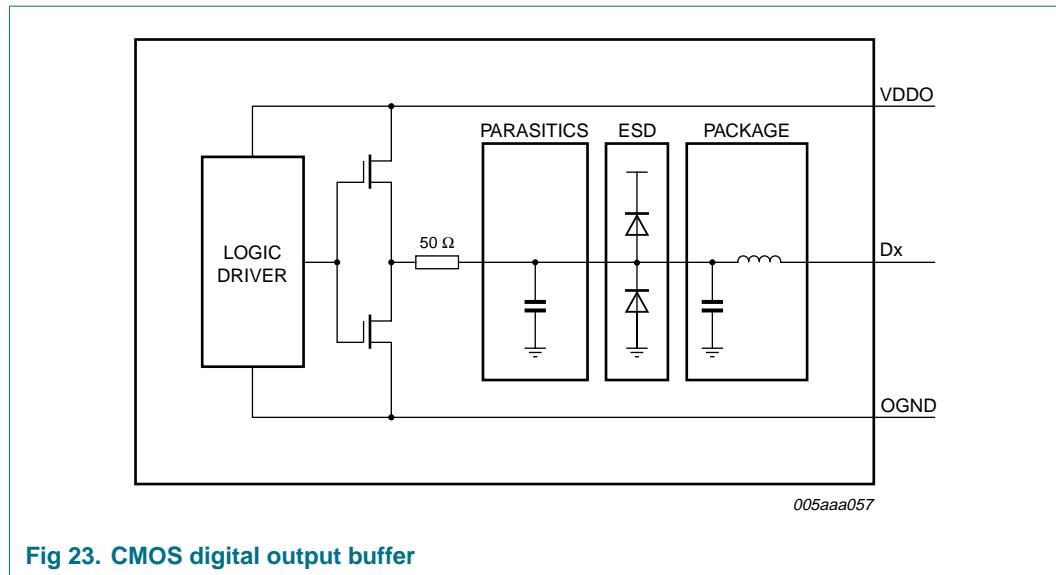

Fig 23. CMOS digital output buffer

The output resistance is 50 Ω and is the combination of the an internal resistor and the equivalent output resistance of the buffer. There is no need for an external damping resistor. The drive strength of both data and DAV buffers can be programmed via the SPI in order to adjust the rise and fall times of the output digital signals (see Table 29):

11.5.2 Digital output buffers: LVDS DDR mode

The digital output buffers can be configured as LVDS DDR by setting bit LVDS/CMOS to 1 (see Table 22).
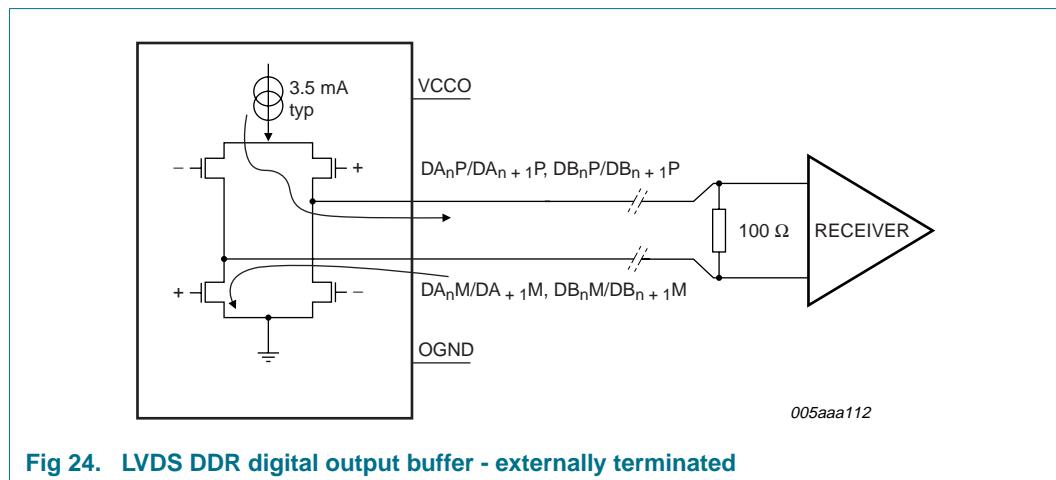
Fig 24. LVDS DDR digital output buffer - externally terminated

Each output should be terminated externally with a 100 Ω resistor (typical) at the receiver side (Figure 24) or internally via SPI control bits LVDS_INTTER (see Figure 25 and Table 31).
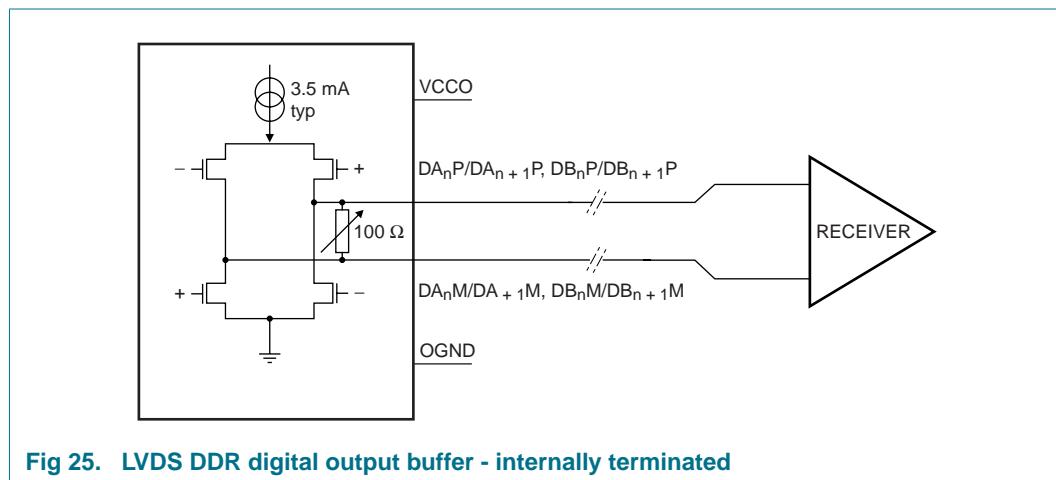

Fig 25. LVDS DDR digital output buffer - internally terminated

The default LVDS DDR output buffer current is set to 3.5 mA. It can be programmed via the SPI (bits DAVI and DATAI; see Table 30) in order to adjust the output logic voltage levels.

11.5.3 Data valid (DAV) output clock

A data valid output clock signal (DAV) is provided that can be used to capture the data delivered by the ADC1412D. Detailed timing diagrams for CMOS and LVDS DDR modes are provided in Figure 26 and Figure 27 respectively.

11.5.4 Out-of-Range (OTR)

An out-of-range signal is provided on pin OTRA for ADC channel A and on pin OTRB for ADC channel B. By default, pins OTRA/B go HIGH fourteen clock cycles after an OTR event has occurred. The OTR response can be speeded up by enabling Fast OTR (bit

FASTOTR = 1; see Table 28). When Fast OTR is enabled, OTRA/B goes HIGH four clock cycles after the OTR event (separately for each ADC channel). The Fast OTR detection threshold (below full scale) can be programmed via bits FASTOTR_DET.

11.5.5 Digital offset

By default, the ADC1412D delivers output code that corresponds to the analog input. However it is possible to add a digital offset to the output code via the SPI (bits DIG_OFFSET; see Table 24).

11.5.6 Test patterns

For test purposes, the ADC1412D can be configured to transmit one of a number of predefined test patterns (via bits TESTPAT_SEL; see Table 25). A custom test pattern can be defined by the user (TESTPAT_USER; see Table 26 and Table 27) and is selected when TESTPAT_SEL = 101. The selected test pattern will be transmitted regardless of the analog input.
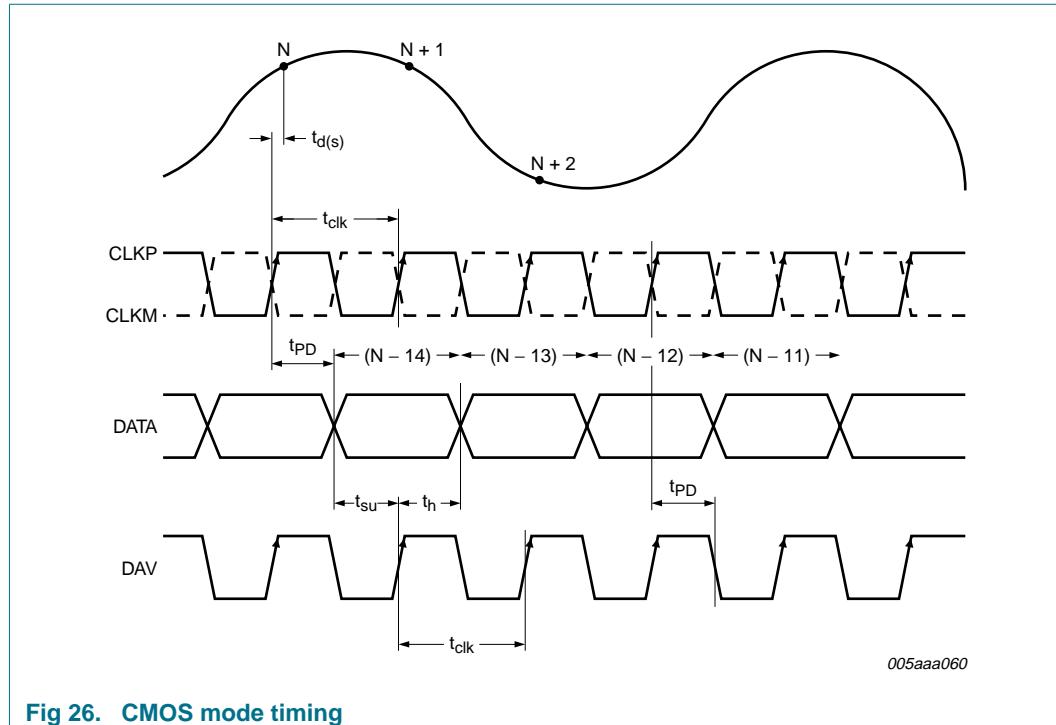
11.5.7 Output codes versus input voltage

Table 14. Output codes
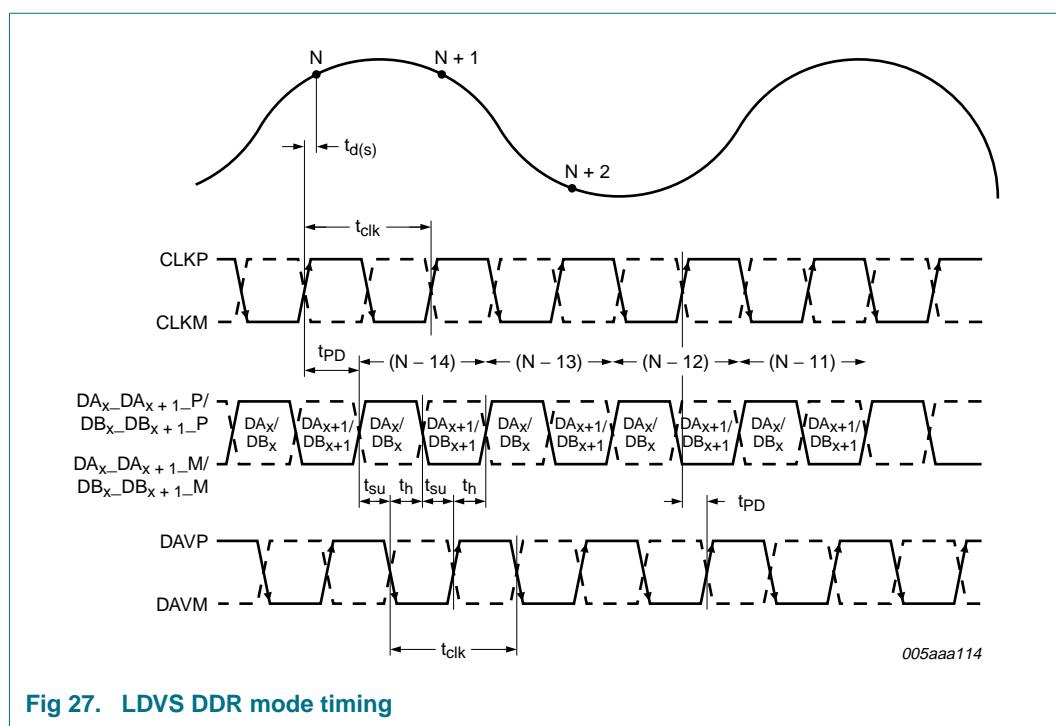
$V_{INAP} - V_{INAM}/$ $V_{INBP} - V_{INBM}$	Offset binary	Two's complement	OTRA/B pin
< −1	00 0000 0000 0000	10 0000 0000 0000	1
−1	00 0000 0000 0000	10 0000 0000 0000	0
−0.9998779	00 0000 0000 0001	10 0000 0000 0001	0
−0.9997559	00 0000 0000 0010	10 0000 0000 0010	0
−0.9996338	00 0000 0000 0011	10 0000 0000 0011	0
−0.9995117	00 0000 0000 0100	10 0000 0000 0100	0
....	....	....	0
−0.0002441	01 1111 1111 1110	11 1111 1111 1110	0
−0.0001221	01 1111 1111 1111	11 1111 1111 1111	0
0	**10 0000 0000 0000**	**00 0000 0000 0000**	0
+0.0001221	10 0000 0000 0001	00 0000 0000 0001	0
+0.0002441	10 0000 0000 0010	00 0000 0000 0010	0
....	....	....	0
+0.9995117	11 1111 1111 1011	01 1111 1111 1011	0
+0.9996338	11 1111 1111 1100	01 1111 1111 1100	0
+0.9997559	11 1111 1111 1101	01 1111 1111 1101	0
+0.9998779	11 1111 1111 1110	01 1111 1111 1110	0
+1	11 1111 1111 1111	01 1111 1111 1111	0
> +1	11 1111 1111 1111	01 1111 1111 1111	1

11.6 Timings summary

11.6.1 CMOS mode timings

Fig 26. CMOS mode timing

11.6.2 LVDS DDR mode timing

Fig 27. LDVS DDR mode timing

11.7 Serial Peripheral Interface (SPI)

11.7.1 Register Description

The ADC1412D serial interface is a synchronous serial communications port that allows for easy interfacing with many commonly-used microprocessors. It provides access to the registers that control the operation of the chip.

This interface is configured as a 3-wire type (SDIO as bidirectional pin)

Pin SCLK is the serial clock input and $\overline{CS}$ is the chip select pin.

Each read/write operation is initiated by a LOW level on $\overline{CS}$. A minimum of three bytes will be transmitted (two instruction bytes and at least one data byte). The number of data bytes is determined by the value of bits W1 and W2 (see Table 16).

Table 15. Instruction bytes for the SPI

	MSB							LSB
Bit	7	6	5	4	3	2	1	0
Description	R/$\overline{W}$[1]	W1[2]	W0[2]	A12	A11	A10	A9	A8
	A7	A6	A5	A4	A3	A2	A1	A0

[1] Bit R/$\overline{W}$ indicates whether it is a read (1) or a write (0) operation.

[2] Bits W1 and W0 indicate the number of bytes to be transferred after the instruction byte (see Table 16).

Table 16. Number of data bytes to be transferred after the instruction bytes

W1	W0	Number of bytes transmitted
0	0	1 byte
0	1	2 bytes
1	0	3 bytes
1	1	4 bytes or more

Bits A12 to A0 indicate the address of the register being accessed. In the case of a multiple byte transfer, this address is the first register to be accessed. An address counter is incriminated to access subsequent addresses.

The steps involved in a data transfer are as follows:

1. A falling edge on $\overline{CS}$ in combination with a rising edge on SCLK determine the start of communications.

2. The first phase is the transfer of the 2-byte instruction.

3. The second phase is the transfer of the data which can vary in length but will always be a multiple of 8 bits. The MSB is always sent first (for instruction and data bytes).

4. A rising edge on $\overline{CS}$ indicates the end on data transmission.
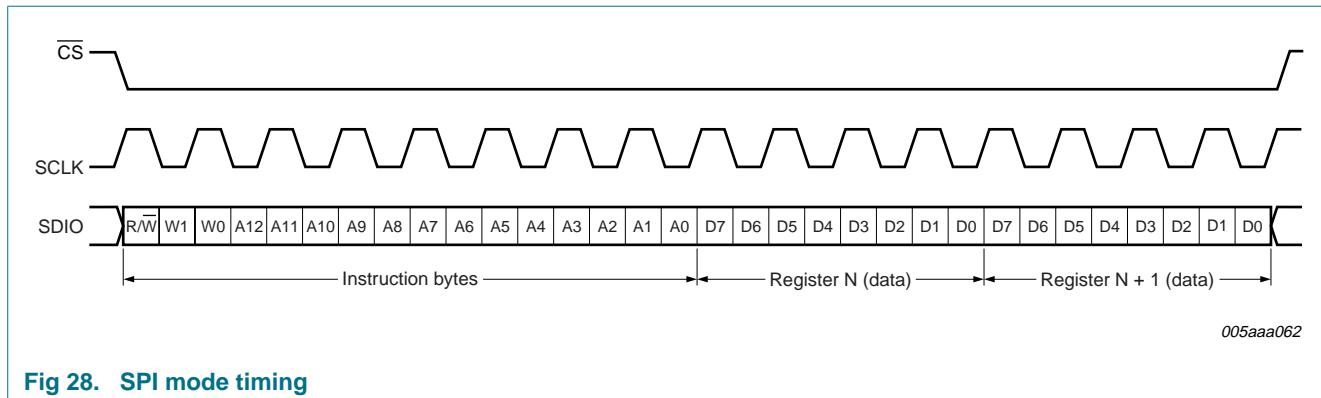
Fig 28. SPI mode timing

11.7.2 Default modes at start-up

During circuit initialization, it doesn't matter which output data standard has been selected. At power-up, the device defaults to PIN control mode.

A falling edge on $\overline{CS}$ will trigger a transition to SPI control mode. When the ADC1412D enters SPI control mode, the output data standard (CMOS/LVDS DDR) is determined by the level on pin SDIO (see Figure 29). Once in SPI control mode, the output data standard can be changed via bit LVDS/CMOS in Table 22.

When the ADC1412D enters SPI control mode, the output data format (2's complement or offset binary) is determined by the level on pin SCLK (grey code can only be selected via the SPI). Once in SPI control mode, the output data format can be changed via bit DATA_FORMAT in Table 22.
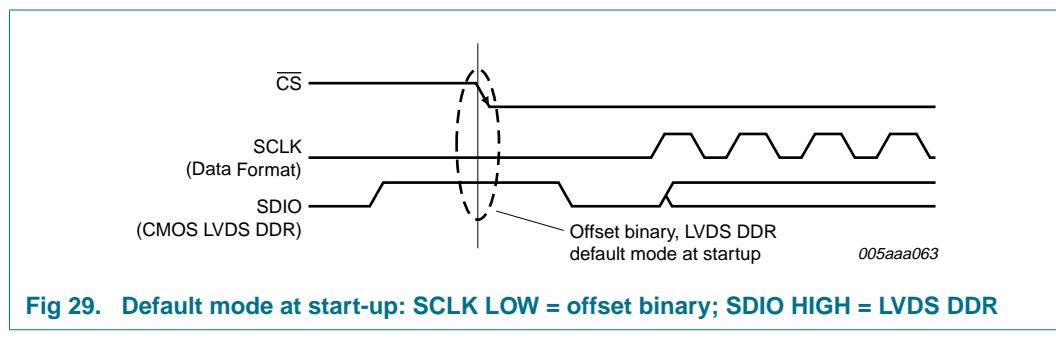

Fig 29. Default mode at start-up: SCLK LOW = offset binary; SDIO HIGH = LVDS DDR
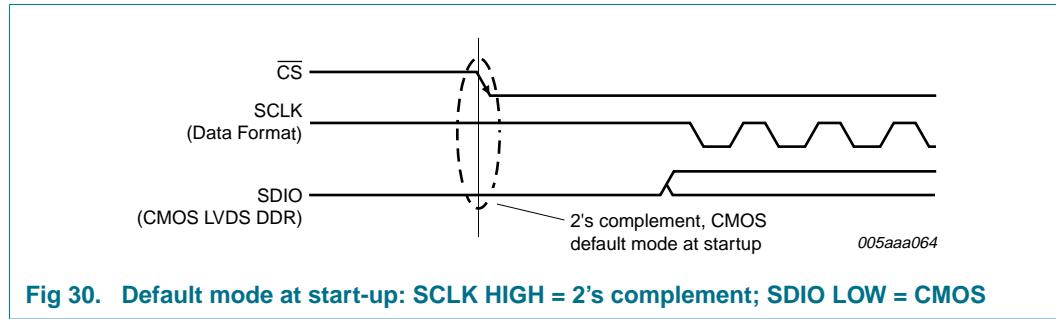

Fig 30. Default mode at start-up: SCLK HIGH = 2's complement; SDIO LOW = CMOS

11.7.3 Register allocation map

Table 17. Register allocation map

Addr Hex	Register name	R/W	Bit definition								Default
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin
0003	Channel index	R/W	-	-	-	-	-	-	ADCB	ADCA	0000 0011
0005	Reset and operating mode	R/W	SW_ RST	-	-	-	-	-	OP_MODE		0000 0000
0006	Clock	R/W	-	-	-	SE_SEL	DIFF/SE	-	CLKDIV	DCS_EN	0000 0001
0008	Internal reference	R/W	-	-	-	-	INTREF_ EN	INTREF			0000 0000
0011	Output data standard.	R/W	-	-	-	LVDS/ CMOS	OUTBUF	-	DATA_FORMAT		0000 0000
0012	Output clock	R/W	-	-	-	-	DAVINV	DAVPHASE			0000 1110
0013	Offset	R/W	-	-	DIG_OFFSET						0000 0000
0014	Test pattern 1	R/W	-	-	-	-	-	TESTPAT_SEL			0000 0000
0015	Test pattern 2	R/W	TESTPAT_USER								0000 0000
0016	Test pattern 2	R/W	TESTPAT_USER						-	-	0000 0000
0017	Fast OTR	R/W	-	-	-	-	FASTOTR	FASTOTR_DET			0000 0000
0020	CMOS output	R/W	-	-	-	-	DAV_DRV	DATA_DRV			0000 1110
0021	LVDS DDR O/P 1	R/W	-	-	-	DAVI		-	DATAI		0000 0000
0022	LVDS DDR O/P 2	R/W	-	-	-	-	BIT/BYTE_ WISE	LVDS_INTTER			0000 0000

Table 18. Channel index control register (address 0003h) bit description

Bit	Symbol	Access	Value	Description
7 to 2	reserved			
1	ADCB	R/W		next SPI command for ADC B
			0	ADC B not selected
			1	ADC B selected
0	ADCA	R/W		next SPI command for ADC A
			0	ADC A not selected
			1	ADC A selected

Table 19.   Reset and operating mode control register (address 0005h) bit description

Bit	Symbol	Access	Value	Description
7	SW_RST	R/W		reset digital section
			0	no reset
			1	performs a reset of the digital section
6 to 2	reserved			
1 to 0	OP_MODE	R/W		operating mode
			00	normal (Power-up)
			01	Power-down
			10	Sleep
			11	normal (Power-up)

Table 20.   Clock control register (address 0006h) bit description

Bit	Symbol	Access	Value	Description
7 to 5	reserved			
4	SE_SEL	R/W		single-ended clock input pin select
			0	CLKM
			1	CLKP
3	DIFF/SE	R/W		differential/single ended clock input select
			0	fully differential
			1	single-ended
2	reserved			
1	CLKDIV	R/W		clock input divide by 2
			0	disabled
			1	enabled
0	DCS_EN	R/W		duty cycle stabilizer
			0	disabled
			1	enabled

Table 21.   Internal reference control register (address 0008h) bit description

Bit	Symbol	Access	Value	Description
7 to 4	reserved			
3	INTREF_EN	R/W		programmable internal reference enable
			0	disable
			1	active

Table 21. Internal reference control register (address 0008h) bit description …*continued*

Bit	Symbol	Access	Value	Description
2 to 0	INTREF	R/W		programmable internal reference
			000	0 dB (FS = 2 V)
			001	−1 dB (FS = 1.78 V)
			010	−2 dB (FS = 1.59 V)
			011	−3 dB (FS = 1.42 V)
			100	−4 dB (FS = 1.26 V)
			101	−5 dB (FS = 1.12 V)
			110	−6 dB (FS = 1 V)
			111	reserved

Table 22. Output data standard control register (address 0011h) bit description

Bit	Symbol	Access	Value	Description
7 to 5	reserved			
4	LVDS/CMOS	R/W		output data standard: LVDS DDR or CMOS
			0	CMOS
			1	LVDS DDR
3	OUTBUF	R/W		output buffers enable
			0	output enabled
			1	output disabled (high Z)
2	reserved			
1 to 0	DATA_FORMAT	R/W		output data format
			00	offset binary
			01	2's complement
			10	gray code
			11	offset binary

Table 23. Output clock register (address 0012h) bit description

Bit	Symbol	Access	Value	Description
7 to 4	reserved			
3	DAVINV	R/W		output clock data valid (DAV) polarity
			0	normal
			1	inverted
2 to 0	DAVPHASE	R/W		DAV phase select
			000	output clock shifted (ahead) by 3 ns
			001	output clock shifted (ahead) by 2.5 ns
			010	output clock shifted (ahead) by 2 ns
			011	output clock shifted (ahead) by 1.5 ns
			100	output clock shifted (ahead) by 1 ns
			101	output clock shifted (ahead) by 0.5 ns
			110	default value as defined in timing section
			111	output clock shifted (delayed) by 0.5 ns

Table 24. Offset register (address 0013h) bit description

Bit	Symbol	Access	Value	Description
7 to 6	reset			
5 to 0	DIG_OFFSET	R/W		digital offset adjustment
			011111	+31 LSB
			...	...
			000000	0
			...	...
			100000	−32 LSB

Table 25. Test pattern register 1(address 0014h) bit description

Bit	Symbol	Access	Value	Description
7 to 3	reserved			
2 to 0	TESTPAT_SEL	R/W		digital test pattern select
			000	off
			001	mid scale
			010	−FS
			011	+FS
			100	toggle '1111..1111'/'0000..0000'
			101	custom test pattern
			110	'1010..1010.'
			111	'010..1010'

Table 26. Test pattern register 2 (address 0015h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	TESTPAT_USER	R/W		custom digital test pattern (bits 13 to 6)

Table 27. Test pattern register 3 (address 0016h) bit description

Bit	Symbol	Access	Value	Description
7 to 2	TESTPAT_USER	R/W		custom digital test pattern (bits 5 to 0)
1 to 0	reserved			

Table 28. Fast OTR register (address 0017h) bit description

Bit	Symbol	Access	Value	Description
7 to 4	reset			
3	FASTOTR	R/W		fast Out-of-Range (OTR) detection
			0	disabled
			1	enabled

Table 28. Fast OTR register (address 0017h) bit description *...continued*

Bit	Symbol	Access	Value	Description
2 to 0	FASTOTR_DET	R/W		set fast OTR detect level
			000	−20.56 dB
			001	−16.12 dB
			010	−11.02 dB
			011	−7.82 dB
			100	−5.49 dB
			101	−3.66 dB
			110	−2.14 dB
			111	−0.86 dB

Table 29. CMOS output register (address 0020h) bit description

Bit	Symbol	Access	Value	Description
7 to 4	reserved			
3 to 2	DAV_DRV	R/W		drive strength for DAV CMOS output buffer
			00	low
			01	medium
			10	high
			11	very high
1 to 0	DATA_DRV	R/W		drive strength for DATA CMOS output buffer
			00	low
			01	medium
			10	high
			11	very high

Table 30. LVDS DDR output register 1 (address 0021h) bit description
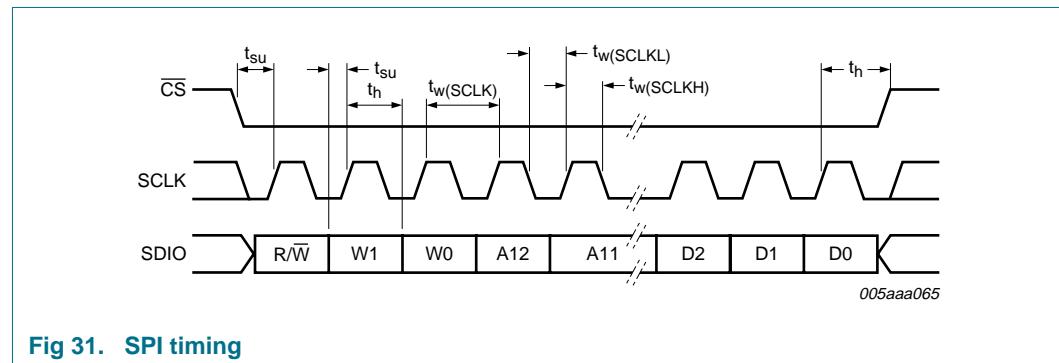
Bit	Symbol	Access	Value	Description
7 to 5	reserved			
4 to 3	DAVI	R/W		LVDS current for DAV LVDS buffer
			00	3.5 mA
			01	4.5 mA
			10	1.25 mA
			11	2.5 mA
2	reserved			
1 to 0	DATAI	R/W		LVDS current for DATA LVDS buffer
			00	3.5 mA
			01	4.5 mA
			10	1.25 mA
			11	2.5 mA

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Table 31. LVDS DDR output register 2 (address 0022h) bit description

Bit	Symbol	Access	Value	Description
7 to 4	reserved			
3	BIT/BYTE_WISE	R/W		DDR mode for LVDS output
			0	bit wise (even data bits output on DAV rising edge / odd data bits output on DAV falling edge)
			1	byte wise (MSB data bits output on DAV rising edge / LSB data bits output on DAV falling edge)
2 to 0	LVDS_INTTER	R/W		internal termination for LVDS buffer (DAV and DATA)
			000	no internal termination
			001	300 Ω
			010	180 Ω
			011	110 Ω
			100	150 Ω
			101	100 Ω
			110	81 Ω
			111	60 Ω

11.7.4 Serial timing interface

SPI timing is shown in Figure 31.

005aaa065

Fig 31. SPI timing

SPI timing characteristics are detailed in Table 9.

12. Package outline

HVQFN64: plastic thermal enhanced very thin quad flat package; no leads;
64 terminals; body 9 x 9 x 0.85 mm
SOT804-3

Dimensions

Unit	A	A$_1$	b	c	D$^{(1)}$	D$_h$	E$^{(1)}$	E$_h$	e	e$_1$	e$_2$	L	v	w	y	y$_1$
max	1.00	0.05	0.30		9.1	7.25	9.1	7.25				0.5				
mm nom	0.85	0.02	0.21	0.2	9.0	7.10	9.0	7.10	0.5	7.5	7.5	0.4	0.1	0.05	0.05	0.1
min	0.80	0.00	0.18		8.9	6.95	8.9	6.95				0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot804-3_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT804-6	- - -	- - -	- - -			~~09-02-23~~ 09-02-24
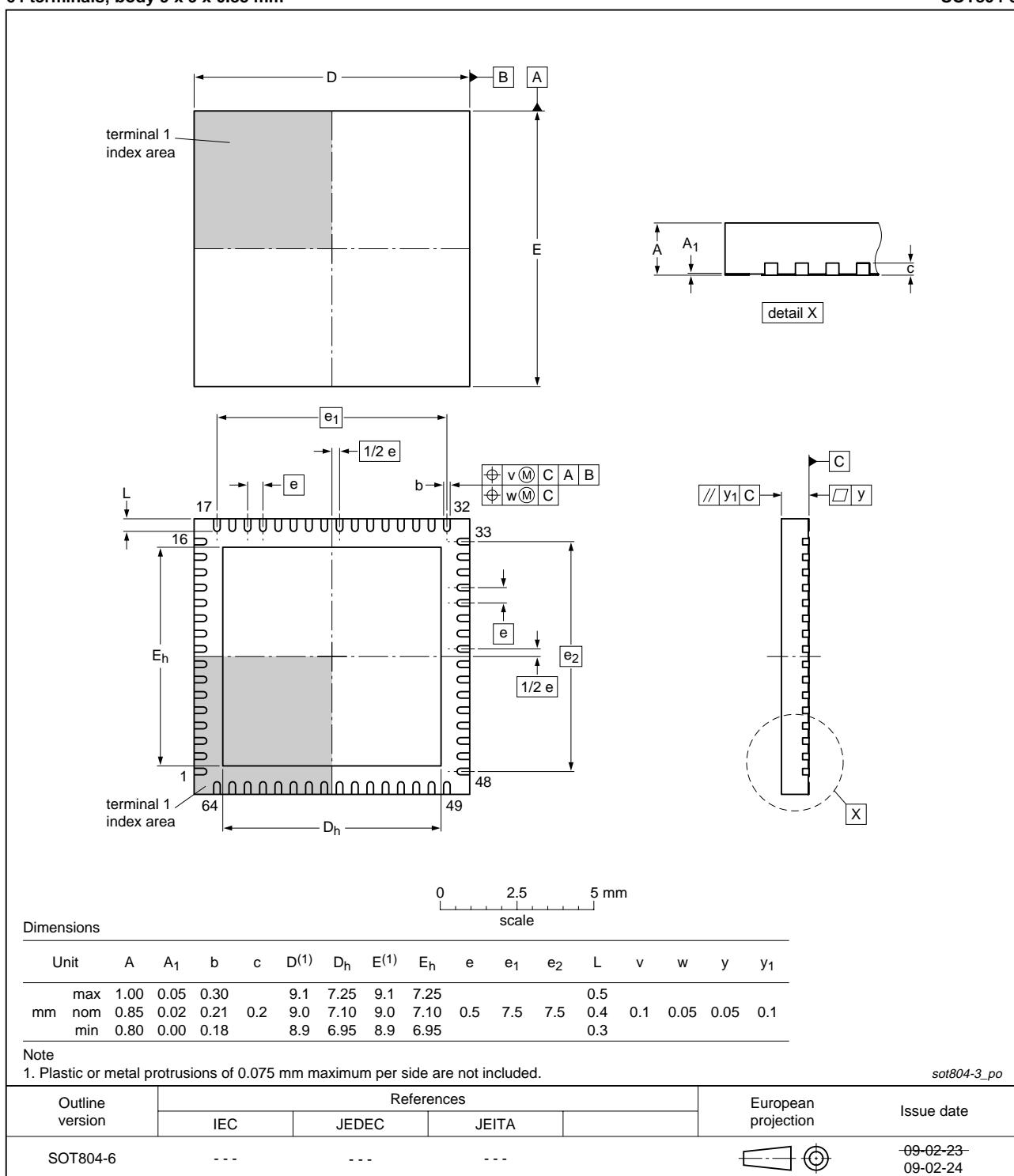
Fig 32. Package outline SOT804-3 (HVQFN64)

13. Revision history

Table 32.   Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ADC1412D065_080_105_125_2	20090604	Objective data sheet	-	ADC1412D065_080_105_125_1
Modifications:		• Values in Table 7 have been updated.		
ADC1412D065_080_105_125_1	20090528	Objective data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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