CADEKA®
Amplify the Human Experience

SPT1019

8-BIT, HIGH SPEED D/A CONVERTER

FEATURES

- 275 MWPS Conversion Rate - Version A
- 165 MWPS Conversion Rate - Version B
- Compatible with the HDAC10181 with Improved Performance
- RS-343-A Compatible
- Complete Video Controls: Sync, Blank, Bright and Reference White (Force High)
- 10KH, 100K ECL Compatible
- Single Power Supply
- Registered Data and Video Controls
- Differential Current Outputs
- Stable On-Chip Bandgap Reference
- ESD Protected Data and Control Inputs

APPLICATIONS

- High Resolution Color or Monochrome Raster Graphics Displays
- Medical Electronics: CAT, PET, MR Imaging Displays
- CAD/CAE Workstations
- Solids Modeling
- General Purpose High-Speed D/A Conversion
- Digital Synthesizers
- Automated Test Equipment
- Digital Transmitters/Modulators

GENERAL DESCRIPTION

The SPT1019 is a monolithic 8-bit digital-to-analog converter capable of accepting video data at a 165 or 275 MWPS rate. Complete with video controls (Sync, Blank, Reference White [Force High], Bright), the SPT1019 directly drives doubly-terminated 50 or 75 ohm loads to standard composite video levels. The standard setup level is 7.5 IRE. The SPT1019 is

pin-compatible with the HDAC10181 with improved performance. The SPT1019 contains data and control input registers, video control logic, reference buffer, and current switches.

The SPT1019 is available in a 24-lead PDIP package in the industrial temperature range. Contact the factory for military temperature and /883 versions.

BLOCK DIAGRAM
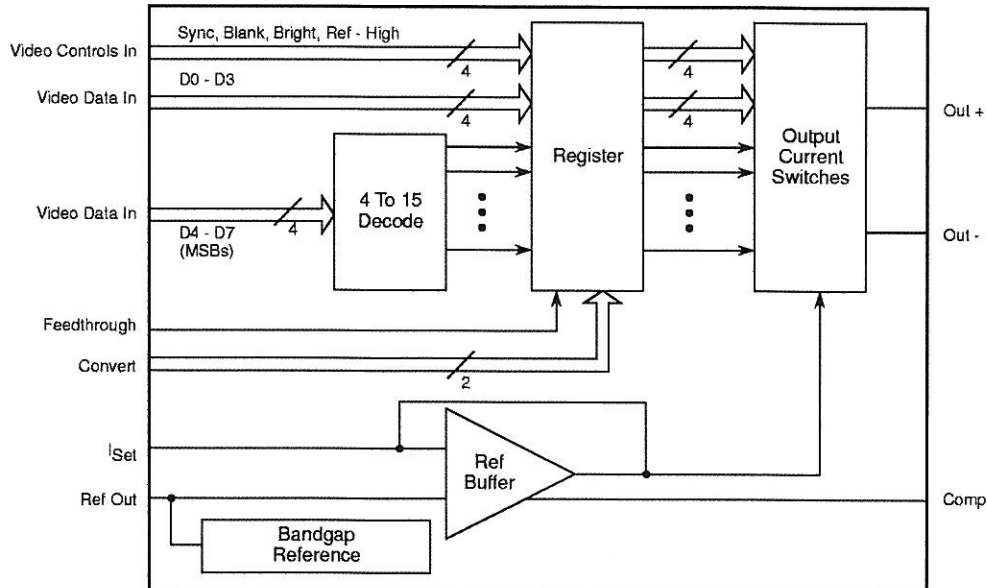
ABSOLUTE MAXIMUM RATING (Beyond which damage may occur)[1]

Supply Voltages
V_{EE} (measured to V_{CC}) .... -7.0 to 0.5 V

Input Voltages
CONV, Data, and Controls .... V_{EE} to 0.5 V
(measured to V_{CC})
Ref+ (measured to V_{CC}) .... V_{EE} to 0.5 V
Ref- (measured to V_{CC}) .... V_{EE} to 0.5 V

Temperature
Operating,   ambient .... -25 to + 85 °C
              junction .... + 175 °C
Lead, Soldering (10 seconds) .... + 300 °C
Storage .... -60 to + 150 °C

Note: 1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

V_{CC} =ground, V_{EE} = -5.2 V ±0.3 V, T_A =T_{MIN} to T_{MAX}, C_C = 0 pF, I_{Set} = 1.105 mA, unless otherwise sprecified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTISTICS						
Integral Linearity Error	1.0 mA<I_{Set}<1.3 mA	VI	-.37 -.95		+.37 +.95	% Full Scale LSB
Differential Linearity Error	1.0 mA<I_{Set}<1.3 mA	VI	-0.2 -0.5		+0.2 +0.5	% Full Scale LSB
Gain Error		VI	-19		+19	% Full Scale
Gain Error Tempco		V		150		PPM/°C
Input Capacitance, Ref Out, I_{Set}		V		5		pF
Compliance Voltage, + Output		VI	-1.2		1.5	V
Compliance Voltage, - Output		VI	-1.2		1.5	V
Equivalent Output Resistance		VI	20			kΩ
Output Capacitance		V		12		pF
Maximum Current, + Output		IV	45			mA
Maximum Current, - Output		IV	45			mA
Output Offset Current		VI		0.05	0.5	LSB
Input Voltage, Logic HIGH		VI	-1.0			V
Input Voltage, Logic LOW		VI			-1.5	V
Convert Voltage, Common Mode Range (V_{ICM})		IV	-0.5		-2.5	V
Convert Voltage, Differential (V_{IDF})		IV	0.4		1.2	V
Input Current, Logic LOW, Data and Controls		VI		35	120	μA
Input Current, Logic HIGH, Data and Controls		VI		40	120	μA
Input Current, Convert		VI		2	60	μA
Bandgap Tempco		V		100		PPM/°C

ELECTRICAL SPECIFICATIONS

V_{CC} =ground, V_{EE} = -5.2 V ±0.3 V, T_A =T_{MIN} to T_{MAX}, C_C = 0 pF, I_{Set} = 1.105 mA, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	LEVEL	MIN	TYP	MAX	UNITS
Reference Voltage Measured to V_{CC}		VI	1.3	-1.2	1.0	V
Input Capacitance, Data and Controls		V		3.0		pF
Power Supply Sensitivity		VI	-120	20	+120	µA/V
Supply Current		VI		155	220	mA
DYNAMIC CHARACTERISTICS (R_L = 37.5 ohms, C_L = 5 pF, T_A = 25 °C, I_{Set} = 1.105 mA)						
Maximum Conversion Rate	B Grade	IV	165			MWPS
	A Grade	IV	275			MWPS
Rise Time	10% to 90% G.S.	IV			1.6	ns
	T_A = T_{MIN} to T_{MAX}	IV			2.0	ns
Rise Time	10% to 90% G.S. R_L = 25 ohms	V		1.0		ns
Current Settling Time, Clocked Mode	To 0.2% G.S.	V		7.0		ns
Current Settling Time, Clocked Mode	To 0.8% G.S.	V		5.5		ns
Current Settling Time, Clocked Mode t_{SI}	To 0.2% G.S. R_L = 25 Ω	V		4.5		ns
Clock to Output Delay, Clocked Mode t_{DSC}	T_A = T_{MIN} to T_{MAX}	IV		2.2	4.0	ns
		IV			4.5	ns
Data to Output Delay, Transparent Mode t_{DST}		IV		3.2	6.0	ns
		IV			6.0	ns
Convert Pulse Width, (LOW or HIGH) t_{PWL}, t_{PWH}	B Grade	IV	3.0			ns
	A Grade	IV	1.8			ns
Glitch Energy	Area = 1/2 VT	V		4		pV-s
Reference Bandwidth, -3 dB		V		1.0		MHz
Setup Time, Data and Controls t_S	T_A = T_{MIN} to T_{MAX}	IV	1.0			ns
		IV	1.0			ns
Hold Time, Data and Controls t_H	T_A = T_{MIN} to T_{MAX}	IV	0.5			ns
		IV	0.5			ns
Slew Rate	20% to 80% G.S.	IV	390			V/µS
	T_A = T_{MIN} to T_{MAX}	IV	325			V/µS
Clock Feedthrough		IV			-48	dB
	T_A = T_{MIN} to T_{MAX}	IV			-48	dB

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25 °C. Parameter is guaranteed over specified temperature range.

Figure 1 - Functional Diagram
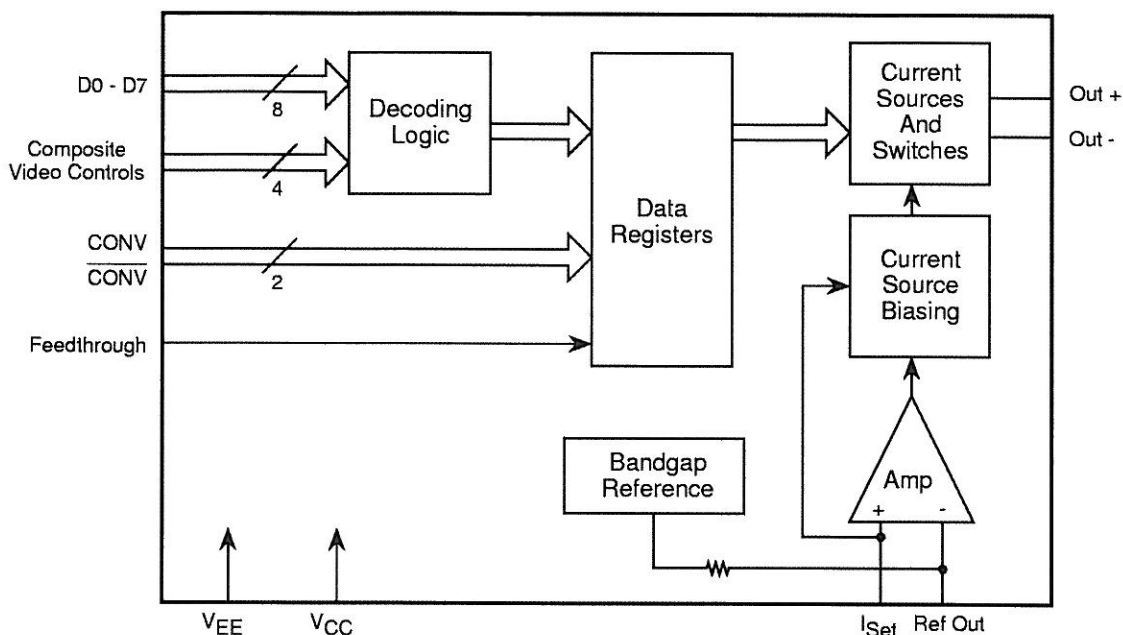
APPLICATION INFORMATION

The SPT1019 is a high speed video digital-to-analog converter capable of conversion rates of up to 275 MWPS. This makes the device suitable for driving 1500 X 1800 pixel displays at 70 to 90 Hz update rates.

The SPT1019 is separated into different conversion rate categories as shown in table I.

The SPT1019 has 10 KH and 100K ECL logic level compatible video controls and data inputs. The complementary analog output currents produced by the devices are proportional to the product of the digital control and data inputs in conjunction with the analog reference current. The SPT1019 is segmented so that the four MSBs of the input data are separated into a parallel thermometer code. From here, fifteen identical current sinks are driven to fabricate sixteen

coarse output levels. The remaining four LSBs drive four binary weighted current switches.

The MSB currents are then summed with the LSBs, which provide a one-sixteenth of full scale contribution, to provide the 256 distinct analog output levels.

The video control inputs drive weighted current sinks that are added to the output current to produce composite video output levels. These controls, Sync, Blank, Reference White (Force High), and Bright are needed in video applications.

Another feature that similar video D/A converters do not have is the Feedthrough Control. This pin allows registered or unregistered operation of the video control and data inputs. In the registered mode, the composite functions are latched to the pixel data to prevent screen-edge distortions generally found on unregistered video DACs.

Table I - The SPT1019 Family and Speed Designations

PART NUMBER	UPDATE	COMMENTS
SPT1019A	275 MWPS	Suitable for 1200 X 1500 to 1500 X 1800 displays at 60 to 90 Hz update rate.
SPT1019B	165 MWPS	Suitable for 1024 X 1280 to 1200 X 1500 displays at 60 to 90 Hz update rate.

Figure 2 - Typical Interface Circuit
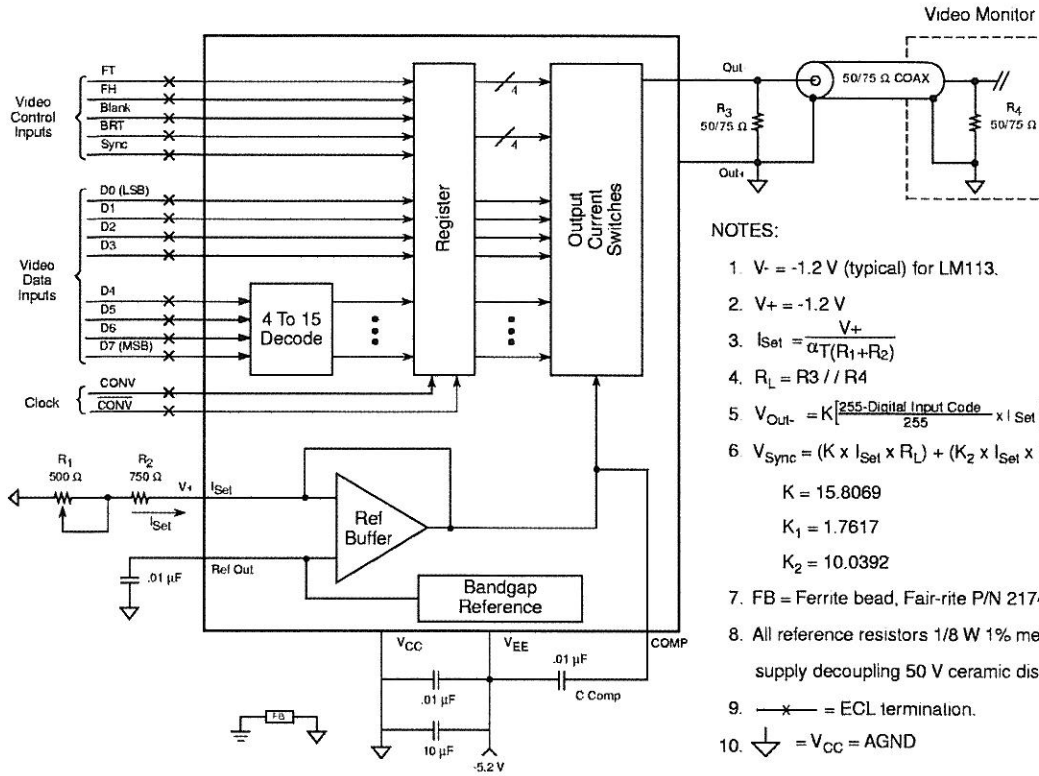
NOTES:

1. V- = -1.2 V (typical) for LM113.

2. V+ = -1.2 V

3. $I_{Set} = \dfrac{V+}{\alpha T (R_1 + R_2)}$

4. $R_L = R3 // R4$

5. $V_{Out-} = K \left[\dfrac{255 \text{-Digital Input Code}}{255} \times I_{Set} \right] R_L + [K_I \times I_{Set} \times R_L (Bright)]$

6. $V_{Sync} = (K \times I_{Set} \times R_L) + (K_2 \times I_{Set} \times R_L)$

   K = 15.8069

   K_1 = 1.7617

   K_2 = 10.0392

7. FB = Ferrite bead, Fair-rite P/N 217430011 or equivalent.

8. All reference resistors 1/8 W 1% metal film power.

   supply decoupling 50 V ceramic disc.

9. ——✕—— = ECL termination.

10. ⏚ = V_{CC} = AGND

11. See figure 8 for detail on Ref Buffer.

12. Ref Out on the SPT1019 can be used to drive up to two SPT1018 reference inputs.

13. = DGND (digital input drivers).

TYPICAL INTERFACE CIRCUIT

GENERAL

A typical interface circuit using the SPT1019 in a color raster application is shown in figure 2. The SPT1019 requires few external components and is extremely easy to use. The very high operating speeds of the SPT1019 require good circuit layout, decoupling of supplies, and proper design of transmission lines. The following considerations should be noted to achieve best performance.

INPUT CONSIDERATIONS

Video input data and controls may be directly connected to the SPT1019. Note that all ECL inputs are terminated as closely to the device as possible to reduce ringing, crosstalk and reflections. A convenient and commonly used microstrip impedance is about 130 ohms, which is easily terminated using a 330 ohm resistor to V_{EE} and a 220 ohm resistor to Ground. This arrangement gives a Thevenin equivalent termination of 130 ohms to -2 volts without the need for a -2 volt supply. Standard SIP (Single Inline Package) 220/330 resistor networks are available for this purpose. It is recommended that stripline or microstrip techniques be used for all ECL interface. Printed circuit wiring of known impedance over a solid ground plane is recommended.

OUTPUT CONSIDERATIONS

The analog outputs are designed to directly drive a dual 50 or 75 ohm load transmission system as shown. The source impedances of the SPT1019 outputs are high impedance current sinks. The load impedance (R_L) must be 25 or 37.5 ohms to attain standard RS-343-A video levels. Any deviation from this impedance will affect the resulting video output levels proportionally. As with the data interface, it is important that the analog transmission lines have matched impedance throughout, including connectors and transitions between printed wiring and coaxial cable. The combination of matched source termination resistor R_S and load terminator R_L minimizes reflections of both forward and reverse traveling waves in the analog transmission system. The return path for analog output current is V_{CC} which is connected to the source termination resistor R_S.

POWER CONSIDERATIONS

The SPT1019 operates from a single -5.2 V standard supply. Proper bypassing of the supplies will augment the SPT1019's inherent supply noise rejection characteristics. As shown in figure 2, each supply pin should be bypassed as close to the device as possible with 0.01 µF and 10 µF capacitors.

The SPT1019 has two analog (V_{EE}) power supply pins. Both supply pins should be properly bypassed as mentioned previously. This device also has two analog (V_{CC}) ground pins. Both ground pins should be tied to the analog ground plane. Power and ground pins must be connected in all applications. If a +5 V power source is required, the ground pins (V_{CC}) become the positive supply pins while the supply pins (V_{EE}) become the ground pins. The relative polarities of the other input and output voltages must be maintained.

REFERENCE CONSIDERATIONS

The SPT1019 has one reference input (I_{Set}) and one reference output (Ref Out). These pins are connected to the inverting and noninverting inputs of an internal amplifier that serves as a reference buffer amplifier. The SPT1019 has a bandgap reference connected internally to the inverting input of the buffer amplifier and Ref Out.

The output of the buffer amplifier is the reference for the current sinks. The amplifier feedback loop is connected around one of the current sinks to achieve better accuracy. (See Figure 8.)

Since the analog output currents are proportional to the digital input data and the reference current (I_{Set}), the full-scale output may be adjusted by varying the reference current. I_{SET} is controlled through the I_{Set} input on the SPT1019. A method and equations to set I_{Set} is shown in Figure 2. The SPT1019 uses its own reference voltage for setting up I_{Set} as shown in Figure 2. The value for I_{Set} can be varied with the 500 Ohm trimmer to change the full scale output. A double 50 Ohm load (25 Ohm) can be driven if I_{Set} is increased 50% more than I_{Set} for doubly terminated 75 Ohm video applications.

COMPENSATION

The SPT1019 provides an external compensation input (COMP) for the reference buffer amplifier. In order to use this pin correctly, a capacitor should be connected between COMP and V_{EE} as shown in figure 2. Keep the lead lengths as short as possible. If the reference is to be kept as a constant, use a large capacitor (.01 µF). The value of the capacitor determines the bandwidth of the amplifier. If modulation of the reference is required, smaller values of capacitance can be used to achieve up to a 1 MHz bandwidth.

Figure 3 - Timing Diagram

SPT1019
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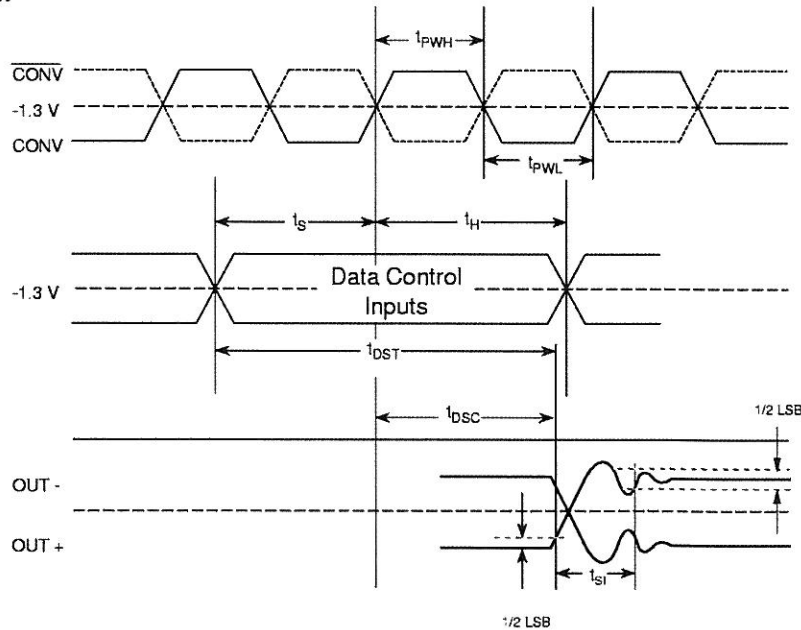
Table II - Video Control Operation (Output values for setup = 10 IRE and 75 ohm standard load)

Sync	Blank	Ref White	Bright	Data Input	Out - (mA)	Out - (V)	Out - (IRE)	Description
1	X	X	X	X	28.57	-1.071	-40	Sync Level
0	1	X	X	X	20.83	-0.781	0	Blank Level
0	0	1	1	X	0.00	0.000	110	Enhanced High Level
0	0	1	0	X	1.95	-0.073	100	Normal High Level
0	0	0	0	000...	19.40	-0.728	7.5	Normal Low Level
0	0	0	0	111...	1.95	-0.073	100	Normal High Level
0	0	0	1	000...	17.44	-0.654	17.5	Enhanced Low Level
0	0	0	1	111...	0.00	0.000	110	Enhanced High Level

DATA INPUTS AND VIDEO CONTROLS

The SPT1019 has standard single-ended data inputs. The inputs are registered to produce the lowest differential data propagation delay (skew) to minimize glitching. There are also four video control inputs to generate composite video outputs. These are Sync, Blank, Bright and Reference White or Force High. Also provided is the Feedthrough control as mentioned earlier. The controls and data inputs are all 10 KH and 100K ECL compatible. In addition, all have internal pulldown resistors to leave them at a logic low so the pins are inactive when not used. This is useful if the devices are applied as standard DACs without the need for video controls or if less than eight bits are used.

The SPT1019 is usually configured in the synchronous mode. In this mode, the controls and data are synchronized to prevent pixel dropout. This reduces screen-edge distortions and provides the lowest output noise while maintaining the highest conversion rate. By leaving the Feedthrough (FT) control open (low), each rising edge of the convert (CONV) clock latches decoded data and control values into a D-type internal register. The registered data is then converted into the appropriate analog output by the switched current sinks. When FT is tied high, the control inputs and data are not registered. The analog output asynchronously tracks the input data and video controls. Feedthrough itself is asynchronous and usually used as a DC control.

The controls and data have to be present at the input pins for a setup time of t_s before, and a hold time of t_h after, the rising edge of the clock (CONV) in order to be synchronously registered. The setup and hold times are not important in the asynchronous mode. The minimum pulse widths high (t_{PWH}) and low (t_{PWL}) as well as settling time become the limiting factors. (See figure 3.)

The video controls produce the output levels needed for horizontal blanking, frame synchronization, etc., to be compatible with video system standards as described in RS-343-A. Table II shows the video control effects on the analog output. Internal logic governs Blank, Sync, and Force High so that they override the data inputs as needed in video applications. Sync overrides both the data and other controls to produce full negative video output (figure 9).

Reference White video level output is provided by Force High, which drives the internal digital data to full scale output or 100 IRE units. Bright gives an additional 10% of full scale value to the output level. This function can be used in graphic displays for highlighting menus, cursors or warning messages. Again, if the devices are used in non-video applications, the video controls can be left open.

CONVERT CLOCK

For best performance, the clock should be ECL driven, differentially, by utilizing CONV and $\overline{CONV}$ (figure 4). By driving the clock this way, clock noise and power supply/output intermodulation will be minimized. The rising edge of the clock synchronizes the data and control inputs to the SPT1019. Since the actual switching threshold of $\overline{CONV}$ is determined by CONV, the clock can be driven single-ended by connecting a bias voltage to $\overline{CONV}$. The switching threshold of CONV is set by this bias voltage.

ANALOG OUTPUTS

The SPT1019 has two analog outputs that are high impedance, complementary current sinks. The outputs vary in proportion to the input data, controls and reference current values so that the full scale output can be changed by setting I_{Set} as mentioned earlier.

In video applications, the outputs can drive a doubly termi-

nated 50 or 75 ohm load to standard video levels. In the standard configuration of figure 5, the output voltage is the product of the output current and load impedance and is between 0 and -1.07 V. The Out- output (figure 9) will provide a video output waveform with the Sync pulse bottom at the -1.07 V level. The Out+ is inverted with Sync up.
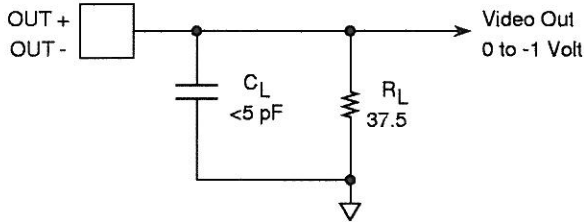
Figure 4 - CONVert, $\overline{\text{CONV}}$ert Switching Levels
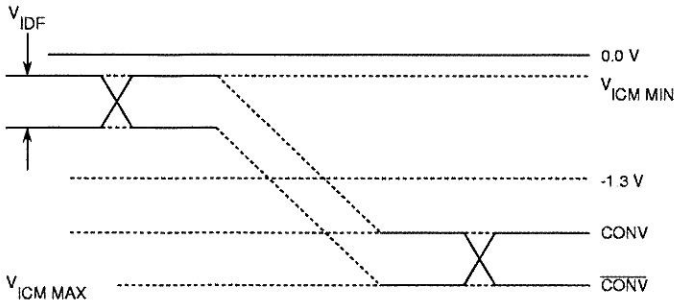
Figure 5A - Standard Load
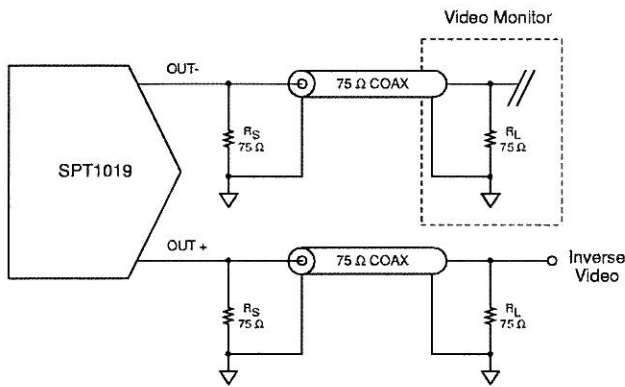
Figure 5B - Test Load

TYPICAL RGB GRAPHICS SYSTEM

In an RGB graphics system, the color displayed is determined by the combined intensities of the red, green and blue (RGB) D/A converter outputs. A change in gain or offset in any of the RGB outputs will affect the apparent hue displayed on the CRT screen.

Thus, it is very important that the outputs of the D/A converters track each other over a wide range of operating conditions. Since the D/A output is proportional to the product of the reference and digital input code, a common reference should be used to drive all three D/As in an RGB system to minimize RGB DAC-to-DAC mismatch and improve TC tracking.

The SPT1019 contains an internal precision bandgap reference which completely eliminates the need for an external reference. The reference can supply up to 50 µA to an external load, such as two other DAC reference inputs.

The circuits shown in figure 6 illustrate how a single SPT1019 may be used as a master reference in a system with multiple DACs (such as RGB). The other DACs are simply slaved from the SPT1019's reference output. The SPT1018s shown are especially well-suited to be slaved to a SPT1019 for a better TC tracking from DAC-to-DAC, since they are essentially SPT1019s without the reference. The SPT1018 is pin-compatible with the TDC1018, that does not have an internal reference. Although either the TDC1018 or the SPT1018 may be slaved from an SPT1019, the higher performance SPT1018 and the above mentioned DAC-to-DAC TC tracking is the best choice for new designs.

No external reference is required for operation of the SPT1019, as this function is provided internally. The internal reference is a bandgap type and is suitable for operation over extended temperature ranges. The SPT1018 must use an external reference.

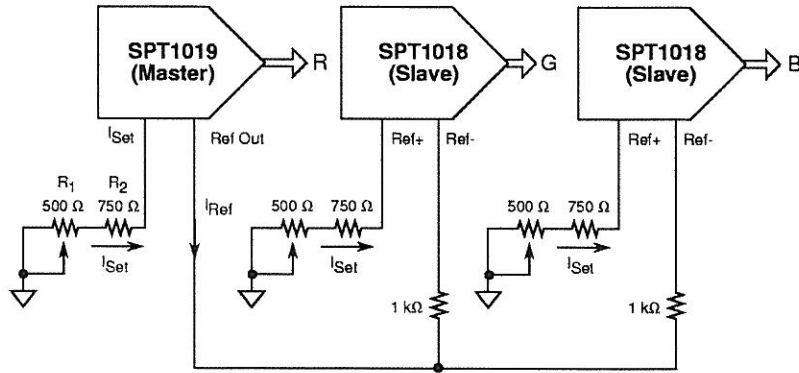### Figure 6 - Typical RGB Graphics System

Figure 7 - Burn-In Circuit

24 Pin DIP
All Resistors Are 5% 1/4 W cc
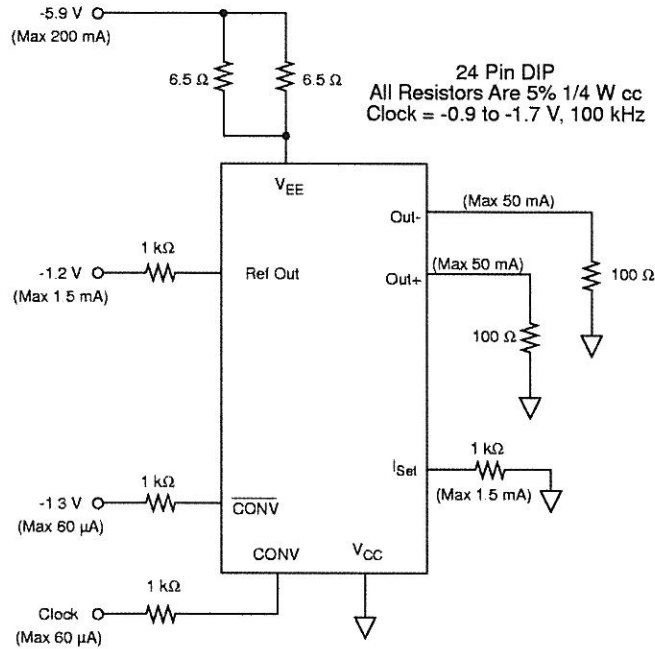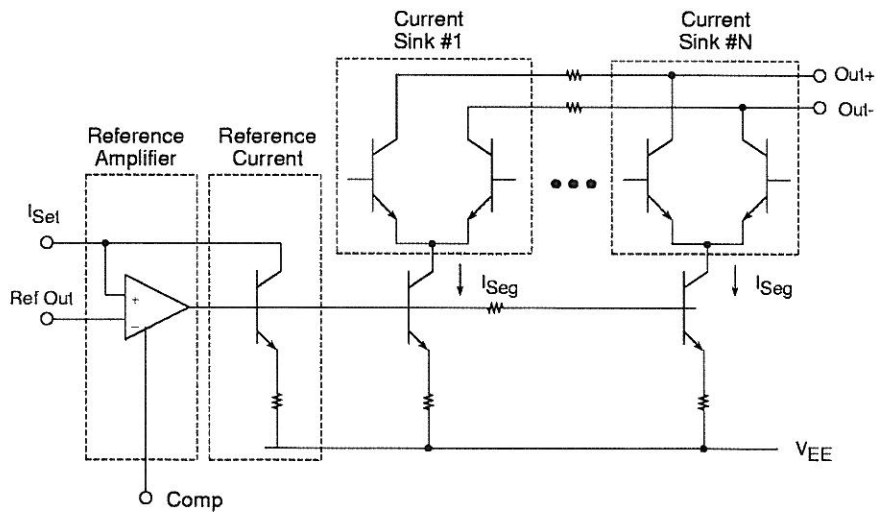Clock = -0.9 to -1.7 V, 100 kHz

Figure 8 - DAC Output Circuit
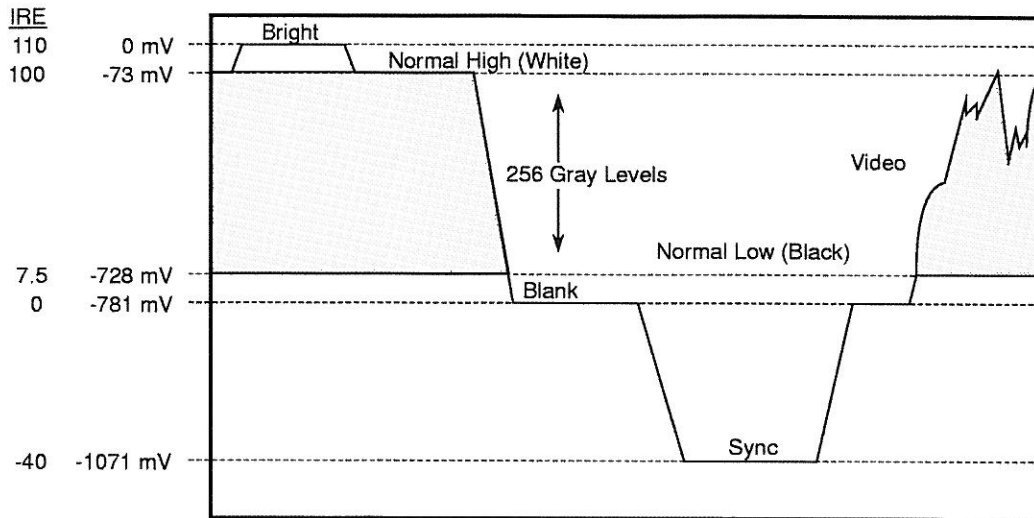
Figure 9 - Video Output Waveform for Standard Load

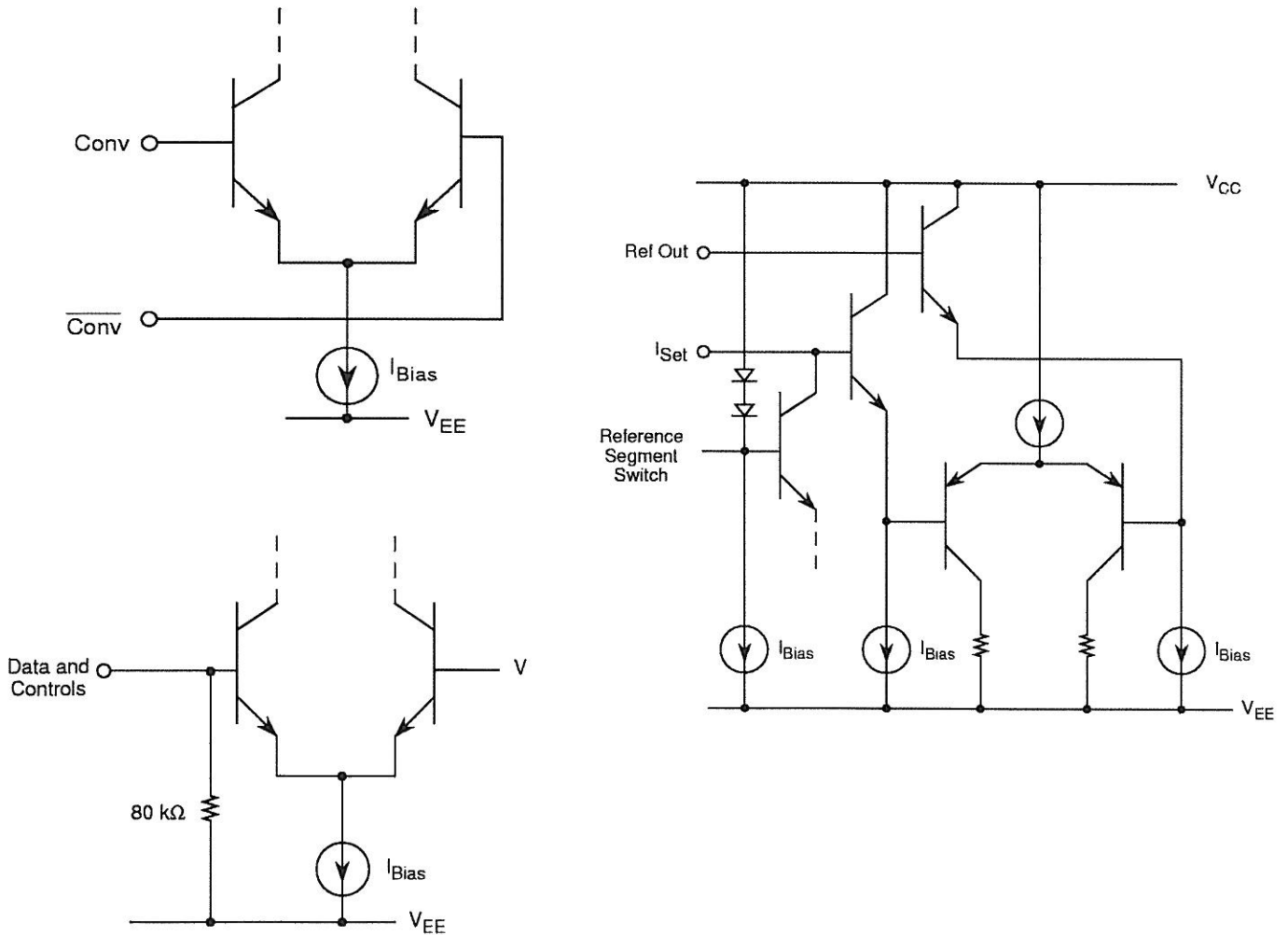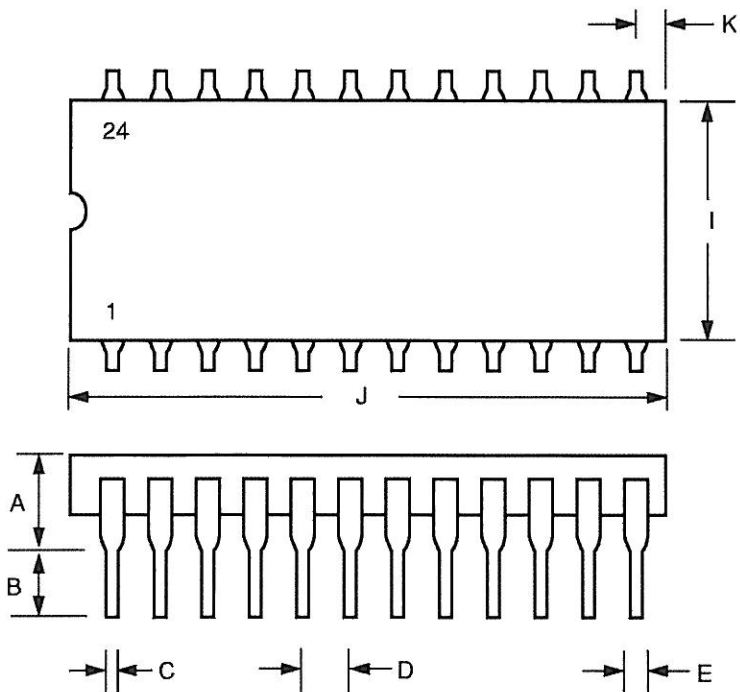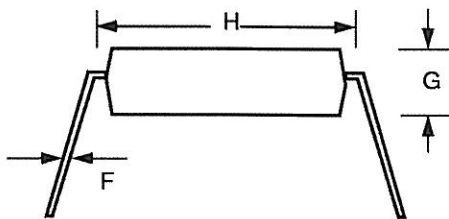**Figure 10- Equivalent Input Circuit - Data, Clock, Controls and Reference**

SPT1019

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PACKAGE OUTLINE
24-Lead PDIP

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		0.190		4.83
B	0.125	0.135	3.18	3.43
C	0.015	0.022	0.38	0.56
D	0.100 typ		2.54 typ	
E	0.055	0.065	1.40	1.65
F	0.008	0.012	0.20	0.30
G	0.150 typ		3.81 typ	
H	0.600	0.625	15.24	15.88
I	0.530	0.550	13.46	13.97
J	1.245	1.255	31.62	31.88
K	0.070	0.080	1.78	2.03

PIN ASSIGNMENTS
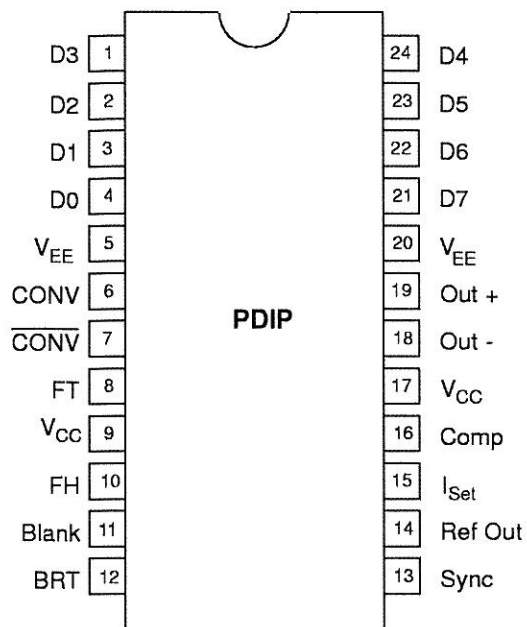
PIN FUNCTIONS

Name	Function
D3	Data Bit 3
D2	Data Bit 2
D1	Data Bit 1
D0	Data Bit 0 (LSB)
V_{EE}	Negative Supply
CONV	Convert Clock Input
$\overline{CONV}$	Convert Clock Input Complement
FT	Register Feedthrough Control
V_{CC}	Positive Supply
FH	Data Force High Control
Blank	Video Blank Input
BRT	Video Bright Input
Sync	Video Sync Input
Ref Out	Reference Output
I_{Set}	Reference Current + Input
COMP	Compensation Input
Out-	Output Current Negative
Out+	Output Current Positive
D7	Data Bit 7 (MSB)
D6	Data Bit 6
D5	Data Bit 5
D4	Data Bit 4

ORDERING INFORMATION

PART NUMBER	DESCRIPTION	TEMPERATURE RANGE	PACKAGE
SPT1019AIN	8-BIT, 275 MWPS DAC	-25 to +85 °C	24L PDIP
SPT1019BIN	8-BIT, 165 MWPS DAC	-25 to +85 °C	24L PDIP

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