

PM75CS1D120

FLAT-BASE TYPE
INSULATED PACKAGE

PM75CS1D120



FEATURE

Inverter + Drive & Protection IC

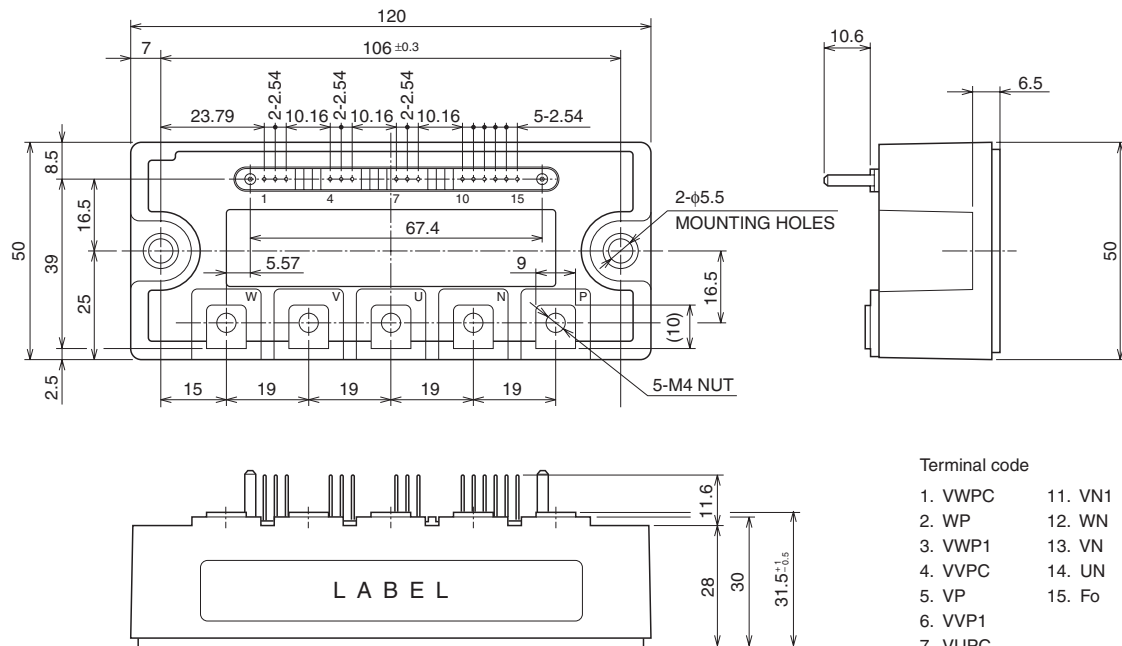
- 3 phase 75A/1200V CSTBT™
(The Current sensor and the thermal sensor with a build-in CSTBT™.)
- Monolithic gate drive & protection logic
- Detection, protection & status indication circuits for, short-circuit, over-temperature & under-voltage

APPLICATION

General purpose inverter, servo drives and other motor controls

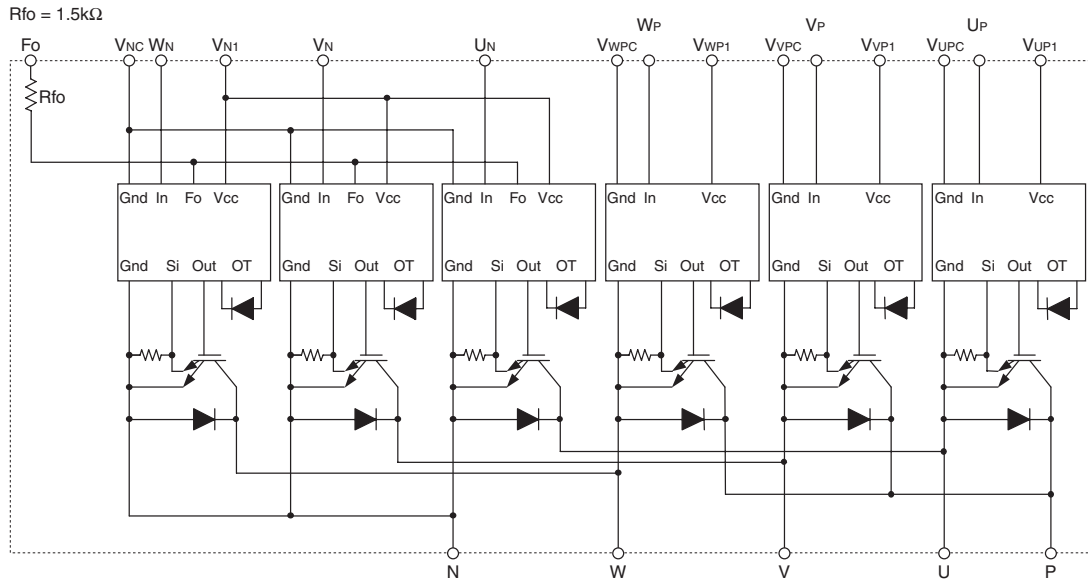
PACKAGE OUTLINES

Dimensions in mm



Terminal code

- | | |
|---------|---------|
| 1. VWPC | 11. VN1 |
| 2. WP | 12. WN |
| 3. VWP1 | 13. VN |
| 4. VVPC | 14. UN |
| 5. VP | 15. Fo |
| 6. VVP1 | |
| 7. VUPC | |
| 8. UP | |
| 9. VUP1 | |
| 10. VNC | |

PM75CS1D120**FLAT-BASE TYPE
INSULATED PACKAGE****INTERNAL FUNCTIONS BLOCK DIAGRAM****MAXIMUM RATINGS** ($T_j = 25^\circ\text{C}$, unless otherwise noted)**INVERTER PART**

Symbol	Parameter	Condition	Ratings	Unit
V_{CES}	Collector-Emitter Voltage	$V_D = 15\text{V}$, $V_{CIN} = 15\text{V}$	1200	V
$\pm I_C$	Collector Current	$T_c = 25^\circ\text{C}$ (Note-1)	75	A
$\pm I_{CP}$	Collector Current (Peak)	$T_c = 25^\circ\text{C}$	150	A
P_C	Collector Dissipation	$T_c = 25^\circ\text{C}$ (Note-1)	625	W
T_j	Junction Temperature		$-20 \sim +150$	$^\circ\text{C}$

*: T_c measurement point is just under the chip.**CONTROL PART**

Symbol	Parameter	Condition	Ratings	Unit
V_D	Supply Voltage	Applied between : $V_{UP1}-V_{UVC}$, $V_{VP1}-V_{VPC}$ $V_{WP1}-V_{WPC}$, $V_{N1}-V_{NC}$	20	V
V_{CIN}	Input Voltage	Applied between : U_P-V_{UVC} , V_P-V_{VPC} , W_P-V_{WPC} $U_N \cdot V_N \cdot W_N-V_{NC}$	20	V
V_{FO}	Fault Output Supply Voltage	Applied between : $FO-V_{NC}$	20	V
I_{FO}	Fault Output Current	Sink current at Fo terminals	20	mA

PM75CS1D120

FLAT-BASE TYPE
INSULATED PACKAGE

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
V _{CC(prot)}	Supply Voltage Protected by SC	V _D = 13.5 ~ 16.5V Inverter Part, T _j = +125°C Start	800	V
V _{CC(surge)}	Supply Voltage (Surge)	Applied between : P-N, Surge value	1000	V
T _{stg}	Storage Temperature		-40 ~ +125	°C
V _{iso}	Isolation Voltage	60Hz, Sinusoidal, Charged part to Base, AC 1 min.	2500	V _{rms}

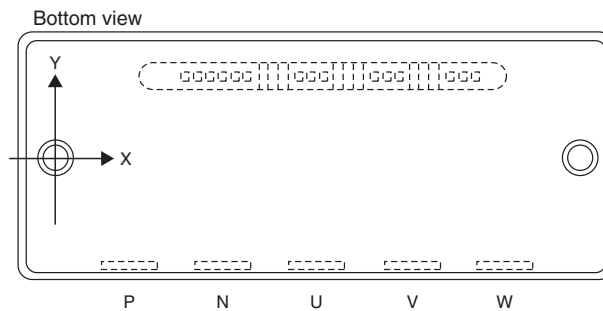
THERMAL RESISTANCES

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
R _{th(j-c)Q}	Junction to case Thermal Resistances	Inverter IGBT part (per 1 element) (Note-1)	—	—	0.20	°C/W
R _{th(j-c)F}		Inverter FWDi part (per 1 element) (Note-1)	—	—	0.32	
R _{th(c-f)}	Contact Thermal Resistance	Case to fin, (per 1 module) Thermal grease applied (Note-1)	—	—	0.046	

(Note-1) T_c (under the chip) measurement point is below.

(unit : mm)

axis	UP		VP		WP		UN		VN		WN	
	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi
X	21.8	21.8	65.0	65.0	90.0	90.0	36.0	36.0	51.0	51.0	76.0	76.0
Y	4.6	-5.0	4.6	-5.0	4.6	-5.0	-0.2	-10.0	-0.2	-10.0	-0.2	-10.0



ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
V _{CE(sat)}	Collector-Emitter Saturation Voltage	V _D = 15V, I _C = 75A V _{CIN} = 0V, Pulsed (Fig. 1)	T _j = 25°C T _j = 125°C	—	1.65 1.85	2.15 2.35	V
V _{EC}	FWDi Forward Voltage	-I _C = 75A, V _D = 15V, V _{CIN} = 15V (Fig. 2)		—	2.50	3.50	V
t _{on}	Switching Time	V _D = 15V, V _{CIN} = 0V↔15V V _{CC} = 600V, I _C = 75A T _j = 125°C Inductive Load (Fig. 3,4)		0.3	0.65	2.0	μs
t _{rr}				—	0.20	0.8	
t _{c(on)}				—	0.35	1.0	
t _{off}				—	1.10	2.8	
t _{c(off)}				—	0.35	1.2	
I _{CES}	Collector-Emitter Cutoff Current	V _{CE} = V _{CES} , V _D = 15V (Fig. 5)	T _j = 25°C T _j = 125°C	—	—	1 10	mA

PM75CS1D120

FLAT-BASE TYPE
INSULATED PACKAGE

CONTROL PART

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
Id	Circuit Current	V _D = 15V, V _{CIN} = 15V	—	6	12	mA
V _{th(ON)}	Input ON Threshold Voltage	Applied between : UP-VU _{PC} , VP-VV _{PC} , WP-VW _{PC} UN • VN • WN-V _{NC}	1.2	1.5	1.8	V
V _{th(OFF)}	Input OFF Threshold Voltage		1.7	2.0	2.3	
SC	Short Circuit Trip Level	−20 ≤ T _j ≤ 125°C, V _D = 15V (Fig. 3,6)	112	—	—	A
t _{off(SC)}	Short Circuit Current Delay Time	V _D = 15V (Fig. 3,6)	—	1.0	—	μs
OT	Over Temperature Protection	Detect Temperature of IGBT chip	135	—	—	°C
UV	Supply Circuit Under-Voltage Protection	−20 ≤ T _j ≤ 125°C	11.5	12.0	12.5	V
I _{FO(H)}	Fault Output Current	V _D = 15V, V _{CIN} = 15V (Note-2)	—	—	0.01	mA
I _{FO(L)}			—	10	15	
t _{FO}	Minimum Fault Output Pulse Width	V _D = 15V (Note-2)	1.0	1.8	—	ms

(Note-2) Fault output is given only when the internal SC, OT & UV protection.
 Fault output of SC, OT & UV protection operate by lower arms.
 Fault output of SC protection given pulse.
 Fault output of OT, UV protection given pulse while over trip level.

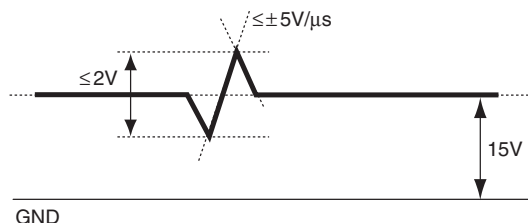
MECHANICAL RATINGS AND CHARACTERISTICS

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
—	Mounting torque	Mounting part screw : M5	2.5	3.0	3.5	N • m
		Main terminal part screw : M4	1.5	1.7	2.0	
—	Weight	—	—	400	—	g

RECOMMENDED CONDITIONS FOR USE

Symbol	Parameter	Condition	Recommended value	Unit
V _{CC}	Supply Voltage	Applied across P-N terminals	≤ 800	V
V _D	Control Supply Voltage	Applied between : VUP1-VU _{PC} , VVP1-VV _{PC} VWP1-VW _{PC} , VN1-V _{NC} (Note-3)	15.0 ± 1.5	V
V _{CIN(ON)}	Input ON Voltage	Applied between : UP-VU _{PC} , VP-VV _{PC} , WP-VW _{PC} UN • VN • WN-V _{NC}	≤ 0.8	V
V _{CIN(OFF)}	Input OFF Voltage		≥ 9.0	
f _{PWM}	PWM Input Frequency	Using Application Circuit of Fig. 8	≤ 20	kHz
t _{dead}	Arm Shoot-through Blocking Time	For IPM's each input signals (Fig. 7)	≥ 2.5	μs

(Note-3) With ripple satisfying the following conditions: dv/dt swing ≤ ±5V/μs, Variation ≤ 2V peak to peak

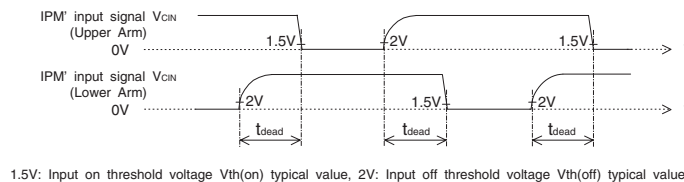
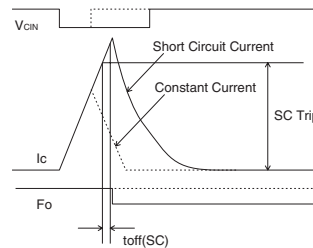
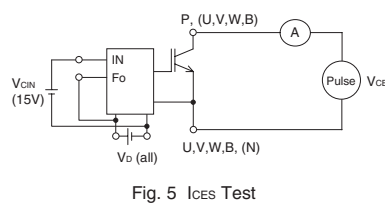
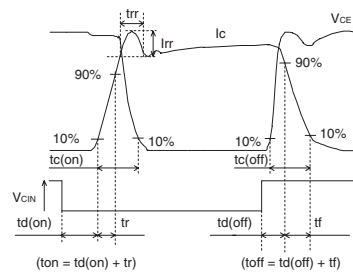
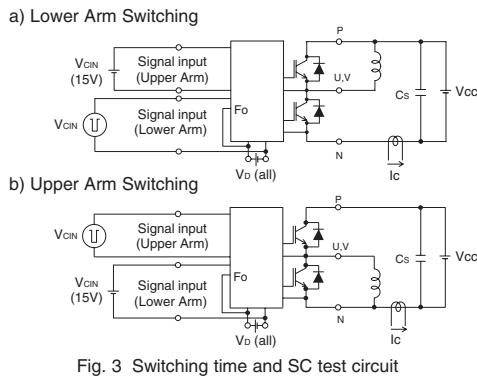
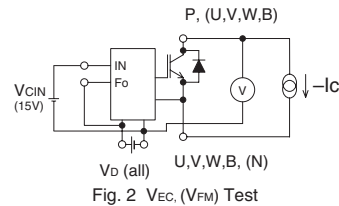
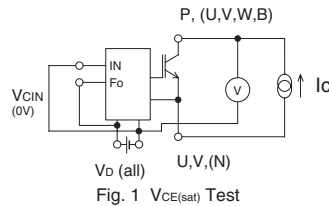


PM75CS1D120

FLAT-BASE TYPE
INSULATED PACKAGE

PRECAUTIONS FOR TESTING

- Before applying any control supply voltage (V_D), the input terminals should be pulled up by resistors, etc. to their corresponding supply voltage and each input signal should be kept off state.
After this, the specified ON and OFF level setting for each input signal should be done.
- When performing "SC" tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above V_{CES} rating of the device.
(These test should not be done by using a curve tracer or its equivalent.)





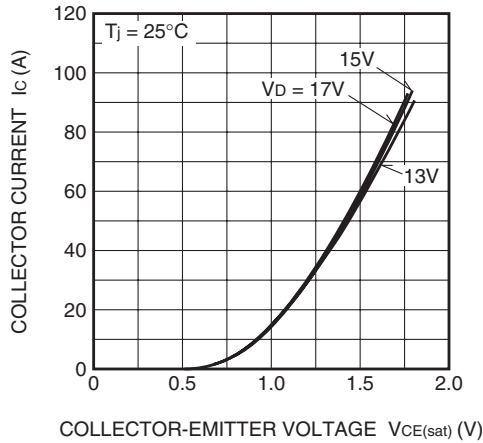
- Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.
- Connect low impedance capacitor between the Vcc and GND terminal of each fast switching opto-coupler.
- Fast switching opto-couplers: $t_{PLH}, t_{PHL} \leq 0.8\mu s$, Use High CMR type.
- Slow switching opto-coupler: CTR > 100%
- Use 3 isolated control power supplies (VD). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.
- Use line noise filter capacitor (ex. 4.7nF) between each input AC line and ground to reject common-mode noise from AC line and improve noise immunity of the system.

PM75CS1D120

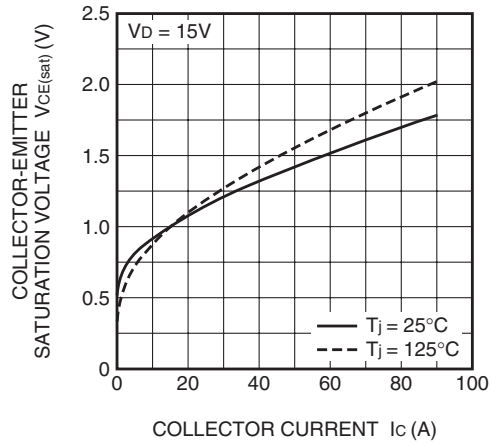
FLAT-BASE TYPE
INSULATED PACKAGE

PERFORMANCE CURVES

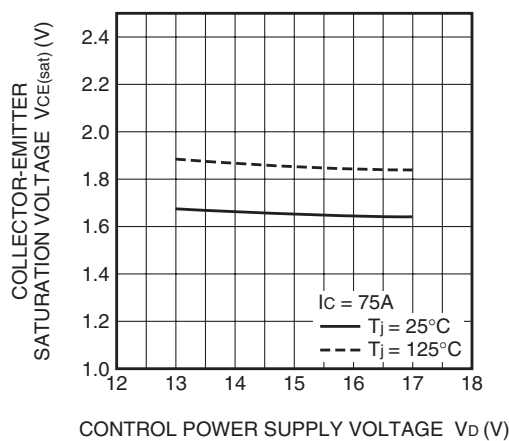
**OUTPUT CHARACTERISTICS
(TYPICAL)**



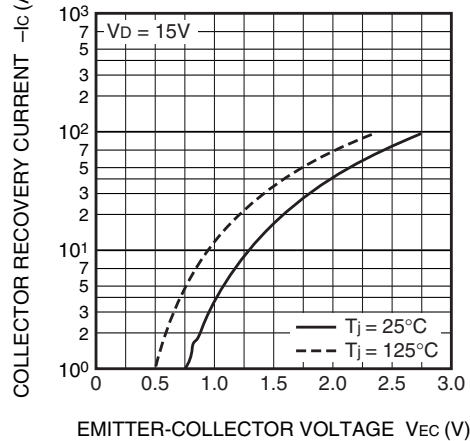
**COLLECTOR-EMITTER SATURATION
VOLTAGE (VS. I_c) CHARACTERISTICS
(TYPICAL)**



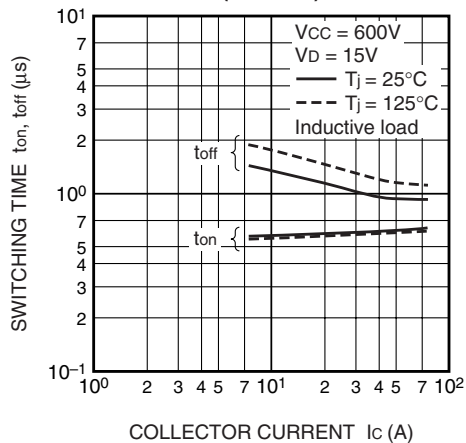
**COLLECTOR-EMITTER SATURATION
VOLTAGE (VS. V_D) CHARACTERISTICS
(TYPICAL)**



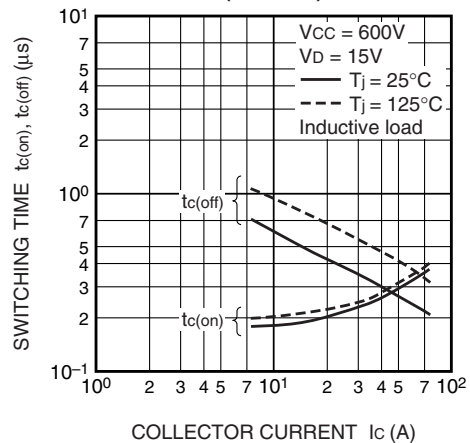
**DIODE FORWARD CHARACTERISTICS
(TYPICAL)**



**SWITCHING TIME (t_{on} , t_{off}) CHARACTERISTICS
(TYPICAL)**



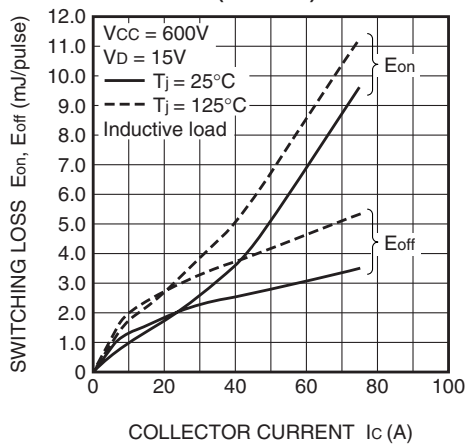
**SWITCHING TIME ($t_{c(on)}$, $t_{c(off)}$) CHARACTERISTICS
(TYPICAL)**



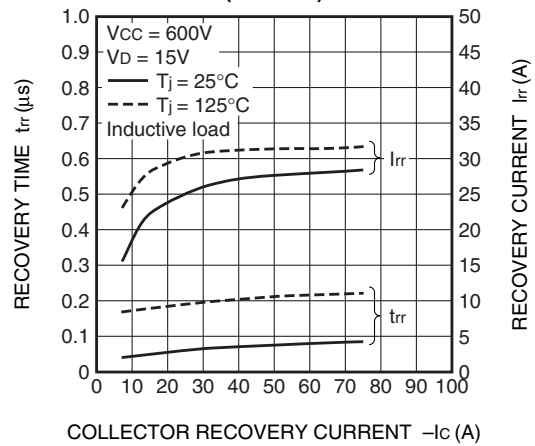
PM75CS1D120

FLAT-BASE TYPE
INSULATED PACKAGE

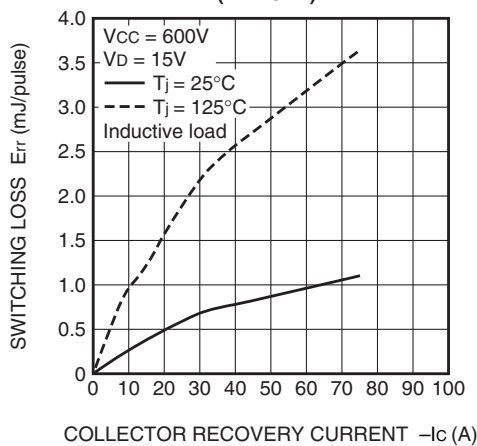
SWITCHING LOSS CHARACTERISTICS
(TYPICAL)



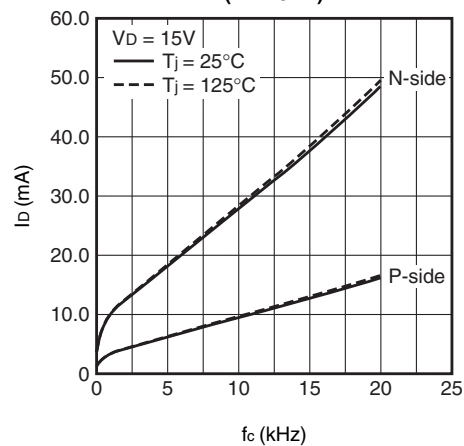
DIODE REVERSE RECOVERY CHARACTERISTICS
(TYPICAL)



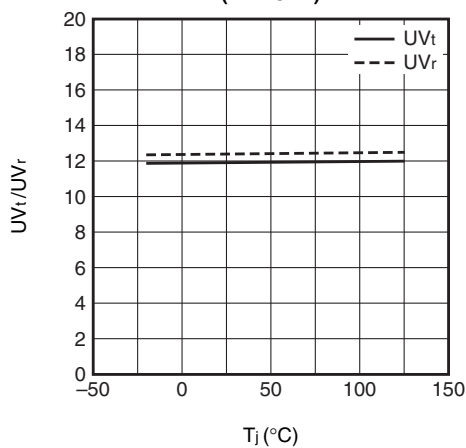
SWITCHING RECOVERY LOSS CHARACTERISTICS
(TYPICAL)



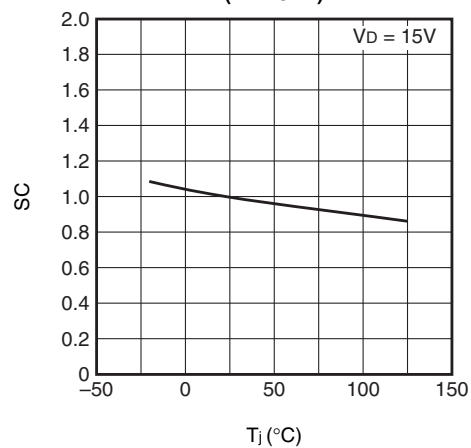
I_D VS. f_c CHARACTERISTICS
(TYPICAL)



UV TRIP LEVEL VS. T_j CHARACTERISTICS
(TYPICAL)



SC TRIP LEVEL VS. T_j CHARACTERISTICS
(TYPICAL)



PM75CS1D120

FLAT-BASE TYPE
INSULATED PACKAGE

