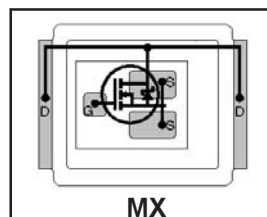


HEXFET® Power MOSFET plus Schottky Diode ②

Typical values (unless otherwise specified)

- RoHS Compliant Containing No Lead and Halogen Free ①
- Integrated Monolithic Schottky Diode
- Low Profile (<0.7 mm)
- Dual Sided Cooling Compatible ①
- Ultra Low Package Inductance
- Optimized for High Frequency Switching ①
- Ideal for CPU Core DC-DC Converters
- Optimized for Sync. FET socket of Sync. Buck Converter①
- Low Conduction and Switching Losses
- Compatible with existing Surface Mount Techniques ①
- 100% Rg tested

V_{DSS}		V_{GS}		$R_{DS(on)}$		$R_{DS(on)}$	
25V max		±20V max		1.4mΩ@ 10V		2.4mΩ@ 4.5V	
Q_g tot	Q_{gd}	Q_{gs2}	Q_{rr}	Q_{oss}	$V_{gs(th)}$		
35nC	10nC	4.8nC	34nC	27nC	1.8V		



Applicable DirectFET Outline and Substrate Outline (see p.7,8 for details)①

SQ	SX	ST		MQ	MX	MT	MP			
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Description

The IRF6795MPbF combines the latest HEXFET® Power MOSFET Silicon technology with the advanced DirectFET™ packaging to achieve the lowest on-state resistance in a package that has the footprint of a SO-8 and only 0.7 mm profile. The DirectFET package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques. Application note AN-1035 is followed regarding the manufacturing methods and processes. The DirectFET package allows dual sided cooling to maximize thermal transfer in power systems, improving previous best thermal resistance by 80%.

The IRF6795MPbF balances industry leading on-state resistance while minimizing gate charge along with ultra low package inductance to reduce both conduction and switching losses. This part contains an integrated Schottky diode to reduce the Q_{rr} of the body drain diode further reducing the losses in a Synchronous Buck circuit. The reduced losses make this product ideal for high frequency/high efficiency DC-DC converters that power high current loads such as the latest generation of microprocessors. The IRF6795MPbF has been optimized for parameters that are critical in synchronous buck converter's Sync FET sockets.

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	25	V
V_{GS}	Gate-to-Source Voltage	±20	
$I_D @ T_A = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ ③	32	A
$I_D @ T_A = 70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ ③	25	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ ④	160	
I_{DM}	Pulsed Drain Current ⑤	250	
E_{AS}	Single Pulse Avalanche Energy ⑥	190	mJ
I_{AR}	Avalanche Current ⑤	25	A

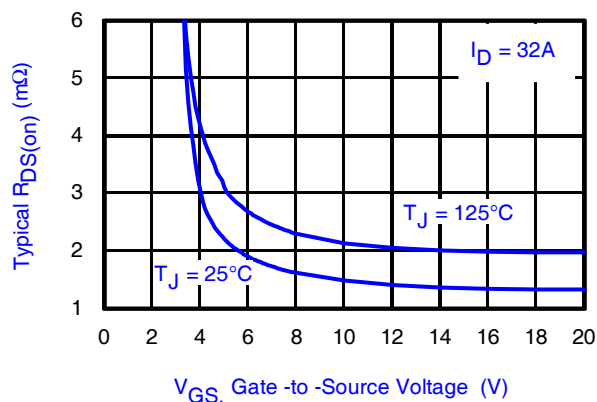


Fig 1. Typical On-Resistance vs. Gate Voltage

Notes:

- ① Click on this section to link to the appropriate technical paper.
- ② Click on this section to link to the DirectFET Website.
- ③ Surface mounted on 1 in. square Cu board, steady state.

www.irf.com

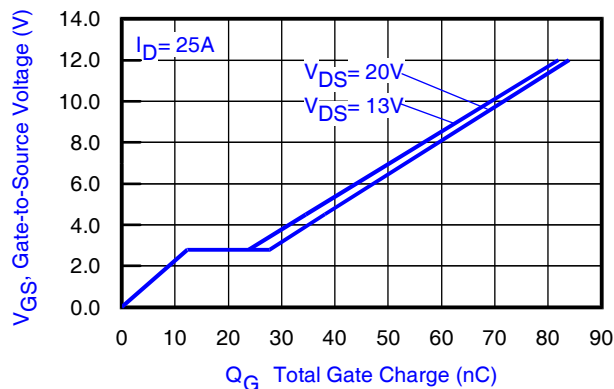


Fig 2. Typical Total Gate Charge vs. Gate-to-Source Voltage

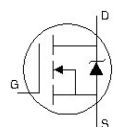
- ④ T_C measured with thermocouple mounted to top (Drain) of part.
- ⑤ Repetitive rating; pulse width limited by max. junction temperature.
- ⑥ Starting $T_J = 25^\circ\text{C}$, $L = 0.60\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 25\text{A}$.

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	25	—	—	V	$V_{GS} = 0V, I_D = 1.0mA$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	11	—	mV/ $^\circ\text{C}$	Reference to 25°C , $I_D = 5mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.4	1.8	m Ω	$V_{GS} = 10V, I_D = 32A$ ②
		—	2.4	3.2		$V_{GS} = 4.5V, I_D = 25A$ ②
$V_{GS(th)}$	Gate Threshold Voltage	1.35	1.8	2.35	V	$V_{DS} = V_{GS}, I_D = 100\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-4.2	—	mV/ $^\circ\text{C}$	$V_{DS} = V_{GS}, I_D = 10mA$
I_{DSS}	Drain-to-Source Leakage Current	—	—	500	μA	$V_{DS} = 20V, V_{GS} = 0V$
		—	—	5.0	mA	$V_{DS} = 20V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS} = -20V$
g_{fs}	Forward Transconductance	100	—	—	S	$V_{DS} = 13V, I_D = 25A$
Q_g	Total Gate Charge	—	35	53	nC	$V_{DS} = 13V$ $V_{GS} = 4.5V$ $I_D = 25A$ See Fig. 15
Q_{gs1}	Pre-V _{th} Gate-to-Source Charge	—	8.8	—		
Q_{gs2}	Post-V _{th} Gate-to-Source Charge	—	4.8	—		
Q_{gd}	Gate-to-Drain Charge	—	10	—		
Q_{godr}	Gate Charge Overdrive	—	11	—		
Q_{sw}	Switch Charge ($Q_{gs2} + Q_{gd}$)	—	14.8	—		
Q_{oss}	Output Charge	—	27	—	nC	$V_{DS} = 16V, V_{GS} = 0V$
R_G	Gate Resistance	—	1.3	2.2	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	16	—	ns	$V_{DD} = 13V, V_{GS} = 4.5V$ ② $I_D = 25A$ $R_G = 1.8\Omega$ See Fig. 17
t_r	Rise Time	—	27	—		
$t_{d(off)}$	Turn-Off Delay Time	—	16	—		
t_f	Fall Time	—	11	—		
C_{iss}	Input Capacitance	—	4280	—	pF	$V_{GS} = 0V$ $V_{DS} = 13V$ $f = 1.0MHz$
C_{oss}	Output Capacitance	—	1280	—		
C_{rss}	Reverse Transfer Capacitance	—	550	—		

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	32	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ⑤	—	—	250		
V_{SD}	Diode Forward Voltage	—	—	0.75	V	$T_J = 25^\circ\text{C}, I_S = 25A, V_{GS} = 0V$ ②
t_{rr}	Reverse Recovery Time	—	27	41	ns	$T_J = 25^\circ\text{C}, I_F = 25A$
Q_{rr}	Reverse Recovery Charge	—	34	51	nC	$di/dt = 200A/\mu s$ ②



Notes:

② Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.

Absolute Maximum Ratings

	Parameter	Max.	Units
P _D @ T _A = 25°C	Power Dissipation ③	2.8	W
P _D @ T _A = 70°C	Power Dissipation ③	1.8	
P _D @ T _C = 25°C	Power Dissipation ④	75	
T _P	Peak Soldering Temperature	270	°C
T _J	Operating Junction and	-40 to + 150	
T _{STG}	Storage Temperature Range		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③⑩	—	45	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient ⑧⑩	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ⑨⑩	20	—	
$R_{\theta JC}$	Junction-to-Case ④⑩	—	1.66	
$R_{\theta J-PCB}$	Junction-to-PCB Mounted	1.0	—	
	Linear Derating Factor ③	0.022		$\text{W}/^\circ\text{C}$

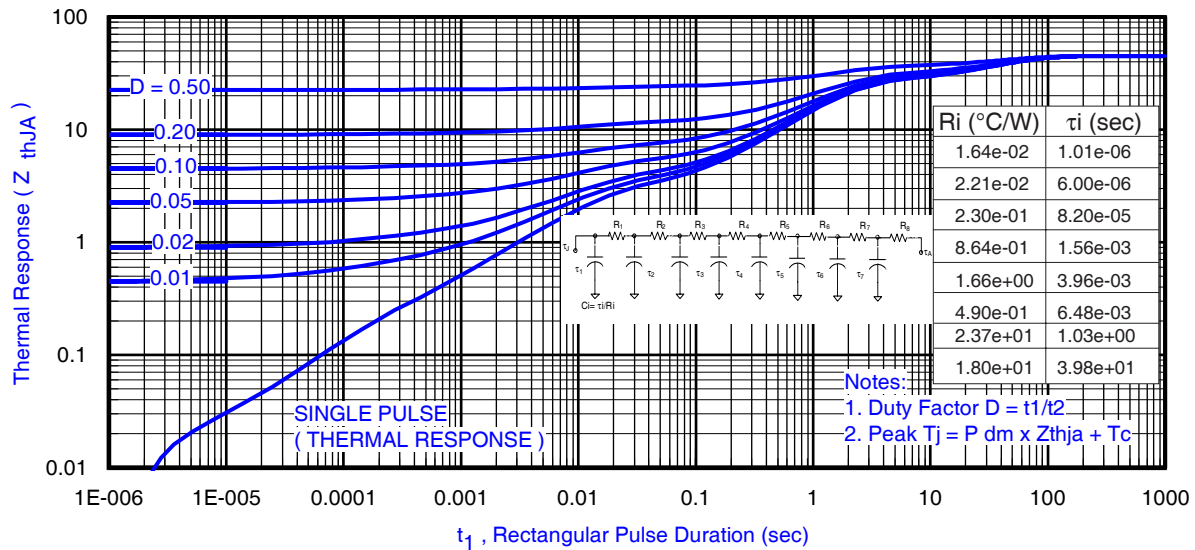
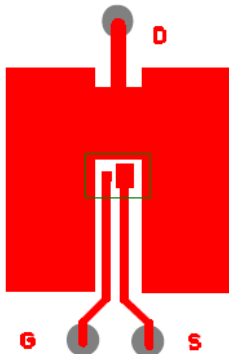


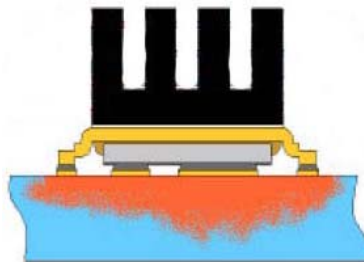
Fig 3. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient ③
(At lower pulse widths Z_{thJA} & Z_{thJC} are combined)

Notes:

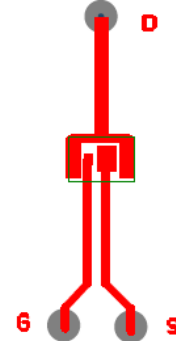
- ③ Used double sided cooling, mounting pad with large heatsink.
- ④ R_{θ} is measured at T_J of approximately 90°C .
- ⑧ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.



③ Surface mounted on 1 in. square Cu (still air).



⑧ Mounted to a PCB with small clip heatsink (still air)



⑨ Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)

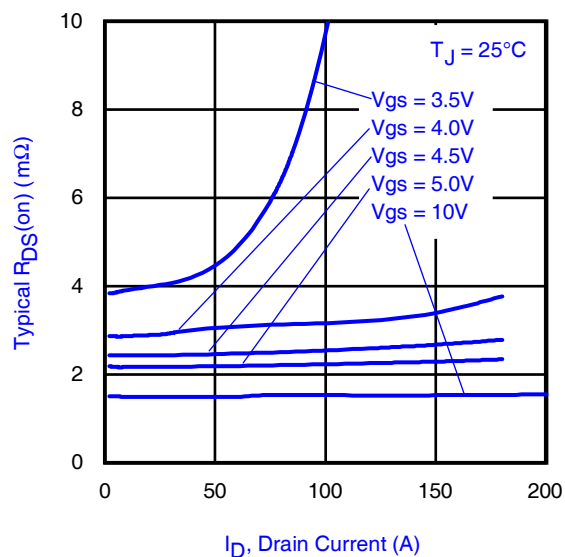
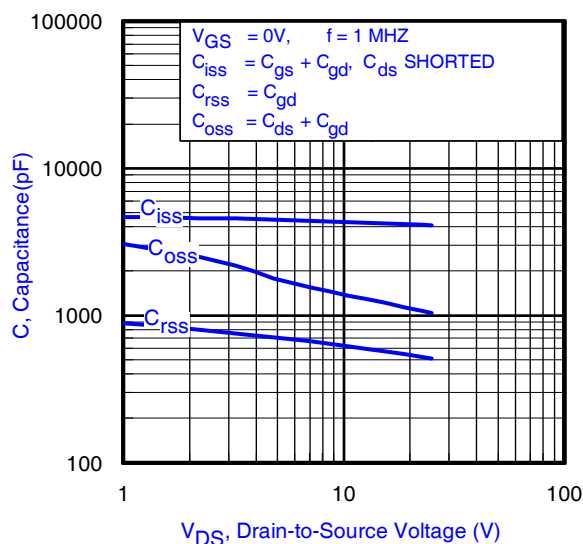
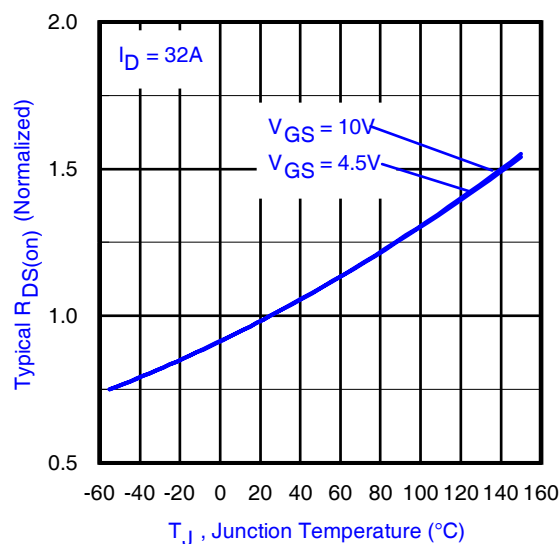
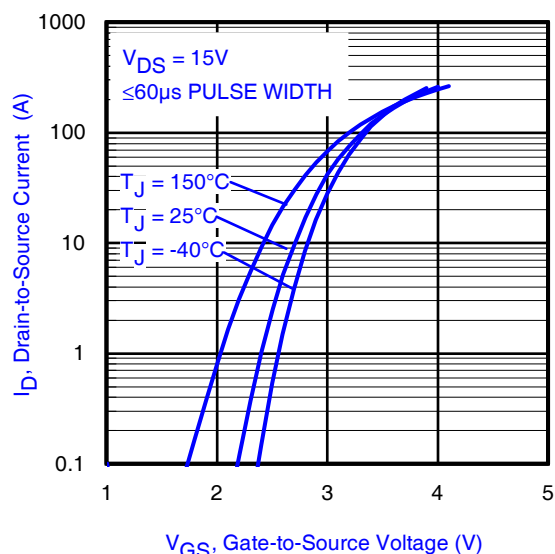
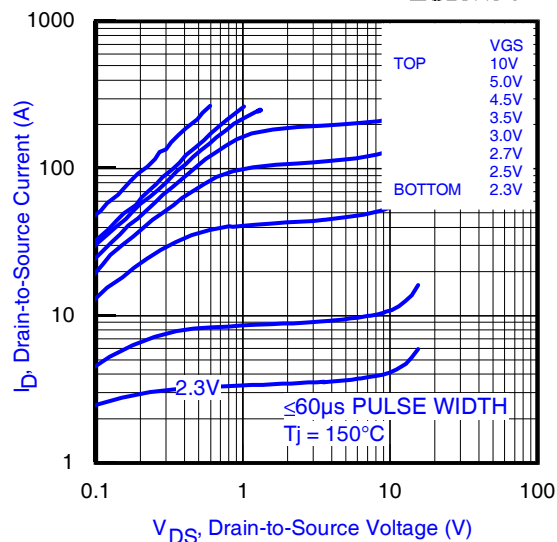
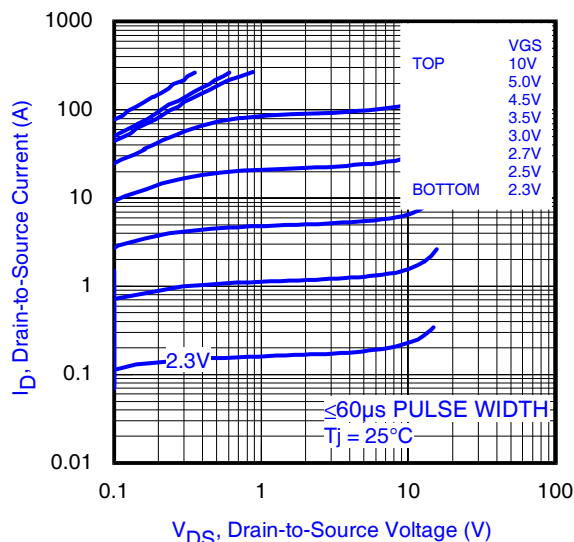


Fig 8. Typical Capacitance vs. Drain-to-Source Voltage

Fig 9. Typical On-Resistance vs. Drain Current and Gate Voltage

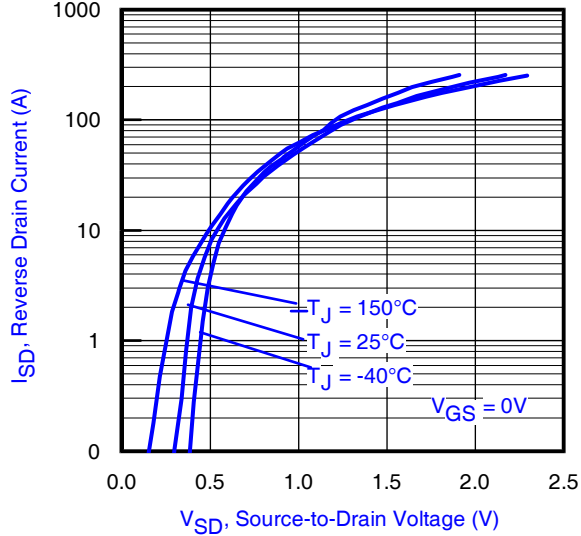


Fig 10. Typical Source-Drain Diode Forward Voltage

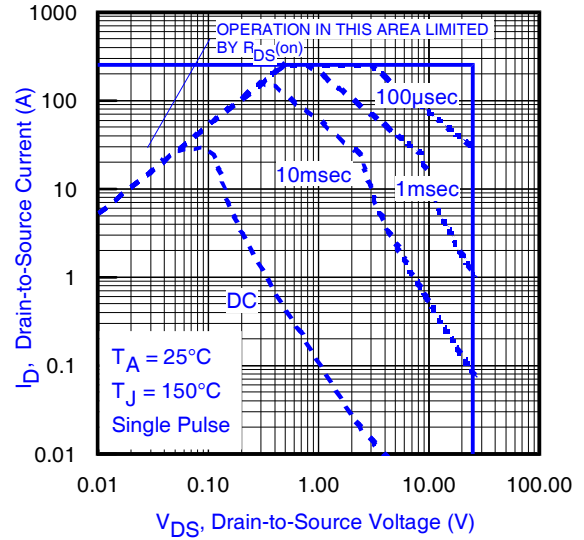


Fig 11. Maximum Safe Operating Area

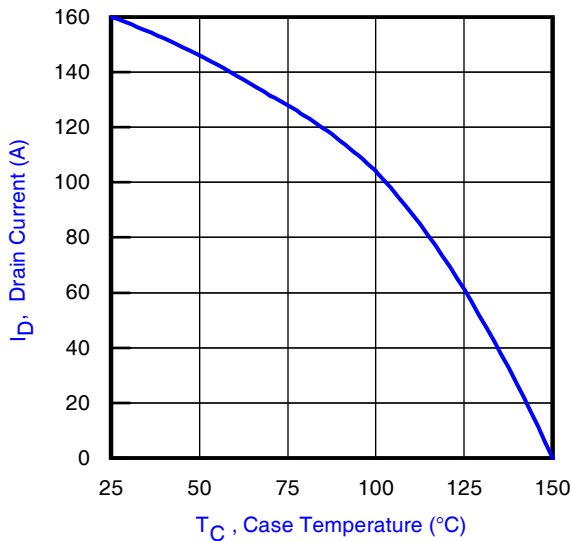


Fig 12. Maximum Drain Current vs. Case Temperature

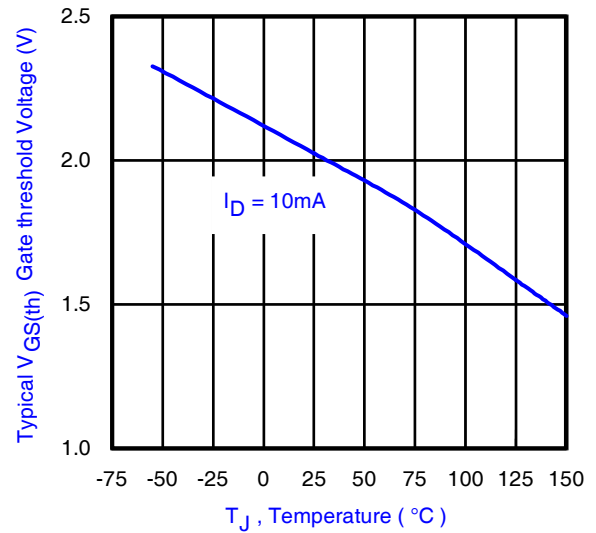


Fig 13. Typical Threshold Voltage vs. Junction Temperature

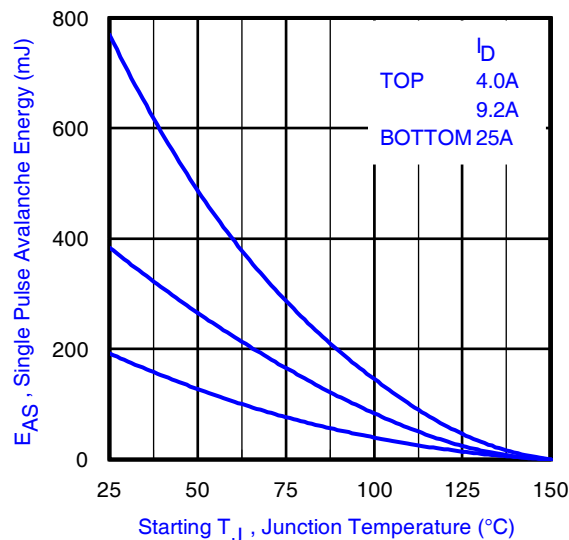


Fig 14. Maximum Avalanche Energy vs. Drain Current

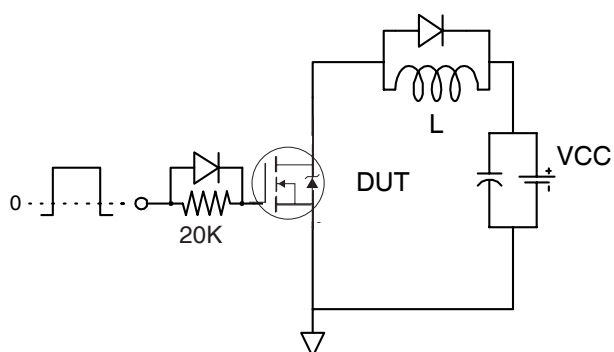


Fig 15a. Gate Charge Test Circuit

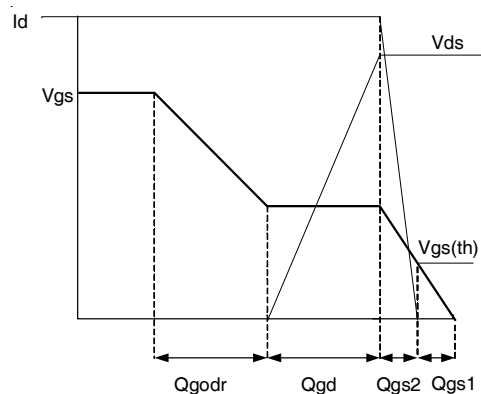


Fig 15b. Gate Charge Waveform

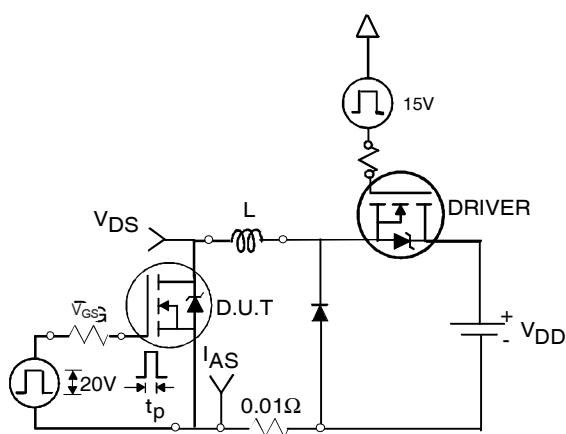


Fig 16a. Unclamped Inductive Test Circuit

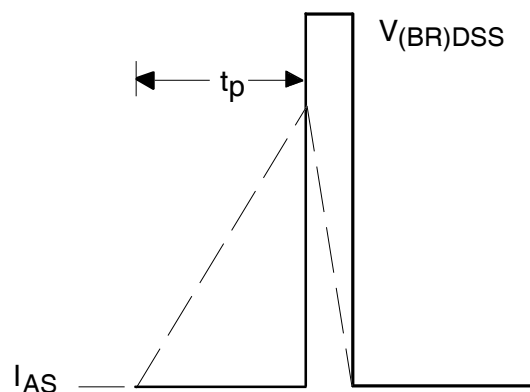


Fig 16b. Unclamped Inductive Waveforms

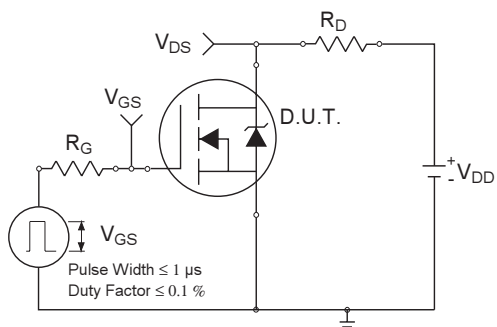


Fig 17a. Switching Time Test Circuit

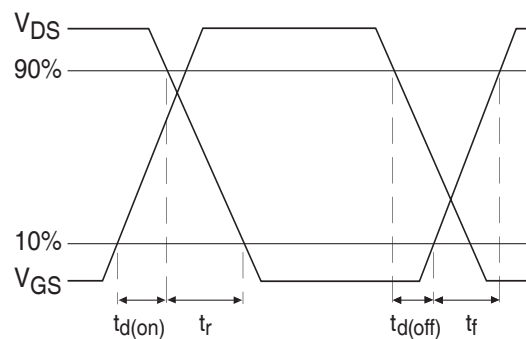


Fig 17b. Switching Time Waveforms

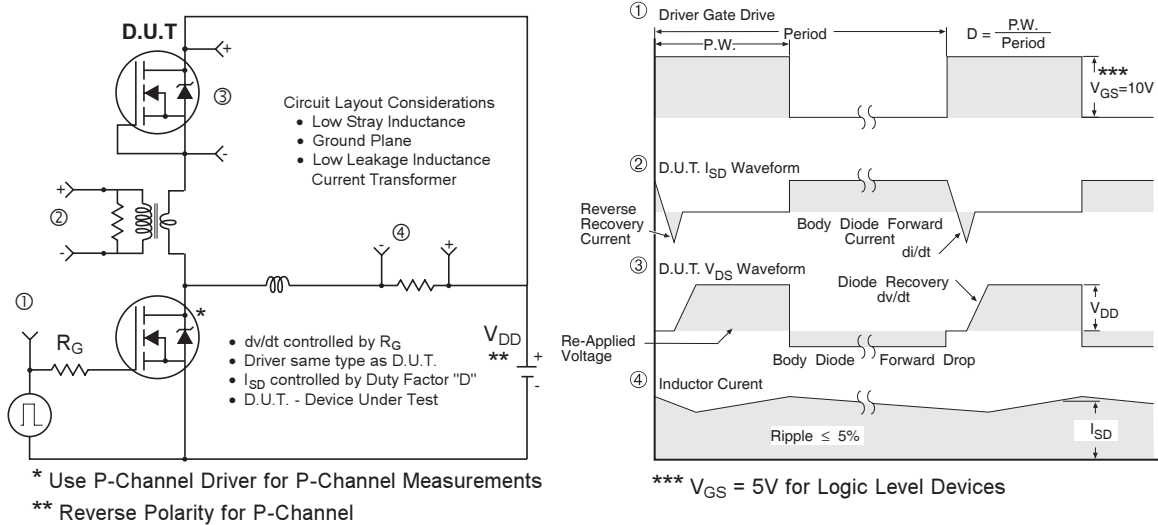
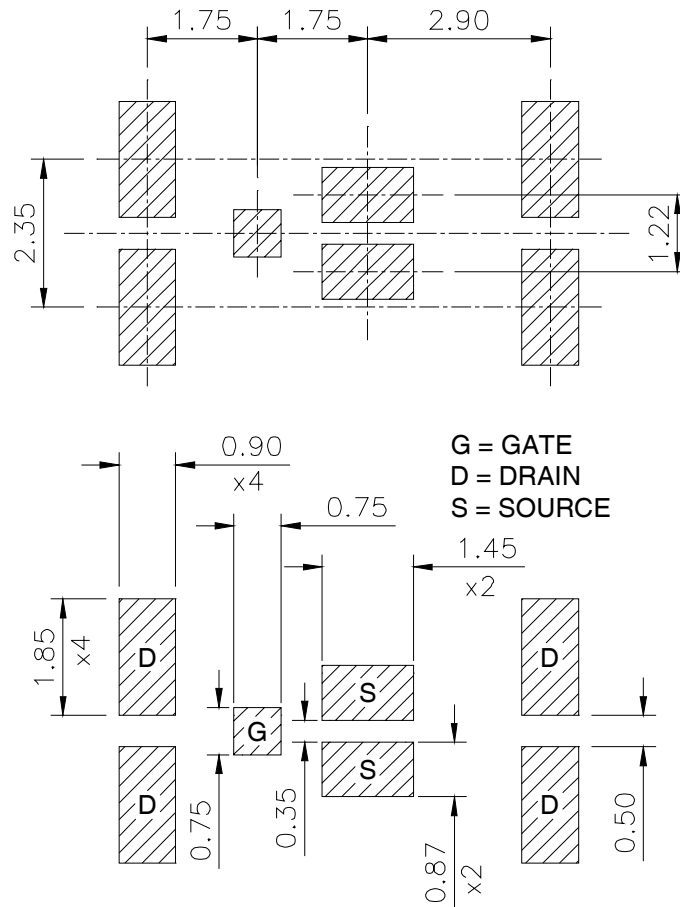


Fig 18. Diode Reverse Recovery Test Circuit for HEXFET® Power MOSFETs

DirectFET™ Board Footprint, MX Outline (Medium Size Can, X-Designation).

Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET.

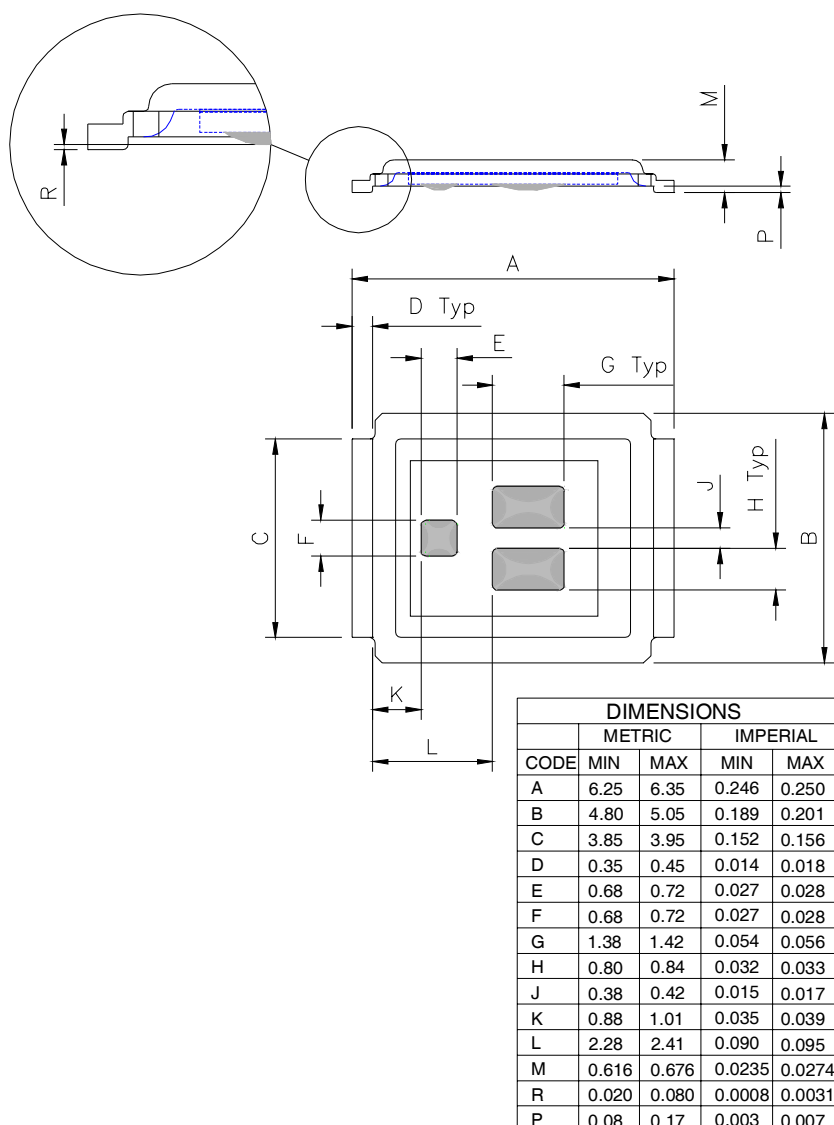
This includes all recommendations for stencil and substrate designs.



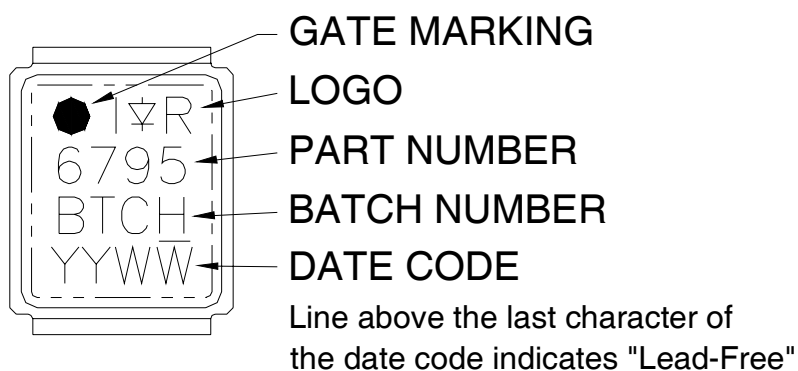
IRF6795MTRPbF

DirectFET™ Outline Dimension, MX Outline (Medium Size Can, X-Designation).

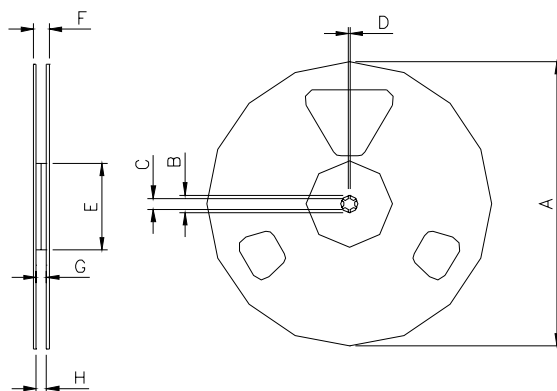
Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET. This includes all recommendations for stencil and substrate designs.



DirectFET™ Part Marking



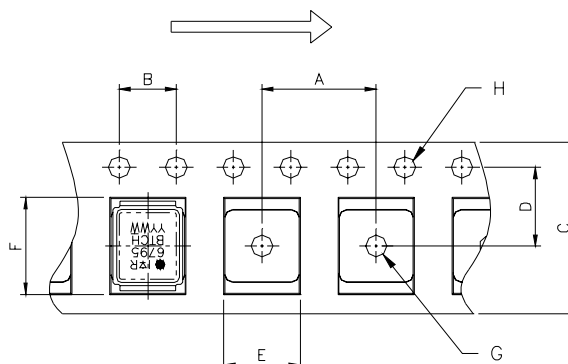
DirectFET™ Tape & Reel Dimension (Showing component orientation).



NOTE: Controlling dimensions in mm
Std reel quantity is 4800 parts. (ordered as IRF6795MTRPbF). For 1000 parts on 7" reel, order IRF6795MTR1PbF

REEL DIMENSIONS								
STANDARD OPTION (QTY 4800)					TR1 OPTION (QTY 1000)			
	METRIC		IMPERIAL		METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	330.0	N.C	12.992	N.C	177.77	N.C	6.9	N.C
B	20.2	N.C	0.795	N.C	19.06	N.C	0.75	N.C
C	12.8	13.2	0.504	0.520	13.5	12.8	0.53	0.50
D	1.5	N.C	0.059	N.C	1.5	N.C	0.059	N.C
E	100.0	N.C	3.937	N.C	58.72	N.C	2.31	N.C
F	N.C	18.4	N.C	0.724	N.C	13.50	N.C	0.53
G	12.4	14.4	0.488	0.567	11.9	12.01	0.47	N.C
H	11.9	15.4	0.469	0.606	11.9	12.01	0.47	N.C

LOADED TAPE FEED DIRECTION



NOTE: CONTROLLING
DIMENSIONS IN MM

DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	5.10	5.30	0.201	0.209
F	6.50	6.70	0.256	0.264
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.