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# AK5367

## 96kHz 24-Bit ΔΣ ADC with 0V Bias Selector

## GENERAL DESCRIPTION

AK5367 is a high-performance 24-bit, 96kHz sampling ADC for consumer audio and digital recording applications. The AK5367 uses an Enhanced Dual-Bit modulator architecture, this analog-to-digital converter has an impressive dynamic range of 102dB with a high level of integration. The AK5367 has a 4-channel stereo input selector, an input Programmable Gain Amplifier with resistance. All this integration with high-performance makes the AK5367 well suited for CD and DVD recording systems. The integrated charge pump circuit can generate the negative power supply and remove the output coupling capacitor.

## FEATURES

**1. 24bit Stereo ADC**
- **4:1 0V Bias Stereo input Selector**
- **Digital HPF for offset cancellation (fc=1.0Hz@fs=48kHz)**
- **Decimation LPF: -0.2dB@ 20kHz, -3.0dB@23kHz (fs=48kHz)**
- **Soft Mute**
- **Single-end Inputs**
- **S/(N+D): 90dB**
- **DR, S/N: 102dB**
- **Audio I/F Format: 24bit MSB justified, $I^2S$**

**2. Control Interface: $I^2C$-Bus**

**3. Master Mode / Slave Mode**

**4. Master Clock:**
- **256fs/384fs (32kHz ~ 96kHz)**
- **512fs/768fs (32kHz ~ 48kHz)**

**5. Sampling Rate: 32kHz to 96kHz**

**6. Power Supply**
- **Analog Supply: 4.5 ~ 5.5V**
- **Digital Supply: 3.0 ~ 3.6V**

**7. Ta = –20 ~ 85°C**

**8. Package: 30pin VSOP**

## ■ Block Diagram

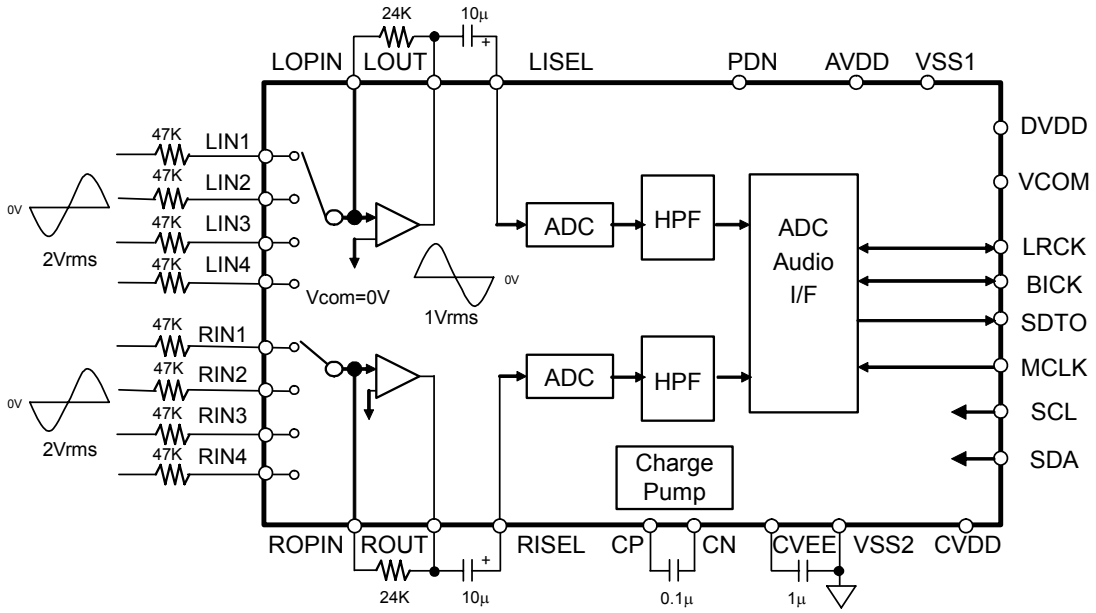
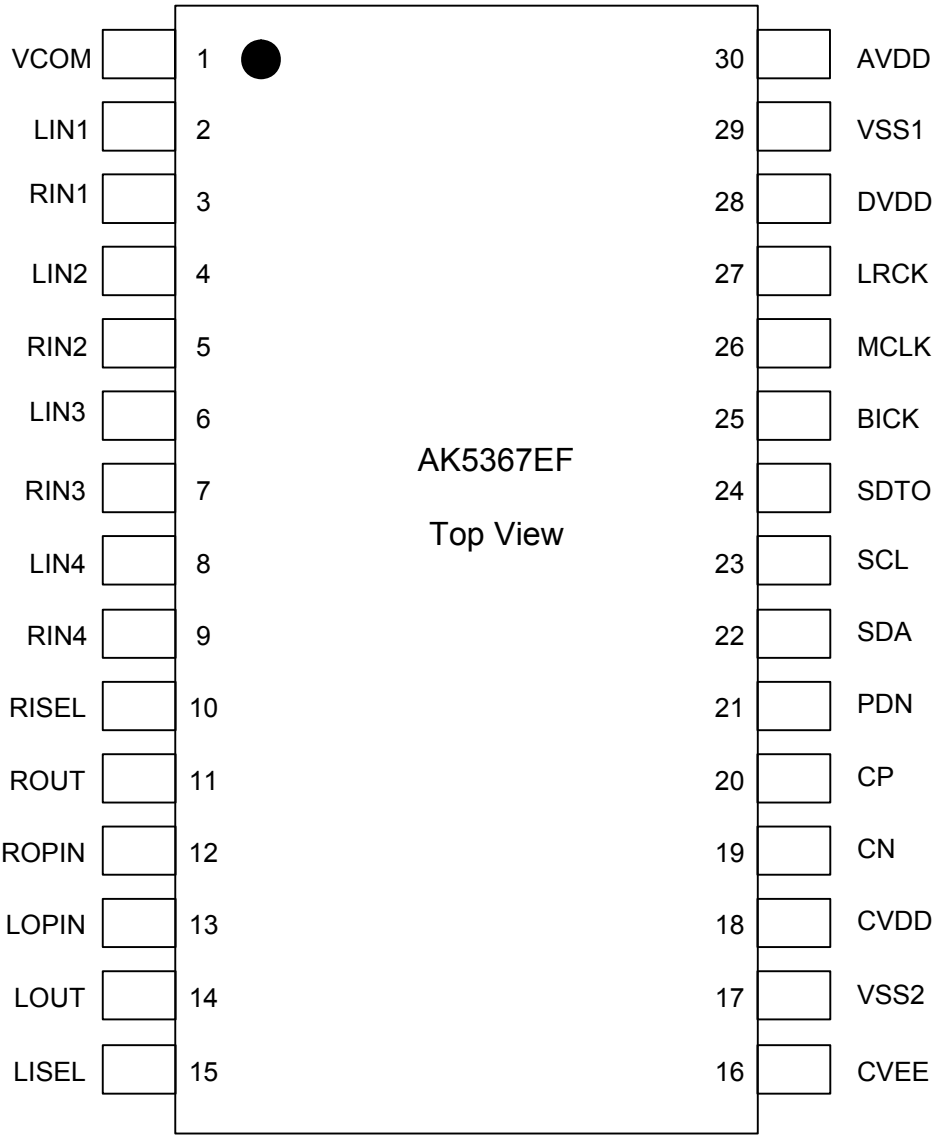



Figure 1. AK5367 Block Diagram

## ■ Ordering Guide

| | | |
|---|---|---|
| AK5367EF | –20 ~ +85°C | 30pin VSOP (0.65mm pitch) |
| AKD5367 | Evaluation Board for AK5367 | |

## ■ Pin Layout



## PIN/FUNCTION

| No. | Pin Name | I/O | Function |
|---|---|---|---|
| 1 | VCOM | O | Common Voltage Output Pin, AVDD/2<br>Bias voltage of ADC input. |
| 2 | LIN1 | I | Lch Analog Input 1 Pin |
| 3 | RIN1 | I | Rch Analog Input 1 Pin |
| 4 | LIN2 | I | Lch Analog Input 2 Pin |
| 5 | RIN2 | I | Rch Analog Input 2 Pin |
| 6 | LIN3 | I | Lch Analog Input 3 Pin |
| 7 | RIN3 | I | Rch Analog Input 3 Pin |
| 8 | LIN4 | I | Lch Analog Input 4 Pin |
| 9 | RIN4 | I | Rch Analog Input 4 Pin |
| 10 | RISEL | I | Rch Analog Input Pin |
| 11 | ROUT | O | Rch Feedback Resistor Output Pin |
| 12 | ROPIN | O | Rch Feedback Resistor Input Pin |
| 13 | LOPIN | O | Lch Feedback Resistor Intput Pin |
| 14 | LOUT | O | Lch Feedback Resistor Output Pin |
| 15 | LISEL | I | Lch Analog Input Pin |
| 16 | CVEE | O | Negative Voltage Output Pin<br>Connect to VSS2 with a 1.0μF capacitor that should have the low ESR (Equivalent Series Resistance) over all temperature range. When this capacitor has the polarity, the positive polarity pin should be connected to the VSS2 pin. Non polarity capacitors can also be used. |
| 17 | VSS2 | - | Charge Pump Ground Pin, 0V<br>Connect to CVEE with a 1.0μF capacitor that should have the low ESR (Equivalent Series Resistance) over all temperature range. When this capacitor has the polarity, the positive polarity pin should be connected to the VSS2 pin. Non polarity capacitors can also be used. |
| 18 | CVDD | - | Charge Pump Power Supply Pin, 3.0V~3.6V |
| 19 | CN | I | Negative Charge Pump Capacitor Terminal Pin<br>Connect to CP with a 0.1μF capacitor that should have the low ESR (Equivalent Series Resistance) over all temperature range. When this capacitor has the polarity, the positive polarity pin should be connected to the CP pin. Non polarity capacitors can also be used. |
| 20 | CP | O | Positive Charge Pump Capacitor Terminal Pin<br>Connect to CN with a 0.1μF capacitor that should have the low ESR (Equivalent Series Resistance) over all temperature range. When this capacitor has the polarity, the positive polarity pin should be connected to the CP pin. Non polarity capacitors can also be used. |
| 21 | PDN | I | Power Down Mode & Reset Pin<br>"H": Power up, "L": Power down & Reset<br>The AK5367 must be reset once upon power-up. |
| 22 | SDA | I/O | Control Data Input / Output Pin in $I^2C$ Control |
| 23 | SCL | I | Control Data Clock Pin in $I^2C$ Control |
| 24 | SDTO | O | Audio Serial Data Output Pin<br>"L" Output at Power-down mode. |
| 25 | BICK | I/O | Audio Serial Data Clock Pin<br>"L" Output in Master Mode at PWN bit= "0". |
| 26 | MCLK | I | Master Clock Input Pin |

| No. | Pin Name | I/O | Function |
|---|---|---|---|
| 27 | LRCK | I/O | Channel Clock Pin<br>"L" Output in Master Mode at PWN bit= "0". |
| 28 | DVDD | - | Digital Power Supply Pin, 3.0~ 3.6V |
| 29 | VSS1 | - | Analog Ground Pin |
| 30 | AVDD | - | Analog Power Supply Pin, 4.5 ~ 5.5V |

Note: All input pins except analog input pins (RISEL, LISEL, LIN1-4, RIN1-4) should not be left floating.

## ■ Handling of Unused Pin

The unused input pins should be processed appropriately as below.

| Classification | Pin Name | Setting |
|---|---|---|
| Analog | LIN1-4,RIN1-4,LISEL,RISEL<br>LOPIN,LOUT,ROPIN,ROUT | These pins should be open. |

## ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=0V; Note 1, Note 2)

| Parameter | | Symbol | min | max | Units |
|---|---|---|---|---|---|
| Power Supplies: | Analog | AVDD | –0.3 | 6.0 | V |
| | Digital | DVDD | –0.3 | 6.0 | V |
| | Charge Pump | CVDD | –0.3 | 4.0 | V |
| Input Current, Any Pin Except Supplies | | IIN | - | ±10 | mA |
| Analog Input Voltage(LISEL,RISEL,LIN1-4, RIN1-4 pins) | | VINA | –0.3 | AVDD+0.3 | V |
| Digital Input Voltage (Note 3) | | VIND | –0.3 | DVDD+0.3 | V |
| Ambient Temperature (Powered applied) | | Ta | –20 | 85 | °C |
| Storage Temperature | | Tstg | –65 | 150 | °C |

Note 1. All voltages with respect to ground.
Note 2. VSS1 and VSS2 must be connected to the same analog ground plane.
Note 3. PDN,SCL,SDA,MCLK,BICK,LRCK pins

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

## RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=0V;Note 1)

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| Power Supplies (Note 4) | Analog | AVDD | 4.5 | 5.0 | 5.5 | V |
| | Digital | DVDD | 3.0 | 3.3 | 3.6 | V |
| | Charge Pump | CVDD | 3.0 | 3.3 | 3.6 | V |
| | DVDD-CVDD | ΔVDD | -0.3 | 0 | +0.3 | V |

Note 4. The power up sequence between AVDD, DVDD and CVDD is not critical.
In slave mode, the AK5367 must be power up at the PDN pin = “L”.
In master mode, the AK5367 must be power up at the PDN pin = “L”, or when DVDD is powered up, MCLK clock must input and the AK5367 must be reset by the PDN pin=“L”. The internal register data is unknown until PDN pin=“L”. The power on/off sequence between AVDD, DVDD and CVDD is not critical, however when DVDD is powered off, all digital input pins must be left floating or held to VSS.
The power off is means that AVDD, CVDD and DVDD are floating or short to VSS.

WARNING: AKEMD assumes no responsibility for the usage beyond the conditions in this datasheet.

## ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=5.0V, DVDD=CVDD=3.3V; VSS1=VSS2=0V; fs=48kHz,96kHz; BICK=64fs;
Signal Frequency=1kHz; 24bit Data; Measurement frequency=20Hz ~ 20kHz at fs=48kHz, 40Hz ~ 40kHz at fs=96kHz;
unless otherwise specified)

| Parameter | | | min | typ | max | Units |
|---|---|---|---|---|---|---|
| **Pre-Amp Characteristics:** | | | | | | |
| Feedback Resistance | | | 10 | | 50 | kΩ |
| S/(N+D) | | (Note 5) | - | 100 | | dB |
| S/N (A-weighted) | | (Note 5) | - | 108 | | dB |
| Load Resistance $R_L$ | | (Note 6) | 15 | | | kΩ |
| Load Capacitance $C_L$ | | (Note 6) | | | 20 | pF |
| **ADC Analog Input Characteristics: (Note 7)** | | | | | | |
| Resolution | | | | | 24 | Bits |
| Input Voltage | | (Note 8) | 2.7 | 3.0 | 3.3 | Vpp |
| S/(N+D) | fs=48kHz BW=20kHz | –1dBFS | 82 | 90 | | dB |
| | | –60dBFS | - | 39 | | dB |
| | fs=96kHz BW=40kHz | –1dBFS | - | 90 | | dB |
| | | –60dBFS | - | 37 | | dB |
| DR (–60dBFS, A-weighted) | | | 94 | 102 | | dB |
| S/N (A-weighted) | | | 94 | 102 | | dB |
| Interchannel Isolation (fs=48kHz) | | (Note 9) | 85 | 96 | | dB |
| Interchannel Gain Mismatch | | | | 0.1 | 0.5 | dB |
| Gain Drift | | | | 100 | - | ppm/°C |
| Power Supply Rejection | | (Note 10) | - | 50 | | dB |
| **Power Supplies** | | | | | | |
| Power Supply Current | | | | | | |
| Normal Operation (PDN pin = "H") | | | | | | |
| AVDD | | | | 15.5 | 23 | mA |
| CVDD | | | | 2.5 | 4 | mA |
| DVDD | (fs=48kHz) | | | 2 | 3 | mA |
| DVDD | (fs=96kHz) | | | 4 | 6 | mA |
| Power down mode (PDN pin = "L") | | (Note 11) | | | | |
| AVDD+DVDD | | | | 10 | 100 | μA |

Note 5. This value is measured at LOUT and ROUT pins using Ri= 47kΩ, Rf= 24 kΩ when the input signal voltage is 2Vrms.

Note 6. This value of $R_L$ and $C_L$ are load resistance and capacitance that the LOUT and ROUT pins can drive. $R_L$ does not include the feedback resistor (Rf) and the input impedance of the LISEL/RISEL pins. The value of $C_L$ does not include the internal impedance of the AK5367.

Note 7. This value is measured via the following path. Pre-Amp → ADC.(Ri= 47kΩ, Rf= 24 kΩ)

Note 8. Input voltage to LISEL and RISEL pins is proportional to AVDD voltage. typ. Vin = 0.6 x AVDD (Vpp)

Note 9. 93dB(typ.) at fs=96kHz.

Note 10. PSR is applied to AVDD and DVDD with 1kHz, 50mVpp Sine wave.

Note 11. All digital input pins are held DVDD or VSS2.

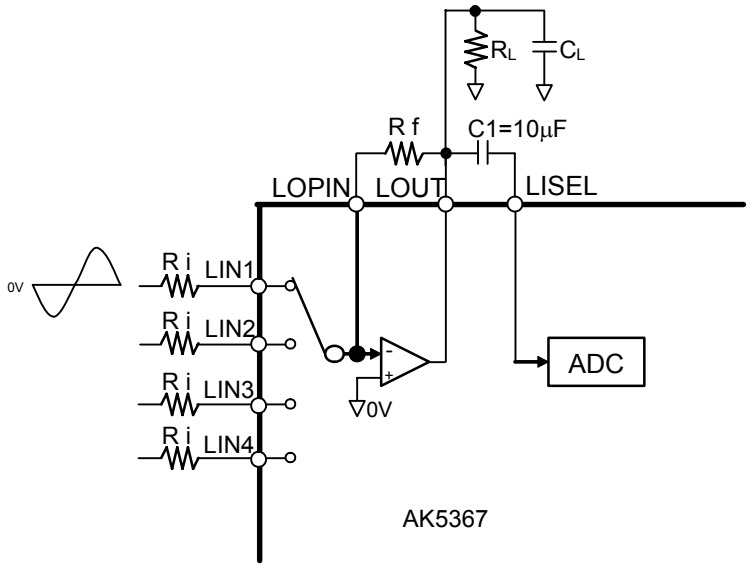



Figure 2. Pre-Amp Circuit

## FILTER CHARACTERISTICS (fs=48kHz)

(Ta=–20 ~ 85°C; AVDD=4.5 ~ 5.5V; DVDD=CVDD=3.0 ~ 3.6V)

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| **ADC Digital Filter (Decimation LPF):** | | | | | | |
| Passband (Note 12) | ±0.1dB | PB | 0 | | 18.9 | kHz |
| | –0.2dB | | - | 20.0 | - | kHz |
| | –3.0dB | | - | 23.0 | - | kHz |
| Stopband | | SB | 28 | | | kHz |
| Passband Ripple | | PR | | | ±0.04 | dB |
| Stopband Attenuation | | SA | 68 | | | dB |
| Group Delay Distortion | | ΔGD | | 0 | | μs |
| Group Delay (Note 13) | | GD | | 20 | | 1/fs |
| **ADC Digital Filter (HPF):** | | | | | | |
| Frequency Response (Note 12) | –3dB | FR | | 1.0 | | Hz |
| | –0.1dB | | | 6.5 | | Hz |

## FILTER CHARACTERISTICS (fs=96kHz)

(Ta=–20 ~ 85°C; AVDD=4.5 ~ 5.5V; DVDD=CVDD=3.0 ~ 3.6V)

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| **ADC Digital Filter (Decimation LPF):** | | | | | | |
| Passband (Note 12) | ±0.1dB | PB | 0 | | 37.8 | kHz |
| | –0.2dB | | - | 40.0 | - | kHz |
| | –3.0dB | | - | 46.0 | - | kHz |
| Stopband | | SB | 56 | | | kHz |
| Passband Ripple | | PR | | | ±0.04 | dB |
| Stopband Attenuation | | SA | 68 | | | dB |
| Group Delay Distortion | | ΔGD | | 0 | | μs |
| Group Delay (Note 13) | | GD | | 20 | | 1/fs |
| **ADC Digital Filter (HPF):** | | | | | | |
| Frequency Response (Note 12) | –3dB | FR | | 2.0 | | Hz |
| | –0.1dB | | | 13.0 | | Hz |

Note 12. The passband and stopband frequencies scale with fs. For example, PB= 18.9kHz@±0.1dB is 0.39375 x fs, (fs=48kHz).

Note 13. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the setting of 24bit data both channels to the ADC output register for ADC.

## DC CHARACTERISTICS

(Ta=-20°C ~ 85°C; AVDD=4.5 ~ 5.5V; DVDD=CVDD=3.0 ~ 3.6V)

| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| High-Level Input Voltage | VIH | 70%DVDD | - | - | V |
| Low-Level Input Voltage | VIL | - | - | 30%DVDD | V |
| High-Level Output Voltage (Iout=–1mA) | VOH | DVDD–0.5 | - | - | V |
| Low-Level Output Voltage | | | | | |
| (Except SDA pin: Iout=1mA) | VOL | - | - | 0.5 | V |
| (SDA pin: Iout=3mA) | VOL | - | - | 0.4 | V |
| Input Leakage Current | Iin | - | - | ±10 | μA |

## SWITCHING CHARACTERISTICS

(Ta=-20°C ~ 85°C; AVDD=4.5 ~ 5.5V; DVDD=CVDD=3.0 ~ 3.6V; $C_L$=20pF)

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| **Master Clock Timing** | | | | | | |
| 512fs, 256fs Frequency | | fCLK | 8.192 | | 24.576 | MHz |
| Pulse Width Low | | tCLKL | 16 | | | ns |
| Pulse Width High | | tCLKH | 16 | | | ns |
| 768fs, 384fs Frequency | | fCLK | 12.288 | | 36.864 | MHz |
| Pulse Width Low | | tCLKL | 10.5 | | | ns |
| Pulse Width High | | tCLKH | 10.5 | | | ns |
| **LRCK Frequency** | | fs | 32 | | 96 | kHz |
| Duty Cycle | Slave mode | | 45 | | 55 | % |
| | Master mode | | | 50 | | % |
| **Audio Interface Timing** | | | | | | |
| **Slave mode** | | | | | | |
| BICK Period | | tSCK | 160 | | | ns |
| BICK Pulse Width Low | | tSCKL | 65 | | | ns |
| Pulse Width High | | tSCKH | 65 | | | ns |
| LRCK Edge to BICK "↑" | (Note 14) | tLRSH | 30 | | | ns |
| BICK "↑" to LRCK Edge | (Note 14) | tSHLR | 30 | | | ns |
| LRCK to SDTO (MSB) (Except $I^2S$ mode) | | tLRS | | | 35 | ns |
| BICK "↓" to SDTO | | tSSD | | | 35 | ns |
| **Master mode** | | | | | | |
| BICK Frequency | | fSCK | | 64fs | | Hz |
| BICK Duty | | dSCK | | 50 | | % |
| BICK "↓" to LRCK | | tMSLR | –20 | | 20 | ns |
| BICK "↓" to SDTO | | tSSD | –20 | | 35 | ns |
| **Control Interface Timing ($I^2C$ Bus mode):** | | | | | | |
| SCL Clock Frequency | | fSCL | - | | 400 | kHz |
| Bus Free Time Between Transmissions | | tBUF | 1.3 | | - | µs |
| Start Condition Hold Time (prior to first clock pulse) | | tHD:STA | 0.6 | | - | µs |
| Clock Low Time | | tLOW | 1.3 | | - | µs |
| Clock High Time | | tHIGH | 0.6 | | - | µs |
| Setup Time for Repeated Start Condition | | tSU:STA | 0.6 | | - | µs |
| SDA Hold Time from SCL Falling | (Note 15) | tHD:DAT | 0 | | - | µs |
| SDA Setup Time from SCL Rising | | tSU:DAT | 0.1 | | - | µs |
| Rise Time of Both SDA and SCL Lines | | tR | - | | 0.3 | µs |
| Fall Time of Both SDA and SCL Lines | | tF | - | | 0.3 | µs |
| Setup Time for Stop Condition | | tSU:STO | 0.6 | | - | µs |
| Pulse Width of Spike Noise Suppressed by Input Filter | | tSP | 0 | | 50 | ns |
| Capacitive load on bus | | Cb | - | | 400 | pF |

Note 14. BICK rising edge must not occur at the same time as LRCK edge.
Note 15. Data must be held long enough to bridge the 300ns-transition time of SCL.

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| **Reset Timing** | | | | | | |
| PDN Pulse Width | (Note 16) | tPD | 150 | | | ns |
| PDN "↑" to SDTO valid at Slave Mode | (Note 17) | tPDV | | 4388 | | 1/fs |
| PDN "↑" to SDTO valid at Master Mode | (Note 17) | tPDV | | 4385 | | 1/fs |

Note 16. The AK5367 can be reset by bringing the PDN pin = "L".
Note 17. This cycle is the number of LRCK rising edges from the PDN pin = "H".

## ■ Timing Diagram

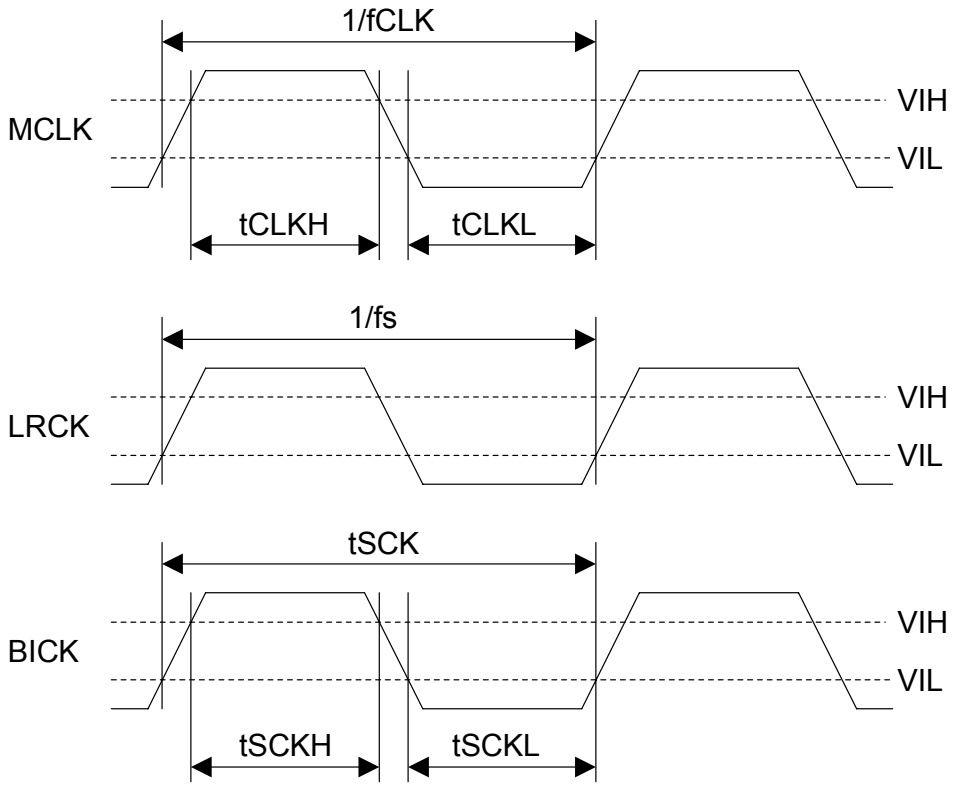



Figure 3. Clock Timing

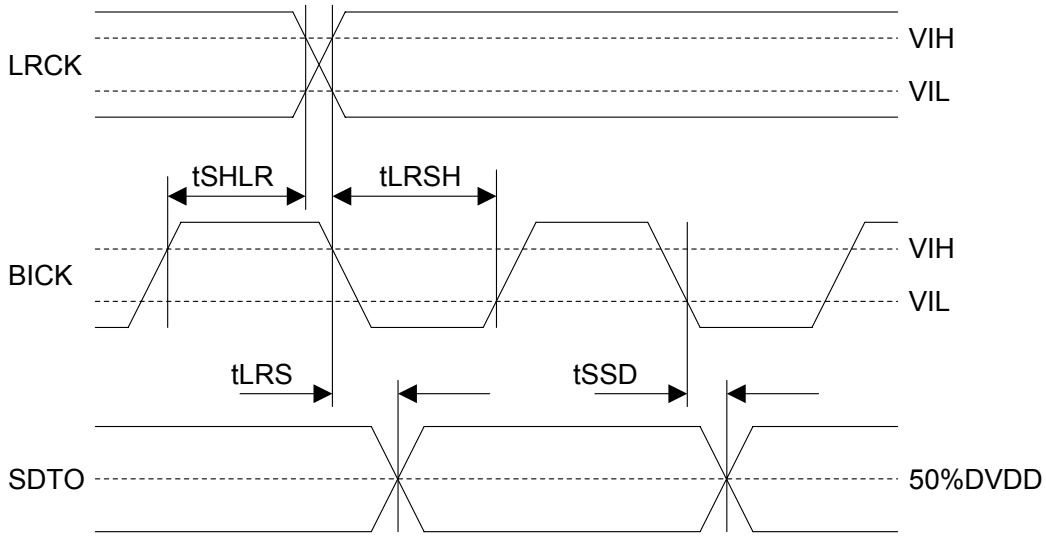



Figure 4. Audio Interface Timing (Slave mode)

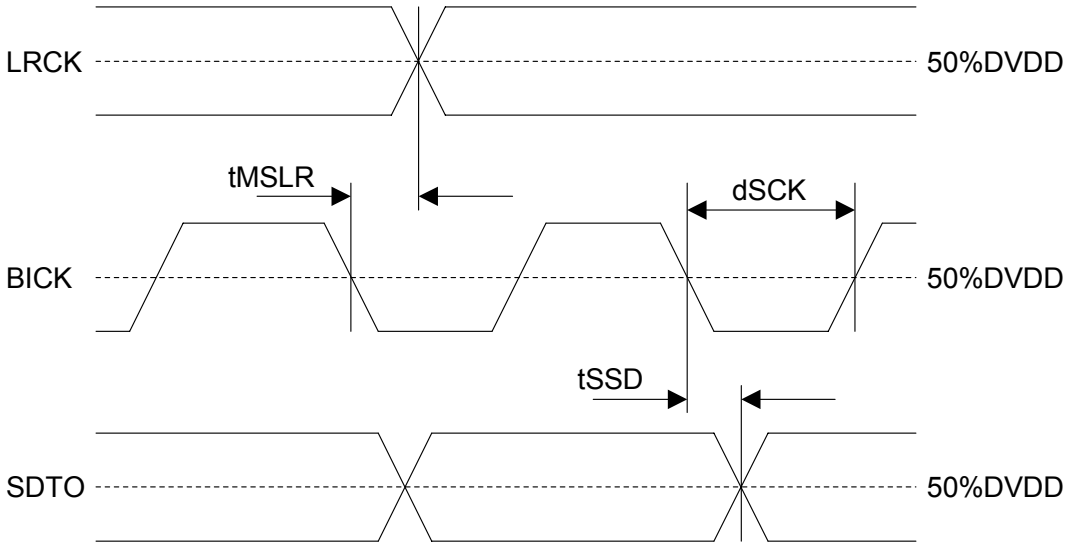



Figure 5. Audio Interface Timing (Master mode)

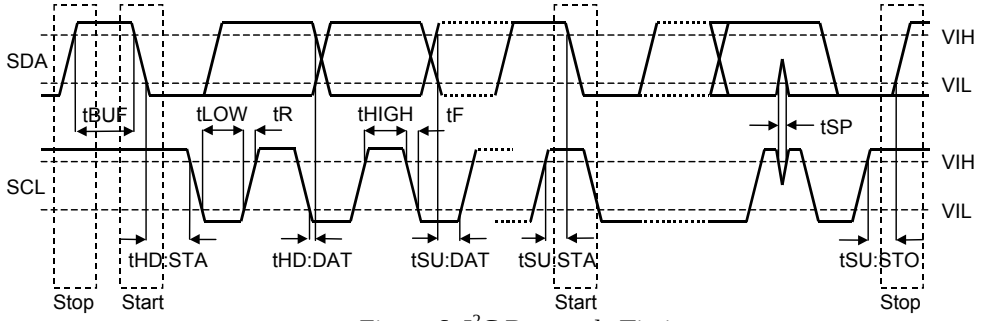



Figure 6. $I^2C$ Bus mode Timing

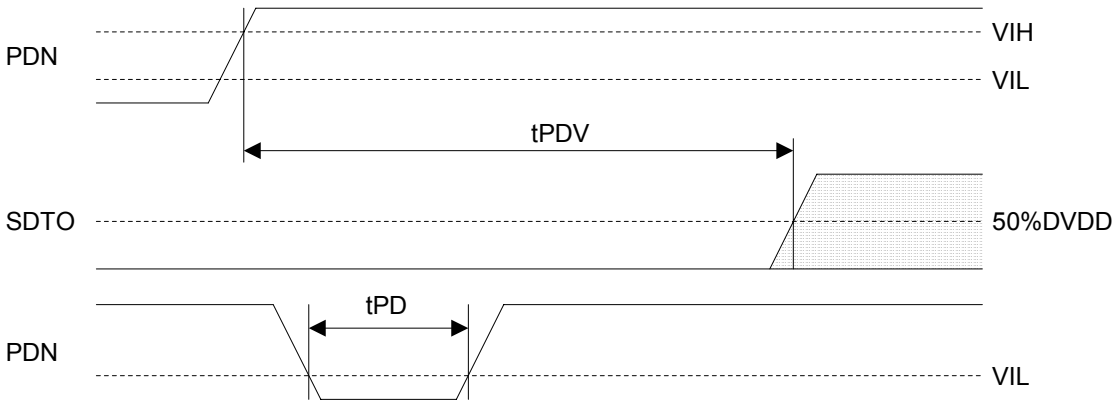



Figure 7. Power Down & Reset Timing

# OPERATION OVERVIEW

## ■ System Clock

MCLK, BICK and LRCK clocks are required. The LRCK clock input must be synchronized with MCLK, however the phase is not critical. Table 1 shows the relationship of typical sampling frequency and the system clock frequency. The MCLK, BICK and master/slave mode setting are selected by CKS2-0 bits(Table 2).

In slave mode, all external clocks (MCLK, BICK and LRCK) must be present unless PDN pin = "L". If these clocks are not provided, the AK5367 may draw excess current due to its use of internal dynamically refreshed logic. If the external clocks are not present, place the AK5367 in power-down mode (PDN pin = "L"). In master mode, the master clock (MCLK) must be provided unless PDN pin = "L". It is not necessary to reset by bringing PDN pin "L" when clocks and fs are changed. They should be changed after soft mute (SMUTE bit = "1") to avoids the switching noise.

| fs | MCLK | | | |
|---|---|---|---|---|
| | 256fs | 384fs | 512fs | 768fs |
| 32kHz | 8.192MHz | 12.288MHz | 16.384MHz | 24.576MHz |
| 44.1kHz | 11.2896MHz | 16.9344MHz | 22.5792MHz | 33.8688MHz |
| 48kHz | 12.288MHz | 18.432MHz | 24.576MHz | 36.864MHz |
| 96kHz | 24.576MHz | 36.864MHz | N/A | N/A |

Table 1. System Clock Example (N/A: Not available)

| Mode | CKS2 | CKS1 | CKS0 | Master/Slave | MCLK | BICK | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Slave | 256/384fs (32k≤fs≤96k)<br>512/768fs (32k≤fs≤48k) | ≥ 48fs or 32fs<br>(Note 18) | (default) |
| 1 | 0 | 0 | 1 | | Reserved | | |
| 2 | 0 | 1 | 0 | Master | 256fs (32k≤fs≤96k) | 64fs | |
| 3 | 0 | 1 | 1 | Master | 512fs (32k≤fs≤48k) | 64fs | |
| 4 | 1 | 0 | 0 | | Reserved | | |
| 5 | 1 | 0 | 1 | | Reserved | | |
| 6 | 1 | 1 | 0 | Master | 384fs (32k≤fs≤96k) | 64fs | |
| 7 | 1 | 1 | 1 | Master | 768fs (32k≤fs≤48k) | 64fs | |

Table 2. Operation Mode Select

Note 18. The SDTO output is 16bit when BICK=32fs input.

## ■ Audio Interface Format

Two kinds of data formats can be chosen with the DIF bit (Table 3). In both modes, the serial data is in MSB first, 2's compliment format. The SDTO is clocked out on the falling edge of BICK. The audio interface supports both master and slave modes. In master mode, BICK and LRCK are output with the BICK frequency fixed to 64fs and the LRCK frequency fixed to 1fs.

| Mode | DIF bit | SDTO | LRCK | BICK(Slave) | BICK(Master) | Figure | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 24bit, MSB justified | H/L | ≥ 48fs or 32fs | 64fs | Figure 8 | (default) |
| 1 | 1 | 24bit, $I^2S$ Compatible | L/H | ≥ 48fs or 32fs | 64fs | Figure 9 | |

Table 3. Audio Interface Format

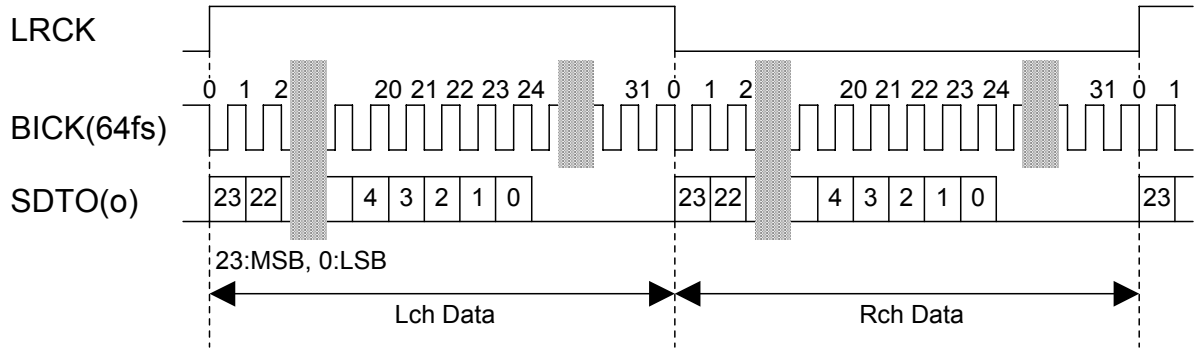



Figure 8. Mode 0 Timing

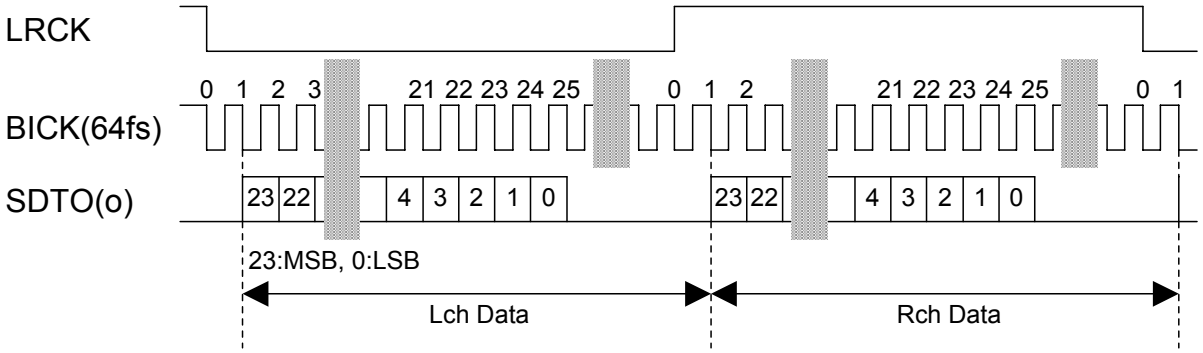



Figure 9. Mode 1 Timing

## ■ Master Mode and Slave Mode

The AK5367 becomes slave mode when it is in the power-down mode (PDN pin = "L") or exiting power-down. After exiting the power-down mode, master mode should be set by CKS0-2 bits.

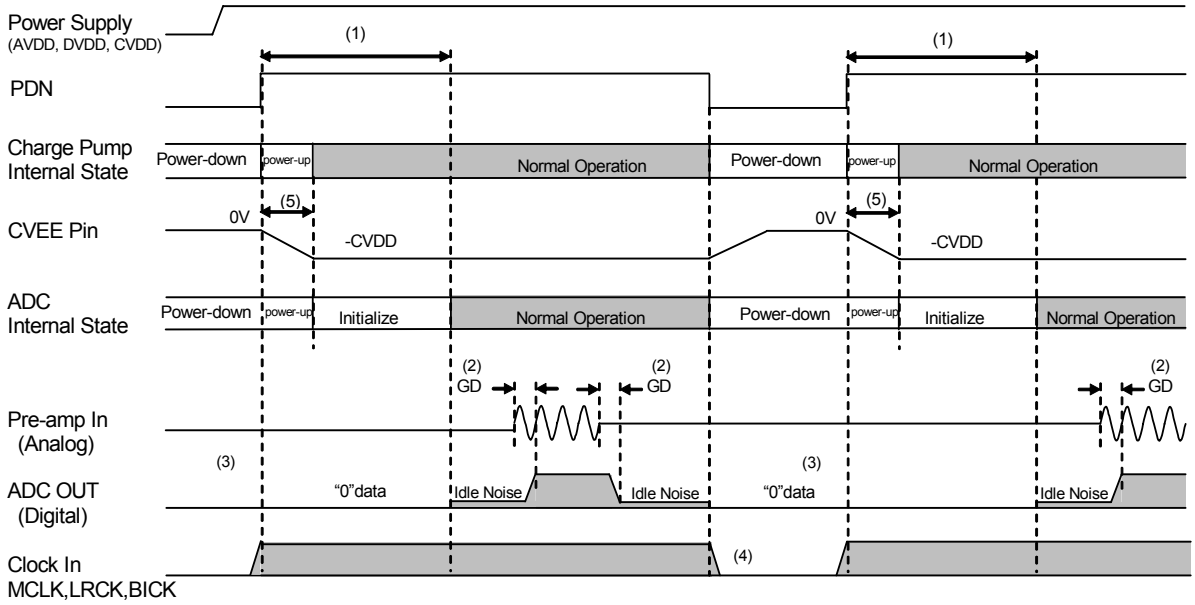
In master mode, LRCK and BICK pins are floating until CKS0-2 bits fixed. Therefore BICK and LRCK pins must be connected with 100 kΩ pull-up or pull-down resistance.

## ■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 1.0Hz (@fs=48kHz) and scales with sampling rate (fs).

## ■ Power-down

The AK5367 is placed in the power-down mode by bringing PDN pin = "L" and the digital filter is also reset at the same time. This reset should always be done after power-up. At the power-down mode, the VCOM voltage is become VSS1. After exiting the power-down mode, the Charge pump circuit is powered up, and then Pre-Amp circuit is auto powered up and an analog initialization cycle starts(Figure 10). Therefore, the output data SDTO becomes available after 4388 x LRCK cycles at slave mode, and 4385 x LRCK cycles at master mode. In the initialization, the both channel of ADC output is "0" of 2's complement. After the initialization, the ADC output is settled to the data equal to analog input signal.(the setting time is same as group delay)




Notes:

(1) 4388/fs at slave mode, 4385/fs at master mode.
(2) Analog output corresponding to digital input has group delay (GD).
(3) ADC output is "0" data at the power-down mode.
(4) Place the AK5367 in power-down mode if MCLK, BICK and LRCK are not present.
(5) Power-up time of Charge Pump Circuit. 260/fs (slave mode), 257/fs (master mode).

Figure 10. Power-down/up sequence example

## ■ System Reset

The AK5367 should be reset once by bringing PDN pin "L" after power-up. At the slave mode, the internal timing starts clocking by the rising edge (falling edge at Mode 1) of LRCK after exiting from reset and power down state by MCLK. The AK5367 is in power-down states until the LRCK is input. At the master mode, bringing PDN pin "H" and exiting from reset and power down state by MCLK input.

## ■ Soft Mute Operation

Soft mute operation is performed in the digital domain of the ADC output. When SMUTE bit goes "1", the ADC output data is attenuated to −∞ within 1024 LRCK cycles. When the SMUTE bit returned "0", the mute is cancelled and the output attenuation gradually changes to 0dB within 1024 LRCK cycles. If the soft mute is cancelled before mute state after starting of the operation, the attenuation is discontinued and returned to 0dB. The soft mute is effective for changing the signal source without stopping the signal transmission.

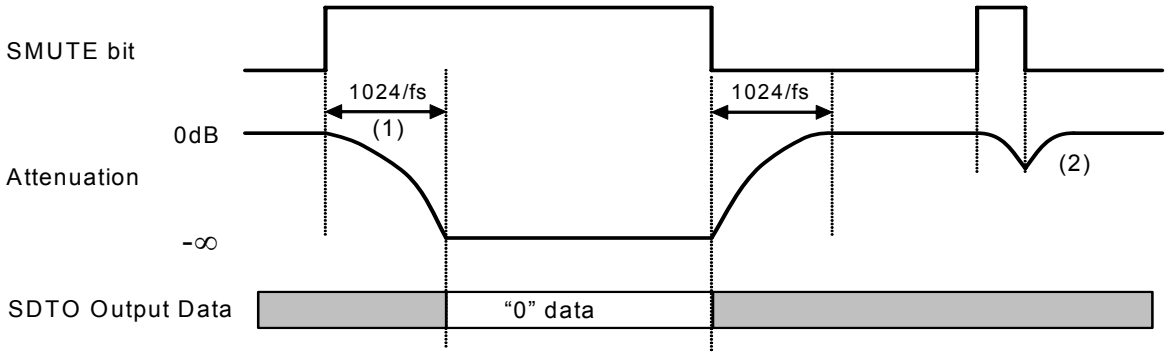



Figure 11. Soft Mute Function

Notes:

(1) The output signal is attenuated by −∞ within 1024 LRCK cycles (1024/fs).

(2) If the soft mute is cancelled before the mute, the attenuation is discontinued and returned to 0dB by the same cycle.

## ■ Input Selector

The AK5367 includes 4ch stereo input selectors. The input selector is 4 to 1 selector and set by SEL2-0 bits (Table 4).

| SEL2 bit | SEL1 bit | SEL0 bit | Input Selector | |
|---|---|---|---|---|
| 0 | 0 | 0 | LIN1 / RIN1 | |
| 0 | 0 | 1 | LIN2 / RIN2 | |
| 0 | 1 | 0 | LIN3 / RIN3 | |
| 0 | 1 | 1 | LIN4 / RIN4 | |
| 1 | 0 | 0 | All off (Note) | (default) |

Table 4. Input Selector

Note: The LOUT, ROUT pin are 0V.

[Input selector switching sequence]

The input selector should be changed after soft mute to avoid the switching noise of the input selector (Figure 12).

1. Enable the soft mute before changing channel.
2. Change channel.
3. Disable the soft mute.

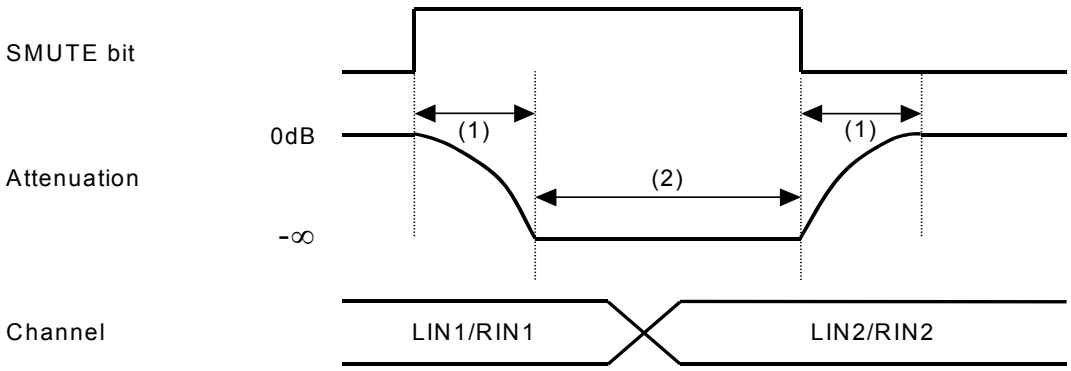



Figure 12. Input channel switching sequence example

Note:

(1) The output signal is attenuated by –∞ within 1024 LRCK cycles (1024/fs).

(2) When changing channels, the input channel should be changed during (2). The period of (2) should be around 200ms because there is some DC difference between the channels.

## ■ Pre-Amp and Input Attenuator

The input ATTs are constructed by adding the input resistor (Ri) for LIN1-4/RIN1-4 pins and the feedback resistor (Rf) between LOPIN/ROPIN pin and LOUT/ROUT pin (Figure 13). The input voltage range of the LISEL/RISEL pin is typically 0.6 x AVDD (Vpp). If the input voltage of the input selector exceeds typ. 0.6 x AVDD, the input voltage of the LISEL/RISEL pins must be attenuated to 0.6 x AVDD by the input ATTs. Table 5 shows the example of Ri and Rf.

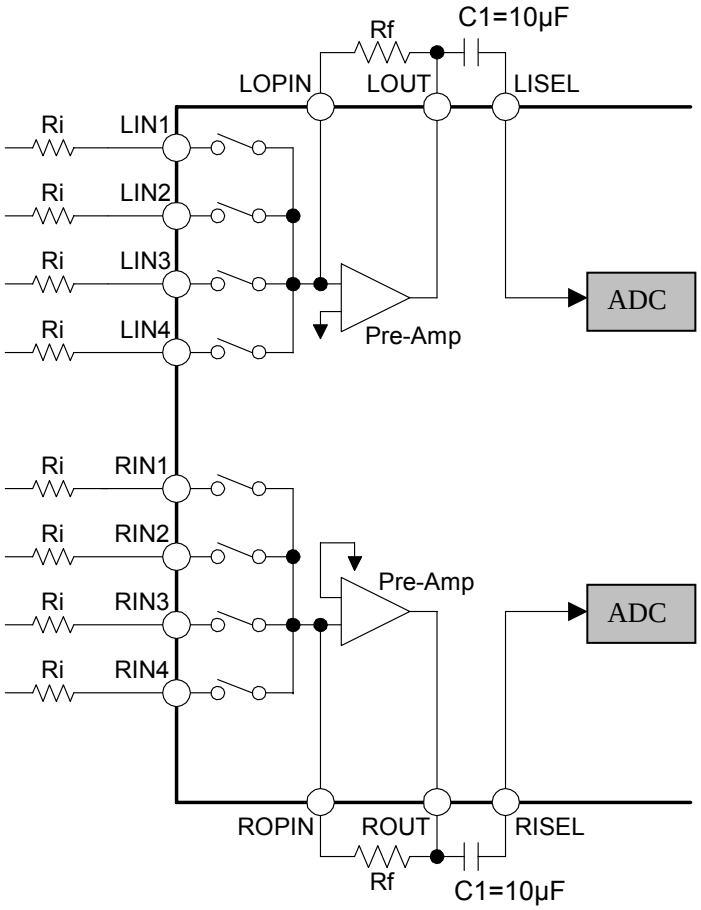



Figure 13. Pre-Amp and Input ATT

- Example for input range

| Input Range | Ri [kΩ] | Rf [kΩ] | ATT Gain [dB] | LISEL/RISEL pin |
|---|---|---|---|---|
| 4Vrms | 47 | 12 | –11.86 | 1.02Vrms |
| 2Vrms | 47 | 24 | –5.84 | 1.02Vrms |
| 1Vrms | 47 | 47 | 0 | 1Vrms |

Table 5. Input ATT example

Note: The value of Ri is over 10kΩ.

## ■ Charge Pump Circuit

The internal charge pump circuit generates negative voltage(CVEE) from CVDD voltage. The generated voltage is used for Pre-Amp.

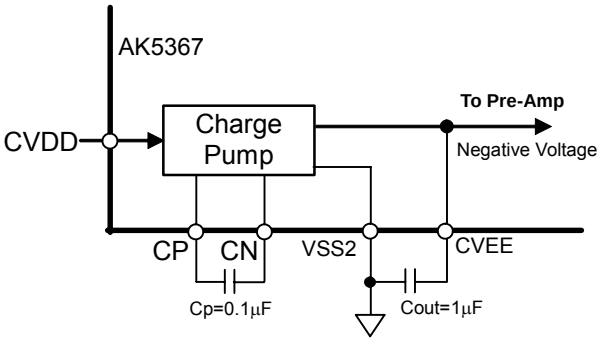



Figure 14. Charge Pump Circuit

## ■ Serial Control Interface

The AK5367 supports the first-mode I$^2$C-bus system (max: 400kHz).
The pull-up resistance of SDA,SCL pins should be connected below the voltage of DVDD+0.3V.

1. WRITE Operations
Figure 15 shows the data transfer sequence for the I$^2$C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 21). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant 7 bits of the slave address are fixed as "0110001". If the slave address matches that of the AK5367, the AK5367 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 22). A R/W bit value of "1" indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK5367. The format is MSB first, and those most significant 6-bits are fixed to zeros (Figure 17). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 18). The AK5367 generates an acknowledge after each byte is received. A data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 21).

The AK5367 can perform more than one byte write operation per sequence. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 2-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 02H prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 23) except for the START and STOP conditions.

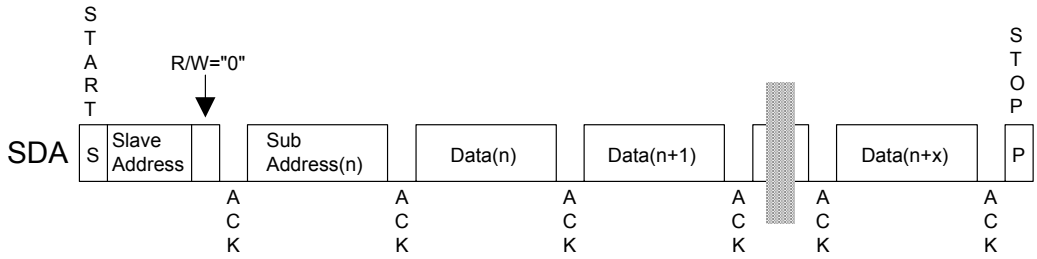



Figure 15. Data Transfer Sequence at the I$^2$C-Bus Mode

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | R/W |

Figure 16. The First Byte

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | A1 | A0 |

Figure 17. The Second Byte

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Figure 18. Byte Structure after the second byte

2. READ Operations

Set the R/W bit = “1” for the READ operation of the AK5367. After transmission of data, the master can read the next address’s data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal 2-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 02H prior to generating a stop condition, the address counter will “roll over” to 00H and the previous data will be overwritten.

The AK5367 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

2-1. CURRENT ADDRESS READ

The AK5367 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) were to address n, the next CURRENT READ operation would access data from the address n+1. After receipt of the slave address with R/W bit set to “1”, the AK5367 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generates a stop condition, the AK5367 ceases transmission.

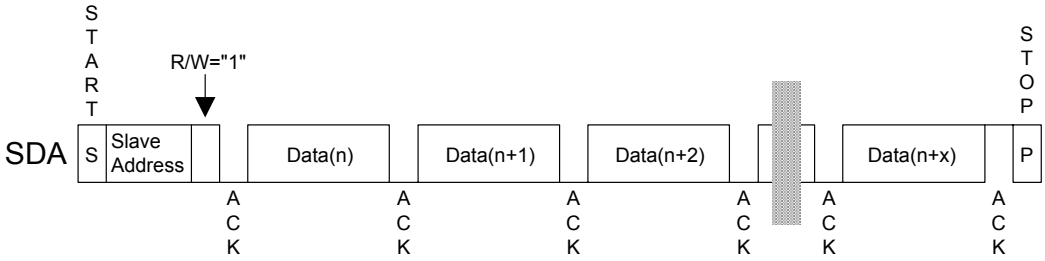



Figure 19. CURRENT ADDRESS READ

2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit “1”, the master must first perform a “dummy” write operation. The master issues a start request, a slave address (R/W bit = “0”) and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit “1”. The AK5367 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generates a stop condition, the AK5367 ceases transmission.

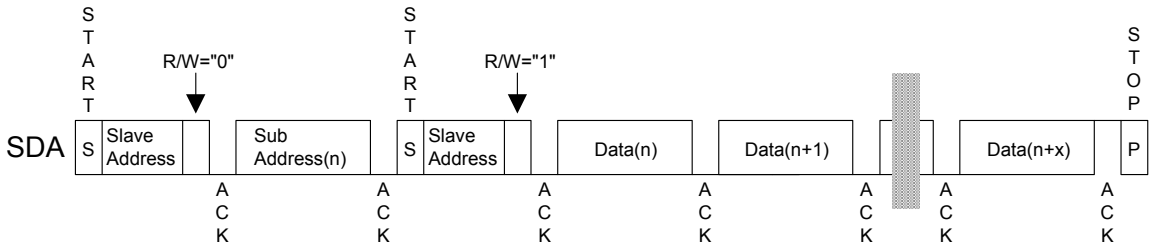



Figure 20. RANDOM ADDRESS READ

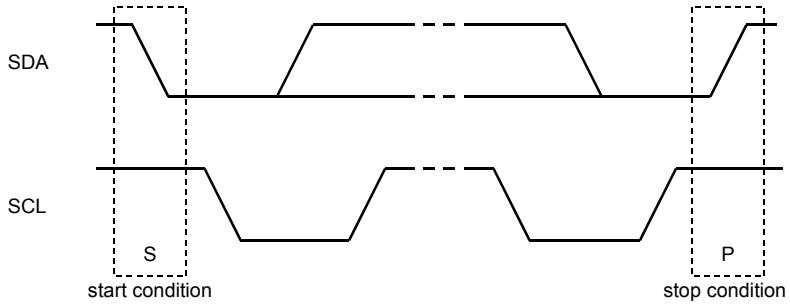



Figure 21. START and STOP Conditions

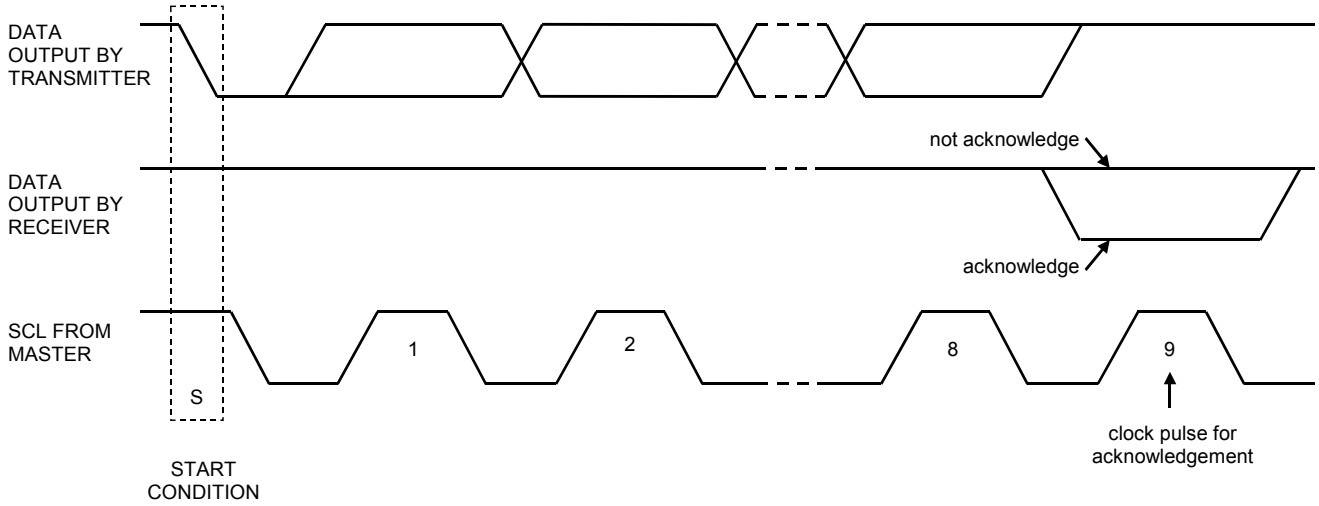



Figure 22. Acknowledge on the $I^2C$-Bus

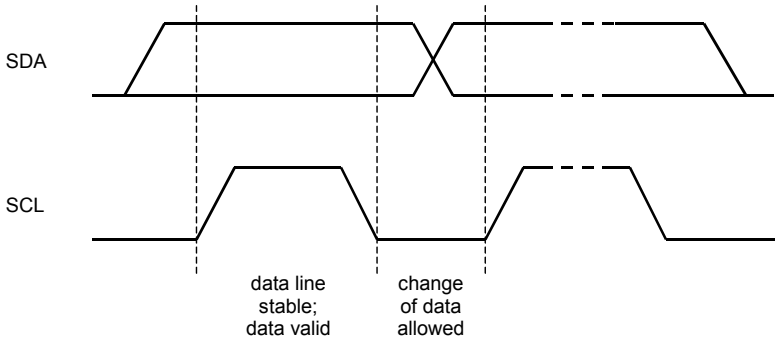



Figure 23. Bit Transfer on the $I^2C$-Bus

## ■ Register Map

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 00H | Power Down Control | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PWN |
| 01H | Input Selector Control | 0 | 0 | 0 | 0 | 0 | SEL2 | SEL1 | SEL0 |
| 02H | Clock & Format Control | 0 | 0 | 0 | DIF | CKS2 | CKS1 | CKS0 | SMUTE |

PDN pin = "L" resets the registers to their default values.

Note: Unused bits must contain a "0" value.
Only write to address 00H to 02H.

## ■ Register Definitions

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 00H | Power Down Control | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PWN |
| R/W | | RD | RD | RD | RD | RD | RD | RD | R/W |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

PWN: Power down control
0: Power down. All registers are not initialized.
1: Normal Operation (default)
"0" powers down all sections and then ADC do not operate. The contents of all register are not initialized and enabled to write to the registers.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 01H | Input Selector Control | 0 | 0 | 0 | 0 | 0 | SEL2 | SEL1 | SEL0 |
| R/W | | RD | RD | RD | RD | RD | RD | R/W | R/W |
| Default | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

SEL2-0: Input selector (Table 4)
Initial values are "100".

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 02H | Clock & Format Control | 0 | 0 | 0 | DIF | CKS2 | CKS1 | CKS0 | SMUTE |
| R/W | | RD | RD | RD | R/W | R/W | R/W | R/W | R/W |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SMUTE: Soft Mute control
0: Normal Operation (default)
1: SDTO outputs soft-muted.

CKS2-0: Operation mode select (Table 2)
Initial values are "000".

DIF: Audio interface format (Table 3)
Initial values are "0" (24bit, MSB justified).

## SYSTEM DESIGN

Figure 24 shows the system connection diagram. The evaluation board (AKD5367) demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

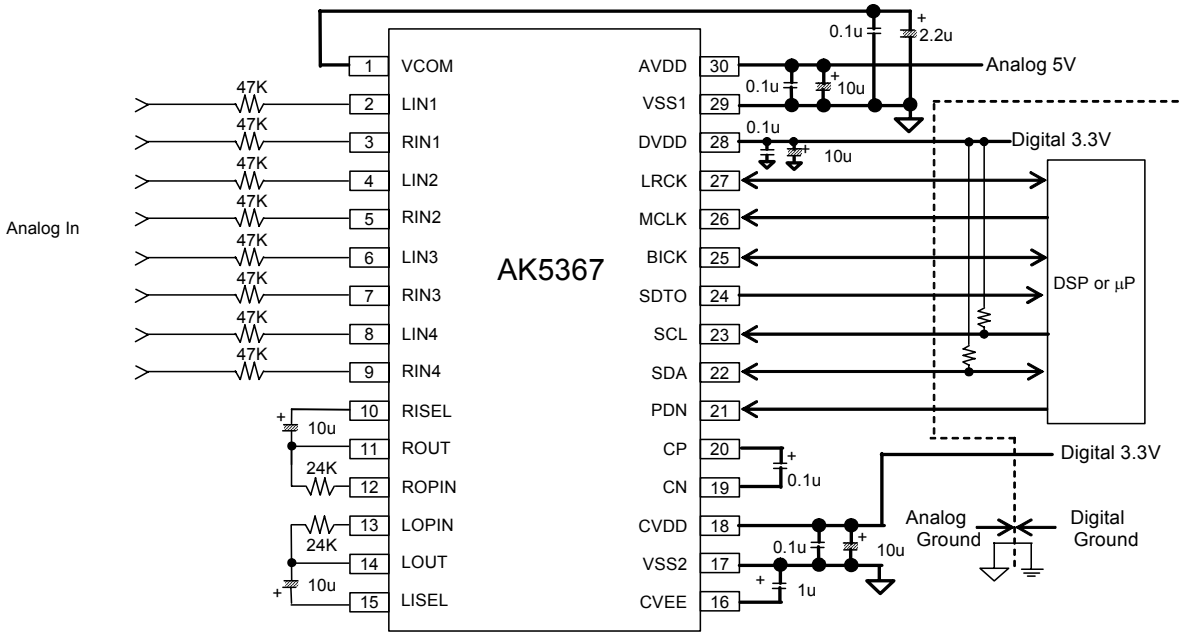



Figure 24. Typical Connection Diagram

### 1. Grounding and Power Supply Decoupling

The AK5367 requires careful attention to power supply and grounding arrangements. AVDD, DVDD and CVDD are usually supplied from the analog supply in the system. Alternatively if AVDD, DVDD and CVDD are supplied separately, the power up sequence is not critical. **VSS1 and VSS2 of the AK5367 must be connected to analog ground plane.** System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK5367 as possible, with the small value ceramic capacitor being the closest.

### 2. Voltage Reference Inputs

The differential voltage between AVDD and VSS1 sets the analog input range. VCOM is a signal common of this chip. An electrolytic capacitor 2.2µF parallel with a 0.1µF ceramic capacitor attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from VCOM pins in order to avoid unwanted coupling into the AK5367.

### 3. Analog Inputs

An analog input of AK5367 is single-ended input to Pre-Amp through the external resistor. For input signal range, adjust feedback resistor so that Pre-Amp output may become the input range (typ. 0.6 x AVDD Vpp) of ADC (LISEL,RISEL pin). Between the Pre-Amp output (LOUT, ROUT pin) and the ADC input (LISEL,RISEL pin) is AC coupled with capacitor. When the impedance of LISEL/RISEL pins is “R” and the capacitor of between the Pre-Amp output and the ADC input is “C”, the cut-off frequency is fc = 1/(2πRC). The ADC output data format is 2’s compliment. The internal HPF removes the DC offset. The AK5367 samples the analog inputs at 64fs. The digital filter rejects noise above the stop band except for multiples of 64fs. The AK5367 includes an anti-aliasing filter (RC filter) to attenuate a noise around 64fs.

### 4. Attention to the PCB Wiring

LIN1-4 and RIN1-4 pins are the summing nodes of the Pre-Amp. Attention should be given to avoid coupling with other signals on those nodes. This can be accomplished by making the wire length of the input resistors as short as possible. The same theory also applies to the LOPIN/ROPIN pins and feedback resistors; keep the wire length to a minimum. Unused input pins among LIN1-4 and RIN1-4 pins should be left open. When external devices are connected to LOUT and ROUT pin, the input impedance is min. 15kΩ.

## 4. I²C bus Connection

SCL and SDA pins should be connected to DVDD through the resistor based on I²C standard. As there is a protection between each pin and DVDD, the pulled up voltage mast be DVDD or lower(Figure 25).

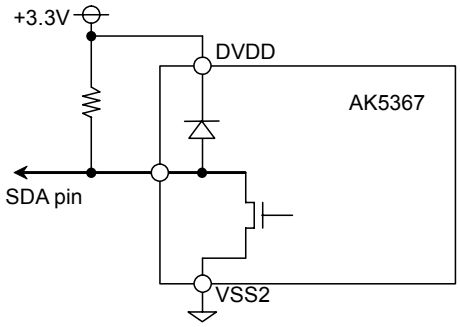
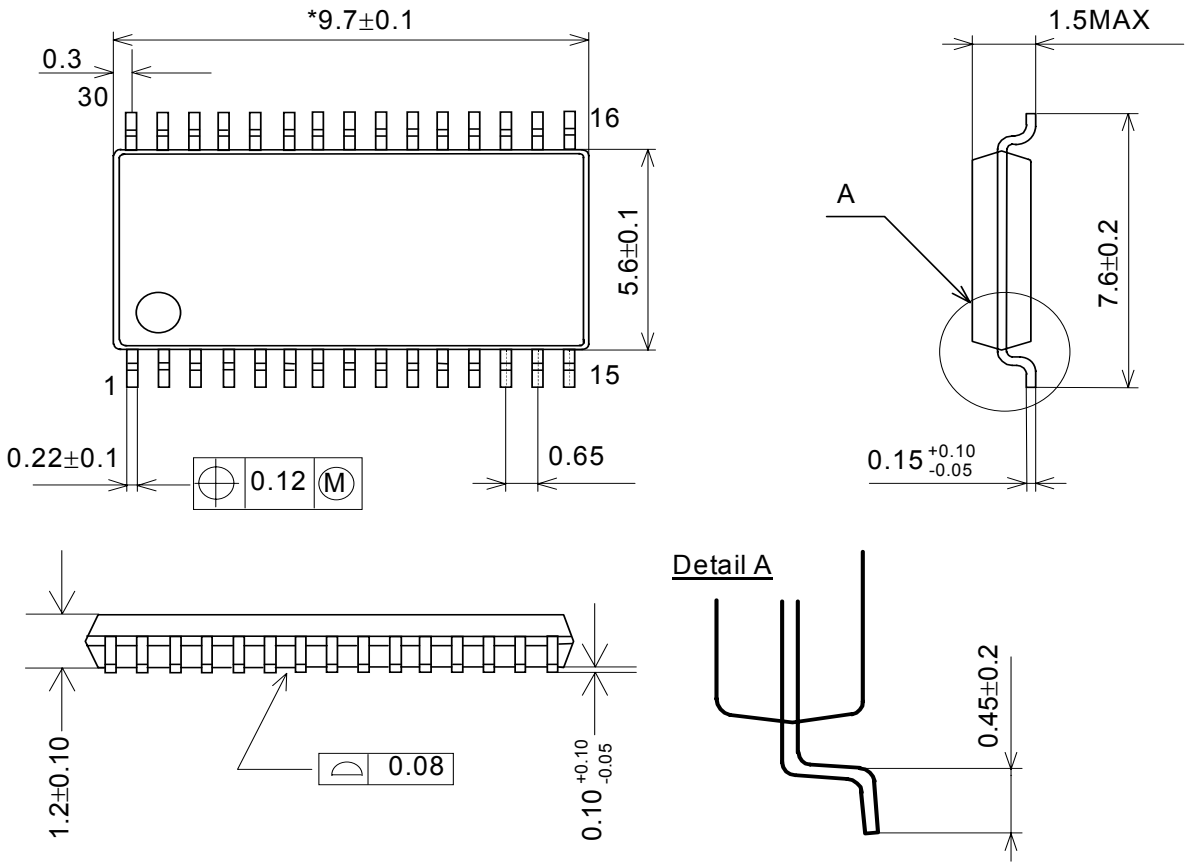



Figure 25. SDA pin output

## PACKAGE

30pin VSOP (Unit: mm)

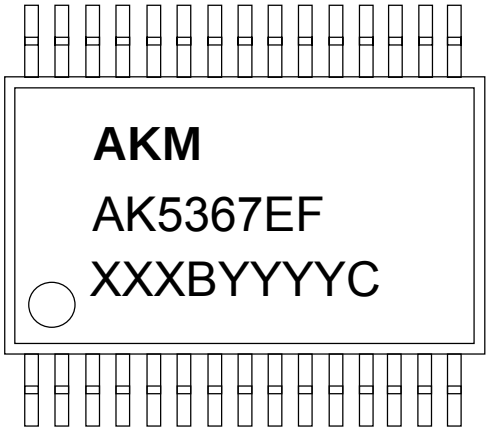



NOTE: Dimension "*" does not include mold flash.

### ■ Material & Lead finish

| | |
|---|---|
| Package molding compound: | Epoxy |
| Lead frame material: | Cu |
| Lead frame surface treatment: | Solder (Pb free) plate |

## MARKING




XXXBYYYYC Date code identifier

XXXB :Lot number (X : Digit number, B : Alpha character)
YYYYC : Assembly date (Y : Digit number, C : Alpha character)

## REVISION HISTORY

| Date (YY/MM/DD) | Revision | Reason | Page | Contents |
|---|---|---|---|---|
| 07/12/27 | 00 | First Edition | | |