D/A Converter Series for Electronic Adjustments

# High-precision 10bit 8ch・10ch Type D/A Converters

**BU2506FV, BU2505FV**

No.09052EAT03

●Description

BU2506FV and BU2505FV ICs are high performance 10bit R-2R type DACs with 8ch and 10ch outputs, respectively. Cascade connection is possible, ensuring suitability with multi-channel applications. Each channel incorporates a full swing output-type buffer amplifier with high speed output response characteristics, resulting in a greatly shortened wait time. The ICs also utilize the TTL level input method, and with the RESET pin the output voltage can be kept in the lower reference voltage range.

●Features

1) High performance, multi-channel R-2R-type 10bit D/A converter built-in (BU2506FV: 8 channels, BU2505FV: 10 channels)
2) Full swing output type buffer amplifier incorporated at each output channel
3) The RESET terminal can keep the output voltage at all channels within the lower reference voltage range
4) Digital input compatible with TTL levels
5) 14bit 3-line serial data + RESET signal input (address 4bit + data 10bit)
6) Cascade connection available
7) LSB first / MSB first of 10bit data can be changed by the REVERSE terminal
8) Compact package: 0.65mm pitch, 20 pins (SSOP-B20)

●Applications

DVDs, CD-Rs, CD-RWs, Digital cameras

●Lineup

| Parameter | BU2505FV | BU2506FV |
|---|---|---|
| Power source voltage range | 4.5 to 5.5V | 4.5 to 5.5V |
| Number of channels | 10ch | 8ch |
| Differential non linearity error | ±1.0LSB | ±1.0LSB |
| Integral non linearity error | ±3.5LSB | ±3.5LSB |
| Data transfer frequency | 10MHz | 10MHz |
| Package | SSOP-B20 | SSOP-B20 |

●Absolute Maximum Ratings(Ta=25℃)

| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| Power source voltage | VCC | -0.3 to 6.0 | V |
| D/A converter upper standard voltage | VDD | -0.3 to 6.0 | V |
| Input voltage | VIN | -0.3 to 6.0 | V |
| Output voltage | VOUT | -0.3 to 6.0 | V |
| Storage temperature range | $T_{stg}$ | -55 to 125 | ℃ |
| Power dissipation | Pd | 400* | mW |

* Derated at 4mW/℃ at Ta>25℃, mounted on a 70x70x1.6mm FR4 glass epoxy board (copper foil area less than 3%)
Note: These products are not robust against radiation

●Recommended Operating Conditions(Ta=25℃)

| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| Power supply voltage range | VCC | 4.5 to 5.5 | V |
| Operating temperature range | Topr | -30 to 85 | ℃ |

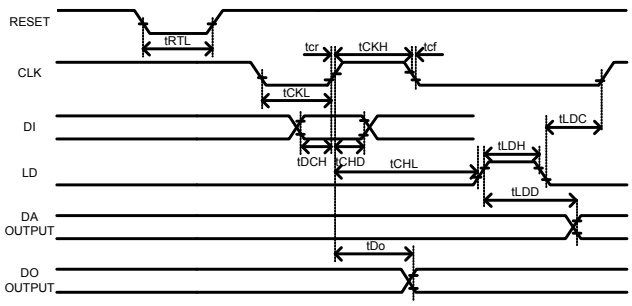
●Electrical Characteristics(Unless otherwise specified, VCC＝5V, VrefH＝5V, VrefL＝0V, Ta＝25℃)

| Parameter | | Symbol | Limits | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | MIN. | TYP. | MAX. | | |
| <Digital unit> | | | | | | | |
| Power source current | | ICC | - | 0.85 | 2.8 | mA | At CLK=10MHz, IAO=0μA |
| Input leak current | | IILK | -5 | - | 5 | μA | VIN=0 to VCC |
| Input voltage L | | VIL | - | - | 0.8 | V | - |
| Input voltage H | | VIH | 2.0 | - | - | V | - |
| Output voltage L | | VOL | 0 | - | 0.4 | V | IOL=2.5mA |
| Output voltage H | | VOH | 4.6 | - | 5 | V | IOH=-2.5mA |
| <Analog unit> | | | | | | | |
| Consumption current | | IrefH | - | 4.5 | 7.5 | mA | Data condition : at maximum current |
| | | | - | 3.7 | 6.2 | mA(*1) | |
| D/A converter upper standard voltage setting range | | VrefH | 3.0 | - | 5 | V | Outputs are not necessarily within the standard voltage setting range, but ARE within the buffer amplifier output voltage range (VO). |
| D/A converter lower standard voltage setting range | | VrefL | 0 | - | 1.5 | V | |
| Buffer amplifier output voltage range | | VO | 0.1 | - | 4.9 | V | IO=±100μA |
| | | | 0.2 | - | 4.75 | | IO=±1.0mA |
| Buffer amplifier output drive range | | IO | -2 | - | 2 | mA | Upper saturation voltage =0.35V<br>Lower saturation voltage =0.23V |
| Precision | Differential non-linearity error | DNL | -1.0 | - | 1.0 | LSB | VrefH =4.796V<br>VrefL=0.7V<br>VCC=5.5V (4mV/LSB)<br>At no load (IO=+0mA ) |
| | Integral non-linearity error | INL | -3.5 | - | 3.5 | | |
| | Zero point error | SZERO | -25 | - | 25 | mV | |
| | Full scale error | SFULL | -25 | - | 25 | | |
| Buffer amplifier output impedance | | RO | - | 5 | 15 | Ω | - |
| Pull-up I/O internal resistance value | | Rup | 12.5 | 25 | 37.5 | kΩ | Input voltage 0V<br>(Resistance value changes according to voltage supplied) |

*1 Value in the case where CH1 ~ CH8 are set to maximum current

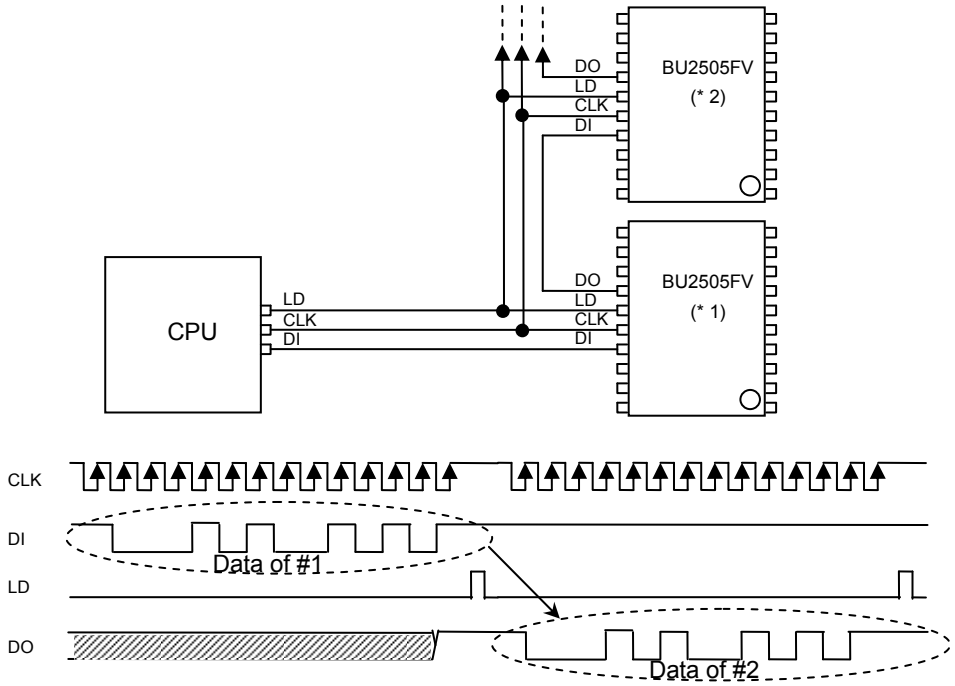
●Timing Characteristics(Unless otherwise specified, VCC＝5V, VrefH＝5V, VrefL＝0V, Ta＝25℃)

| Parameter | Symbol | Limits | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | | Judgment level is 80% / 20% of VCC. |
| Reset L pulse width | tRTL | 50 | - | - | nS | - |
| Clock L pulse width | tCKL | 50 | - | - | | - |
| Clock H pulse width | tCKH | 50 | - | - | | - |
| Clock rise time | tcr | - | - | 50 | | - |
| Clock fall time | tcf | - | - | 50 | | - |
| Data setup time | tDCH | 20 | - | - | | - |
| Data hold time | tCHD | 40 | - | - | | - |
| Load setup time | tCHL | 50 | - | - | | - |
| Load hold time | tLDC | 50 | - | - | | - |
| Load H pulse width | tLDH | 50 | - | - | | - |
| Data output delay time | tDO | - | - | 90 | | CL=100pF |
| DA output settling time | tLDD | - | 7 | 20 | μS | CL≦1000pF, VO:0.5V⇔4.5V .<br>Until output becomes the final value 1/2LSB |



●Cascade Connection

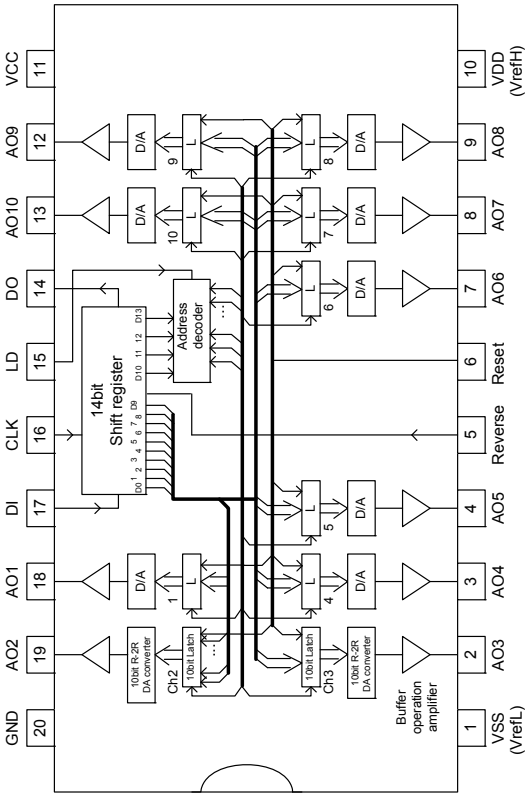
A cascade connection data output terminal (DO) is available for reducing the design load when the number of channels is increased. The DO terminal can be connected directly to the data input terminal (DI) of the next stage. Its effectiveness increases as the number of channels increases.The data transition timing is as shown below.



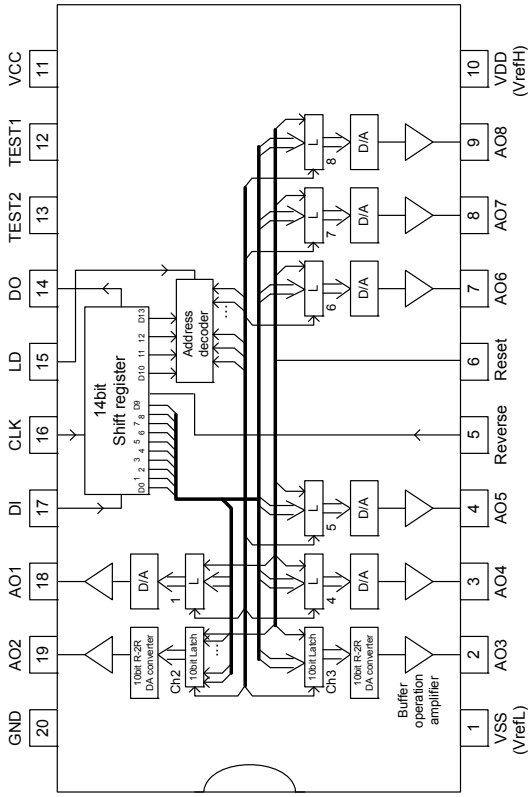

In a cascade connection, in order to have sufficient data change and clock edge time margins, make the clock line the shortest.

●Block Diagrams

BU2505FV




BU2506FV



●Terminal Descriptions

| No. | Terminal Name | Analog / Digital | I/O | Description | Equivalent Circuit |
|---|---|---|---|---|---|
| 1 | VSS | Analog | - | DA converter lower standard voltage (VrefL) input terminal | 6 |
| 2 | AO3 | Analog | O | 10bit D/A output(CH3) | 4 |
| 3 | AO4 | Analog | O | 10bit D/A output(CH4) | 4 |
| 4 | AO5 | Analog | O | 10bit D/A output(CH5) | 4 |
| 5 | Reverse | Digital | I | The reverse LSB and MSB of data designation 10bit in 14bit. | 2 |
| 6 | Reset | Digital | I | All ch analog output L fixed | 2 |
| 7 | AO6 | Analog | O | 10bit D/A output(CH6) | 4 |
| 8 | AO7 | Analog | O | 10bit D/A output(CH7) | 4 |
| 9 | AO8 | Analog | O | 10bit D/A output(CH8) | 4 |
| 10 | VDD | Analog | - | DA converter upper standard voltage (VrefH) input terminal | 5 |
| 11 | VCC | - | - | Power source terminal | - |
| 12 | AO9(TEST1) | Analog | O | 10bit D/A output(CH9) (BU2506FV : test terminal) | 4 |
| 13 | AO10(TEST2) | Analog | O | 10bit D/A output(CH10) (BU2506FV : test terminal) | 4 |
| 14 | DO | Digital | O | This outputs bit data of LSB of 14bit shift register. | 3 |
| 15 | LD | Digital | I | LD terminal. When High level is input, the value of 14bit shift register is loaded to decoder and D/A output register. | 1 |
| 16 | CLK | Digital | I | Shift clock input terminal. At rise of shift clock, the signal from DI terminal is input to 14bit shift register. | 1 |
| 17 | DI | Digital | I | Serial data input terminal. Serial data whose data length is 14bit (address 4bit + data 10bit) is input. | 1 |
| 18 | AO1 | Analog | O | 10bit D/A output(CH1) | 4 |
| 19 | AO2 | Analog | O | 10bit D/A output(CH2) | 4 |
| 20 | GND | - | - | GND terminal | - |

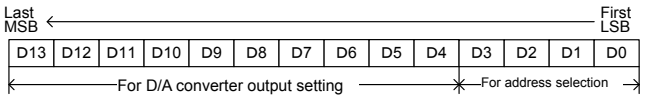
*In the case of BU2506FV, be sure to leave the TEST1 and TEST2 terminals open

●Command Transmission

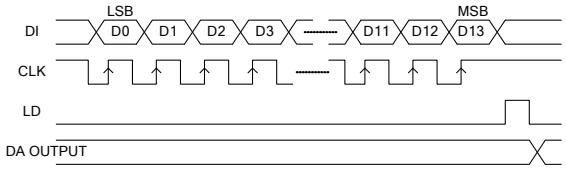
1) Reverse = open (or VCC short-circuit) setting

(Data: LSB first)

(1) Data format




(2) Data timing diagram

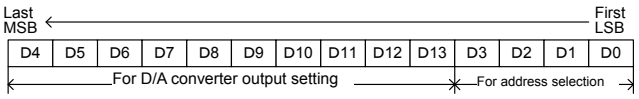



| D3 | D2 | D1 | D0 | Address Selection |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Inconsequential |
| 0 | 0 | 0 | 1 | AO1 selection |
| 0 | 0 | 1 | 0 | AO2 selection |
| 0 | 0 | 1 | 1 | AO3 selection |
| 0 | 1 | 0 | 0 | AO4 selection |
| 0 | 1 | 0 | 1 | AO5 selection |
| 0 | 1 | 1 | 0 | AO6 selection |
| 0 | 1 | 1 | 1 | AO7 selection |
| 1 | 0 | 0 | 0 | AO8 selection |
| 1 | 0 | 0 | 1 | AO9 selection*1 |
| 1 | 0 | 1 | 0 | AO10 selection*1 |
| 1 | 0 | 1 | 1 | Inconsequential |
| 1 | 1 | 0 | 0 | Inconsequential |
| 1 | 1 | 0 | 1 | Inconsequential |
| 1 | 1 | 1 | 0 | Inconsequential |
| 1 | 1 | 1 | 1 | Inconsequential |

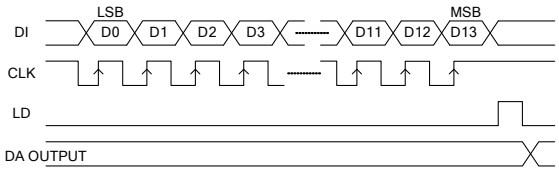
| D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D/A output (VrefH=VDD, VrefL=VSS) |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VrefL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (VrefH-VrefL)/1024×1+VrefL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | (VrefH-VrefL)/1024×2+VrefL |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | (VrefH-VrefL)/1024×3+VrefL |
| : | : | : | : | : | : | : | : | : | : | : |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | (VrefH-VrefL)/1024×1022+VrefL |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | (VrefH-VrefL)/1024×1023+VrefL |

2) Reverse = L setting(Data: MSB first )

(1) Data format




(2) Data timing diagram




| D3 | D2 | D1 | D0 | Address selection |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Inconsequential |
| 0 | 0 | 0 | 1 | AO1 selection |
| 0 | 0 | 1 | 0 | AO2 selection |
| 0 | 0 | 1 | 1 | AO3 selection |
| 0 | 1 | 0 | 0 | AO4 selection |
| 0 | 1 | 0 | 1 | AO5 selection |
| 0 | 1 | 1 | 0 | AO6 selection |
| 0 | 1 | 1 | 1 | AO7 selection |
| 1 | 0 | 0 | 0 | AO8 selection |
| 1 | 0 | 0 | 1 | AO9 selection*1 |
| 1 | 0 | 1 | 0 | AO10 selection*1 |
| 1 | 0 | 1 | 1 | Inconsequential |
| 1 | 1 | 0 | 0 | Inconsequential |
| 1 | 1 | 0 | 1 | Inconsequential |
| 1 | 1 | 1 | 0 | Inconsequential |
| 1 | 1 | 1 | 1 | Inconsequential |

| D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D/A output (VrefH=VDD, VrefL=VSS) |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VrefL |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | (VrefH-VrefL)/1024×1+VrefL |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | (VrefH-VrefL)/1024×2+VrefL |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | (VrefH-VrefL)/1024×3+VrefL |
| : | : | : | : | : | : | : | : | : | : | : |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | (VrefH-VrefL)/1024×1022+VrefL |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | (VrefH-VrefL)/1024×1023+VrefL |

*1 In the BU2506FV, this channel is for testing, therefore, do not designate.

●Electrical Characteristics Curves

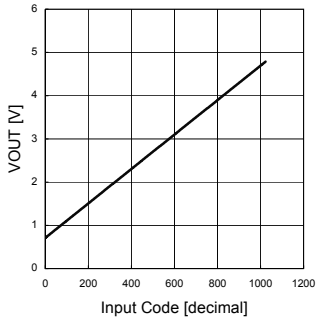



Fig.1 Output voltage linearity(-30℃)

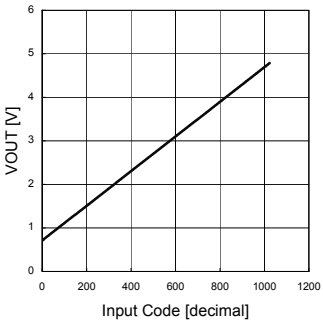



Fig.2 Output voltage linearity(25℃)

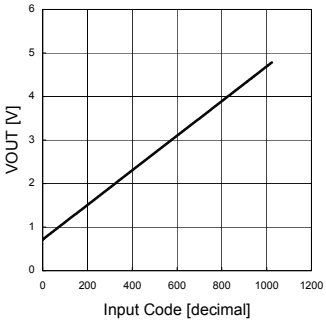



Fig.3 Output voltage linearity(85℃)

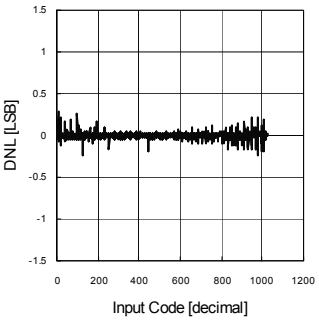



Fig.4 Differential linearity error (－30℃)

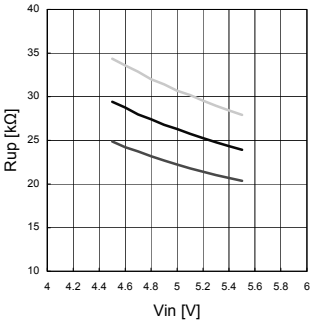



Fig.5 Differential linearity error(25℃)

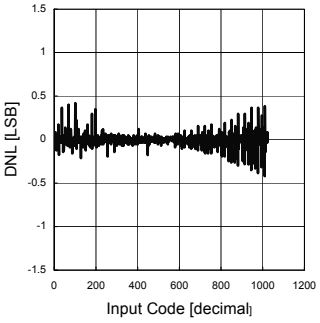



Fig.6 Differential linearity error(85℃)

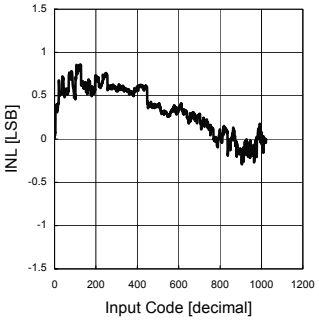



Fig.7 Integral linearity error(-30℃)

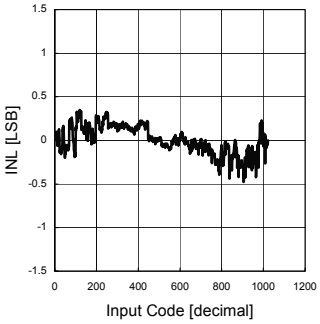



Fig.8 Integral linearity error(25℃)

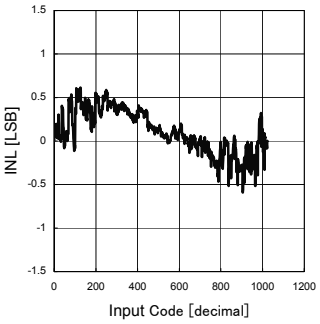



Fig.9 Integral linearity error(85℃)

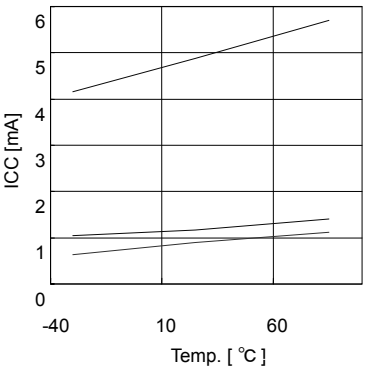



Fig.10 Circuit current temperature characteristic

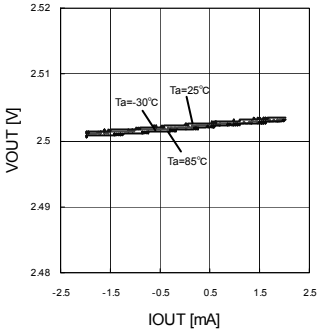



Fig.11 Output load fluctuation characteristic (input code : 1FFh)

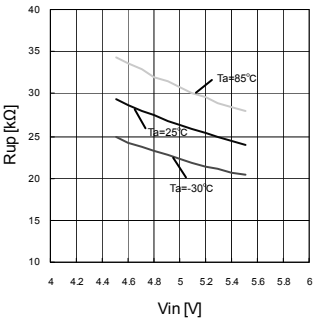
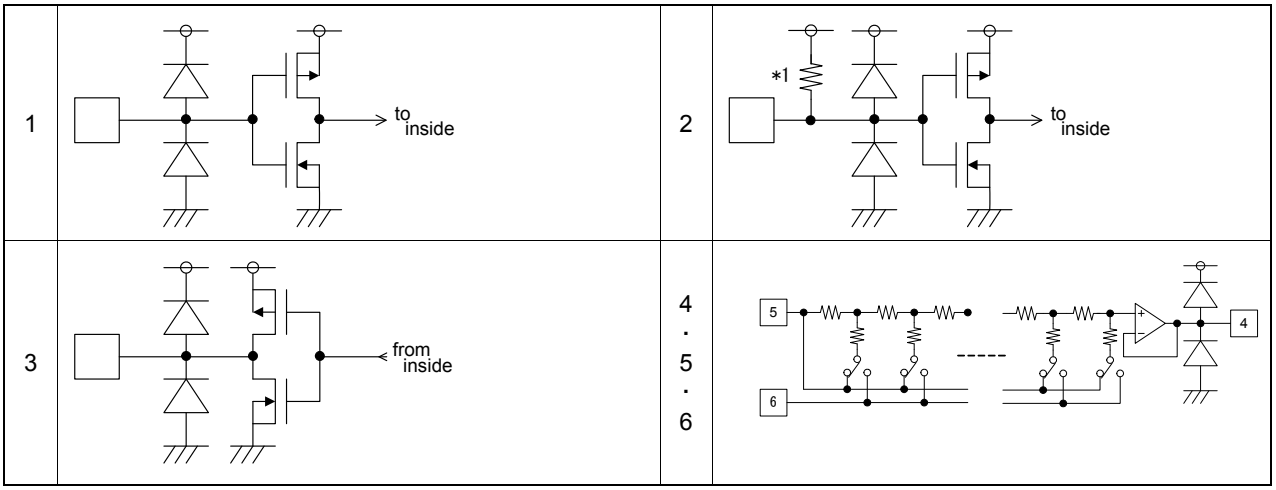


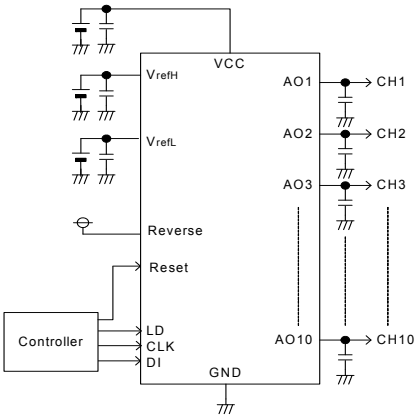

Fig.12 Pull-up built in resistance characteristic

●Equivalent Circuits




*1 25kΩ at Vcc = 5.0V (changes according to voltage supplied)

●Standard Example Application Circuit




●Operation Notes

Ensure that a constant voltage is supplied to each of the 1 ground and 3 power supply terminals.

Insert a bypass capacitor between each power supply terminal and ground in order to prevent deterioration of the D/A conversion accuracy due to ripple and noise signals.

A capacitor should be inserted between the output and ground in order to eliminate jitter and noise.
A capacitance up to 100pF is recommended (including the capacitance of the wire).

This IC can select to decode the 10bit DI data pattern using either LSB first or MSB first, depending on the conditions of the REVERSE terminal. Therefore, be sure to stabilize the REVERSE terminal by leaving it open or short-circuiting VDD (LSB first), or short-circuiting GND (MSB first).

Inserting a capacitor between the RESET terminal and GND and utilizing a time constant enables power ON reset functionality. Furthermore, when inputting the reset signal from the controller, it is possible to fix the output of all channels to Low at the low area of pulse.

●Ordering part number

| B | U | 2 | 5 | 0 | 6 | F | V | - | E | 2 |
|---|---|---|---|---|---|---|---|---|---|---|

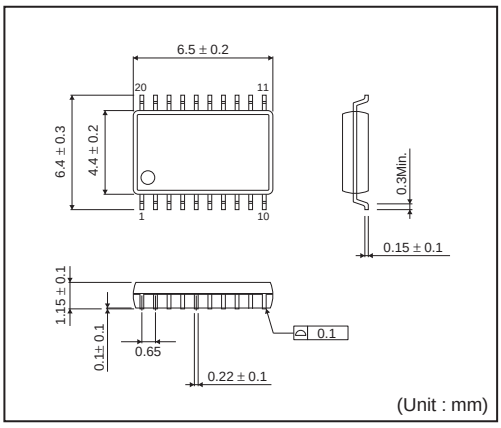
Part No.

Part No.
2506
2505

Package
FV: SSOP-B20

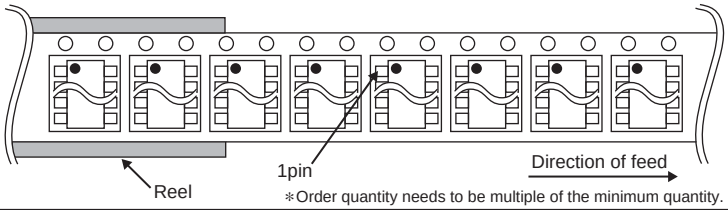
Packaging and forming specification
E2: Embossed tape and reel

**SSOP-B20**




<Tape and Reel information>

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 2500pcs |
| Direction of feed | E2<br>( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand ) |




∗Order quantity needs to be multiple of the minimum quantity.

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The Products are not designed or manufactured to be used with any equipment, device or system which requires an extremely high level of reliability the failure or malfunction of which may result in a direct threat to human life or create a risk of human injury (such as a medical instrument, transportation equipment, aerospace machinery, nuclear-reactor controller, fuel-controller or other safety device). ROHM shall bear no responsibility in any way for use of any of the Products for the above special purposes. If a Product is intended to be used for any such special purpose, please contact a ROHM sales representative before purchasing.

If you intend to export or ship overseas any Product or technology specified herein that may be controlled under the Foreign Exchange and the Foreign Trade Law, you will be required to obtain a license or permit under the Law.

ROHM SEMICONDUCTOR

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