



# DS28DG02

## 2Kb SPI EEPROM with PIO, RTC, Reset, Battery Monitor, and Watchdog

[www.maxim-ic.com](http://www.maxim-ic.com)

### GENERAL DESCRIPTION

The DS28DG02 combines 2Kb (256 x 8) EEPROM with 12 PIO lines, a real-time clock (RTC) and calendar with alarm function, a CPU reset monitor, a battery monitor, and a watchdog. Communication with the device is accomplished with an industry-standard SPI™ interface. The user EEPROM is organized as four blocks of 64 bytes each with single-byte and up to 16-byte page write capability. Additional registers provide access to PIOs and to setup functions. Individual PIO lines can be configured as inputs or outputs. The power-on state of PIOs programmed as outputs is stored in nonvolatile (NV) memory. All PIOs may be reconfigured by the user through the serial interface. The RTC/calendar operates in the 12/24-hour format and automatically corrects for leap years. Battery monitor threshold and watchdog timeout are user-programmable through NV registers. The reset monitor generates a reset to the CPU if the voltage at the V<sub>CC</sub> pin falls below the factory-set limit. The reset output includes a debounce circuit for manual pushbutton reset.

### APPLICATIONS

Asset-Tracking Systems  
Broadband Access Network Equipment  
Patient-Monitoring Systems  
Home Lighting Control Systems  
Holter Heart Monitors

*Typical Operating Circuit appears on page 32.*

*Pin Configuration appears on page 33.*

### ORDERING INFORMATION

PART	TEMP RANGE	V <sub>CC</sub> TRIP	PIN-PACKAGE	PKG CODE
DS28DG02E-3C+	-40°C to +85°C	3.3V -5%	28 TSSOP-EP <sup>*</sup> (4.4mm)	U28E+5
DS28DG02E-3C+T	-40°C to +85°C	3.3V -5%	28 TSSOP-EP <sup>+</sup> T&R	U28E+5
DS28DG02G-3C+	-40°C to +85°C	3.3V -5%	36 TQFN-EP <sup>*</sup> (6mm × 6mm)	T3666+3
DS28DG02G-3C+T	-40°C to +85°C	3.3V -5%	36 TQFN-EP <sup>+</sup> T&R	T3666+3

\*EP = Exposed Paddle.

+Denotes lead-free/RoHS compliant device.

For additional V<sub>CC</sub> monitor trip points or other device options, contact the factory.

**Note:** Registers are capitalized for clarity.

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### FEATURES

- 2Kb (256 x 8) EEPROM Organized in Four 64-Byte Blocks
- Single Byte and Up to 16-Byte EEPROM Write Sequences
- EEPROM Write-Protect Control Pin Protects 1, 2, or All 4 Blocks
- Endurance 200k Cycles per Page at +25°C; 10ms (max) EEPROM Write Cycle
- SPI Serial Interface Supporting Modes (0,0) and (1,1) at Up to 2MHz Clock Frequency
- 12 PIO Lines with LED Drive Capability
- Each PIO is Configured to Input or Output, Open-Drain/Push-Pull on Startup by Stored Value
- All PIOs are Reconfigurable After Startup
- RTC/Calendar/Alarm with BCD Format and Leap-Year Compensation
- RTC Controlled Through 32.768kHz, 12.5pF Crystal or External TCXO
- CPU Reset Through Fast-Response Precision V<sub>CC</sub> Monitor with Hysteresis or Pushbutton
- Battery Monitor 2.5V, 2.25V, 2.0V, 1.75V, -5%
- Watchdog Timer 1.6s, 0.8s, 0.4s, 0.2s (typ)
- Unique Factory-Programmed 64-Bit Device Registration Number
- Operating Range: 2.2V to 5.25V, -40°C to +85°C
- ±4kV IEC 1000-4-2 ESD Protection Level (Except Crystal Pins)
- Available in 28-Lead, 4.4mm TSSOP or 36-Lead 6mm × 6mm QFN Package

**Note:** Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: [www.maxim-ic.com/errata](http://www.maxim-ic.com/errata).

**ABSOLUTE MAXIMUM RATINGS**

Voltage Range on Any Pin Relative to Ground	-0.5V, +6V
Maximum Current SO, ALMZ, RSTZ, WDOZ Pins	±20mA
Maximum Current Each PIO Pin	±50mA
Maximum GND and V <sub>CC</sub> Current	270mA
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See IPC/JEDEC J-STD-020

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device.

**ELECTRICAL CHARACTERISTICS**(T<sub>A</sub> = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V <sub>CC</sub>	Battery monitor off	2.2		5.25	V
		Battery monitor enabled	2.7		5.25	
Battery Voltage	V <sub>BAT</sub>	(Note 1)	1.5	3.0	V <sub>CC</sub>	V
Battery Current (V <sub>BAT</sub> = 3.0V, Note 1)	I <sub>BAT</sub>	RTC oscillator off			2	µA
		RTC oscillator on		0.4	10	
		RTC oscillator on, +25°C			4.7	
Standby Current (Note 2)	I <sub>CCS</sub>	SPI idle, ALMZ, WDOZ, RTSZ high, V <sub>CC</sub> = 5.25V, RTC oscillator on, all PIOs grounded		60	100	µA
Operating Current	I <sub>CCA</sub>	Reading EEPROM at 2 Mbps, ALMZ, WDOZ, RTSZ high, V <sub>CC</sub> = 5.25V, RTC oscillator on, all PIOs grounded		550	800	µA
Programming Current	I <sub>PROG</sub>	V <sub>CC</sub> = 5.25V		600	1000	µA
V <sub>CC</sub> Monitor Trip Point	V <sub>TRIP</sub>	(Note 3)	2.97	3.05	3.14	V
V <sub>CC</sub> Monitor Trip-Point Tolerance	V <sub>TRIP</sub> TOL	+25°C	-1.5		+1.5	%V <sub>TRIP</sub>
		-40°C to +85°C	-2.5		+2.5	
V <sub>CC</sub> Monitor Hysteresis	V <sub>HYST</sub>		0.4	0.5	0.6	%V <sub>TRIP</sub>
Power-Up Wait Time	t <sub>POIP</sub>				60	µs
<b>EEPROM</b>						
Programming Time	t <sub>PROG</sub>				10	ms
Endurance	N <sub>CYCLE</sub>	At +25°C (Notes 4, 5)	200k			—
Data Retention	t <sub>RET</sub>	At +85°C (Notes 5, 6)	40			years
<b>REAL-TIME CLOCK</b>						
Frequency Deviation	Δ <sub>F</sub>	(Notes 5, 7)	-46		+46	PPM
<b>PIO PINS (See Figures 21, 22, 23)</b>						
LOW-Level Output Current at V <sub>OL</sub> = 0.5V (Note 8)	I <sub>OL</sub>	V <sub>CC</sub> = 2.2V	6	9.5		mA
		V <sub>CC</sub> = 3.3V	12.5	22.0		
		V <sub>CC</sub> = 5.25V	19	30		
HIGH-Level Output Current (Note 8)	I <sub>OH</sub>	V <sub>OH</sub> = 2.4V, V <sub>CC</sub> = 3.3V	6.5	11.0		mA
		V <sub>OH</sub> = 4.5V, V <sub>CC</sub> = 5.25V	12.5	18.0		

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOW-Level Input Voltage	$V_{IL}$				0.8	V
HIGH-Level Input Voltage	$V_{IH}$		$0.7 \times V_{CC}$		$V_{CC} + 0.5V$	V
Output Transition Time	$t_{OT}$	Low-current mode (Note 9)			1	$\mu s$
		High-current mode (Note 10)			25	
Power-On Setting Time	$t_{POS}$	High-current mode (Note 11)			25	$\mu s$
PIO Read Setup Time	$t_{PS}$	(Note 5)	100			ns
PIO Read Hold Time	$t_{PH}$	(Note 5)	100			ns
Leakage Current	$I_L$	High impedance, at $V_{CCMAX}$	-1		+1	$\mu A$
<b>RSTZ PIN (Note 12) (See Figures 6, 7)</b>						
LOW-Level Output Voltage	$V_{OL}$	At 4mA sink current			0.3	V
LOW-Level Input Voltage	$V_{IL}$				$0.3 \times V_{CC}$	V
Input Leakage Current	$I_L$		-1		+1	$\mu A$
Minimum $V_{CC}$ for Valid RSTZ	$V_{POR}$	(Notes 5, 13)			2.13	V
RSTZ Pulse Duration	$t_{RST}$		176	328	532	ms
Manual Reset Pulse Width	$t_{MPW}$		1			$\mu s$
Manual Reset Release Threshold	$V_{TRMS}$	(Note 14)		$V_{IL}$		V
Manual Reset Debounce Time	$t_{DEB}$			$t_{RST}$		ms
RSTZ Delay	$t_{DEL}$	$V_{CC}$ falling below $V_{TRIP}$ (Note 15)			90	$\mu s$
<b>ALMZ, WDOZ PINS</b>						
LOW-Level Output Voltage	$V_{OL}$	At 4mA sink current			0.3	V
<b>WDI PIN</b>						
LOW-Level Input Voltage	$V_{IL}$				$0.3 \times V_{CC}$	V
HIGH-Level Input Voltage	$V_{IH}$		$0.7 \times V_{CC}$		$V_{CC} + 0.5V$	V
Input Leakage Current	$I_L$		-1		+1	$\mu A$
Minimum Input Pulse Width	$t_{MPW}$		1			$\mu s$
Watchdog Timeout	$t_{WD}$	User programmable	0.88	1.64	2.66	s
			0.44	0.82	1.33	
			0.22	0.41	0.67	
			0.11	0.20	0.33	
<b>WPZ, SI, SCK, CSZ PINS</b>						
LOW-Level Input Voltage	$V_{IL}$				$0.3 \times V_{CC}$	V
HIGH-Level Input Voltage	$V_{IH}$		$0.7 \times V_{CC}$		$V_{CC} + 0.5V$	V
Input Leakage Current	$I_L$		-1		+1	$\mu A$
<b>SO PIN</b>						
LOW-Level Output Voltage	$V_{OL}$	At 1mA sink current and $V_{CCmin}$			0.2	V
HIGH-Level Output Voltage	$V_{OH}$	At 1mA source current	$0.7 \times V_{CC}$			V
Output Leakage Current	$I_L$	High impedance, at $V_{CCmax}$	-1		+1	$\mu A$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>BATTERY MONITOR (See Figure 8)</b>						
$V_{BAT}$ Trip Point	$V_{BTP}$	Measured with $V_{BAT}$ falling; trip point is user programmable	2.25 2.03 1.80 1.58	2.31 2.08 1.85 1.62	2.38 2.14 1.90 1.66	V
$V_{BAT}$ Monitor Trip-Point Tolerance	$V_{TRIPTOL}$	+25°C -40°C to +85°C	-1.5 -2.5		+1.5 +2.5	% $V_{BTP}$
Battery Test Load Current	$I_{LOAD}$		7.5		20	μA
Battery Test Duration	$t_{BTPW}$	Load applied to battery (Notes 5, 16)		2		s
<b>SPI INTERFACE TIMING (See Figures 9, 10)</b>						
CSZ Setup Time	$t_{CSS}$	(Note 5)	0.4			μs
CSZ Hold Time	$t_{CSH}$	(Note 5)	0.4			μs
CSZ Standby Pulse Width (Note 5)	$t_{CPH}$	Normal communication (Note 17)	0.25 2.0			μs
CSZ to High-Z at SO	$t_{CHZ}$				0.25	μs
SCK Clock Frequency	$f_{CLK}$				2	MHz
Data Setup Time	$t_{DS}$	(Note 5)	50			ns
Data Hold Time	$t_{DH}$	(Note 5)	50			ns
SCK Rise Time	$t_{SCKR}$	(Note 5)			1	μs
SCK Fall Time	$t_{SCKF}$	(Note 5)			1	μs
Output Valid time	$t_V$	(Note 5)	0		120	ns

- Note 1:** If no battery is used, connect the  $V_{BAT}$  pin to  $V_{CC}$ . The RTC is powered by  $V_{BAT}$  if  $V_{CC}$  falls below  $V_{CCmin}$ .
- Note 2:** To the first order, this current is independent of the supply voltage value.
- Note 3:** Nominal values: 3.3V -5%, set at factory. Measured with  $V_{CC}$  falling; for  $V_{CC}$  rising, the actual threshold is  $V_{TRIP} + V_{HYST}$ .
- Note 4:** This specification is valid for each 16-byte memory page.
- Note 5:** Not production tested. Either guaranteed by design (GBD) or guaranteed by a reliability study (EEPROM lifetime parameters).
- Note 6:** EEPROM writes can become nonfunctional after the data-retention time is exceeded. Long-time storage at elevated temperatures is not recommended; the device can lose its write capability after 10 years at +125°C or 40 years at +85°C.
- Note 7:** Valid with 32KHz crystal, 12.5pF,  $ESR \leq 45k\Omega$ , +25°C.
- Note 8:** Total PIO sink and source currents through all PIO pins must be externally limited to less than the absolute maximum rating of 270mA minus 1.5mA for EEPROM programming and SPI communication. Exceeding the absolute maximum rating can cause damage.
- Note 9:** Assumes the configuration of the system and the part is such that changing GOV<i> (0 ≤ i ≤ 11) between 'b1 and 'b0 switches between sourcing no current and sinking the absolute maximum current at the PIO<i> pin. The limit refers to the switching time between sinking 20% of the DC current and 80% of the DC current. The same is true for changing between 'b0 and 'b1 causing the part to switch from sinking no current to sourcing the absolute maximum current at the PIO<i> pin.
- Note 10:** Each output pin transitions in 1μs with a pause of 1μs before the next pin transitions.
- Note 11:** All PIO are tri-stated at beginning of reset prior to setting to power-on values.
- Note 12:** If the part has battery power (normal case) the active pulldown of RSTZ is supported by the battery.
- Note 13:** If  $V_{BAT}$  is tied to  $V_{CC}$  (no battery supply) the state of the RSTZ pulldown transistor is not guaranteed when  $V_{CC}$  falls below  $V_{POR}$ .
- Note 14:** Threshold refers to the manual reset function obtained by forcing RSTZ low.
- Note 15:** Transient response to a step on  $V_{CC}$  from above  $V_{TRIP}$  down to ( $V_{TRIP} - 1mV$ ). Glitches on  $V_{CC}$  that are shorter than  $t_{DELmin}$  are guaranteed to be suppressed, regardless of their amplitude. Glitches on  $V_{CC}$  that are longer than  $t_{DELmax}$  are guaranteed not to be suppressed. This parameter is tested at high  $V_{CC}$  and guaranteed by design at low.
- Note 16:** If enabled, this test takes place every hour on the hour. The battery voltage is compared to  $V_{BTP}$  during the second half of the  $t_{BTPW}$  window. The timing is controlled by the RTC.
- Note 17:** Extended duration applies to the following cases:
- 1) Aborted WREN, WRDI, RDSR, and WRSR command.
  - 2) WRITE command aborted before transmitting the first complete data byte after command and address.
  - 3) READ command aborted before reading the first complete data byte after command and address.
  - 4) Read aborted before the end of a byte.

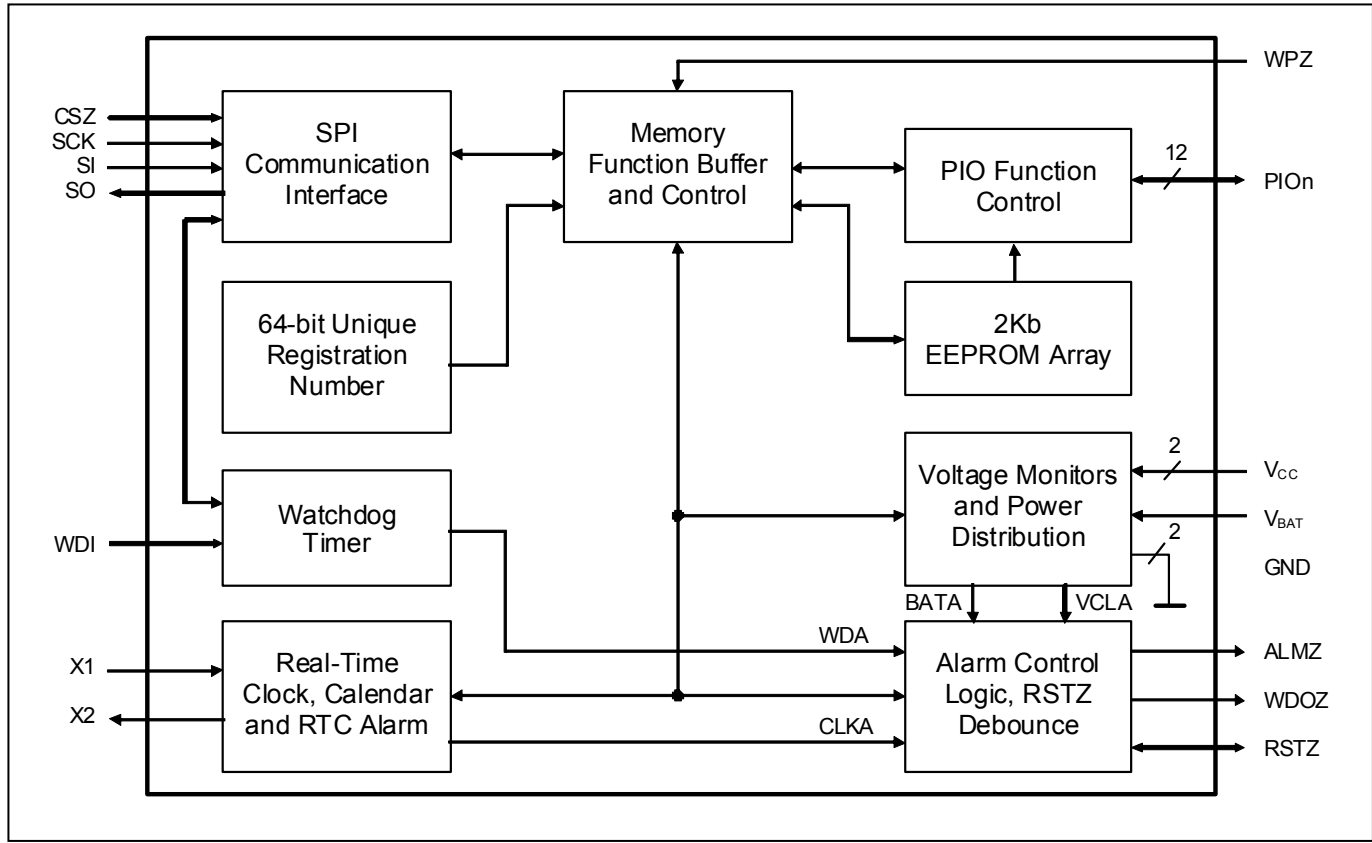
## PIN DESCRIPTION

NAME	PIN		FUNCTION
	TSSOP28	TQFN36	
X1	1	33	<b>32.768kHz Crystal Connection 1 or 32.768kHz Input from TCXO</b>
X2	2	34	<b>32.768kHz Crystal Connection 2</b>
RSTZ	3	36	<b>Open-Drain Output Pin (Active Low)</b> for $V_{CC}$ power-fail reset, watchdog alarm, and <b>Manual Reset Input</b> . See <i>Multifunction Control/Setup Register</i> description for more information.
WDI	4	2	<b>Watchdog Input Pin (Active High)</b> . See <i>Multifunction Control/Setup Register</i> description at address 134h for more information.
WDOZ	5	3	<b>Open-Drain Output Pin (Active Low)</b> for (user-choice) watchdog alarm. See <i>Multifunction Control/Setup Register</i> description for more information.
WPZ	6	4	<b>Hardware Write-Protect Input Pin (Active Low)</b> . See the <i>SPI Interface</i> description for more information.
PIO0	7	5	<b>PIO Line #0</b>
PIO4	8	6	<b>PIO Line #4</b>
PIO8	9	7	<b>PIO Line #8</b>
GND	10, 19	9, 19	<b>Ground Supply</b>
PIO10	11	10	<b>PIO Line #10</b>
PIO6	12	11	<b>PIO Line #6</b>
PIO2	13	12	<b>PIO Line #2</b>
$V_{CC}$	14, 15	13, 15	<b>Power Supply Input</b>
PIO3	16	16	<b>PIO Line #3</b>
PIO7	17	17	<b>PIO Line #7</b>
PIO11	18	18	<b>PIO Line #11</b>
PIO9	20	21	<b>PIO Line #9</b>
PIO5	21	22	<b>PIO Line #5</b>
PIO1	22	23	<b>PIO Line #1</b>
ALMZ	23	24	<b>Open-Drain Output Pin (Active Low)</b> for RTC, battery monitor, and (user-choice) watchdog alarms. See the <i>Multifunction Control/Setup Register</i> description for more information.
SO	24	25	<b>SPI Serial Data Output (tristate)</b>
SI	25	26	<b>SPI Serial Data Input</b>
SCK	26	28	<b>SPI Serial Clock Input</b>
CSZ	27	30	<b>Chip Select Input (Active Low)</b>
$V_{BAT}$	28	31	<b>Backup Battery Supply</b> for RTC and RSTZ support.
N.C.	—	1, 8, 14, 20, 27, 29, 32, 35	<b>No Connection</b>
GND	EP	EP	<b>Exposed Paddle</b> . Solder evenly to the board's ground plane for proper operation. See <a href="#">Application Note 3273</a> for additional information.

## OVERVIEW

The DS28DG02 features 2Kb of EEPROM, 12 bidirectional PIO channels, an RTC with calendar and alarm function, a watchdog timer, two voltage monitors with precision trip points, and three alarm/reset outputs. Each DS28DG02 has its own unique registration number, which serves as identification of the product the device is embedded in. All these resources are accessed through a serial SPI interface, as shown in the block diagram in Figure 1. The SPI interface automatically adjusts to SPI modes (0,0) and (1,1). The  $V_{CC}$  trip point, which controls the power-fail reset output (RSTZ pin), is set at the factory. The user can set the battery monitor threshold and the watchdog time-out through software. The RTC uses the common BCD format for time, calendar and day of the week. The device can be programmed to generate an RTC alarm every second, minute, hour, or day and once a week or once a month at a user-defined time. RTC, watchdog, and battery alarm can be individually enabled.

Figure 1. Block Diagram



The PIO configuration and setup of RTC/calendar with alarm are part of the *Detailed Register Description*. This section also includes specifics of the Multifunction Control/Setup register, which enables/disables several device functions, and the Alarm/Status register. For detailed information on the operation of the V<sub>CC</sub> monitor/power-fail reset and the battery monitor see the *Monitoring Functions* section. The *SPI Interface* description explains the communication protocol for memory and register access and the use of the watchdog function. The *PIO Read/Write Access* section illustrates the behavior of the PIOs, in particular the address generation and timing in low- and high-current mode.

The DS28DG02 memory map (Figure 2) begins with 256 bytes of general-purpose user EEPROM, organized as four blocks of 64 bytes. Additional EEPROM is set aside to store power-on defaults for PIO state (high, low, in output mode), data direction (in, out), read-inversion (true, false), port output type (push-pull, open-drain), and output mode (high current, low current). Once powered up, the PIO settings can be overwritten through SRAM registers without affecting the power-on defaults. PIO state, direction, and read-inversion can be set for individual ports. The output type is set for groups of four PIOs and the selected output mode applies to all PIOs in output mode. The RTC/calendar, associated Alarm registers and the Multifunction Control/Status registers are kept nonvolatile through battery backup. Write-protection, if enabled, is available for all four EEPROM blocks, blocks 2 and 3 only, or block 3 only and for all writeable registers from address 120h and higher.

**Figure 2. Memory Map**

ADDRESS	TYPE	ACCESS	DESCRIPTION
000h to 03Fh	EEPROM	R/W	User memory block 0.
040h to 07Fh	EEPROM	R/W	User memory block 1.
080h to 0BFh	EEPROM	R/W	User memory block 2.
0C0h to 0FFh	EEPROM	R/W	User memory block 3.
100h to 109h	—	—	Reserved, contents undefined.
10Ah	EEPROM	R/W	Power-on default for PIO output state (PIO0 to PIO7).
10Bh	EEPROM	R/W	Power-on default for PIO output state (PIO8 to PIO11).
10Ch	EEPROM	R/W	Power-on default for PIO direction (PIO0 to PIO7).
10Dh	EEPROM	R/W	Power-on default for PIO direction (PIO8 to PIO11).
10Eh	EEPROM	R/W	Power-on default for PIO read-inversion (PIO0 to PIO7).
10Fh	EEPROM	R/W	Power-on default for PIO read-inversion (PIO8 to PIO11), PIO output type (PIO0 to PIO11 in groups of 4 PIOs), PIO output mode (same mode for all PIOs).
110h to 117h	—	—	Reserved, contents is undefined.
118h to 11Fh	ROM	R	64-bit unique registration number.
120h	SRAM	R/W	PIO output state (PIO0 to PIO7).
121h	SRAM	R/W	PIO output state (PIO8 to PIO11).
122h	SRAM	R/W	PIO direction (PIO0 to PIO7).
123h	SRAM	R/W	PIO direction (PIO8 to PIO11).
124h	SRAM	R/W	PIO read-inversion (PIO0 to PIO7).
125h	SRAM	R/W	PIO read-inversion (PIO8 to PIO11), PIO output type (PIO0 to PIO11 in groups of 4 PIOs), PIO output mode (same mode for all PIOs).
126h	—	R	PIO read access (PIO0 to PIO7).
127h	—	R	PIO read access (PIO8 to PIO11).
128h	—	—	Reserved, contents undefined.
129h to 12Fh	NV SRAM	R/W	RTC and calendar.
130h to 133h	NV SRAM	R/W	RTC alarm.
134h	NV SRAM	R/W	Multifunction control/setup register.
135h	NV SRAM	R/Clear	Alarm and status register.
136h and above	—	—	Reserved, contents undefined.

## DETAILED REGISTER DESCRIPTIONS

### Power-On Default for PIO Output State

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
10Ah	POV7	POV6	POV5	POV4	POV3	POV2	POV1	POV0
10Bh	X	X	X	X	POV11	POV10	POV9	POV8

There is general read and write access to these addresses. Factory default: 10Ah: FFh; 10Bh: 0Fh. The contents of this register are automatically transferred to address 120h/121h when the device powers up.

BIT DESCRIPTION	BIT(S)	DEFINITION
POVn: PIO Power-On Default State	—	Power-on default output <b>state</b> of PIO0 to PIO11. POV0 applies to PIO0, etc.
X: (Not Assigned)	—	Reserved for future use.

### Power-On Default for PIO Direction

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
10Ch	POD7	POD6	POD5	POD4	POD3	POD2	POD1	POD0
10Dh	X	X	X	X	POD11	POD10	POD9	POD8

There is general read and write access to these addresses. Factory default: 10Ch: FFh; 10Dh: 0Fh. The contents of this register are automatically transferred to address 122h/123h when the device powers up.

BIT DESCRIPTION	BIT(S)	DEFINITION
PODn: PIO Power-On Default Direction	—	Power-on default direction of PIO0 to PIO11. POD0 applies to PIO0, etc. <b>Legend:</b> 0 → output; 1 → input
X: (Not Assigned)	—	Reserved for future use.

### Power-On Default for PIO Read Inversion (PIO0 to PIO7)

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
10Eh	PIM7	PIM6	PIM5	PIM4	PIM3	PIM2	PIM1	PIM0

There is general read and write access to this address. Factory default: 00h. The contents of this register are automatically transferred to address 124h when the device powers up.

BIT DESCRIPTION	BIT(S)	DEFINITION
PIMn: PIO Power-On Default Read-Inversion	—	Power-on default state of the read-inversion bit of PIO0 to PIO7. PIM0 applies to PIO0, etc. <b>Legend:</b> 0 → no inversion; 1 → inversion



**Power-On Default for PIO Read Inversion (PIO8 to PIO11), PIO Output Type and Output Mode**

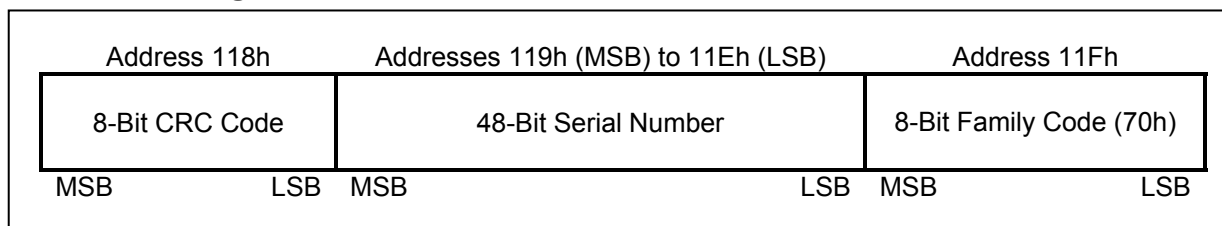
ADDR	b7	b6	b5	b4	b3	b2	b1	b0
10Fh	POTM	POT3	POT2	POT1	PIM11	PIM10	PIM9	PIM8

There is general read and write access to this address. Factory default: 80h. The contents of this register are automatically transferred to address 125h when the device powers up.

BIT DESCRIPTION	BIT(S)	DEFINITION
PIMn: PIO Power-On Default Read-Inversion	b0 to b3	Power-on default state of the read-inversion bit of PIO8 to PIO11. PIM8 applies to PIO8, etc. <b>Legend:</b> 0 → no inversion; 1 → inversion
POT1: Power-On Default Output Type	b4	Power-on default output type of PIO0 to PIO3; <b>Legend:</b> 0 → push-pull; 1 → open drain
POT2: Power-On Default Output Type	b5	Power-on default output type of PIO4 to PIO7; <b>Legend:</b> 0 → push-pull; 1 → open drain
POT3: Power-On Default Output Type	b6	Power-on default output type of PIO8 to PIO11; <b>Legend:</b> 0 → push-pull; 1 → open drain
POTM: Power-On Default Output Mode	b7	Power-on default output mode of PIO0 to PIO11; <b>Legend:</b> 0 → low-current, simultaneous switching; 1 → high-current, sequential switching

**Unique Registration Number (118h to 11Fh)**

Each DS28DG02 has a unique registration number that is 64 bits long, as shown in Figure 3. The registration number begins with the Cyclic Redundancy Check (CRC) of the subsequent 56 bits at address 118h followed by the 48-bit serial number (MS-byte at the lower address) and ends at address 11Fh with the family code. This CRC is generated using the a polynomial  $X^8 + X^5 + X^4 + 1$ . Additional information about CRCs is available in *Application Note 27*.

**Figure 3. 64-Bit Registration Number****PIO Output State**

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
120h	OV7	OV6	OV5	OV4	OV3	OV2	OV1	OV0
121h	X	X	X	X	OV11	OV10	OV9	OV8

There is general read and write access to these addresses. These registers are automatically loaded with data from address 10Ah/10Bh when the device powers up.

BIT DESCRIPTION	BIT(S)	DEFINITION
OVn: PIO Output State	—	Output state of PIO0 to PIO11. OV0 applies to PIO0, etc. <b>Legend:</b> 0 → LOW; 1 → HIGH if PIO direction is output
X: (Not Assigned)	—	Reserved for future use.

**PIO Direction**

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
122h	DIR7	DIR6	DIR5	DIR4	DIR3	DIR2	DIR1	DIR0
123h	X	X	X	X	DIR11	DIR10	DIR9	DIR8

There is general read and write access to these addresses. These registers are automatically loaded with data from address 10Ch/10Dh when the device powers up.

BIT DESCRIPTION	BIT(S)	DEFINITION
DIRn: PIO Direction	—	Direction of PIO0 to PIO11. DIR0 applies to PIO0, etc. <b>Legend:</b> 0 → output; 1 → input
X: (Not Assigned)	—	Reserved for future use.

**PIO Read Inversion (PIO0 to PIO7)**

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
124h	IMSK7	IMSK6	IMSK5	IMSK4	IMSK3	IMSK2	IMSK1	IMSK0

There is general read and write access to this address. This register is automatically loaded with data from address 10Eh when the device powers up.

BIT DESCRIPTION	BIT(S)	DEFINITION
IMSKn: PIO Read-Inversion	—	Read-inversion bit of PIO0 to PIO7. IMSK0 applies to PIO0, etc. <b>Legend:</b> 0 → no inversion; 1 → inversion

**PIO Read Inversion (PIO8 to PIO11), PIO Output Type and Output Mode**

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
125h	OTM	OT3	OT2	OT1	IMSK11	IMSK10	IMSK9	IMSK8

There is general read and write access to this address. This register is automatically loaded with data from address 10Fh when the device powers up.

BIT DESCRIPTION	BIT(S)	DEFINITION
IMSKn: PIO Read-Inversion	b0 to b3	Read-inversion bit of PIO8 to PIO11. PIM8 applies to PIO8, etc. <b>Legend:</b> 0 → no inversion; 1 → inversion
OT1: Output Type	b4	Output type of PIO0 to PIO3; <b>Legend:</b> 0 → push-pull; 1 → open drain
OT2: Output Type	b5	Output type of PIO4 to PIO7; <b>Legend:</b> 0 → push-pull; 1 → open drain
OT3: Output Type	b6	Output type of PIO8 to PIO11; <b>Legend:</b> 0 → push-pull; 1 → open drain
OTM: Output Mode	b7	Output mode of PIO0 to PIO11; <b>Legend:</b> 0 → low-current, simultaneous switching; 1 → high-current, sequential switching

**PIO Read Access**

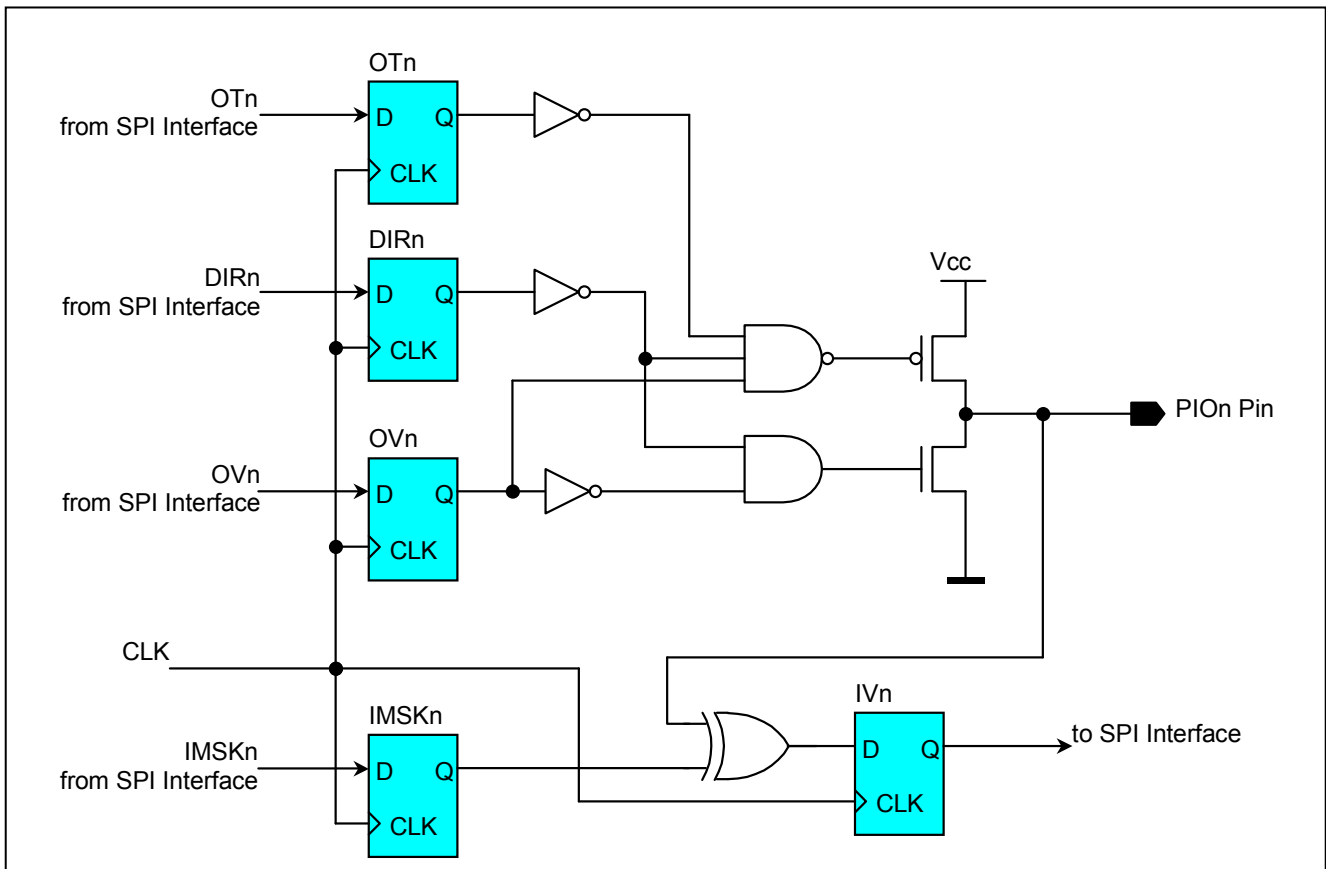
ADDR	b7	b6	b5	b4	b3	b2	b1	b0
126h	IV7	IV6	IV5	IV4	IV3	IV2	IV1	IV0
127h	0	0	0	0	IV11	IV10	IV9	IV8

There is only read access to these addresses. Bits 4 to 7 of address 127h always read 0. Read access is functional for all PIOs, regardless of their direction setting. Reported is the logic state of the pin, which may be different from what the PIO output value register implies.

BIT DESCRIPTION	BIT(S)	DEFINITION
IVn: Input Value of PIO <sub>n</sub>	—	Logic state read from PIO0 to PIO11 pins. IV0 applies to PIO0, etc. <b>Legend:</b> IV <sub>n</sub> = PIO <sub>n</sub> XOR'ed with IMSK <sub>n</sub>

Figure 4 shows a simplified schematic of a PIO. The flip flops are accessed through the PIO Output State (OV<sub>n</sub>) and Read Access (IV<sub>n</sub>) registers and memory addresses 122h to 125 (DIR<sub>n</sub>, IMSK<sub>n</sub>, OT<sub>n</sub>). They are initialized at power-up or during Refresh (see the *SPI Interface Description*) according to the data stored at memory addresses 10Ah to 10Fh. When a PIO is configured as input, the PIO output is tri-stated (high impedance). When a PIO is configured as output, the PIO input is the same as the output state XORed with the corresponding read inversion bit. The differences of the PIO behavior in low current and high current mode are explained in the *PIO Read/Write Access* section near the end of this document.

**Figure 4. PIO Simplified Schematic**



**RTC and Calendar Registers**

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
129h	0	10 Seconds			Single Seconds			
12Ah	0	10 Minutes			Single Minutes			
12Bh	0	12/24	10hrs	10hrs	Single Hours			
			A/P					
12Ch	0	0	0	0	0	Day of Week		
12Dh	0	0	10 Date		Single Date			
12Eh	0	0	0	Single Months				
12Fh	10 Years				Single Years			

There is general read and write access to these addresses. Bits shown as 0 cannot be written to 1. The RTC and calendar registers are reset to 00h when the battery voltage ramps up. Writes take effect immediately. To prevent unexpected increments during write access, first update the seconds; this creates a 1s window to finish updating the RTC/Calendar registers without any carryover from the Seconds register. Whenever the DS28DG02 receives a SPI Read command, the RTC and Calendar registers are copied to a buffer. When during a read access the address counter points to the RTC/Calendar registers, data from the buffer is transmitted. To obtain most accurate RTC data, start reading at the Seconds register.

The number representation of the RTC/Calendar registers is BCD (binary-coded decimal). The RTC can run in the 12-hour AM/PM and the 24-hour mode. The "12/24" bit (bit 6 of address 12Bh) defines the mode. For 12-hour AM/PM mode, set this bit to 1; bit 5 of address 12Bh then indicates AM (0b) or PM (1b). In the 24-hour mode, bit 5 and bit 4 together indicate the multiple of 10 hours. The Day of Week register counts from 1 to 7. The calendar logic is designed to automatically compensate for leap years. For every year value that is either 00 or a multiple of 4 the device will add a 29th of February. This will work correctly up to (but not including) the year 2100.

**RTC Alarm Registers**

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
130h	AM1	10 Seconds			Single Seconds			
131h	AM2	10 Minutes			Single Minutes			
132h	AM3	12/24	10hrs	10hrs	Single Hours			
			A/P					
133h	AM4	DY/DT	0	0	0	Day of Week		
			10 Date		Single Date			

There is general read and write access to these addresses. Bits shown as 0 cannot be written to 1. The RTC Alarm registers are reset to 00h when the battery voltage ramps up. To generate an alarm, there must be a match between Alarm registers and RTC registers. Alarm register addresses 130h to 132h correspond to RTC register addresses 129h to 12Bh; bits 6:0 participate in the comparison. The lower 6 bits of register address 133h correspond to 12Ch if DY/DT is 1 and to 12Dh if DY/DT is 0; the upper 2 bits of this register do not participate in the comparison. The control bits AM1, AM2, AM3, and AM4 determine the frequency of the alarm, as shown in Table 1. When the alarm occurs, the CLKA bit of the Alarm and Status register at address 135h changes to 1. The RTC must be running for the device to generate RTC alarms (OSCE at address 134h = 1).

**Table 1. Alarm Frequency Control**

DY/DT	AM4	AM3	AM2	AM1	ALARM OCCURRENCE
X	X	X	X	1	Every second
X	X	X	1	0	Every minute, when the seconds match
X	X	1	0	0	Every hour, when minutes and seconds match
X	1	0	0	0	Every day, when hours, minutes, and seconds match
1	0	0	0	0	Every week, when day, hours, minutes, and seconds match
0	0	0	0	0	Every month, when date, hours, minutes, and seconds match

**Multifunction Control/Setup Register**

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
134h	0	BME	BTRP		WDOS	WDE	OSCE	CAE

There is general read and write access to this address. Bit 7 always reads 0; it cannot be written to 1. This register is reset to 00h when the battery voltage ramps up. See Figure 5 for the use of the CAE, WDE, WDOS, and BME bits in the generation of the ALMZ, RSTZ, and WDOZ signals.

BIT DESCRIPTION	BIT(S)	DEFINITION
CAE: Clock Alarm Enable	b0	Enable/disable control of the RTC/Calendar alarm. <b>Legend:</b> 0 → disabled (power-on default); 1 → enabled
OSCE: RTC Oscillator Enable	b1	Run/halt control of the RTC's 32KHz oscillator <b>Legend:</b> 0 → halted (power-on default); 1 → running
WDE: Watchdog Enable	b2	Enable/disable control of the watchdog and its alarm. <b>Legend:</b> 0 → disabled (power-on default); 1 → enabled The watchdog timer is reset by changing WDE from 0 to 1, $V_{CC}$ ramp up (Power-on reset) or applying a positive pulse at the WDI pin.
WDOS: Watchdog Output Selection	b3	Pin selection for watchdog alarm signaling. <b>Legend:</b> 0 → WDOZ pin (power-on default); 1 → ALMZ pin
BTRP: Battery Monitor Trip Point	b5:b4	Selection of the <b>nominal</b> Battery Monitor Trip Point voltage. <b>Legend:</b> 00b → 1.75V (power-on default); 01b → 2.00V; 10b → 2.25V; 11b → 2.50V
BME: Battery Monitor Enable	b6	Enable/disable control of the Battery Monitor and its alarm. <b>Legend:</b> 0 → disabled (power-on default); 1 → enabled The battery test takes place a) after BME changes to 1, b) after $V_{CC}$ ramps up, c) every hour on the hour. The RTC must be running (OSCE = 1) for the battery monitor to function.

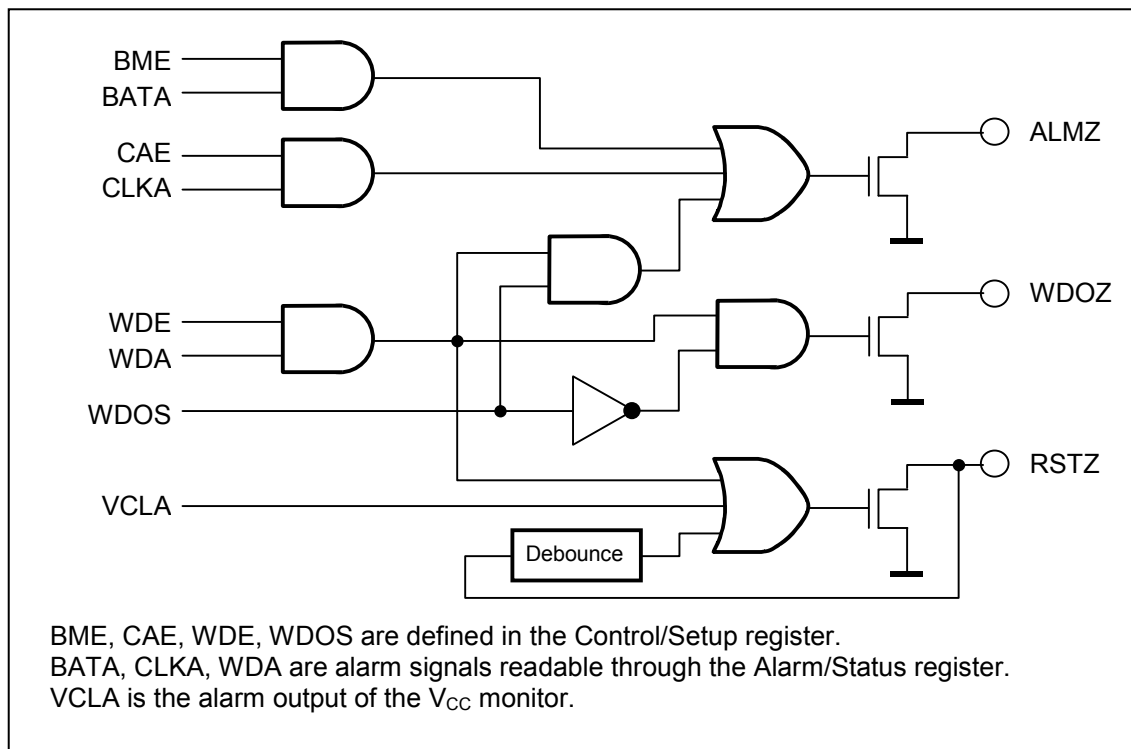
**Alarm and Status Register**

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
135h	0	BATA	WPZV	POR	BOR	CLKA	WDA	RST

There is general read access to this address; writing clears all bits to 0. Bit 7 always reads 0. See Figure 5 for the use of the CLKA, WDA, and BATA bits in the generation of the ALMZ, RSTZ, and WDOZ signals.

BIT DESCRIPTION	BIT(S)	DEFINITION
RST: Reset Flag	b0	RSTZ pin activity indicator; set whenever there is a pulse at RSTZ; cleared by writing to the Alarm and Status register. V <sub>CC</sub> ramp up: 1; V <sub>BAT</sub> attach: 0
WDA: Watchdog Alarm	b1	Watchdog Alarm indicator; set whenever the watchdog is enabled AND the watchdog timer expires; cleared by writing to the Alarm and Status register. V <sub>CC</sub> ramp up: 0; V <sub>BAT</sub> attach: 0
CLKA: Clock Alarm	b2	RTC/Calendar Alarm indicator; set whenever the clock alarm is enabled AND RTC and RTC Alarm register match; cleared by writing to the Alarm and Status register. V <sub>CC</sub> ramp up: 0; V <sub>BAT</sub> attach: 0
BOR: Battery-On Reset Flag	b3	Battery attach indicator; set whenever the voltage at V <sub>BAT</sub> ramps up above V <sub>BATmin</sub> ; cleared by writing to the Alarm and Status register. V <sub>CC</sub> ramp up: not affected; V <sub>BAT</sub> attach: 1
POR: Power-On Reset Flag	b4	Power-On Reset indicator; set whenever the voltage at V <sub>CC</sub> ramps up above V <sub>CCmin</sub> ; cleared by writing to the Alarm and Status register. V <sub>CC</sub> ramp up: 1; V <sub>BAT</sub> attach: 0
WPZV: Hardware Write Protect Value	b5	WPZ pin state readout; reports the logic state at the WPZ pin; V <sub>CC</sub> ramp up: WPZ pin state; V <sub>BAT</sub> attach: not affected.
BATA: Battery Alarm	b6	Low Battery indicator; set whenever the battery alarm is enabled AND if, during a battery test, V <sub>BAT</sub> is below the selected V <sub>BAT</sub> trip point; cleared by writing to the Alarm and Status register. V <sub>CC</sub> ramp up: battery test if BME = 1; V <sub>BAT</sub> attach: 0

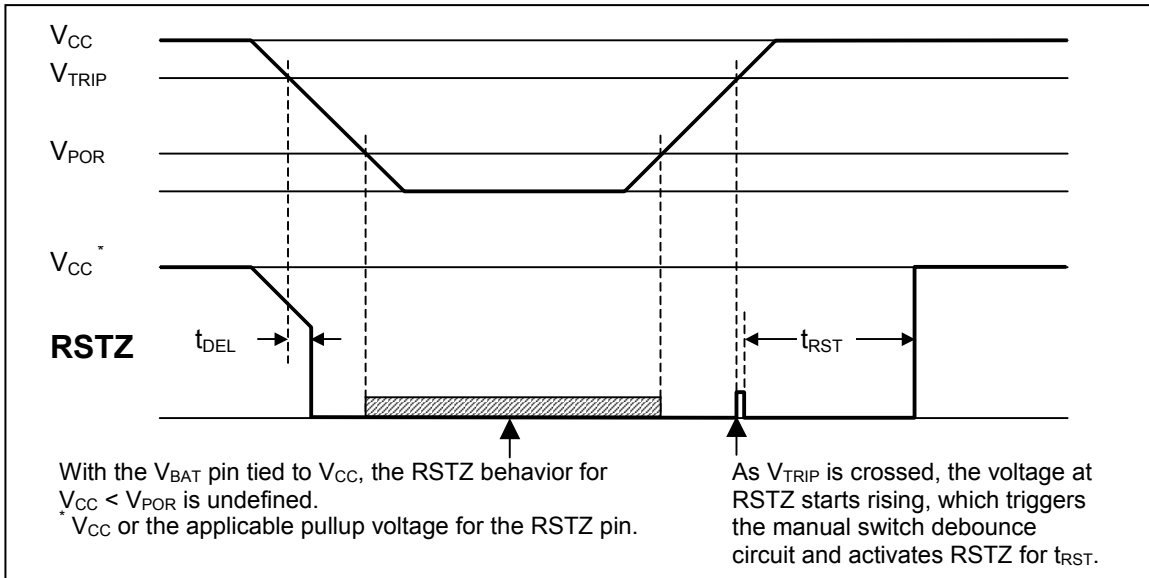
Figure 5. ALMZ, WDOZ, and RSTZ Generation



## MONITORING FUNCTIONS

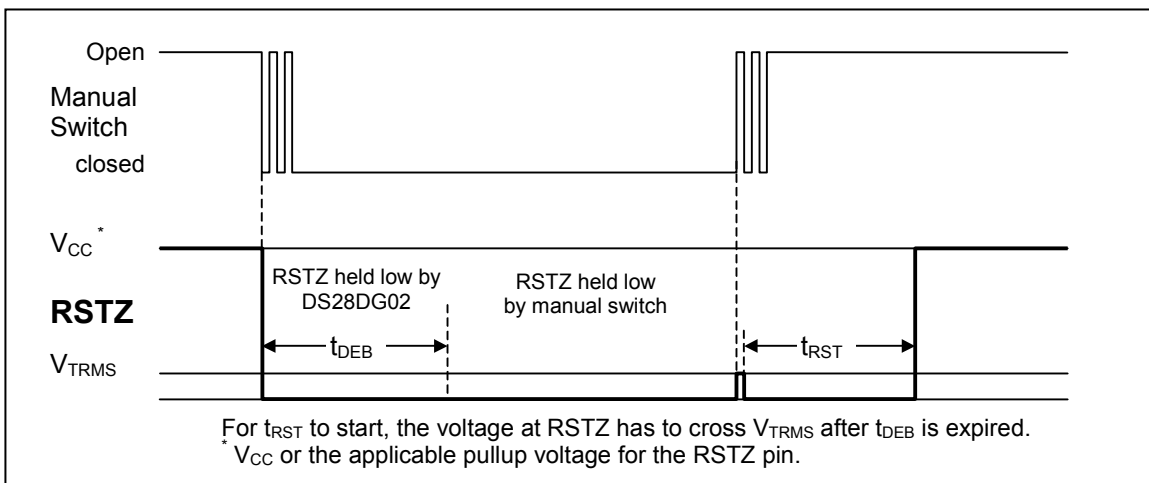
The DS28DG02 has two voltage monitors: one for the  $V_{CC}$  supply voltage and another one for the battery that supplies the RTC and associated registers if  $V_{CC}$  is switched off. If  $V_{CC}$  falls below the  $V_{TRIP}$  threshold the  $V_{CC}$  monitor activates the open-drain RSTZ output, as shown in Figure 6. There is a delay of  $t_{DEL}$  between crossing the trip point and RSTZ going LOW. As long as  $V_{CC}$  is above  $V_{POR}$  or the device has a functioning battery backup, the logic level at RSTZ does not exceed  $V_{OLmax}$ . Without battery support, the state of the RSTZ output is undefined for  $V_{CC}$  values below  $V_{POR}$ . When  $V_{CC}$  ramps up, RSTZ remains at LOW until the  $V_{TRIP}$  threshold is reached. As  $V_{TRIP}$  is crossed, the voltage at RSTZ rises until it reaches  $V_{TRMS}$ , the manual reset release threshold. This activates the debounce circuit, which holds RSTZ low for  $t_{RST}$ . After  $t_{RST}$  is expired, the voltage at RSTZ ramps up to the value of the applied pullup voltage.

**Figure 6. RSTZ Power-Fail Reset**



The RSTZ pin is internally connected to a debounce circuit, which allows using a manually operated switch to generate a reset signal. Figure 7 illustrates the timing of the manual reset. As the switch closes, it forces the voltage at RSTZ to fall below  $V_{ILmax}$ , which triggers the debounce circuit. Now the voltage at RSTZ is held at logic LOW by both, the manual switch and the debounce circuit. When the manual switch is opened or  $t_{DEB}$  is over, (whichever occurs later) the voltage at RSTZ rises until it reaches  $V_{TRMS}$ . This again triggers the debounce circuit, which holds RSTZ low for  $t_{RST}$ , after which the voltage at RSTZ ramps up to the pullup voltage. The minimum LOW time of a manually generated reset is  $t_{DEB} + t_{RST}$ .

**Figure 7. RSTZ Manual Switch Debounce**

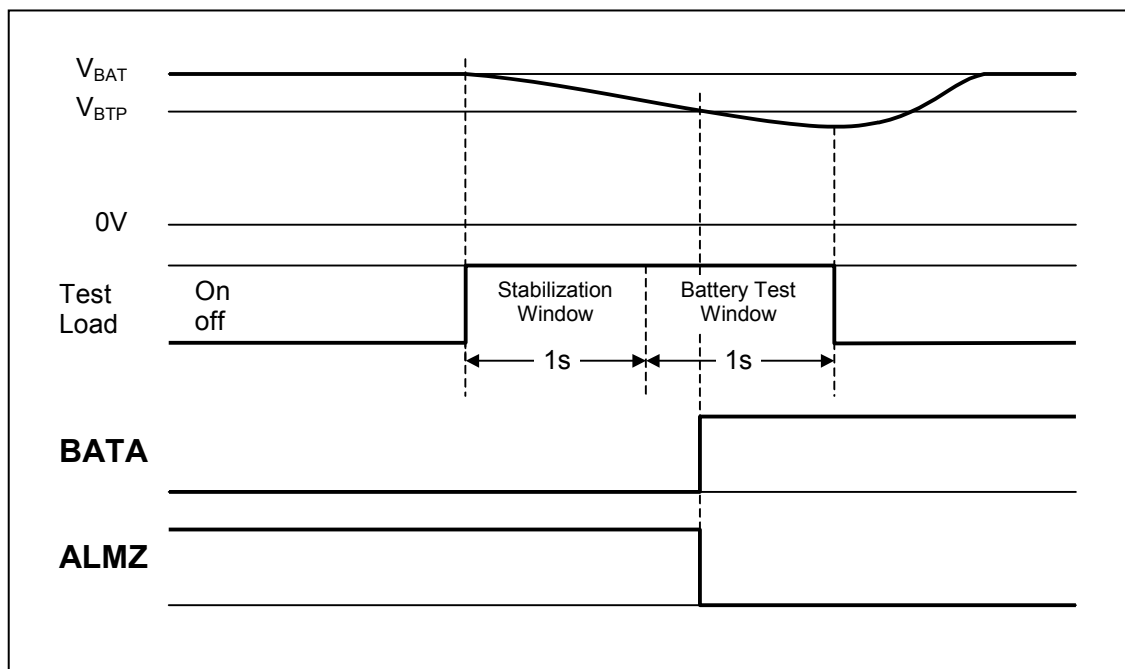


In contrast to the  $V_{CC}$  monitor, the battery monitor is active only for two seconds per hour, and only if it is enabled through the BME bit in the Multifunction Control/Setup register. In addition to this, the DS28DG02 must have sufficient  $V_{CC}$  power and the RTC must be running ( $OSCE = 1$ ). The battery test takes place a) immediately after enabling the battery monitor, and, if the battery monitor is enabled, b) every hour on the full hour, and c) immediately after  $V_{CC}$  ramps up above  $V_{POR}$ . Figure 8 shows the details.

The battery test procedure begins with the DS28DG02 internally connecting the test load to the  $V_{BAT}$  pin. If the battery is near the end of its lifetime, this extra load causes the battery voltage to fall below  $V_{BTP}$ , the Battery Trip Point. After the stabilization window is over, the actual comparison of the battery voltage to the battery trip point takes place. If at the beginning of or during the battery test window the battery voltage falls below  $V_{BTP}$ , the battery alarm flag BATA in the Alarm and Status register is set, which in turn activates the ALMZ output. The BATA flag is cleared by a) replacing the battery, or b) by writing to the Alarm and Status register. The BATA flag is not cleared if a subsequent battery test, e.g., one hour later or after power-cycling the DS28DG02, determines that the battery voltage is above  $V_{BTP}$ . Note that replacing the battery resets the RTC and clears the Multifunction Control/Setup register.

Battery monitoring is only useful when performed regularly. Equipment that is powered-down for excessively long periods can completely drain its battery without receiving any advanced warning. To prevent such an occurrence, equipment using the battery-monitoring feature should be switched on periodically, e.g., once a month, to perform a battery test.

**Figure 8. Battery Monitor Operation**





## SPI INTERFACE

The DS28DG02 is a slave device that communicates with its master, a microcontroller, through the serial SPI interface. This interface uses the signals CSZ (chip select), SCK (bit transfer clock), SI (serial input), and SO (serial output). Common to SPI devices is a WPZ input (write protect), which can protect the nonvolatile bits in the SPI Status register from inadvertent changes.

### Pin Description

#### Chip Select (CSZ)

A low level on the CSZ pin selects the device; a high level deselects the device. A low-to-high transition on CSZ after a valid EEPROM write sequence initiates an internal programming cycle. A programming cycle already initiated or in progress will be completed, regardless of the CSZ input signal. When the device is deselected, SO goes to the high-impedance state, allowing multiple parts to share the same SPI bus. After powerup, a low level on CSZ is required prior to any sequence being initiated. The CSZ pin must remain low while the DS28DG02 is receiving or transmitting data.

#### Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the DS28DG02. Instructions, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

#### Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses, and data. Data is latched on the rising edge of the serial clock.

#### Serial Output (SO)

The SO pin is used to transfer data out of the DS28DG02. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

#### Write Protect (WPZ)

The WPZ pin, if enabled, prevents writes to the nonvolatile bits in the SPI Status register. As factory default, the WPZ pin function is disabled. This allows the user to install the DS28DG02 in a system with WPZ pin grounded and still being able to write to the Status register. For more details see *Principles of Operation*.

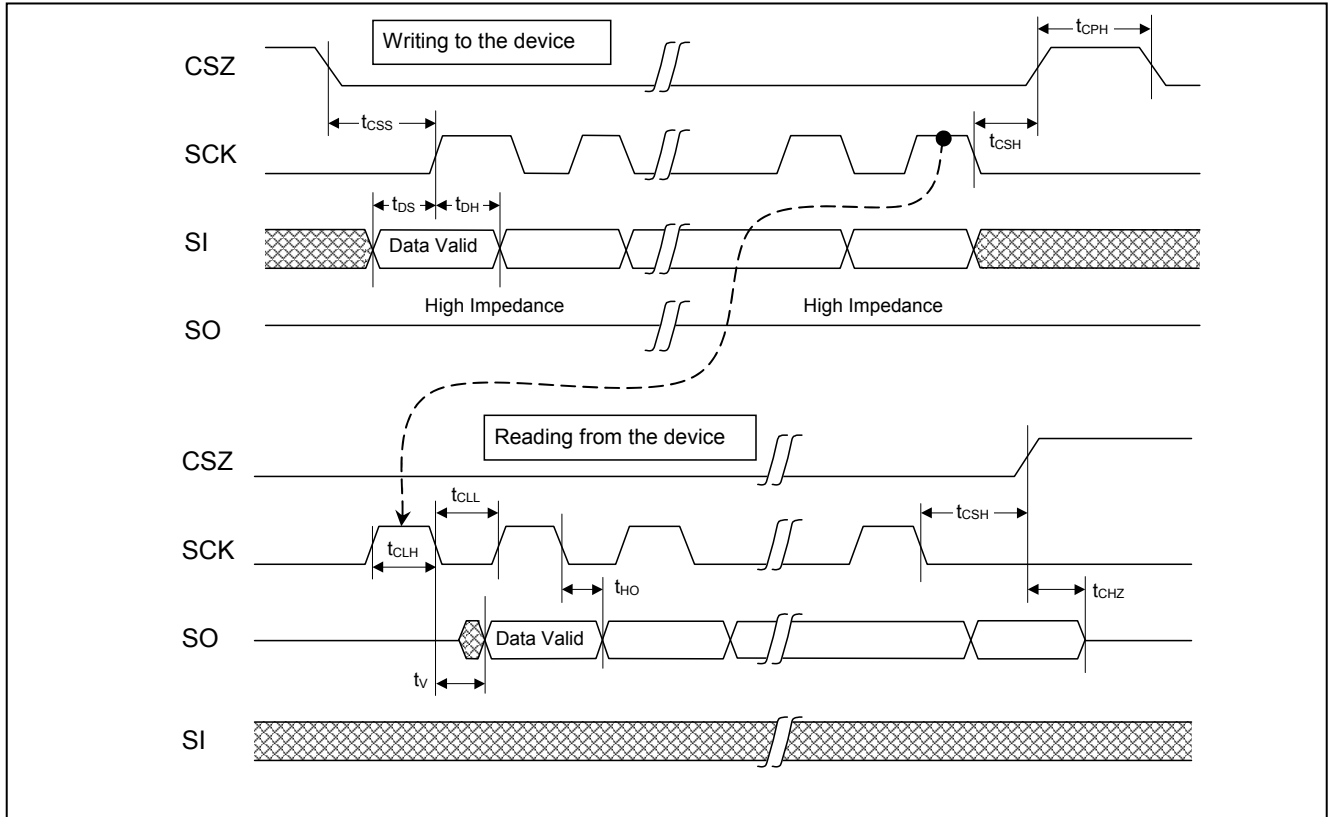
### SPI Modes and Bit Timing

The SPI protocol defines communication in full bytes with the MS bit being transmitted first. Every SPI communication sequence begins with at least one byte written to the slave device. The first byte that the slave receives from the master is understood as an instruction. Depending on the instruction the slave may need more bytes, e.g., address and data; for a read function, after having received the instruction and address, the slave starts sending data to the master.

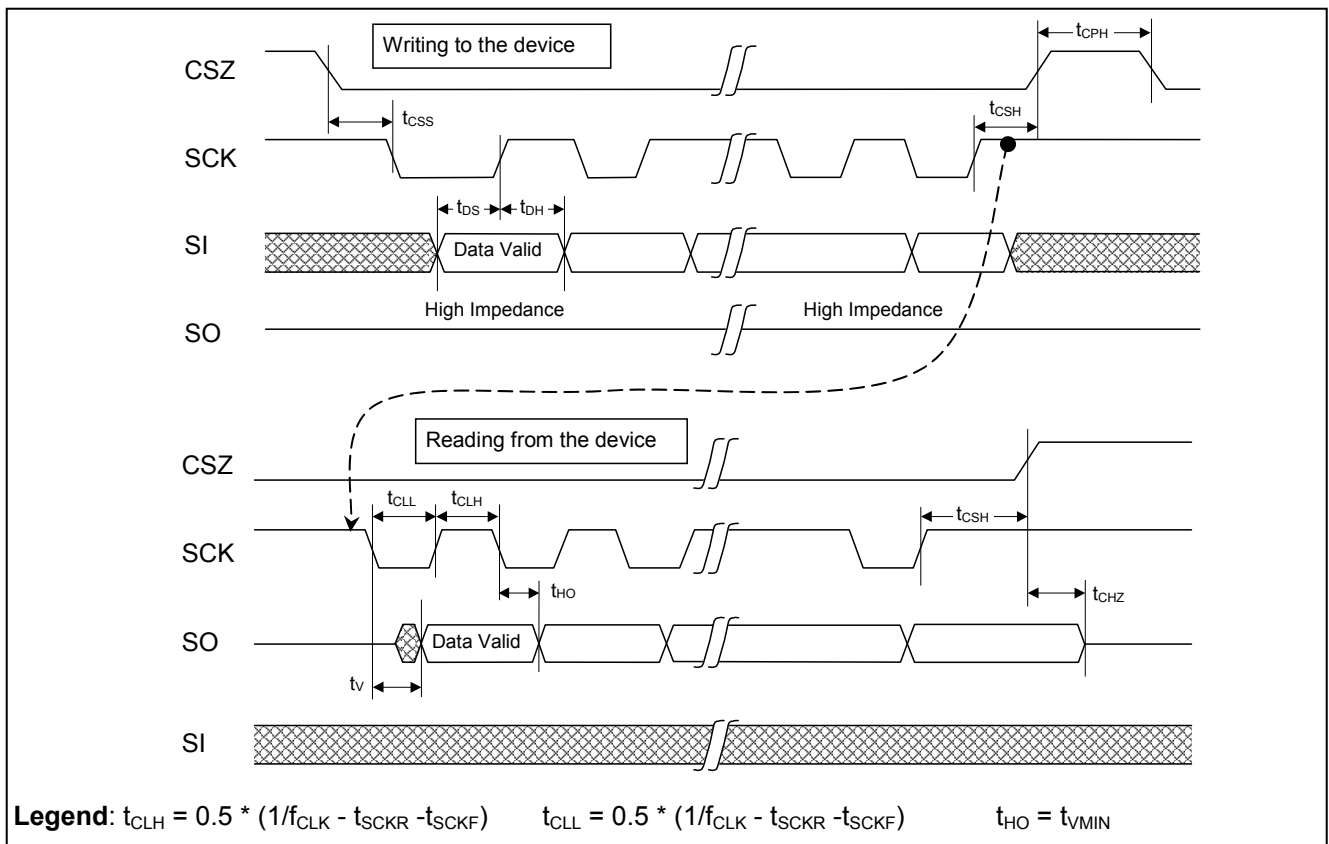
The SPI protocol knows four communication modes, which differ in the polarity and phase of the SCK signal. The DS28DG02 supports modes (0,0) and mode (1,1). These modes have in common that data is clocked into the slave on the rising edge and clocked out to the master on the falling edge of SCK. The master then clocks in the data on the rising edge of SCK. The DS28DG02 detects the mode from the logic state of SCK when CSZ gets active (high to low transition). Therefore, SCK must be stable for the duration of a setup and hold time around the falling edge of CSZ. Figures 9 and 10 show the timing details.

The read timing of these graphics begins with the first bit that the DS28DG02 transmits to the master and ends when the master ends the communication by deactivating CSZ (low to high transition). The dotted line indicates the transition between read and write, with the last bit of the command or address being clocked in on the rising edge and the first bit of read data appearing at SO after the falling edge of SCK.

**Figure 9. SPI Timing, Mode (0,0)**



**Figure 10. SPI Timing, Mode (1,1)**



## Principles of Operation

The first byte that the DS28DG02 receives from the master after a falling edge on CSZ is interpreted as an instruction. The DS28DG02 supports a set of seven instructions, which are summarized in Figure 11. The protocol uses only a single address byte. The 9th address bit necessary to access addresses of 100h and higher is included in the instruction code, marked as "X".

**Figure 11. SPI Instruction Set**

INSTRUCTION NAME	INSTRUCTION CODE	PROTOCOL	PURPOSE
WREN Write Enable	0000 0110b	Tx Instruction Code	To set the WEN bit in the SPI Status register. (Enable Writes to Memory)
WRDI Write Disable	0000 0100b	Tx Instruction Code	To clear the WEN bit in the SPI Status register. (Disable Writes to Memory)
WRSR Write Status Register	0000 0001b	Tx Instruction Code Tx SPI Status Byte	To update the SPI Status register.
RDSR Read Status Register	0000 0101b	Tx Instruction Code Rx SPI Status Byte	To read SPI Status register; to detect the end of an EEPROM write cycle.
RFSH Refresh Registers	0000 0111b	Tx Instruction Code	To update the SRAM registers at addresses 120h to 125h with their power-on default values without power-cycling.
WRITE Write to Memory	0000 X010b	Tx Instruction Code Tx Address Byte Tx Data Byte(s)	To write to the memory, register, PIOs, or the RTC, depending on the specified address.
READ Read Memory	0000 X011b	Tx Instruction Code Tx Address Byte Rx Data Byte(s)	To read from the memory, register, PIOs, or the RTC, depending on the specified address.

The first four instructions relate to the SPI Status register, which contains control bits and a status bit. The SPI Status register is not memory-mapped and can only be updated through SPI instructions. It holds several bits that control an elaborate scheme to prevent inadvertent changes of data stored in the device:

- A write-enable bit WEN that needs to be set through a write-enable instruction WREN before a write instruction is accepted. The WEN bit is automatically cleared after successful execution of a write instruction.
- Hardware write-protection of b7:b2 (nonvolatile bits) of the SPI Status register through the write-protect enable bit WPEN in conjunction with the logic state at the WPZ pin.
- Write-Protect bits for memory blocks and the registers from address 120h and higher.

The combined effect of WEN, WPEN, and WPZ is summarized in Table 2. The full description of the SPI Status register bit functions is found in Figure 12.

**Table 2. Write Protection Summary**

WEN BIT	WPEN BIT	WPZ PIN	SPI STATUS REGISTER	MEMORY
0	x	x	Write-protected (because WEN = 0).	Write-protected (because WEN = 0).
1	0	x	Writeable (because WPEN = 0).	Conditional write access: BP1:BP0 control protection of addresses 00h to FFh. RPROT controls protection of addresses 120h and higher.
1	1	0	Write-protected (because WPEN = 1 AND the WPZ pin is at logic 0).	
1	1	1	Writable (because WPEN = 1 AND the WPZ pin is at logic 1).	

**Figure 12. SPI Status Register**

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
N/A	WPEN	RPROT	WD1	WD0	BP1	BP0	WEN	RDYZ

BIT DESCRIPTION	BIT(S)	DEFINITION
RDYZ: Ready (Read-Only Bit)	b0	Indicates whether an EEPROM write cycle is in progress. <b>Legend:</b> 0 → ready (normal state); 1 → write cycle in progress
WEN: Write Enabled (Read-Only Bit)	b1	Indicates whether the device will accept a WRITE instruction; set through the WREN instruction; cleared through the WRDI instruction or completion of a valid WRITE or a valid WRSR instruction. <b>Legend:</b> 0 → write disabled (power-on default); 1 → write enabled
BP1:BP0: Block Write Protect	b3:b2	These bits specify which of the four user memory blocks are write-protected (independent of WPEN and WPZ). <b>Legend:</b> 00b → not protected (factory default) 01b → block 3 (0C0h to 0FFh) protected 10b → blocks 2 and 3 (080h to 0FFh) protected 11b → blocks 0 to 3 (000h to 0FFh) protected
WD1:WD0: Watchdog Timeout	b5:b4	These bits specify the duration of the watchdog timeout if the watchdog is enabled (WDE at address 134h = 1). <b>Legend:</b> 00b → 1.64s (factory default); 01b → 820ms 10b → 410ms; 11b → 200ms These are nominal values; for tolerances see Electrical Characteristics.
RPROT: Register Protection	B6	Specifies whether the writeable addresses in the range of 120h and higher are write-protected (independent of WPEN and WPZ). <b>Legend:</b> 0 → not protected (factory default); 1 → protected
WPEN: Hardware Write Protect Enable	b7	Specifies whether b7:b2 of the SPI Status register (nonvolatile bits) are writeable or whether the WPZ pin state controls the write-protection. <b>Legend:</b> 0 → writeable (factory default) 1 → protection controlled by WPZ pin state If WPEN = 1 and WPZ pin state is 0 the SPI Status register is write-protected and a WRSR instruction is not valid.

## DETAILED DESCRIPTION—SPI INSTRUCTION SET

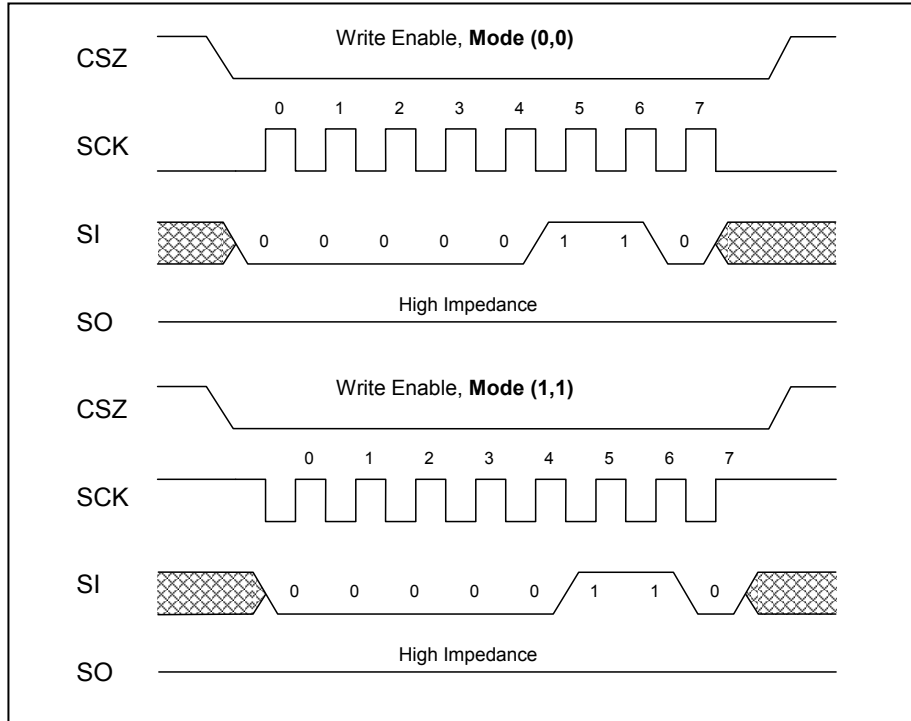
### WREN Write Enable

Before any write access to the device, the WEN bit in the SPI Status register must be set. The only way to set this bit is through the write-enable instruction. The WEN bit is cleared when the device powers up, after the successful execution of a write access instruction (WRSR or WRITE) and through WRDI. Figure 13 shows the instruction's timing diagram for both SPI communication modes.

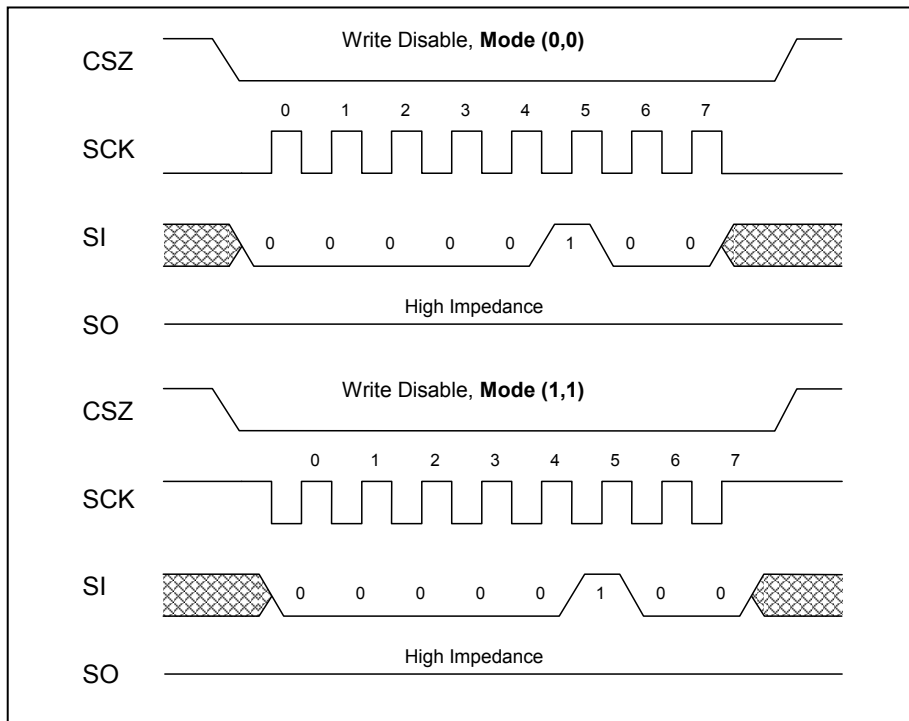
### WRDI Write Disable

The WRDI instruction can be used to clear the WEN bit of the SPI Status register, e.g., after an unsuccessful write access instruction. Figure 14 shows the instruction's timing diagram for both SPI communication modes.

**Figure 13. Write-Enable Timing**



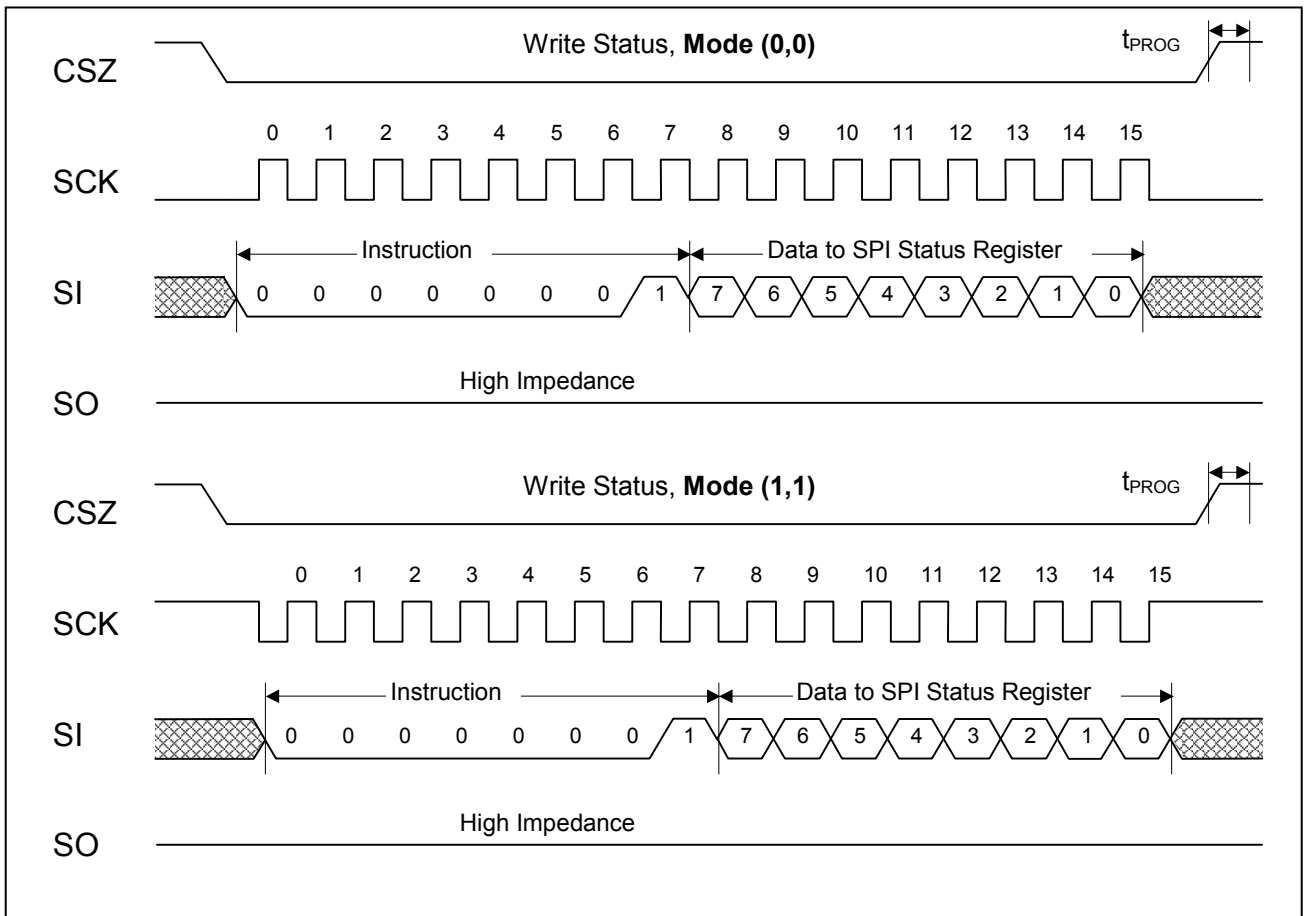
**Figure 14. Write-Disable Timing**



### WRSR Write SPI Status Register

The WRSR instruction is the only way to update the nonvolatile bits (b7:b2) of the SPI Status register. See Figure 12 for a detailed description of the nonvolatile bits and their function. As a precondition for a successful write access to the Status register, the WEN bit must be 1 and either the WPEN bit must be 0, or both WPEN and the logic state at the WPZ pin must be 1, as shown in the write protection summary of Table 2. The WEN bit is set through the WREN instruction, which must be completed before any write instruction. The WRSR timing diagram for both SPI communication modes is shown in Figure 15. The graphic assumes that only a single byte follows the instruction code. In case of multiple bytes following the instruction code, the last of these data bytes is used to update the SPI Status register. If the SPI Status register is not write-protected AND the WEN bit 1, the write cycle (transfer to EEPROM) begins with the positive edge of CSZ. The duration of the write cycle is  $t_{PROG}$ , during which the RDYZ bit of the SPI Status register reads 1. After the write cycle is completed, the WEN bit is cleared. If the SPI Status register is write-protected OR WEN was not set to 1 before issuing the WRSR instruction, the positive edge on CSZ does not start a write cycle and the WEN bit is not cleared. The first Read Memory sequence executed after WRSR always delivers data from addresses 100h and higher, regardless of the address bit in the instruction code.

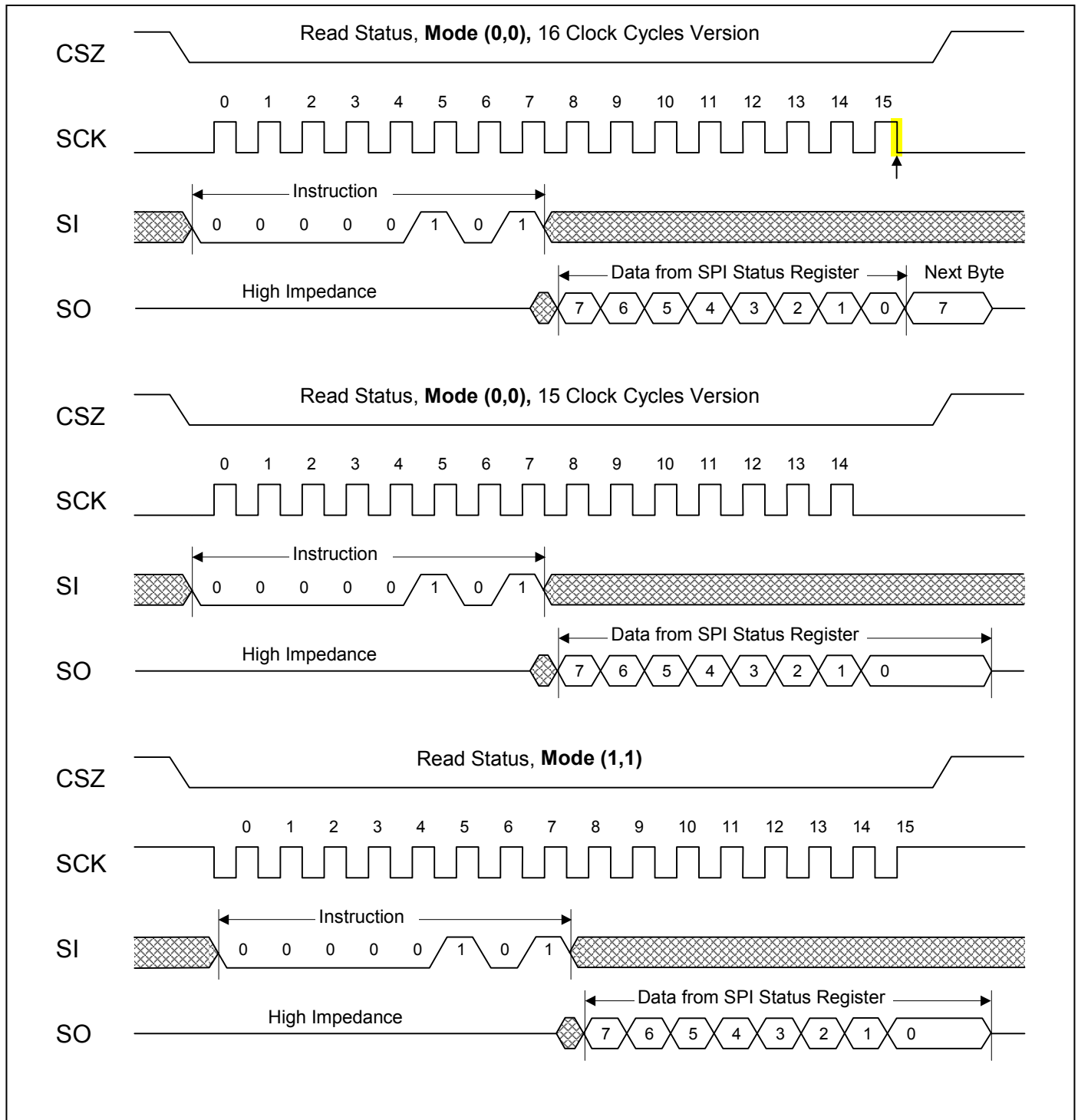
**Figure 15. Write SPI Status Register Timing**



### RDSR Read SPI Status Register

RDSR is the only instruction that the DS28DG02 accepts and executes at any time, even if an EEPROM write cycle is in progress. See Figure 12 for a detailed description of the SPI Status register bits. Besides providing general read access to the SPI Status register, the main use of this instruction is for the master to test the RDYZ bit, which signals the end of an EEPROM write cycle. Figure 16 shows the RDSR timing diagram for both SPI communication modes. The RDYZ state reported through the RDSR instruction is updated on the negative edge of SCK during the transmission of the LS-bit of the status byte (highlighted in Figure 16, the Mode (0,0) 16 clock cycles graphic). This allows the master to repeatedly read the SPI Status register by generating additional SCK pulses, without having to resend the instruction code. The RDSR instruction ends with the positive edge on CSZ.

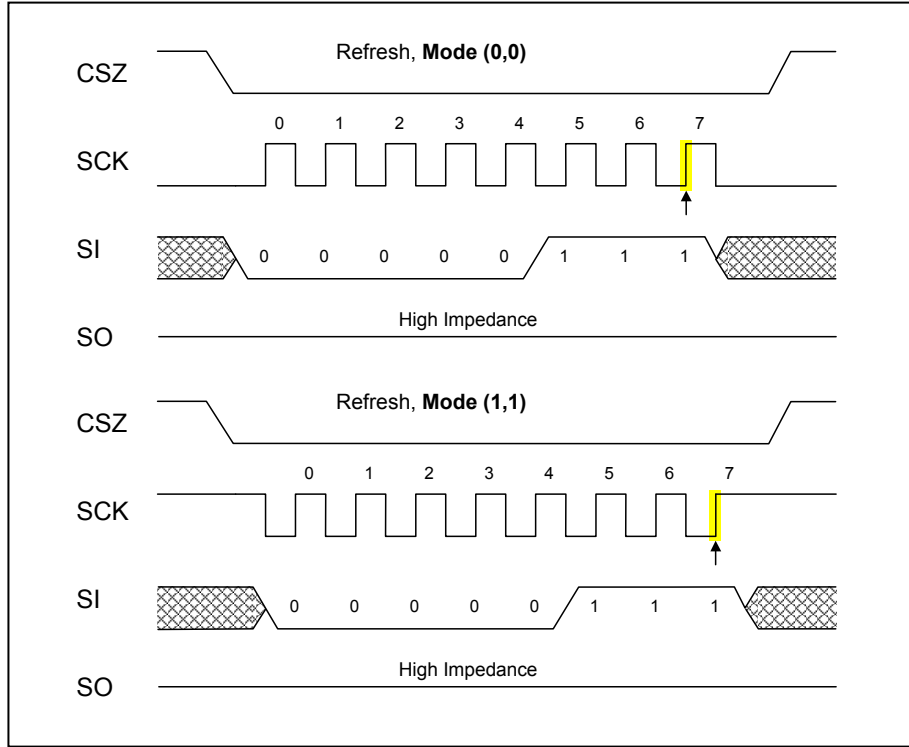
**Figure 16. Read SPI Status Register Timing**



### RFSH Refresh PIO Registers

The volatile PIO-related registers from address 120h to 125h are preset with their power-on default values stored in EEPROM when the device powers up. The fastest way for the master to restore the power-on state without power-cycling the DS28DG02 is through the RFSH instruction. The RFSH timing diagram for both SPI communication modes is shown in Figure 17. The PIO register restore begins when the last bit of the instruction code is clocked into the device (highlighted SCK transition) and ends after the power-up wait time ( $t_{POIP}$ ) is over.

**Figure 17. Refresh PIO Registers Timing**



### WRITE Write to Memory and PIO

From the perspective of the master, the DS28DG02 is a memory device with memory ranges made of EEPROM, SRAM and ROM. Depending on the memory type, the behavior of the device upon receiving a write instruction varies. Table 3 shows the cases that need to be distinguished.

**Table 3. Write Access Cases**

STARTING ADDRESS	DESCRIPTION
000h to 0FFh	User memory (can be write-protected through BP1:BP0).
100h to 10Fh	EEPROM registers (reserved and power-on default values, no write-protection).
110h to 11Fh	Read-only memory.
120h to 135h	SRAM, PIO, and NV SRAM (may be write-protected through RPROT).
136h to 1FFh	Nonexisting memory.

The four blocks of user memory consist of 16 segments of 16 bytes each. The first segment begins at address 000h and ends at address 00Fh; segment 2 ranges from 010h to 01Fh, etc. Upon receiving a write instruction with an address targeting the user memory, any data bytes that follow the address are written to a 16-byte buffer, beginning at an offset that is determined by the 4 least significant bits of the target address. This buffer is initialized (pre-loaded) with data from the addressed 16-byte EEPROM segment. Incoming data replaces pre-loaded data. With every byte received, the buffer's write pointer is incremented. This allows updating from 1 to 16 bytes starting anywhere within the segment. If the write pointer has reached its maximum value of 1111b and additional data is received, the pointer wraps around (rolls over) and the incoming data is written to the beginning of the EEPROM write buffer and continuing. If the target memory is not write-protected AND the WEN bit of the SPI Status register



is 1 AND the number of bits sent by the master is a multiple of 8 (i.e., full byte only), the write cycle (transfer from the buffer to EEPROM) begins with the positive edge of CSZ. The duration of the write cycle is  $t_{\text{PROG}}$ , during which the RDYZ bit of the SPI Status register reads 1. After the write cycle is completed, the WEN bit is cleared. If the target memory is write-protected OR WEN was not set to 1 before issuing the WRITE instruction OR the number of data bits that followed the address byte was not a multiple of 8, the positive edge on CSZ does not start a write cycle and the WEN bit is not cleared.

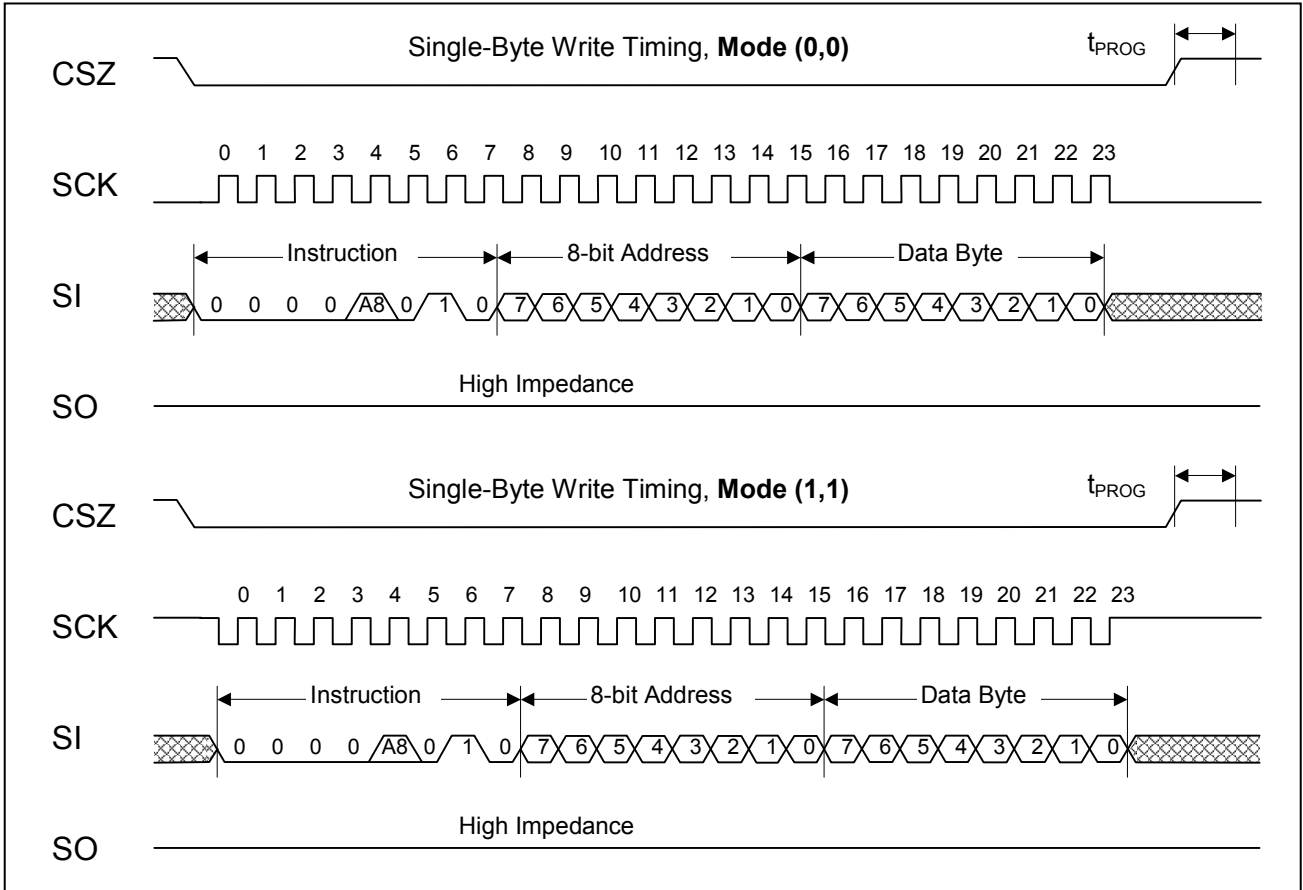
The six EEPROM registers, together with the reserved addresses, form another memory segment. Write access to this segment is essentially the same as for the user memory with the following differences: The data sent by the master that normally would apply to the first 10 bytes of the segment is discarded. A write cycle is initiated only if the WEN bit of the SPI Status register is 1 AND the number of bits sent by the master is a multiple of 8 (i.e., full byte only) AND at least one EEPROM byte is to be updated. If WEN was not set to 1 before issuing the WRITE instruction OR the number of data bits that followed the address byte was not a multiple of 8 OR all data bytes sent by the master applied to the nonwriteable addresses, the positive edge on CSZ does not start a write cycle and the WEN bit is not cleared.

Write access to the SRAM, PIO, and NV SRAM does not involve a write buffer. If the WEN bit is 1 AND RPROT = 0 AND the target address is writeable, a data byte that follows the target address becomes effective as soon as its transmission is completed. The address pointer increments after each data byte, directing subsequent bytes to the next higher addresses. If the target address is read-only, data for that address is discarded. After address 135h is updated, the address pointer wraps around to 120h. The master may continue sending data bytes indefinitely. The write access ends with the positive edge on CSZ. The last byte, if incomplete, is ignored. The WEN bit is cleared only if at least one byte was written to a writeable address. If RPROT = 1 the memory is not updated and the WEN bit remains set. The RTC should be updated starting with the Seconds register. If the starting target address specified after the instruction code points to the PIO Output State registers (address 120h or 121h) and the PIO output mode OTM is 0 (low current) the address pointer toggles between 120h and 121h after the data byte is transmitted. This allows fast PIO updates, e.g., for generating data patterns. For OTM = 1 (high-current) the address pointer increments to the next higher address. For a PIO-update timing diagram and the differences between low-current and high-current mode, see the *PIO Read/Write Access* section.

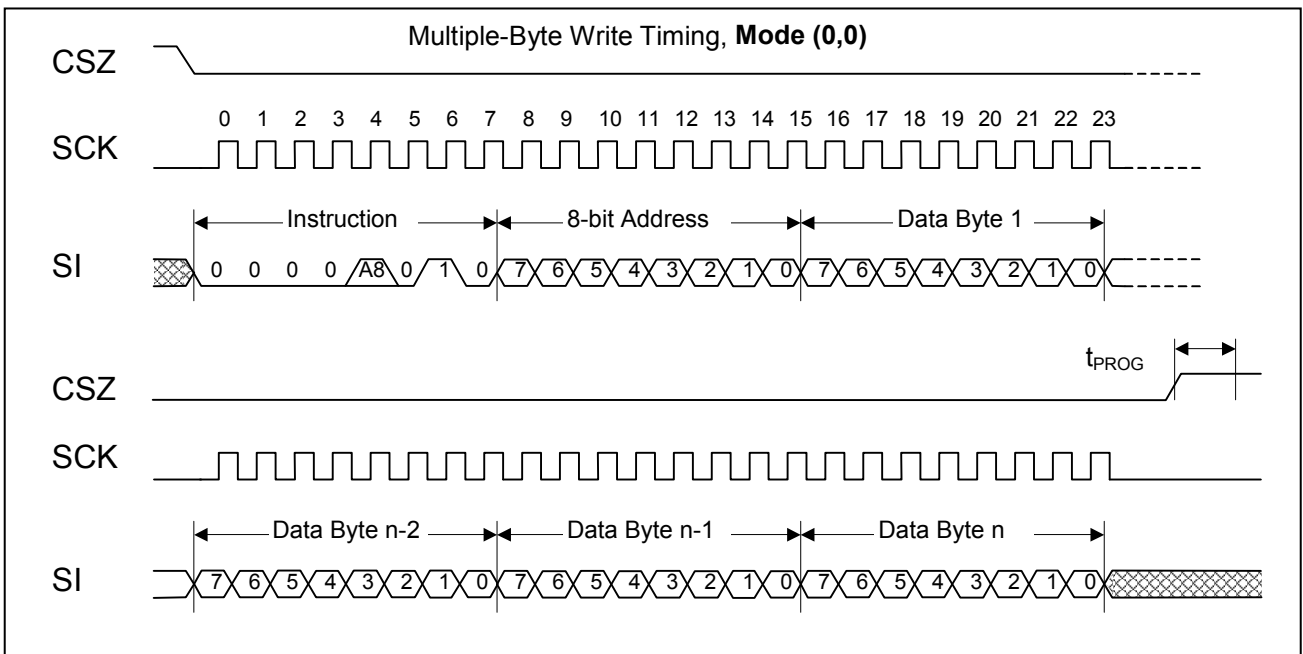
Upon receiving a write instruction with an address targeting the read-only memory or non-existing memory, all data is discarded and no write cycle or data update takes place. Since the write access is not successful, the WEN bit in the SPI Status register is not cleared.

As a precondition for a successful WRITE instruction, the WEN bit in the SPI Status register must be 1. The WEN bit is set through the WREN instruction, which must be completed before the WRITE instruction. The WRITE timing diagram for both SPI communication modes is shown in Figure 18 (single-byte write) and Figure 19 (multiple-byte write). The programming time  $t_{\text{PROG}}$  applies only to EEPROM writes. For writes to the SRAM, PIO, and NV SRAM in SPI mode (0,0) the actual transfer to the target memory takes place on the falling SCK edge of the LS-bit of a data byte. In SPI mode (1,1) the actual transfer to the target memory also takes place on the falling SCK edge of the LS-bit of a data byte, except for the last byte, which is transferred on the rising edge of CSZ.

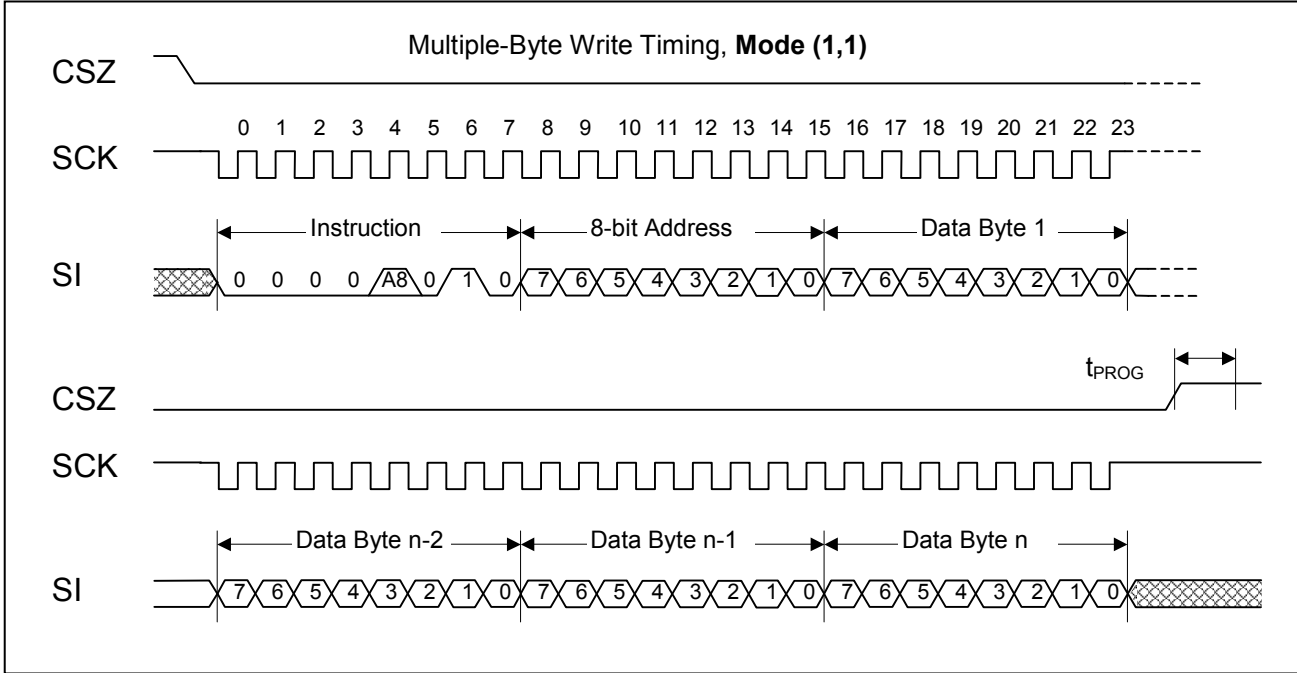
**Figure 18. Single-Byte Write to Memory and PIO Timing**



**Figure 19. Multiple-Byte Write to Memory and PIO Timing**



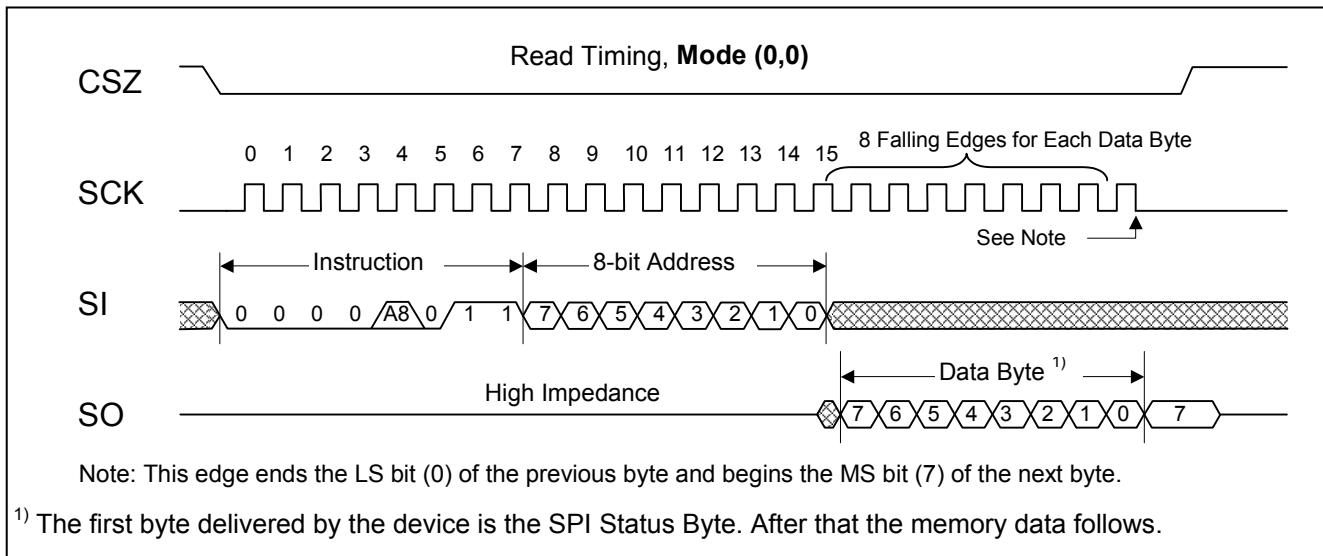
**Figure 19. Multiple-Byte Write to Memory and PIO Timing (continued)**



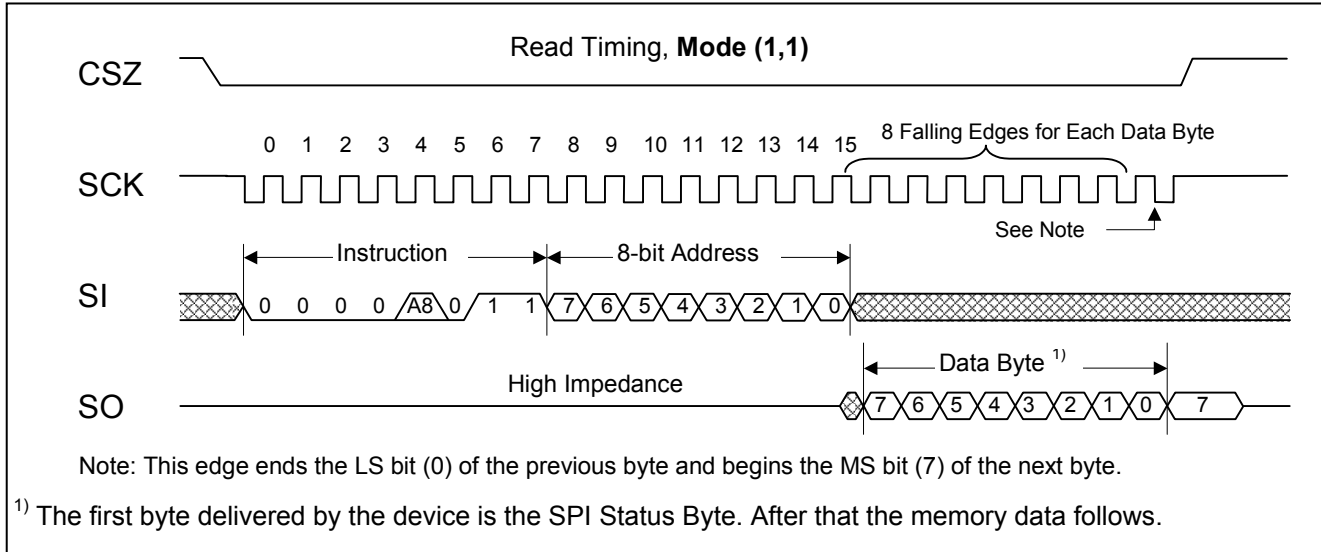
**Read Memory and PIO**

The read timing diagram for both SPI communication modes is shown in Figure 20. The read-access timing is independent of the addressed memory type. Upon receiving a read instruction with an address in the range of 000h to 135h the DS28DG02 transmits data, first the SPI Status register value and then data from the specified target address. Addresses marked “reserved” read 00h. The address pointer increments with every data byte transmitted to the master. After data from address 135h is read, the address pointer wraps around to 000h. The master may continue reading data bytes indefinitely. The read access ends with the positive edge on CSZ. If prior to the Read Memory and PIO sequence a WRSR command was executed, the address bit embedded in the instruction code is ignored and data is delivered from addresses 100h and higher. The application firmware should include a command such as WRDI after WRSR to ensure reading from the intended address.

**Figure 20. Read Memory and PIO Timing**



<sup>1)</sup> The first byte delivered by the device is the SPI Status Byte. After that the memory data follows.

**Figure 20. Read Memory and PIO Timing (continued)**

When reading the RTC and Calendar registers, the data reported to the master is taken from a buffer. This buffer is loaded when the least significant address bit is transmitted during a READ instruction. This buffer is not updated between bytes or when the address pointer wraps around. If the starting target address specified after the instruction code points to the PIO Read Access registers (address 126h or 127h) the address pointer toggles between 126h or 127h after a data byte is transmitted. This allows fast PIO reads, e.g., to monitor several signals. For a PIO-read timing diagram see the *PIO Read/Write Access* section.

If a read instruction requests data from nonexistent memory, the DS28DG02 initially transmits 00h bytes until the address pointer eventually changes to 000h. Subsequently, the device transmits valid data and the read pointer increments normally, wrapping around to 000h after having reached 135h.

## PIO Read/Write Access

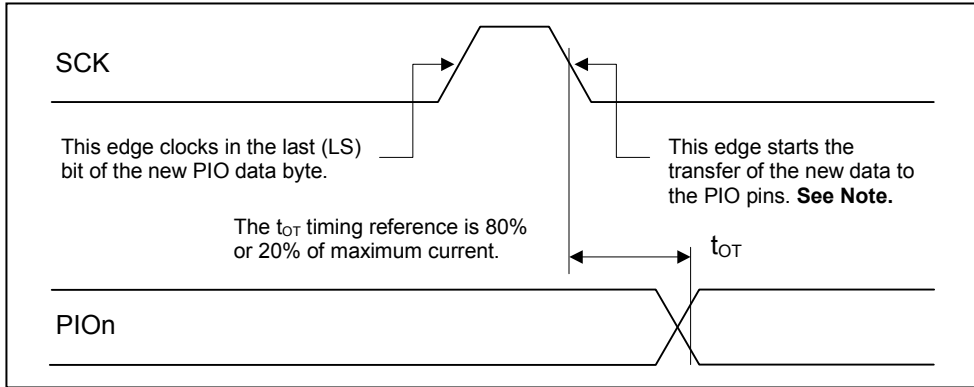
### General Information

When the DS28DG02 powers up, the PIO direction, output state, output type, output mode, and read-inversion are set automatically from power-on default values stored in EEPROM. The duration of this initialization phase is  $t_{POIP}$ , during which each PIO is temporarily set as input with the output driver tri-stated to prevent conflicts with circuitry connected to the PIO pins. The output drivers of PIOs that are configured as input are tri-stated (high impedance). The PIO output drivers of the DS28DG02 are designed to deliver high currents for driving LEDs or similar loads. Switching multiple PIOs conducting high current simultaneously could errantly trigger the reset monitor circuit. To prevent this from happening, it is necessary to set the OTM bit at address 125h, which activates the high-current mode where the PIO channels switch sequentially. In high-current mode changes in direction or output type do not take effect immediately; they are delayed until the next PIO write access when the associated bit transition is evaluated. Since writing to PIOs is a write function, the WEN bit must be set before issuing the WRITE instruction.

### Writing in Low-Current Mode

When writing to PIOs in low-current mode, as shown in Figure 21, any state change is triggered by the falling edge of SCK after the last bit of the new PIO state is shifted into the DS28DG02. All addressed PIOs (8 with address 120h or 4 with address 121h) change their state approximately at the same time. After the output transition time  $t_{OT}$  is expired, the state change is completed. If the WRITE instruction is issued with starting address 120h, the DS28DG02 enters a loop in which incoming data is directed to both groups of PIOs alternating between PIO0:7 and PIO8:11. This way the fastest rate for a PIO to change its state is  $f_{CLK} / 16$ .

**Figure 21. PIO Write Access Timing, Low-Current Mode**

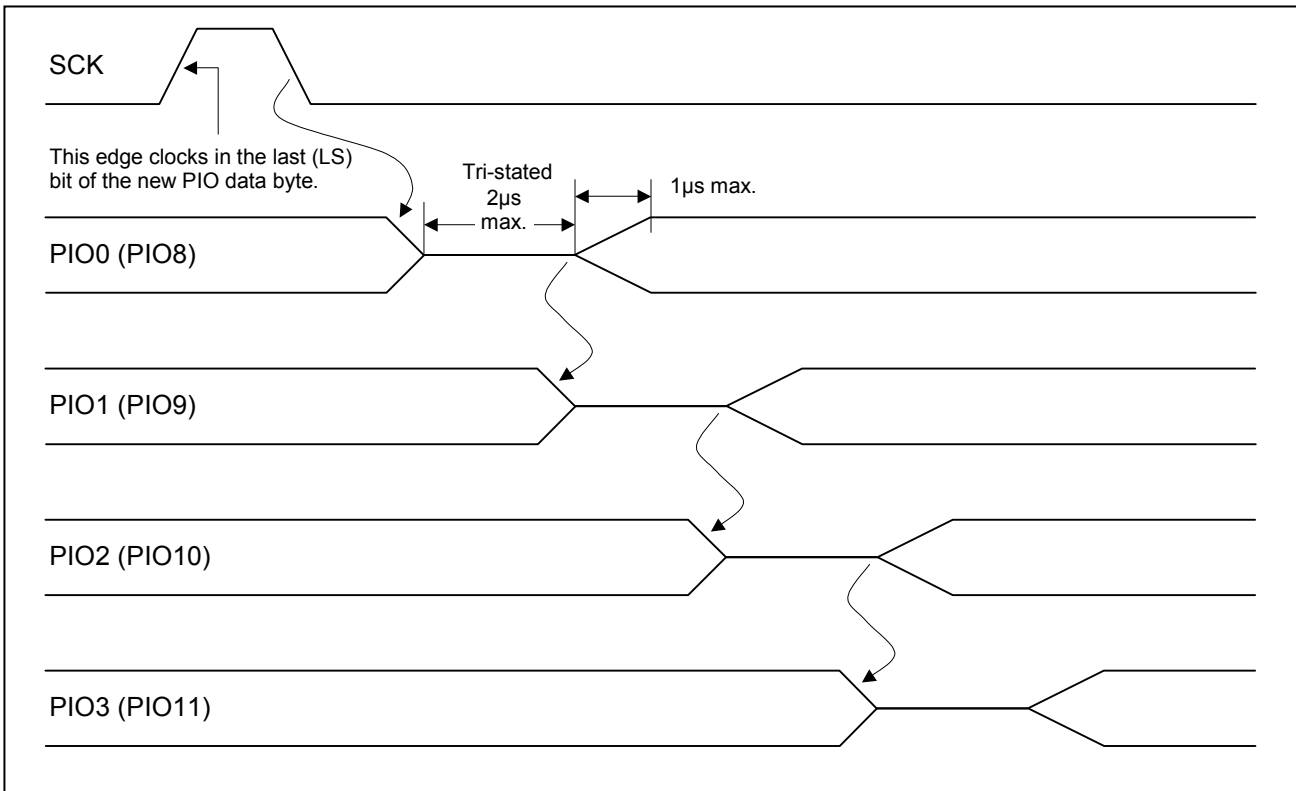


**Note:** In SPI Mode (1,1) there is no falling SCK edge for the last bit of the last byte sent to the device; in this case, the transfer to the PIO is initiated with the rising edge of CSZ. This note also applies to the high-current mode.

**Writing in High-Current Mode**

When writing to PIOs in high-current mode, the state change is triggered by the falling edge of SCK after the last bit of the new PIO state is shifted into the DS28DG02. The PIOs change their state sequentially, as shown in Figure 22, beginning with PIO0 or PIO8, respectively, depending on the address. A PIO that is changing its state is first tri-stated for 2µs maximum. This 2µs delay also applies to PIOs configured as input and to PIOs configured as output that do not change their state. The state transition of PIOs in high-current mode is slew-rate controlled to prevent immediate full current-drive or release. Each pin’s slew-rate circuit is designed to ramp up to the full current drive or release over the course of 1µs. The  $t_{OT}$  value specified for high-current delay mode is valid when updating all 12 PIOs in a single write access. In this case there is an extra 1µs maximum delay when transitioning from PIO7 to PIO8. In high-current mode, the automatic alternation between groups of PIOs does not apply; another WREN and WRITE sequence is necessary to update the PIO states again.

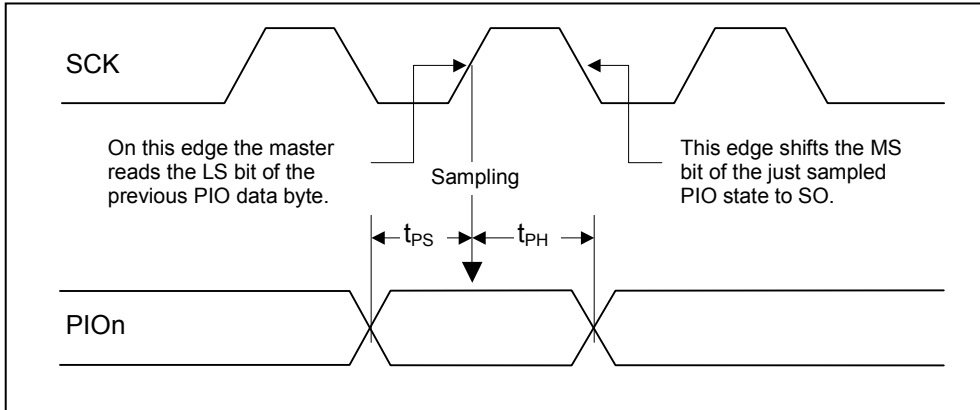
**Figure 22. PIO Write Access Timing, High-Current Mode**



**Reading from PIO**

When reading from PIOs, as shown in Figure 23, the sampling is triggered by the same edge that the master uses to clock in (read) the last data (LS) bit of the preceding byte, which may be PIO data or SRAM data. To be correctly assessed, the PIO state must not change during the  $t_{PS}$  and  $t_{PH}$  interval. The SO state is valid  $t_V$  after the falling edge of SCL. When reading from address 126h, the PIO state appearing first on SO is that of PIO7. With every falling edge on SCK the next PIO state appears on SO. On the rising SCK edge after the state of PIO0 is shifted out to SO, the PIOs of address 127h are sampled. Reading from address 127 first results in four 0-bits followed by the state of PIO11 to PIO8. If the READ instruction is issued with starting address 126h, the DS28DG02 enters a loop in which both groups of PIOs are read alternating between PIO0:7 and PIO8:11. This way the fastest PIO sampling rate is  $f_{CLK} / 16$ .

**Figure 23. PIO Read-Access Timing**



**SPI Communication—Legend**

SYMBOL	DESCRIPTION
SEL	Falling Edge on CSZ
DSEL	Rising Edge on CSZ
WREN	Write Enable Instruction
WRDI	Write Disable Instruction
WRSR	Write Status Register Instruction
RFSH	Refresh Instruction

SYMBOL	DESCRIPTION
WRITEL	Write Instruction with A8 = 0
WRITEH	Write Instruction with A8 = 1
READL	Read Instruction with A8 = 0
READH	Read Instruction with A8 = 1
<byte>	Transfer of 1 Byte

## Command-Specific Communication—Color Codes

Master-to-Slave	Slave-to-Master	Programming
-----------------	-----------------	-------------

### Communication Examples

#### Set the WEN Bit in the SPI Status Register (Write Enable)

SEL	WREN	DSEL
-----	------	------

#### Clear the WEN Bit in the SPI Status Register (Write Disable)

SEL	WRDI	DSEL
-----	------	------

#### Write to the SPI Status Register Sequence

SEL	WREN	DSEL	SEL	WRSR	<byte>	DSEL	Programming
-----	------	------	-----	------	--------	------	-------------

**Note:** It is advisable to execute a WRDI command right after the WRSR sequence is completed to ensure read access to the user memory.

#### Read Status Register (e.g., to Detect the End of a Write Cycle)

SEL	RDSR	<byte>	<byte>	<byte>	DSEL
-----	------	--------	--------	--------	------

Continue reading until RDYZ bit is 0

#### Refresh PIOs with Power-On Defaults

SEL	RFSH	DSEL
-----	------	------

#### Write 3 Bytes to User Memory Sequence, Starting Address = 067h

SEL	WREN	DSEL	SEL	WRITEL	<67h>	<byte>	<byte>	<byte>	DSEL	Programming
-----	------	------	-----	--------	-------	--------	--------	--------	------	-------------

See Read Status register example to test for the end of the write cycle.

#### Set RTC and Calendar, Starting Address = 129h

SEL	WREN	DSEL	SEL	WRITEH	<29h>	<7 bytes RTC data>	DSEL
-----	------	------	-----	--------	-------	--------------------	------

SRAM, no programming time.

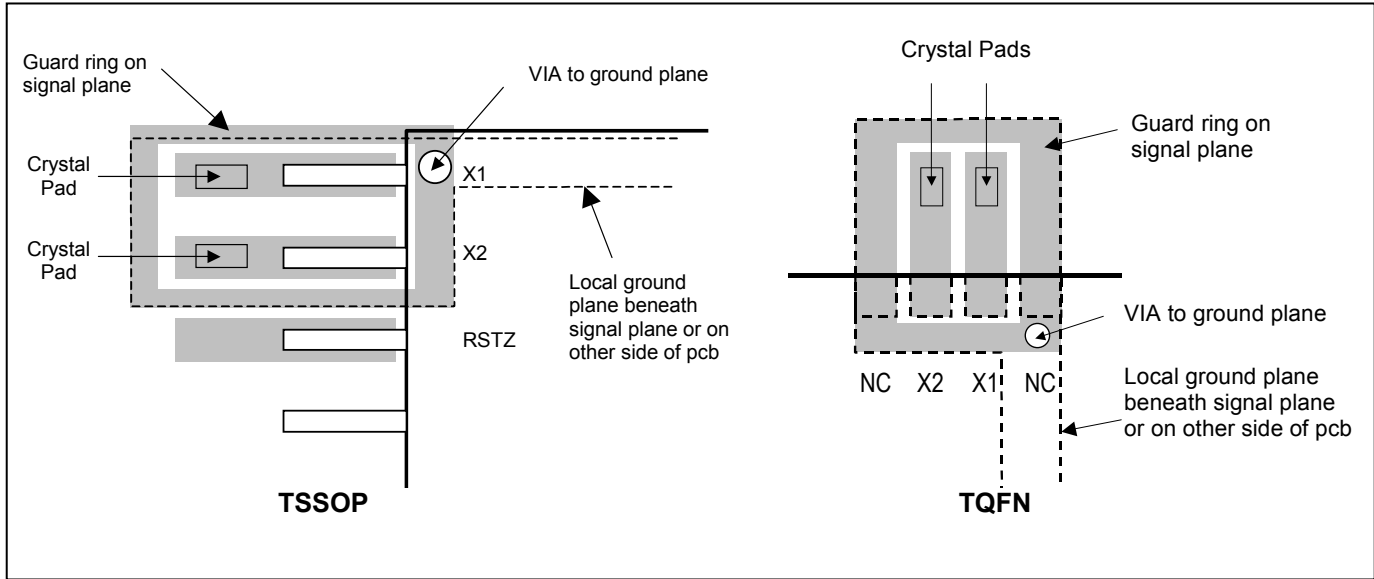
#### Read User Memory Block 1, Starting Address = 040h, 64 Bytes

SEL	READL	<40h>	<64 bytes memory data>	DSEL
-----	-------	-------	------------------------	------

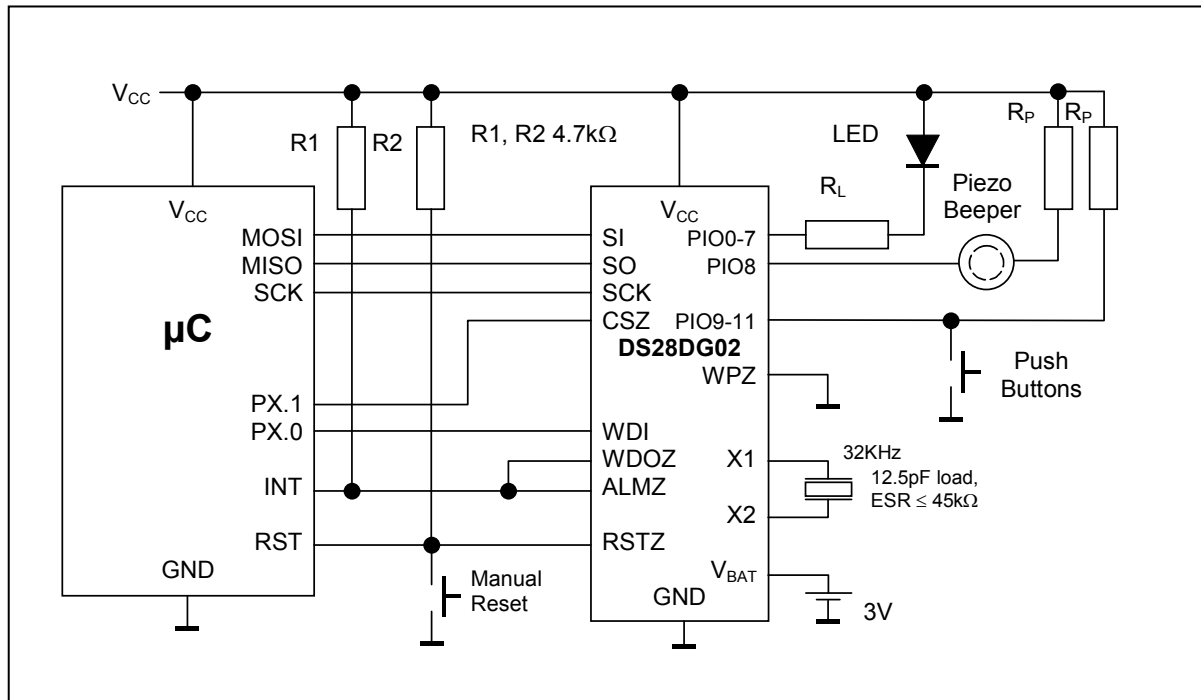
#### Read all PIOs 3 Times, Starting Address = 126, 6 Bytes

SEL	READH	<26h>	<6 bytes PIO data>	DSEL
-----	-------	-------	--------------------	------

**Figure 24. Crystal Placement on PCB**

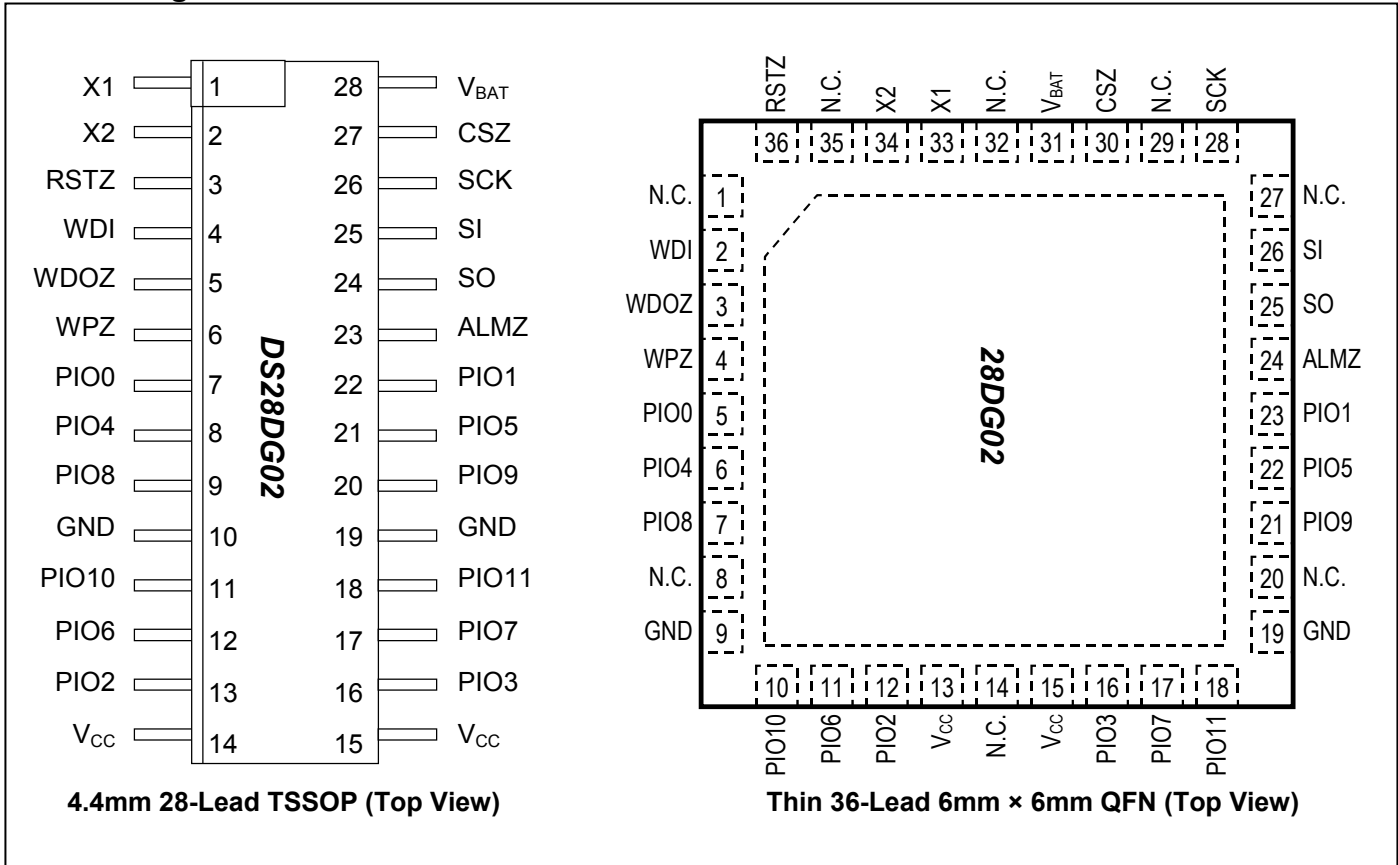


**Typical Operating Circuit**





## Pin Configurations



## PACKAGE INFORMATION

For the latest package outline information and land patterns, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 TSSOP	—	<a href="#">21-0108</a>
36 TQFN	—	<a href="#">21-0141</a>

**REVISION HISTORY**

<b>REVISION DATE</b>	<b>DESCRIPTION</b>	<b>PAGES CHANGED</b>
11/09	<ul style="list-style-type: none"><li>• Text in <i>Unique Registration Number</i> section was rewritten. In compliance with SPI conventions, the registration number is stored with the CRC at 118h and family code at 11Fh (not the opposite sequence, as originally described).</li><li>• Added address information to Figure 3 (118h over CRC, 119h-11Eh over 48-bit S/N, 11Fh over family code)</li></ul>	9