System Power Supply for TV Series

FET Controller Type 3ch System Power Supply ICs

BD8606FV

●Description

BD8606FV has realized the high performance and reliability required as a power supply for thin-screen TV.
Due to the high-speed load response, it is most suitable for TV-purpose processors with increasingly high performance, and due to the wide phase margin it leaves a good margin for board pattern & constant setting and so facilitates its application design.
As a high-reliability design, it has various built-in protection circuits (overcurrent protection, output voltage abnormal protection, thermal protection, and off-latch function at the time of abnormality etc.), therefore as an advantage it does not easily damage in every possible abnormal condition such as all-pin short circuit test etc. and hence most suitable for thin-screen TV which requires the high reliability.

●Features

1) 3ch synchronous rectification step-down system DC/DC converter controller
2) 3ch independent ON/OFF. controllable
3) Soft start, soft off function
4) Concentrated protection control with built-in sequencer
5) Built-in low voltage protection function
6) Built-in overvoltage protection function
7) Built-in overcurrent protection function
8) Built-in RT terminal open/short protection function
9) Frequency setting by external resistance is available.
10) Protection condition is output from PDET terminal.
11) Built-in external reset output function

Aug. 2008

● **Electric characteristic**

(Ta=25℃, VIN1, VIN2, VIN3=5.0V, VCC=5.0V, and GND=0V unless otherwise specified.)

Parameter	Symbol	specification value			UNIT	Condition
		MIN	TYP	MAX		
Circuit current 1	I_{Q1}	-	2.5	5	mA	CTL1,2,3=0V
Circuit current 2	I_{Q2}	-	5.0	10	mA	CTL1,2,3=VCC
< Error amplifier part Ch1,Ch2,Ch3 >						
Standard voltage（VREF）	V_{REF}	0.792	0.8	0.808	V	Terminal FB and FC terminal short
Terminal FB Input bias current	I_{FBB}	-1	0	1	μA	V_{FB}=0.9V
Terminal FC Clamping voltage H	V_{FCH}	1.8	-	-	V	V_{FB}=0.7V
Terminal FC Clamping voltage L	V_{FCL}	-	-	0.2	V	V_{FB}=0.9V
Terminal FC Sink current	I_{FCSINK}	0.5	-	-	mA	V_{FB}=0.9V, V_{FC}=0.4V
Terminal FC Source current	$I_{FCSOURCE}$	-	-	-70	μA	V_{FB}=0.7V, V_{FC}=1.6V
Open loop gain	A_{VERR}	-	100	-	dB	
< OSC part >						
Oscillation frequency	F_{OSC}	100	-	600	kHz	
< Soft start part Ch1,Ch2,Ch3 >						
Charging current	I_{SS}	-4.0	-2.5	-1.0	μA	V_{SS}=1.0V
Terminal SS Threshold voltage	V_{SSTH}	1.0	1.1	1.2	V	V_{SS} voltage, V_{FC}=0.8V
Terminal SS Clamping voltage	V_{SSCLM}	1.44	1.72	2.0	V	
Terminal SS Standby voltage	V_{SSSTB}	0.11	0.15	0.19	V	V_{SS} voltage (L→H)
Terminal SS Standby voltage Maximum hysteresis error	V_{SSSTB_HYS}	5	50	100	mV	
Terminal SS Discharge resistance	R_{SS}	49	70	91	kΩ	
Terminal SS Protection circuit start voltage	V_{SSPON}	1.0	1.1	1.2	V	V_{SS} voltage (L→H)
Terminal SS Protection circuit start voltage Maximum hysteresis error	V_{SSPON_HYS}	10	100	200	mV	V_{SS} voltage
< Low voltage, over voltage detection part Ch1,Ch2,Ch3 >						
Terminal FB Low voltage detection voltage	V_{LVP}	0.27	0.32	0.37	V	V_{FB} voltage
Terminal FB Low voltage detection Maximum hysteresis error	V_{LVP_HYS}	10	100	200	mV	V_{FB} voltage
Terminal FB Overvoltage detection voltage	V_{OVP}	1.08	1.2	1.32	V	V_{FB} voltage
< Over current detection part Ch1,Ch2,Ch3 >						
Terminal LX input bias current	I_{LXB}	-1	0	1	uA	
Terminal OCP input bias current	I_{OCPB}	20	50	80	uA	
< Reset detection part >						
Terminal MONVCC reset detection voltage	V_{RSTO}	0.98	1.0	1.02	V	V_{MONVCC} voltage (H→L)
Terminal MONVCC input bias current	$I_{MONVCCB}$	-1	0	1	uA	
Terminal RSTDLY charging current	I_{RSTDLY}	-15	-10	-5	uA	
Terminal RESET L output voltage	V_{OL_RST}	-	-	0.4	V	I_{OL}=100uA
< Others >						
Terminal PDET L output voltage	V_{OL_RDET}	-	-	0.4	V	I_{OL}=100uA
Terminal CTL input voltage H level voltage	V_{IH_CTL}	2.0	-	VCC	V	Terminal CTL1,2,3
Terminal CTL input voltage L level voltage	V_{IL_CTL}	-	-	0.5	V	Terminal CTL1,2,3
Terminal CTL input current	I_{I_CTL}	-	40	70	uA	Terminal CTL1,2,3, CTL=VCC
Terminal DRV H output voltage	V_{OH_DRV}	4.5	-	-	V	Terminal DRV1A,2A,3A,1B,2B,3B
Terminal DRV L output voltage	V_{OL_DRV}	-	-	0.5	V	Terminal DRV1A,2A,3A,1B,2B,3B

V_{FB} : FB terminal voltage, V_{FC} : FC terminal voltage, V_{SS} : SS terminal voltage, V_{MONVCC} : MONVCC terminal voltage

Not designed for radiation resistance.

Current capability should not exceed Pd.

● **Block diagram**

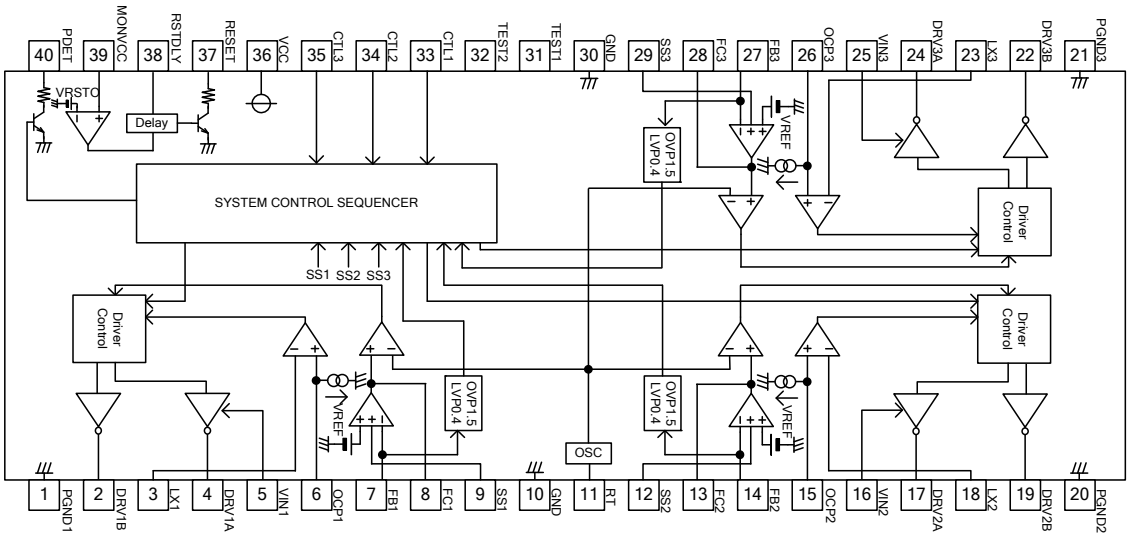


Figure 1 Block char

● Terminal explanation

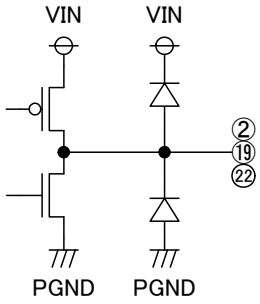
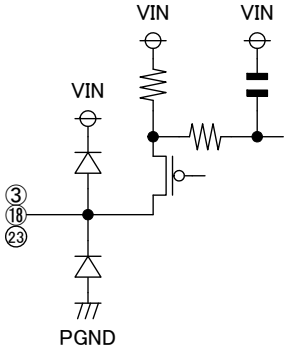
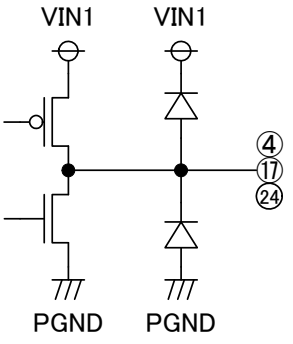
Table 1 terminal explanation

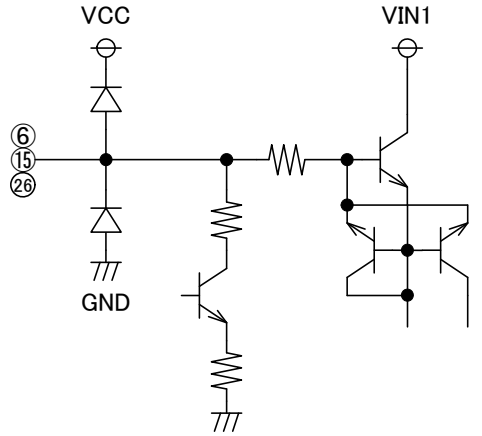
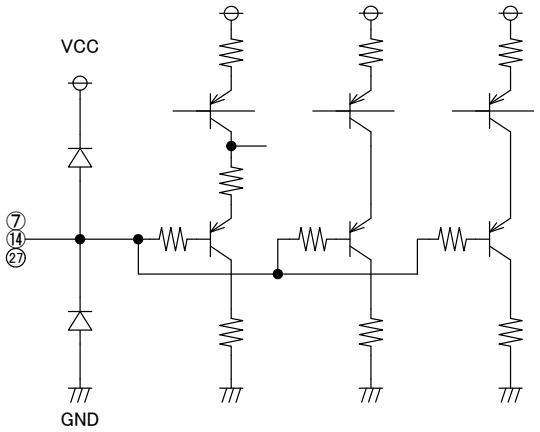
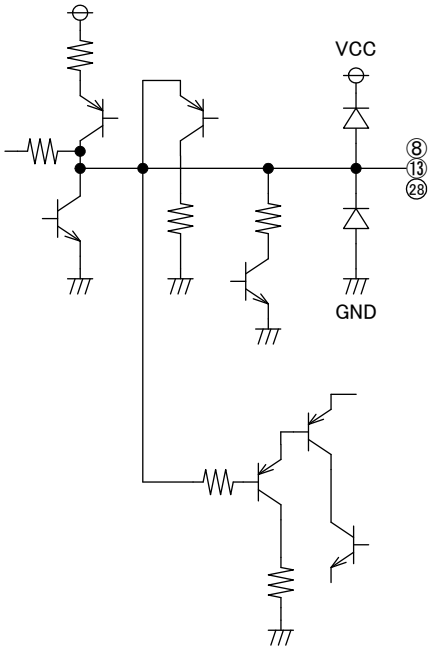
No.	Symbol	Description	No.	Symbol	Description
1	PGND1	Ch1 power GND (same potential as GND terminal)	21	PGND3	Ch3 power GND (same potential as terminal GND)
2	DRV1B	Ch1 Nch drive output terminal	22	DRV3B	Ch3 Nch drive output terminal
3	LX1	Ch1 overcurrent detection terminal	23	LX3	Ch3 overcurrent detection terminal
4	DRV1A	Ch1 Pch drive output terminal	24	DRV3A	Ch3 Pch drive output terminal
5	VIN1	Ch1 power supply input terminal	25	VIN3	Ch3 power supply input terminal
6	OCP1	Ch1 overcurrent detection level resistance connection terminal	26	OCP3	Ch3 overcurrent detection level resistance connection terminal
7	FB1	Ch1 voltage detection terminal	27	FB3	Ch3 voltage detection terminal
8	FC1	Ch1 phase compensation terminal	28	FC3	Ch3 phase compensation terminal
9	SS1	Ch1 soft start adjustment capacity connection terminal	29	SS3	Ch3 soft start adjustment capacity connection terminal
10	GND	GND (0V connection)	30	GND	GND (0V connection)
11	RT	Frequency adjustment resistance connection terminal	31	TEST1	Test terminal (Connect to GND)
12	SS2	Ch2 soft start adjustment capacity connection terminal	32	TEST2	Test terminal (connect to GND)
13	FC2	Ch2 phase compensation terminal	33	CTL1	Ch1 control terminal
14	FB2	Ch2 voltage detection terminal	34	CTL2	Ch2 control terminal
15	OCP2	Ch2 overcurrent detection level resistance connection terminal	35	CTL3	Ch3 control terminal
16	VIN2	Ch2 power supply input terminal	36	VCC	Power supply input terminal
17	DRV2A	Ch2 Pch drive output terminal	37	RESET	Reset output terminal
18	LX2	Ch2 overcurrent detection terminal	38	RSTDLY	Reset delay adjustment capacity connection terminal
19	DRV2B	Ch2 Nch drive output terminal	39	MONVCC	VCC monitor terminal
20	PGND2	Ch2 power GND (same potential as terminal GND)	40	PDET	Off latch signal output

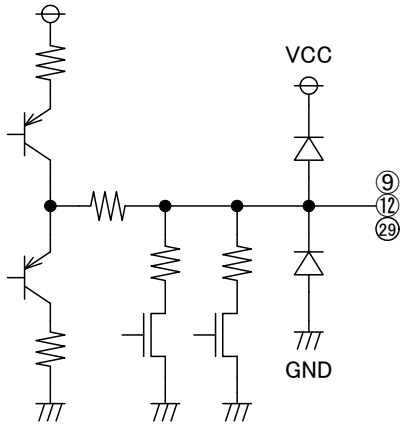
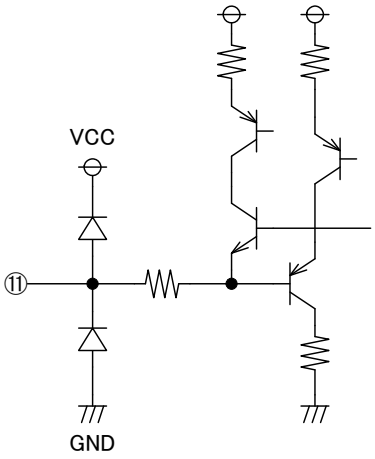
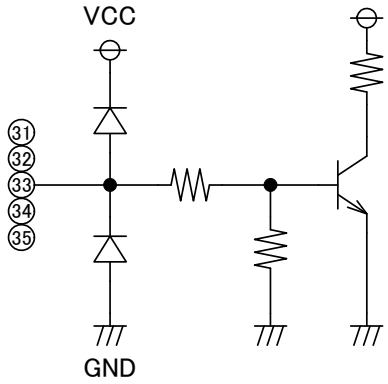
※Please give to VCC+0.3V as an operation condition in all input terminals.

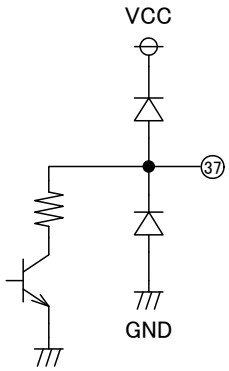
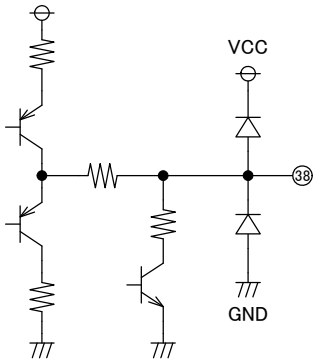
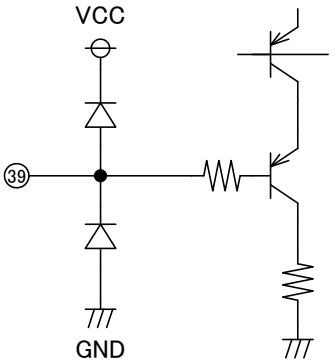
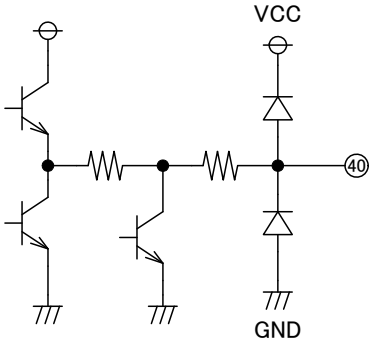
However, please do not exceed the absolute maximum rating as VCC=VIN1=VIN2=VIN3.

● Terminal equivalent circuit chart

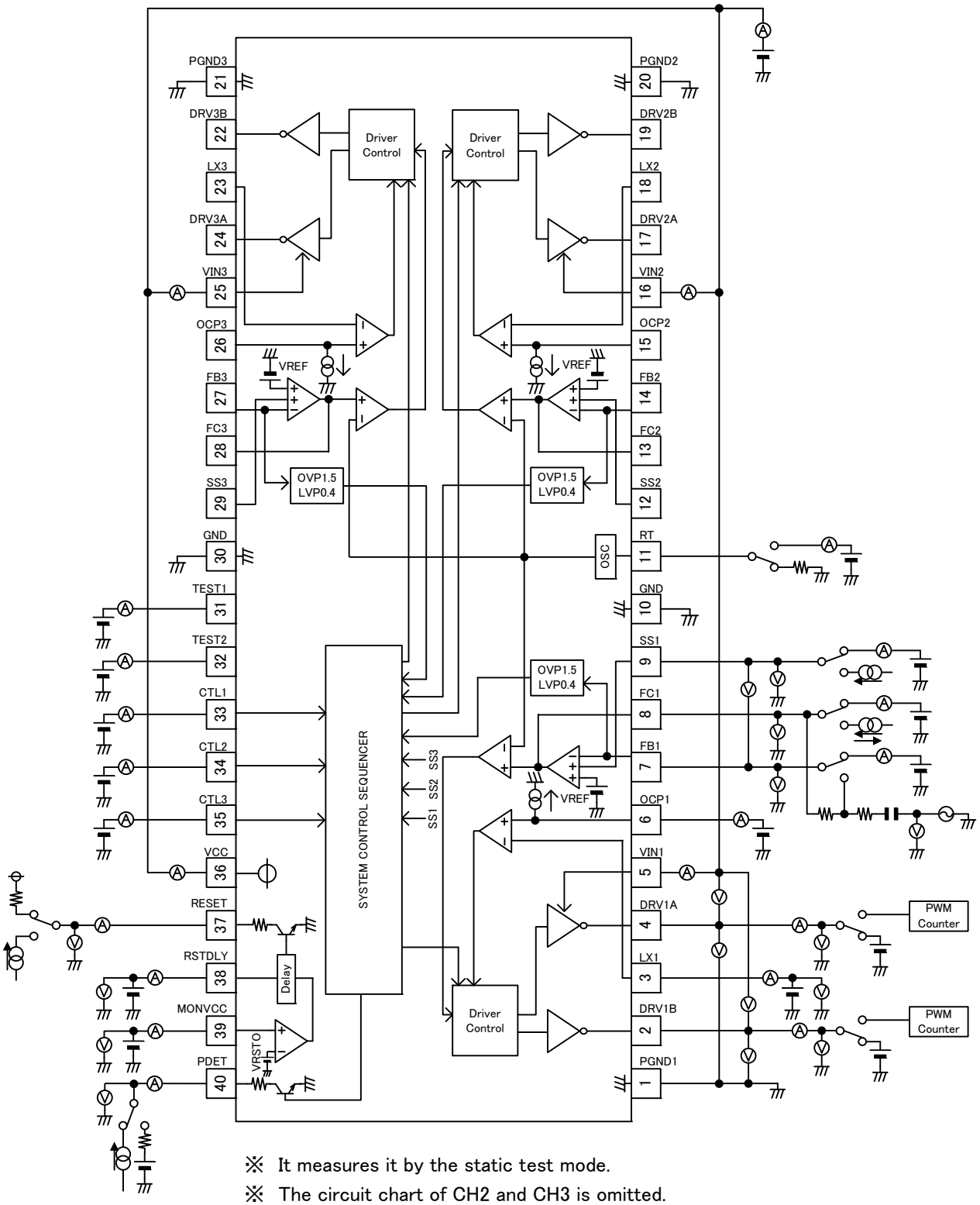
Terminal No.	Terminal name	Explanation	Terminal equivalent circuit chart
1	PGND1	Ch1 Power GND (GND Terminal and this potential)	
20	PGND2	Ch2 Power GND (GND Terminal and this potential)	
21	PGND3	Ch3 Power GND (GND Terminal and this potential)	
2	DRV1B	Ch1 Nch Driving output terminal	
19	DRV2B	Ch2 Nch Driving output terminal	
22	DRV3B	Ch3 Nch Driving output terminal	
3	LX1	Ch1 Over current detection terminal	
18	LX2	Ch2 Over current detection terminal	
23	LX3	Ch3 Over current detection terminal	
4	DRV1A	Ch1 Pch Driving output terminal	
17	DRV2A	Ch2 Pch Driving output terminal	
24	DRV3A	Ch3 Pch Driving output terminal	
5	VIN1	Ch1 Power supply input terminal	
16	VIN2	Ch2 Power supply input terminal	
25	VIN3	Ch3 Power supply input terminal	

Terminal No.	Terminal name	Explanation	Terminal equivalent circuit chart
6	OCP1	Ch1 Over current detection level Set resistance connection terminal	
15	OCP2	Ch2 Over current detection level Set resistance connection terminal	
26	OCP3	Ch3 Over current detection level Set resistance connection terminal	
7	FB1	Ch1 Voltage detection terminal	
14	FB2	Ch2 Voltage detection terminal	
27	FB3	Ch3 Voltage detection terminal	
8	FC1	Ch1 Phase amends terminal	
13	FC2	Ch2 Phase amends terminal	
28	FC3	Ch3 Phase amends terminal	

Terminal No..	Terminal name	Explanation	Terminal equivalent circuit chart
9	SS1	Ch1 Soft start Adjustment capacity connection terminal	
12	SS2	Ch2 Soft start Adjustment capacity connection terminal	
29	SS3	Ch3 Soft start Adjustment capacity connection terminal	
10	GND	GND （0V Connection）	
30	GND	GND （0V Connection）	
11	RT	Frequency adjustment resistance connection terminal	
31	TEST1	Test terminal	
32	TEST2	Test terminal	
33	CTL1	Ch1 Control terminal	
34	CTL2	Ch2 Control terminal	
35	CTL3	Ch3 Control terminal	

Terminal No.	Terminal name	Explanation	Terminal equivalent circuit chart
36	VCC	Power supply input terminal	
37	RESET	Reset output terminal	
38	RSTDLY	Reset Delay Adjustment capacity connection terminal	
39	MONVCC	VCC Monitor terminal	
40	PDET	Off latch output terminal	

● Circuit chart



※ It measures it by the static test mode.

※ The circuit chart of CH2 and CH3 is omitted.

Figure 2 Circuit chart

● Application circuit chart

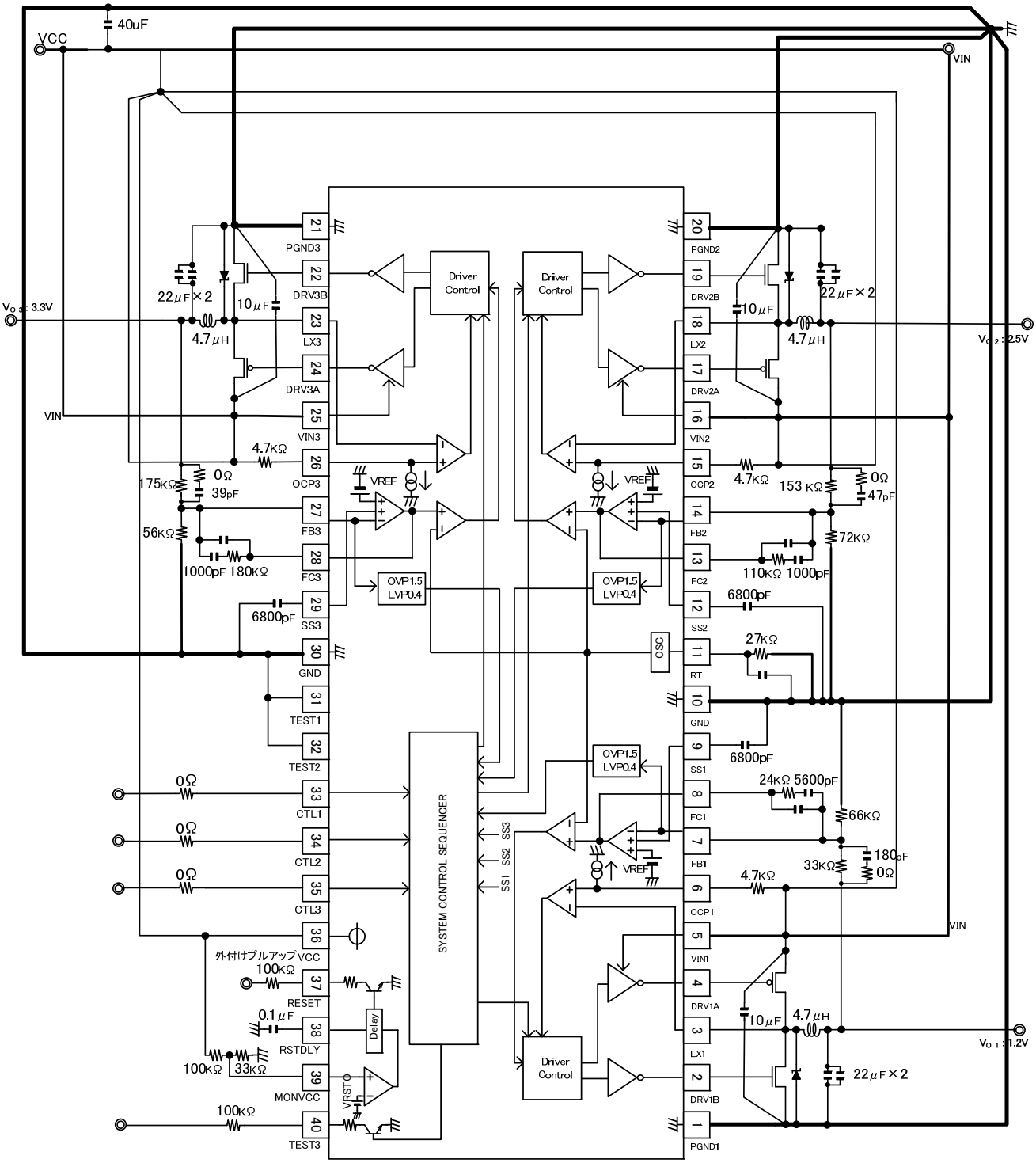


Figure 3 Application circuit chart

● . Each characteristic reference data

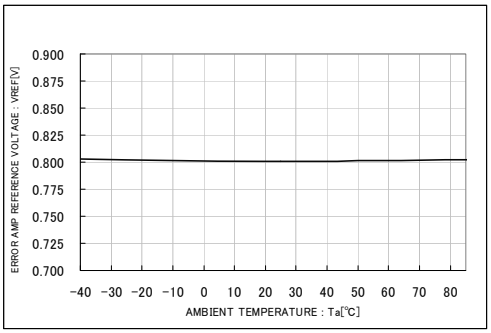


Figure 4 Standard voltage-temperature characteristic

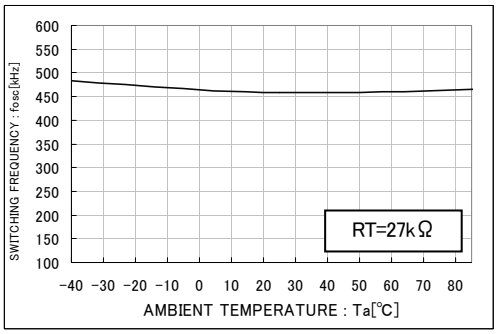


Figure 5 Switching frequency-temperature characteristic

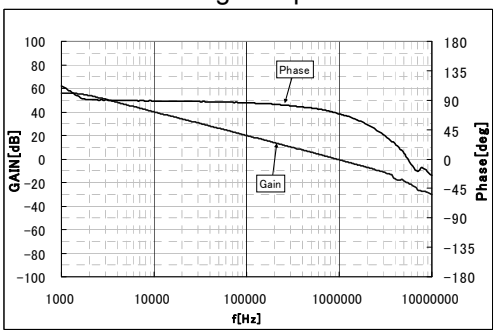


Figure 6 Open loop characteristic

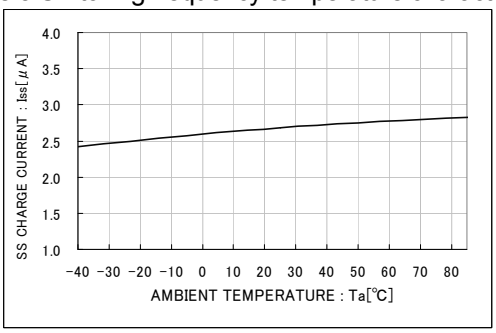


Figure 7 Terminal SS charge current-temperature characteristic

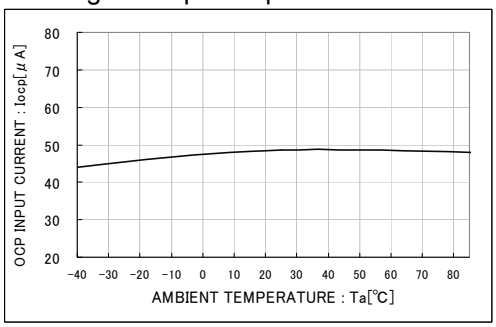


Figure 8 Terminal OCP inflow current-temperature characteristic

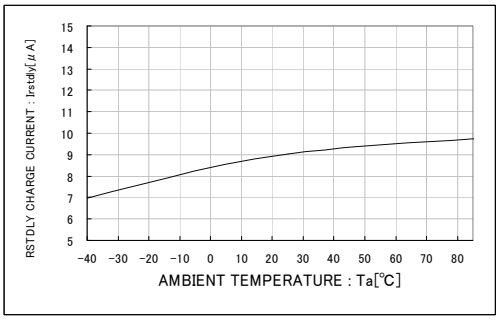


Figure 9 Terminal RSTDLY charge current-temperature characteristic

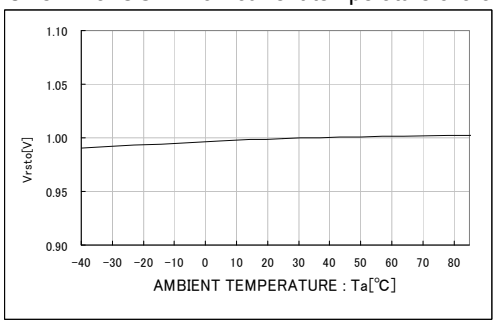


Figure 10 MONVCC reset detection voltage-temperature characteristic

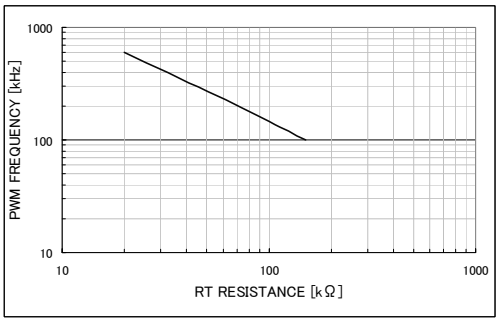


Figure 11 Switching frequency-terminal RT resistance characteristic

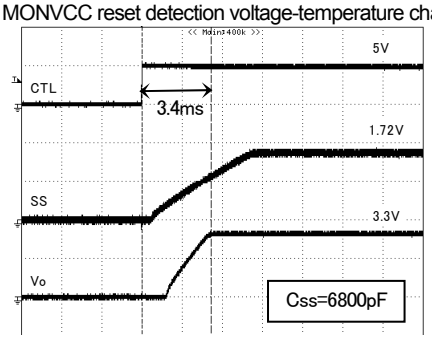


Figure 12 Soft start crimp

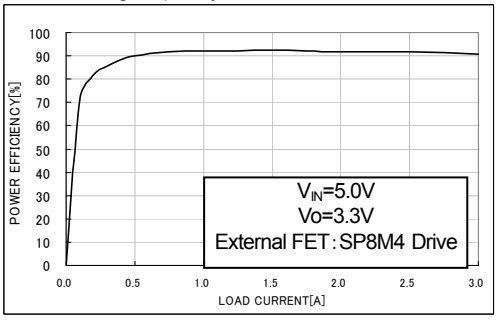


Figure 13 Efficiency

Reference data of dead time

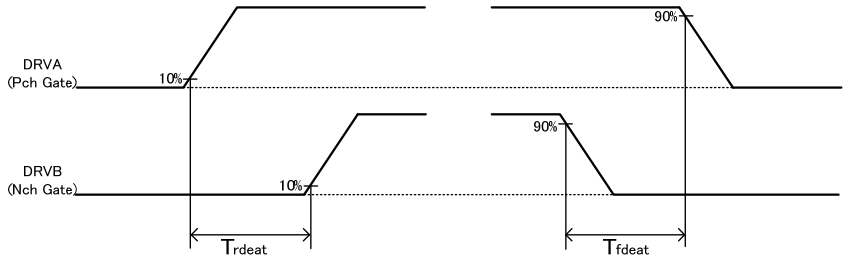


Figure 14 Dead time

(VCC=5.0V,VIN=5.0V,Ta=25℃)

Parameter	Symbol	min	typ	max	UNIT
PchMOS OFF→NchMOS ON Dead time	Trdeat	90	120	160	ns
NchMOS OFF→PchMOS ON Dead time	Tfdeat	100	140	190	ns

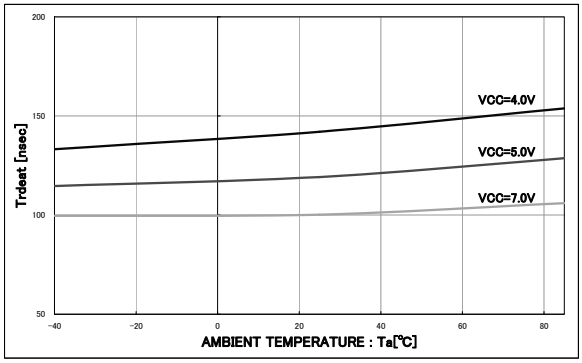


Figure 15 Dead time Trdeat - Temperature characteristic

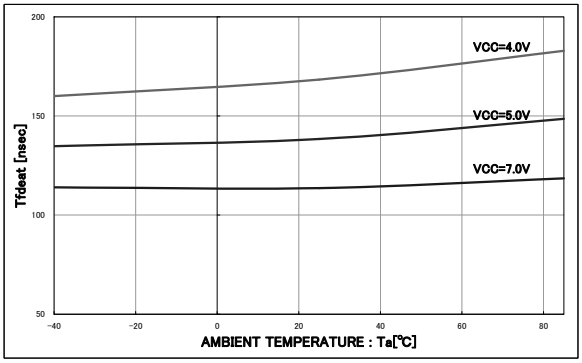


Figure 16 Dead time Tfdeat - Temperature characteristic

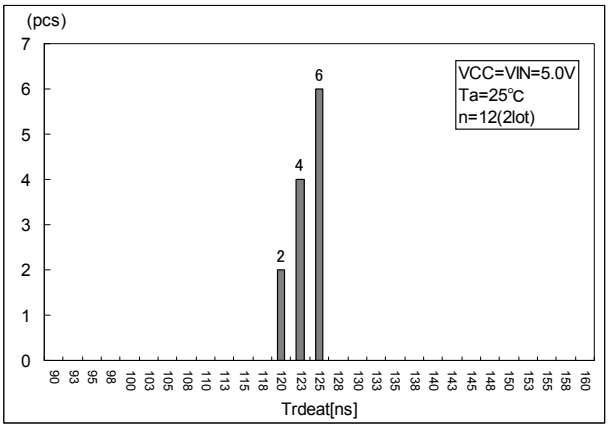


Figure 17 Dead time Trdeat - Difference

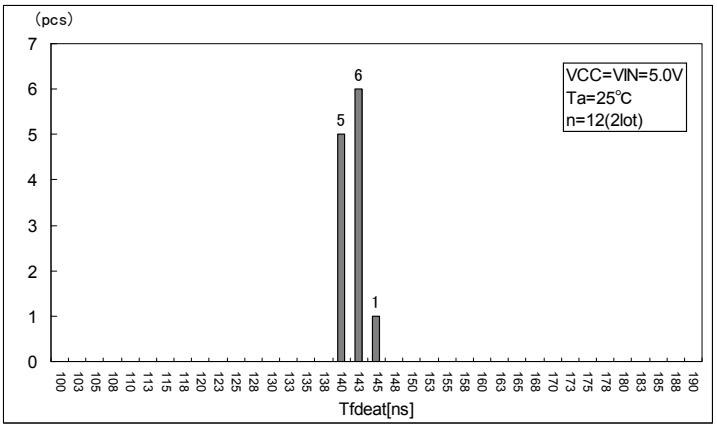


Figure 18 Dead time Tfdeat - Difference

Reset detection data

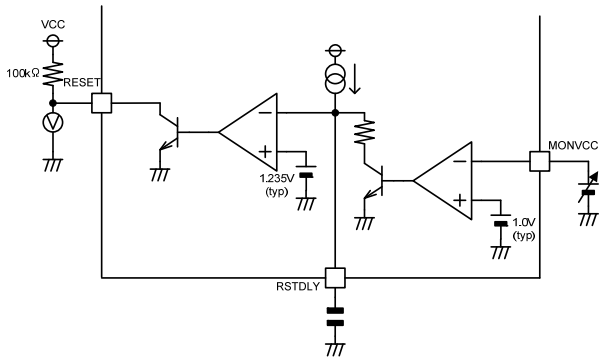


Figure 19 Circuit chart

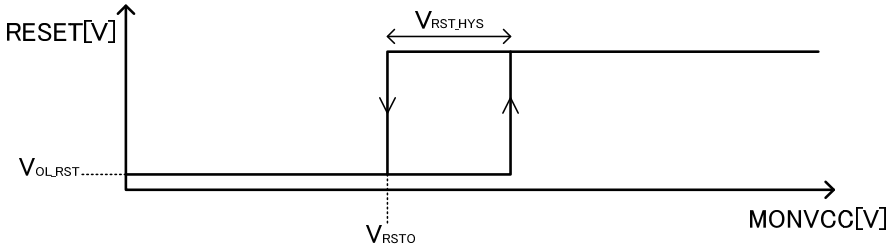


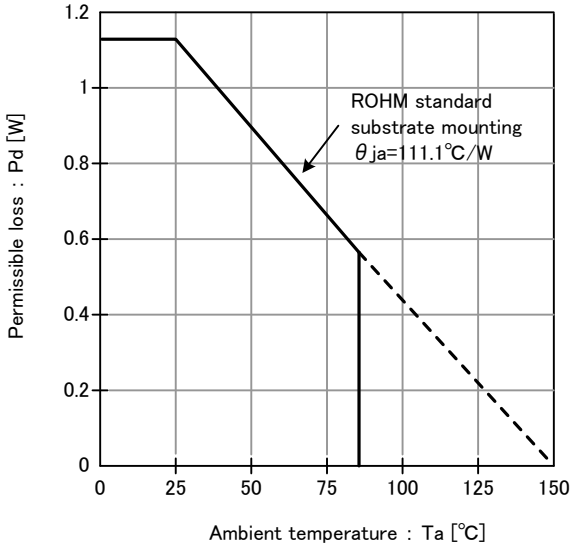
Figure 20 Reset detection

(VCC=5V,Ta=25℃)

Parameter	Symbol	min	typ	max	UNIT
Terminal MONVCC reset detection voltage	V_{RSTO}	0.98	1.0	1.02	V
Terminal MONVCC reset detection voltage Maximum hysteresis error	V_{RST_HYS}	20	72	180	mV

Permissible loss

θ jc [℃/W]	θ ja [℃/W]	T_{STGmin} [℃]	T_{STGmax} [℃]	$T_{a\,min}$ [℃]	$T_{a\,max}$ [℃]	T_{cmax} Destruction temperature [℃]	$T_{j\,max}$ Destruction temperature [℃]
28.0	111.1	-50.0	150.0	-45.0	85.0	150.0	150.0



ROHM standard substrate specification
Material The glass epoxy
Size 70mm × 70mm × 1.6mmt

Figure 2 Heat decrease curve

※These values are the example values, and no guarantee values.

● Operation description

ON/OFF control

DC/DC converter controller ON/OFF function

DC/DC converter controller of each Ch can be independently controlled ON/OFF by CTL1, CTL2, and CTL3 terminal.

Analog circuit of Ch interlocked to each CTL terminal starts operation at ON control (on mode), and goes down to setting output voltage.

Analog circuit of Ch interlocked to each CTL terminal should be standby at OFF control (off mode), and output voltage becomes 0V.

Table1 DC/DC converter controller ON/OFF function

CTL1 terminal voltage	Ch1	CTL2 terminal voltage	Ch2	CTL3 terminal voltage	Ch3
>VIHCTL1	ON control	>VIHCTL2	ON control	>VIHCTL3	ON control
<VILCTL1	OFF control	<VILCTL2	OFF control	<VILCTL3	OFF control

Soft start time set function

DC/DC converter controller of each Ch can do soft start without overshoot by charging soft start capacity (Css) connected between ss terminal and GND in each Ch by charging current at ON control.

The mute of the output is released when it reaches V_{SS}=0.15V (V_{SSSTB}), and the output voltage does the soft start operation from the point of V_{SS}=0.3V (typ) in proportion to the voltage of the terminal SS.

Also, soft start time (tss) can be set by setting soft start capacity arbitrarily.

Soft start time (tss) should be set at 3msec < tss < 30msec.

※Please note that the overshoot is not caused in the output setting voltage when setting it to tss≦3msec.

$$t_{SS} = 400us + \frac{1.1V \times C_{SS}}{2.5uA}$$

Discharge function

DC/DC converter controller of each Ch can do soft off by discharging load discharged to soft start capacity connected between SS terminal to GND by discharging resistance at OFF control.

Soft off operates in proportion to the voltage of the terminal SS the output voltage from the point of VSS=0.8V (typ).

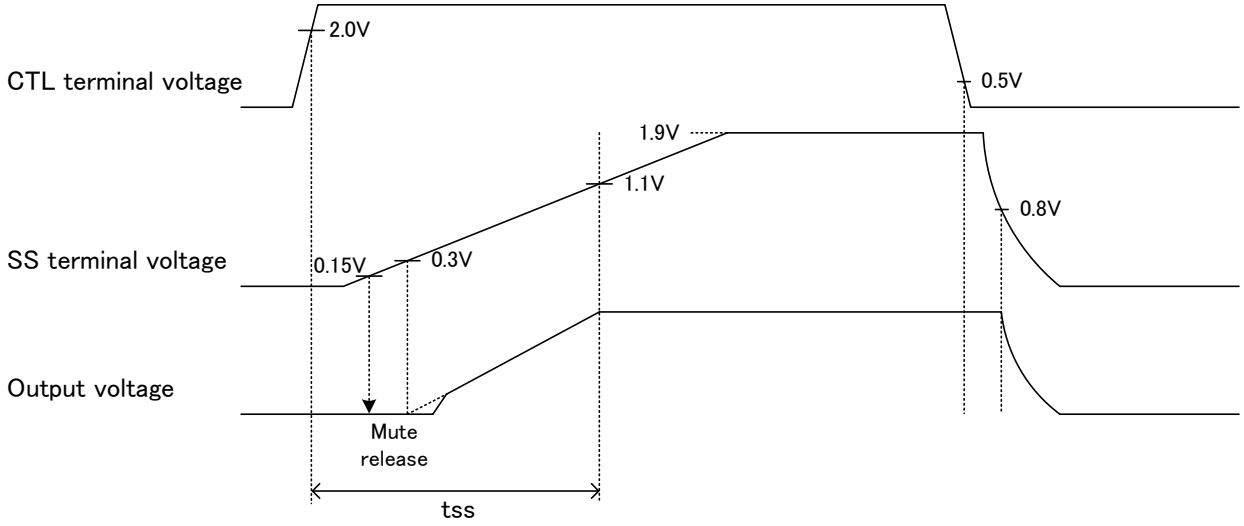


Figure 22 Wave form at ON/OFF control

OSC oscillation frequency setting function

DRVA and DRVB output oscillation frequency of DC/DC converter controller of each Ch can be set by installing resistance between RT terminal and GND externally.

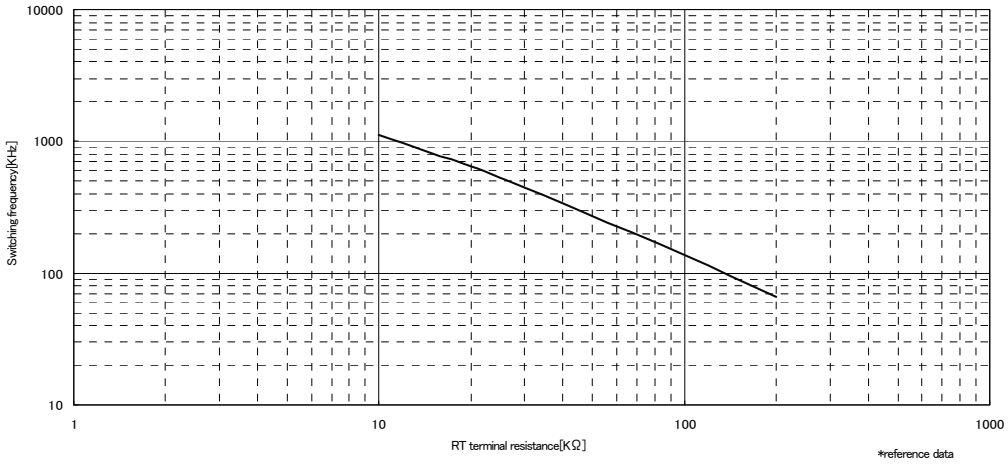


Figure 23 Terminal RT resistance-oscillation frequency

Off latch signal output function

PDET terminal outputs condition of off latch when protection operation of DC/DC converter controller of each Ch operates.

Table 2 PDET terminal　off latch signal output function

Protection operation	Terminal PDET
ON	LOW
OFF	Hi-Z

Reset output function

Reset output function observes voltage value from MONVCC terminal and does reset operation compared to internal reference level.

Set MONVCC terminal external resistance to make VCC voltage more than 5.0V at reset release.

Table 3 DC/DC converter controller ON/OFF function

MONVCC terminal voltage	RESET terminal
＜1.0V(typ)	LOW
＞1.072V(typ)	Hi-Z

Delay time until detecting reset release is settable by capacitor connected to RSTDLY terminal.

$$T_{RSTDLY} = \frac{1.235V \times C_{RSTDLY}}{I_{RSTDLY}}$$

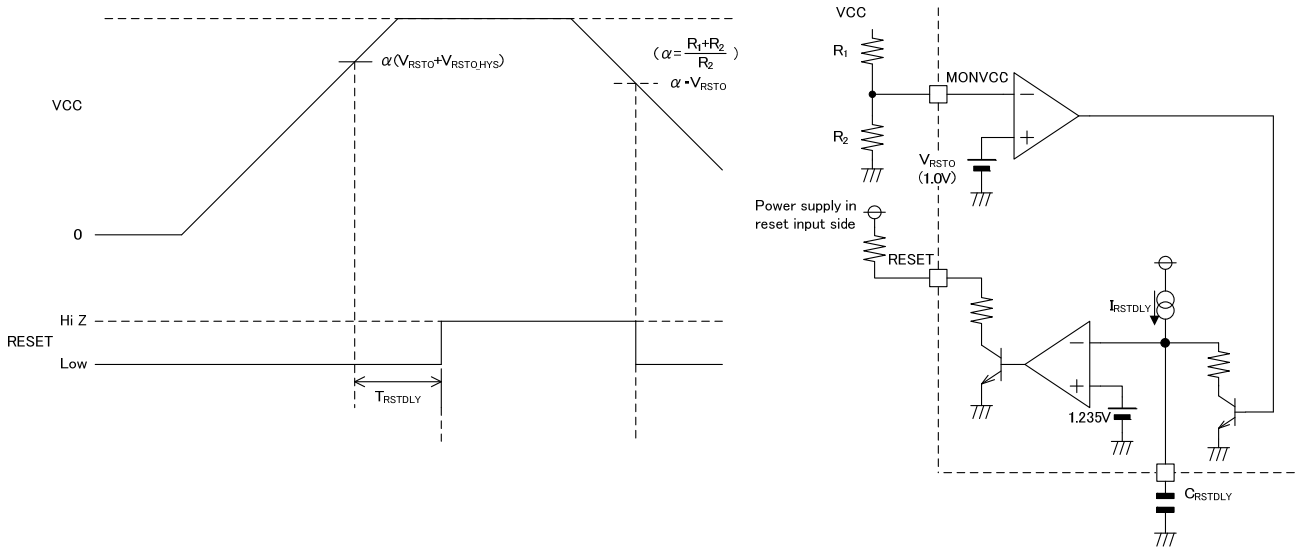


Figure 24 Reset operation

(TRSTDLY : Delay time until detecting reset release)

Output Duty

Output Duty of DRVA of the DC/DC converter controller of each Ch is decided depending on the voltage of the terminal FC of each Ch.

$$Setting\ output\ Duty = \frac{Output\ setting\ voltage}{VIN\ voltage} \times 100 \quad [\%]$$

$$9\% \ < \ Setting\ output\ Duty \ < \ 92\%$$

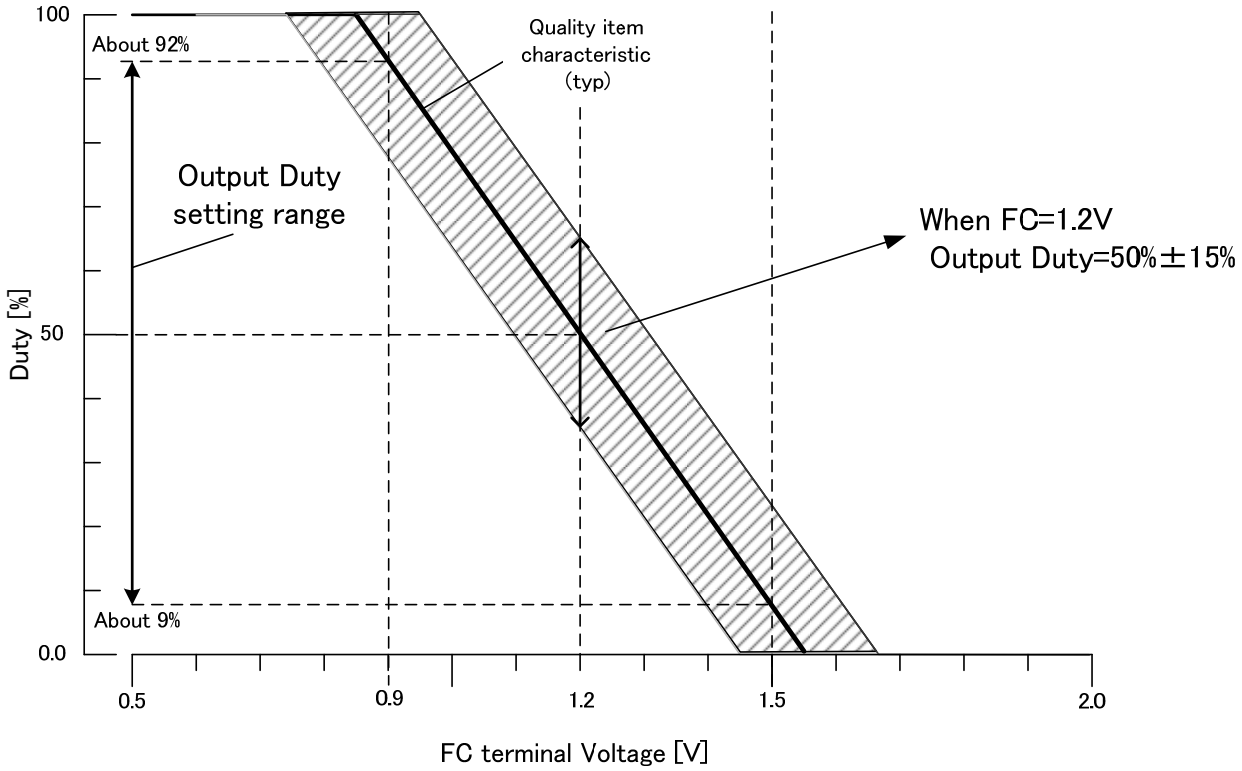


Figure 25 FC Voltage-Output Duty Linearity

● Protection function

Protection circuit is effective for destruction prevention due to accident so that avoid using by continuous protection operation.

Low voltage protection function(LVP)

Low voltage protection function detects output voltage V_O set in each Ch from FB terminal of each Ch and off-latched all DC/DC converter controller compared to internal reference level.

Low voltage protection function operates when FB terminal voltage falls below V_{LVP} (=1.5 × VREF) and continues about more than 400μsec (typ).

Table 4 Low voltage protection function

CTL terminal	SS terminal	FB terminal	Low voltage protection function	Low voltage protection operation
>V_{IHCTL}	>1.1V(typ)	<V_{LVP}	Enable	ON
		>V_{LVP}+V_{LVP_HYS}		OFF
	<1.0V(typ)	-	Disable	OFF
<V_{ILCTL}	-	-	Disable	OFF

※Constant voltage protection function is enabled when SS terminal voltage of each Ch becomes more than 1.1V (typ) in the transition to ON control (during soft start).

Overvoltage protection function(OVP)

Overvoltage protection function detects output voltage VO set in each Ch from FB terminal of each Ch and off-latched all DC/DC converter controller compared to internal reference level.

Overvoltage protection function operates when FB terminal voltage exceeds VOVP (=1.5 × VREF) and continues about more than 400μsec (typ).

Table 5 Overvoltage protection function

CTL terminal	SS terminal	FB terminal	Overvoltage protection function	Overvoltage protection operation
>V_{IHCTL}	>1.1V(typ)	>V_{OVP}	Effective	ON
		<V_{OVP}		OFF
	<1.0V(typ)	-	Invalidity	OFF
<V_{ILCTL}	-	-	Invalidity	OFF

※Overvoltage protection function is enabled when SS terminal voltage of each Ch becomes more than 1.1V (typ) in the transition to ON control (during soft start).

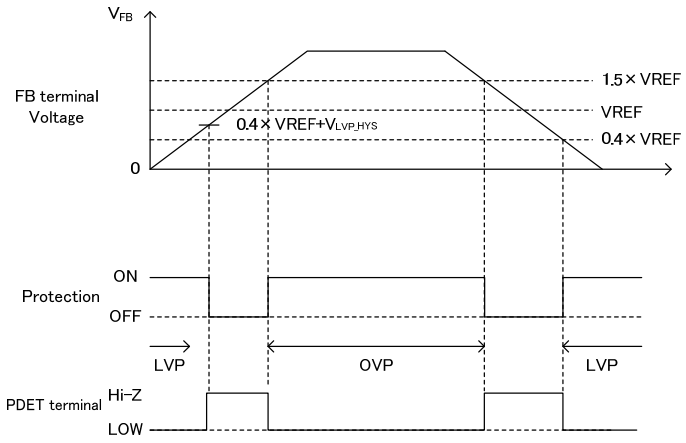


Figure 26 Low voltage and over voltage protection

Overcurrent protection function(OCP)

Overcurrent protection function compared drain voltage (LX terminal voltage) with OCP terminal voltage when external Pch POWER MOS is ON. When LX terminal voltage becomes lower than OCP terminal voltage, external MOS would be OFF. Up to 50uA (typ) of constant current from OCP terminal is synchronized. Overcurrent detection level (OCP terminal voltage) can be set arbitrarily by external resistance value.

Off latch by overcurrent protection function operates when LX terminal voltage falls below OCP terminal voltage and continues about more than 400μsec (typ).

Table 6 overcurrent protection function

CTL terminal	SS terminal	LX terminal voltage	Overcurrent protection function	Overcurrent protection operation
>V_{IHCTL}	>1.1V(typ)	<V_{OCP}	Enable	ON
		>V_{OCP}		OFF
	<1.0V(typ)	-	Disable	OFF
<V_{ILCTL}	-	-	Disable	OFF

※Set OCP terminal voltage to be more than VIN-2.5V (typ).

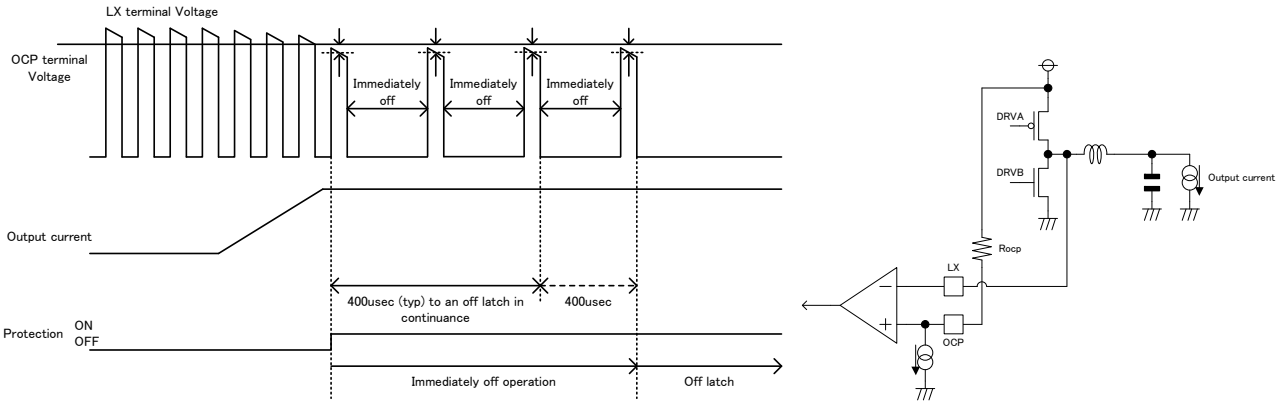
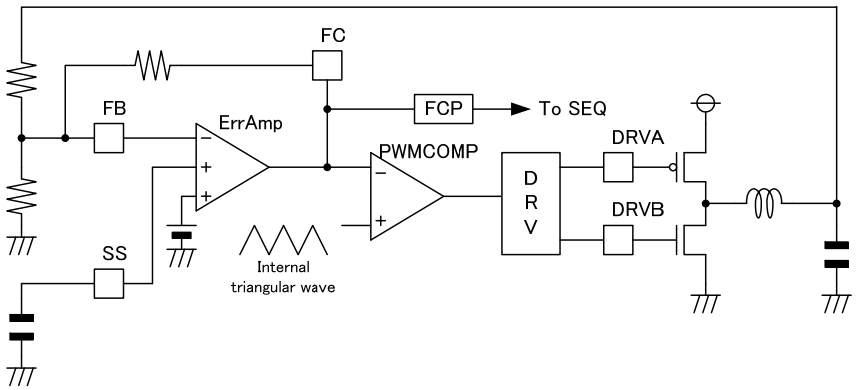
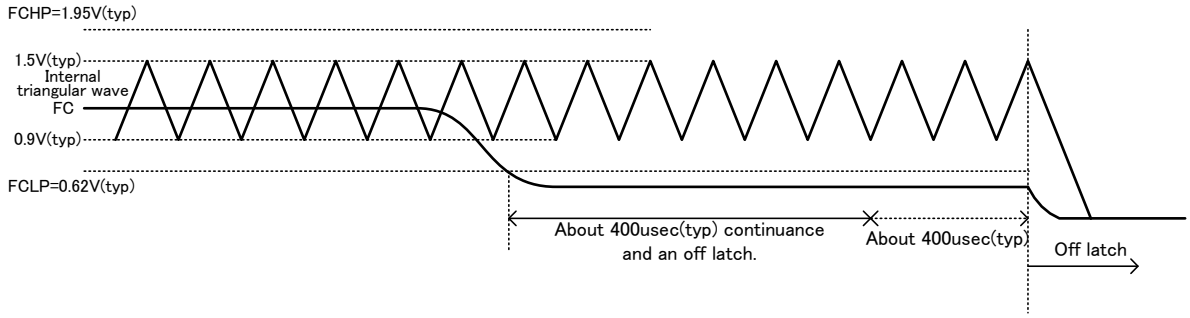


Figure 27 Overcurrent protection

Terminal FC abnormality protection function





The terminal FC abnormality protection function Ofrattis it all DC/DC converter controller detecting the continuance of the state that FC which is the difference input of PWMCOMP does not intersect with an internal triangular wave.
The terminal FC abnormality protection function is exceeded 1.95V(typ) by the voltage of the terminal FC or operates when it falls below 0.62V(typ), and about 400usec(typ) or more continues.

CTL terminal	SS terminal	Protection operation	FC terminal	Terminal FC abnormality protection operation
> V_{IHCTL}	> 1.1V(typ)	Enable	> 1.95V(typ)	ON
			0.62V(typ) < , < 1.95V(typ)	OFF
	< 1.0V(typ)	Disable	< 0.62V(typ)	ON
< V_{IHCTL}			-	OFF

※Terminal FC abnormality protection function is enabled when SS terminal voltage of each Ch becomes more than 1.1V (typ) in the transition to ON control (during soft start).

RT terminal open/short protection function

RT terminal open/shot protection function off-latches all DC/DC converter controller by detecting open/short condition internally from RT terminal to prevent from output voltage error caused by abnormal oscillation of internal triangular wave at RT terminal open/short.

RT terminal open/short protection function is regularly enabled after boot-up.
RT terminal open/short protection function operates when error detection condition continues about more than 400µsec (typ).

Soft start time-out function

Each Ch DC/DC converter controller off-latch-controls when V_{SS} does not exceed V_{SSPON} from $V_{SS} > V_{SSSTB}+V_{SSSTB\_HYS}$ after 50msec (typ) passed from soft start.

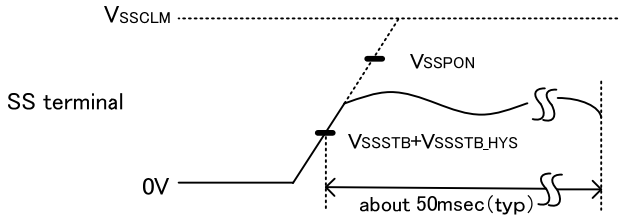


Figure 28 At soft start time-out

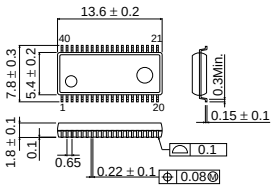
Error detection (off latch) release method

Each Ch DC/DC converter controller comes into off latch condition when protection function operates. Off latch can be released by the following method. Each Ch DC/DC converter controller becomes able to do ON control transition by releasing off latch.

1. Set all Ch CTL terminal voltage as $< V_{ILCTL}$ and continue that condition about more than 200usec (typ).
2. Drop down power supply VCC to below 3.7V.

SSOP-B40

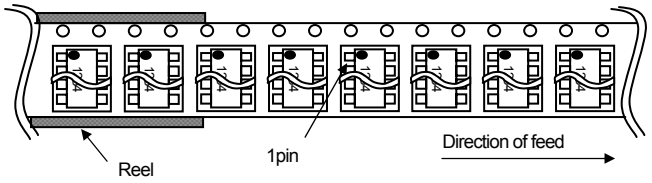
<Dimension>



(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

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