
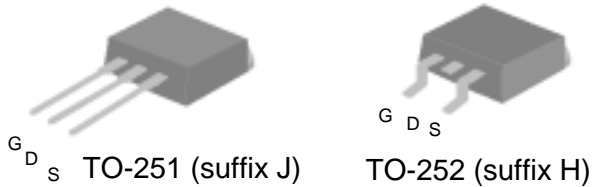


N-channel Enhancement-mode Power MOSFET

PRODUCT SUMMARY

BV_{DSS}	30V
$R_{DS(ON)}$	9m Ω
I_D	60A

 **Pb-free; RoHS-compliant TO-251 (IPAK) and TO-252 (DPAK)**



DESCRIPTION

The SSM70T03 achieves fast switching performance with low gate charge without a complex drive circuit. It is suitable for low voltage applications such as DC/DC converters and general load-switching circuits.

The SSM70T03GH is in a TO-252 package, which is widely used for commercial and industrial surface-mount applications.

The through-hole version, the SSM70T03GJ in TO-251, is available for vertical mounting, where a small footprint is required on the board, and/or an external heatsink is to be attached.

These devices are manufactured with an advanced process, providing improved on-resistance and switching performance. The devices have a maximum junction temperature rating of 175°C for improved thermal margin and reliability.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Units
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Continuous drain current, $T_C = 25^\circ\text{C}$	60	A
	$T_C = 100^\circ\text{C}$	43	A
I_{DM}	Pulsed drain current ¹	195	A
P_D	Total power dissipation, $T_C = 25^\circ\text{C}$	53	W
	Linear derating factor	0.36	W/ $^\circ\text{C}$
E_{AS}	Single pulse avalanche energy ³	29	mJ
T_{STG}	Storage temperature range	-55 to 175	$^\circ\text{C}$
T_J	Operating junction temperature range	-55 to 175	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Units
$R_{\theta JC}$	Maximum thermal resistance, junction-case	2.8	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum thermal resistance, junction-ambient	110	$^\circ\text{C}/\text{W}$

Notes:

1. Pulse width must be limited to avoid exceeding the safe operating area.
2. Pulse width <300us, duty cycle <2%.
3. $V_{DD}=25\text{V}$, $L=100\mu\text{H}$, $R_G=25\Omega$, $I_{AS}=24\text{A}$.

ELECTRICAL CHARACTERISTICS (at $T_j = 25^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-source breakdown voltage	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown voltage temperature coefficient	Reference to 25°C , $I_D=1\text{mA}$	-	0.032	-	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static drain-source on-resistance	$V_{GS}=10V, I_D=33A$	-	-	9	$\text{m}\Omega$
		$V_{GS}=4.5V, I_D=20A$	-	-	18	$\text{m}\Omega$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	3	V
g_{fs}	Forward transconductance	$V_{DS}=10V, I_D=33A$	-	35	-	S
I_{DSS}	Drain-source leakage current	$V_{DS}=30V, V_{GS}=0V$	-	-	1	μA
		$V_{DS}=24V, V_{GS}=0V, T_j=175^\circ\text{C}$	-	-	250	μA
I_{GSS}	Gate-source leakage current	$V_{GS}=\pm 20V$	-	-	± 100	nA
Q_g	Total gate charge ²	$I_D=33A$	-	16.5	-	nC
Q_{gs}	Gate-source charge	$V_{DS}=20V$	-	5	-	nC
Q_{gd}	Gate-drain ("Miller") charge	$V_{GS}=4.5V$	-	10.3	-	nC
$t_{d(on)}$	Turn-on delay time ²	$V_{DS}=15V$	-	8.2	-	ns
t_r	Rise time	$I_D=33A$	-	105	-	ns
$t_{d(off)}$	Turn-off delay time	$R_G=3.3\Omega, V_{GS}=10V$	-	21.4	-	ns
t_f	Fall time	$R_D=0.45\Omega$	-	8.5	-	ns
C_{iss}	Input capacitance	$V_{GS}=0V$	-	1485	-	pF
C_{oss}	Output capacitance	$V_{DS}=25V$	-	245	-	pF
C_{riss}	Reverse transfer capacitance	$f=1.0\text{MHz}$	-	170	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward voltage ²	$I_S=60A, V_{GS}=0V$	-	-	1.3	V
t_{rr}	Reverse-recovery time ²	$I_S=30A, V_{GS}=0V,$	-	29	-	ns
Q_{rr}	Reverse-recovery charge	$di/dt=100A/\mu s$	-	12	-	nC

Notes:

1. Pulse width must be limited to avoid exceeding the safe operating area.
2. Pulse width < 300 μs , duty cycle < 2%.
3. $V_{DD}=25V, L=100\mu H, R_G=25\Omega, I_{AS}=24A$.

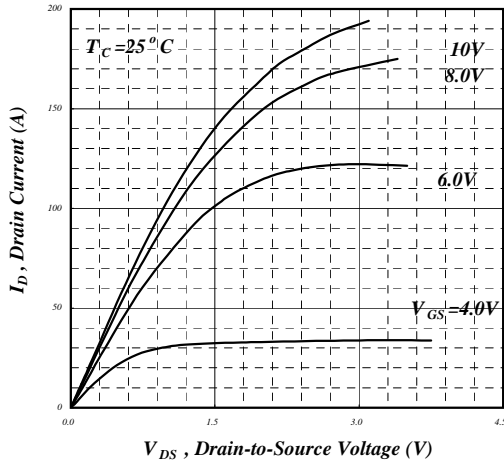


Fig 1. Typical Output Characteristics

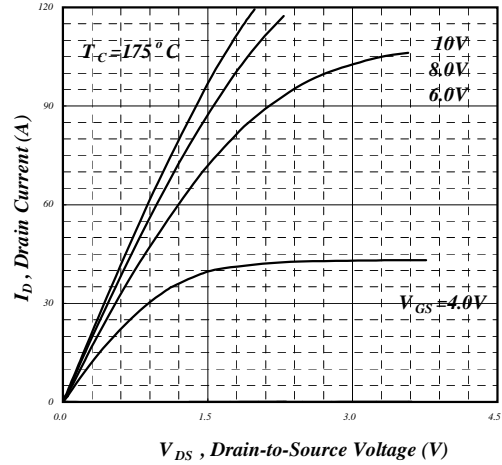


Fig 2. Typical Output Characteristics

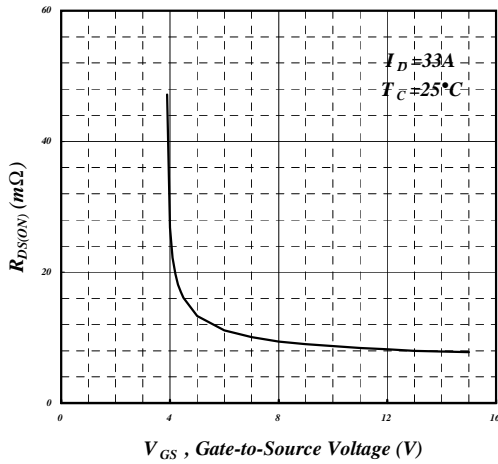


Fig 3. On-Resistance vs. Gate Voltage

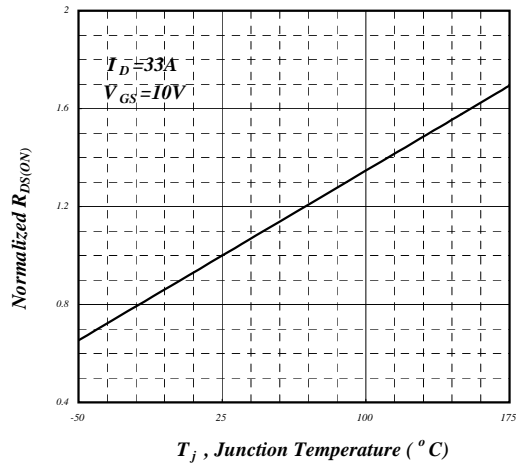


Fig 4. Normalized On-Resistance vs. Junction Temperature

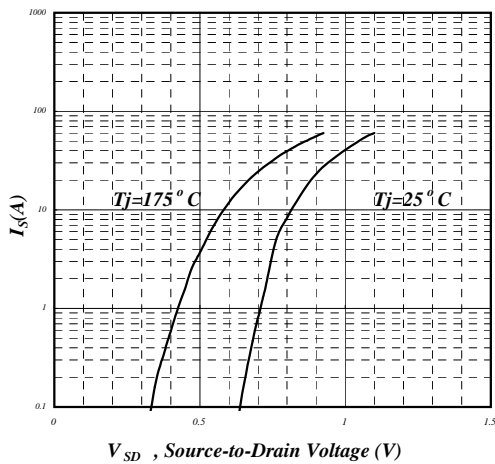


Fig 5. Forward Characteristic of Reverse Diode

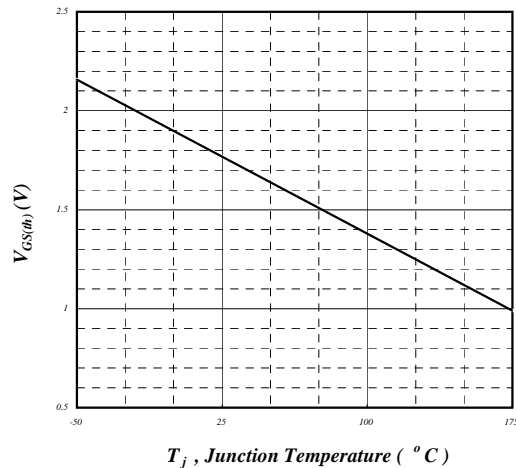


Fig 6. Gate Threshold Voltage vs. Junction Temperature

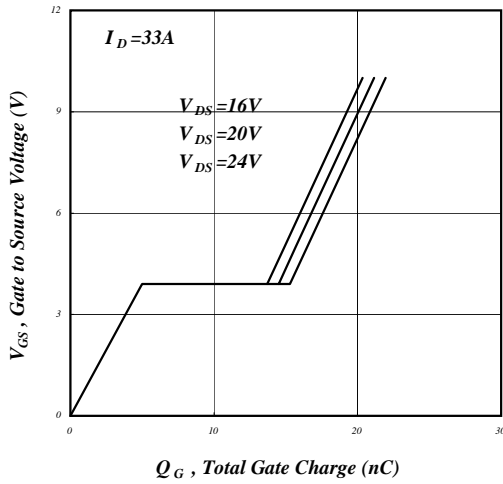


Fig 7. Gate Charge Characteristics

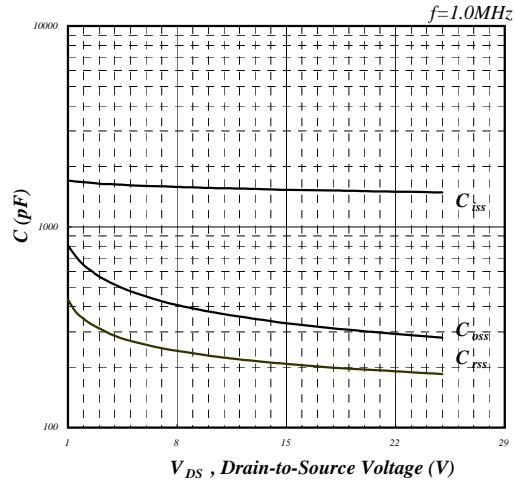


Fig 8. Typical Capacitance Characteristics

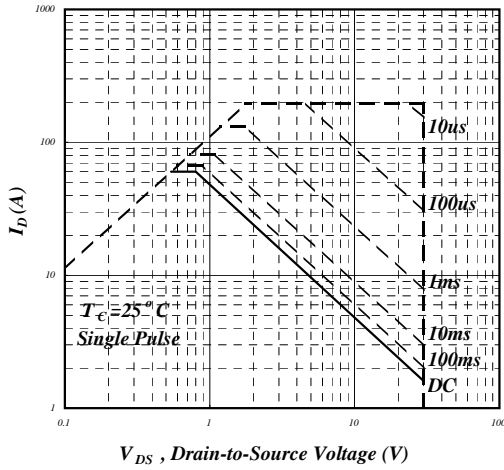


Fig 9. Maximum Safe Operating Area

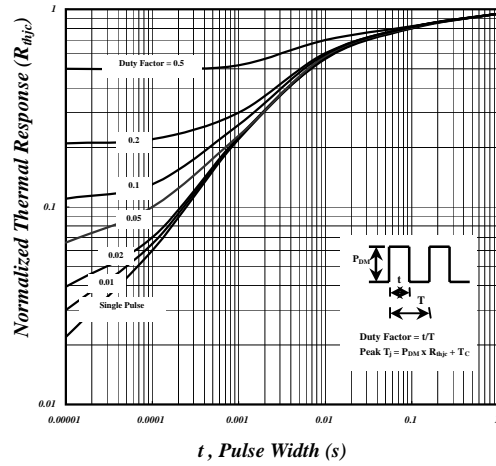


Fig 10. Effective Transient Thermal Impedance

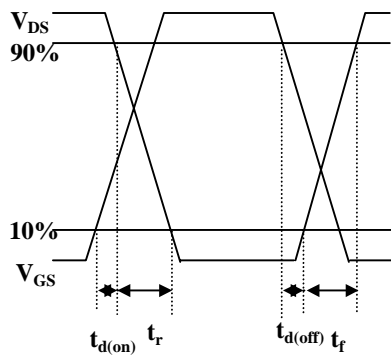


Fig 11. Switching Time Waveform

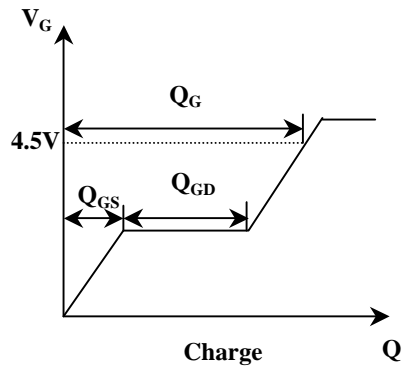
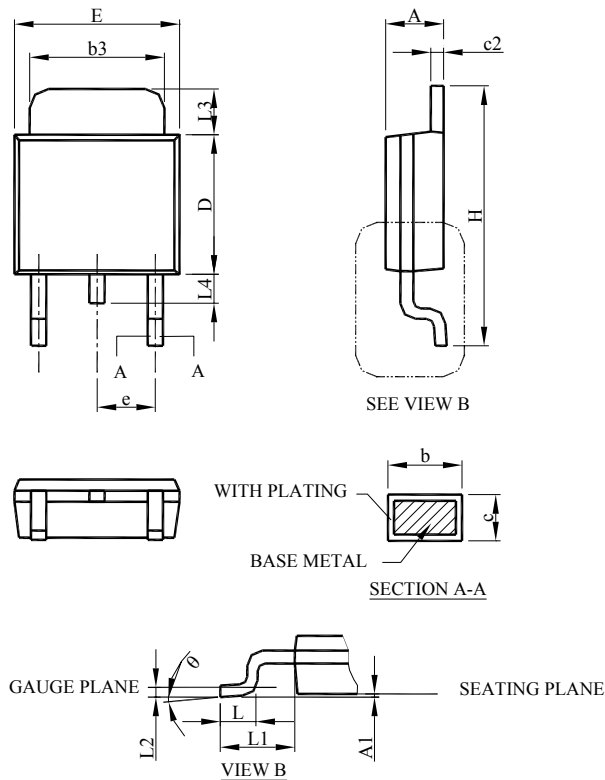


Fig 12. Gate Charge Waveform

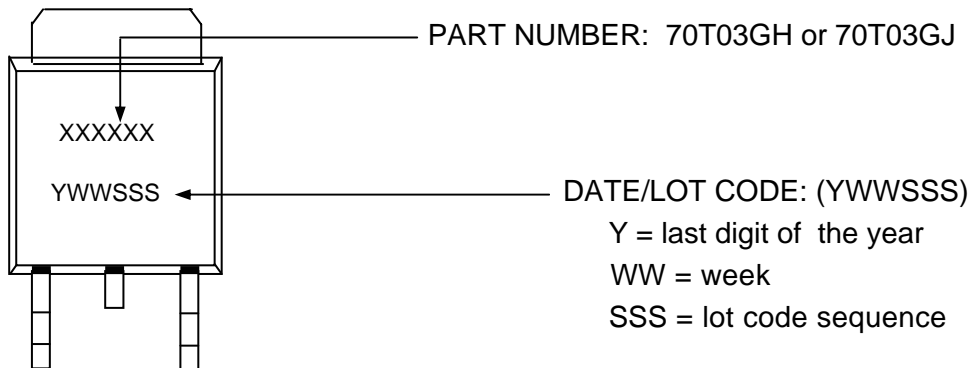
PHYSICAL DIMENSIONS



SYMBOL	TO-252-3L	
	MILLIMETERS	
	MIN.	MAX.
A	1.80	2.80
A1	0.00	0.13
b	0.40	1.00
b3	4.80	5.90
c	0.35	0.65
c2	0.40	0.89
D	5.10	6.30
E	6.00	7.00
e	2.30 BSC	
H	7.80	11.05
L	1.00	2.55
L1	2.20	3.05
L2	0.35	0.65
L3	0.50	2.03
L4	0.50	1.20
θ	0°	8°

*Dimensions do not include mold protrusions.

PART MARKING



PACKING: Moisture sensitivity level MSL3

TO-252: 3000 pcs in antistatic tape on a reel packed inside a moisture barrier bag (MBB).

TO-251: 1000pcs in an antistatic bag packed inside a moisture barrier bag (MBB).

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