

PHK18NQ03LT

N-channel TrenchMOS logic level FET

Rev. 01 — 18 December 2006

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

1.2 Features

- Optimized for use in DC-to-DC converters
- Logic level compatible
- Very low switching and conduction losses

1.3 Applications

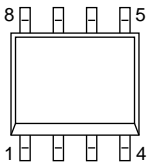
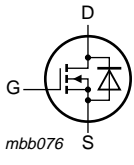
- DC-to-DC converters
- Voltage regulators
- Switched-mode power supplies
- Notebook computers

1.4 Quick reference data

- $V_{DS} \leq 30\text{ V}$
- $I_D \leq 20.3\text{ A}$
- $R_{DS(on)} \leq 8.9\text{ m}\Omega$
- $Q_{GD} = 2.5\text{ nC (typ)}$

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1, 2, 3	source (S)		
4	gate (G)		
5, 6, 7, 8	drain (D)		

SOT96-1 (SO8)

3. Ordering information

Table 2. Ordering information

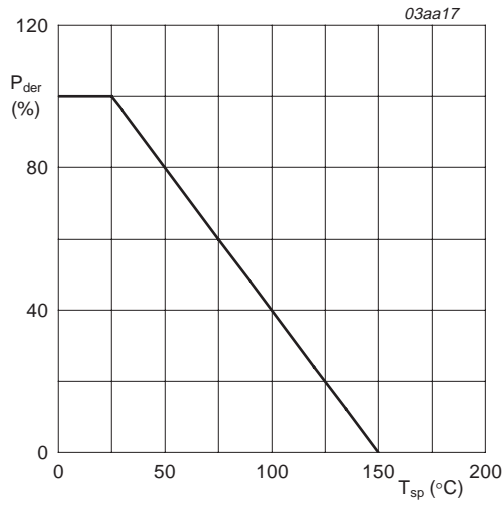
Type number	Package		Version
	Name	Description	
PHK18NQ03LT	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4. Limiting values

Table 3. Limiting values

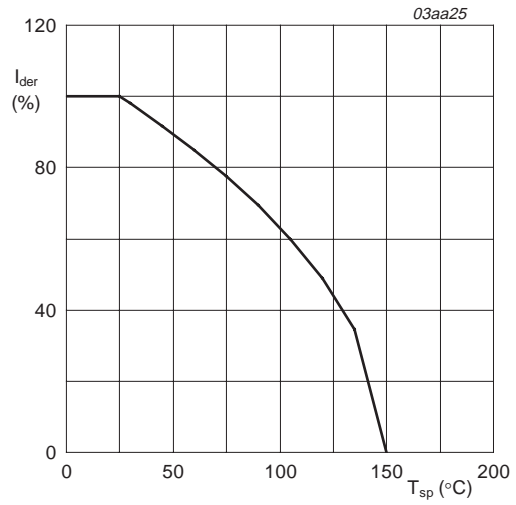
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	gate-source voltage		-	± 20	V
I_D	drain current	$T_{sp} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 2 and 3	-	20.3	A
		$T_{sp} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 2	-	12.1	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; see Figure 3	-	80	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; see Figure 1	-	6.25	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C
Source-drain diode					
I_S	source current	$T_{sp} = 25\text{ °C}$	-	5.2	A
I_{SM}	peak source current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	20.8	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 31.5\text{ A}$; $t_p = 0.07\text{ ms}$; $V_{DS} \leq 25\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; starting at $T_j = 25\text{ °C}$	-	50	mJ



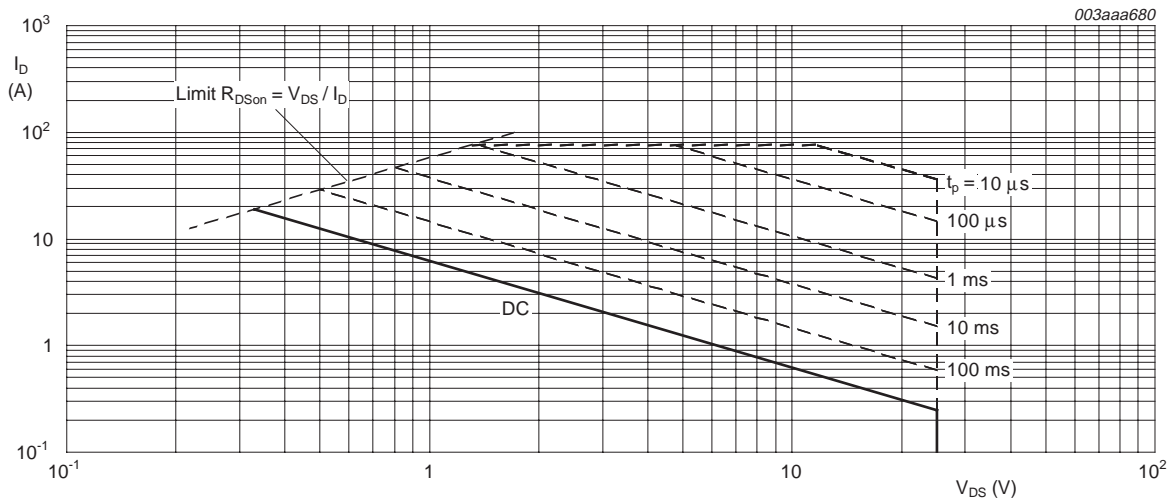
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature



T_{sp} = 25 °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see Figure 4	-	-	20	K/W

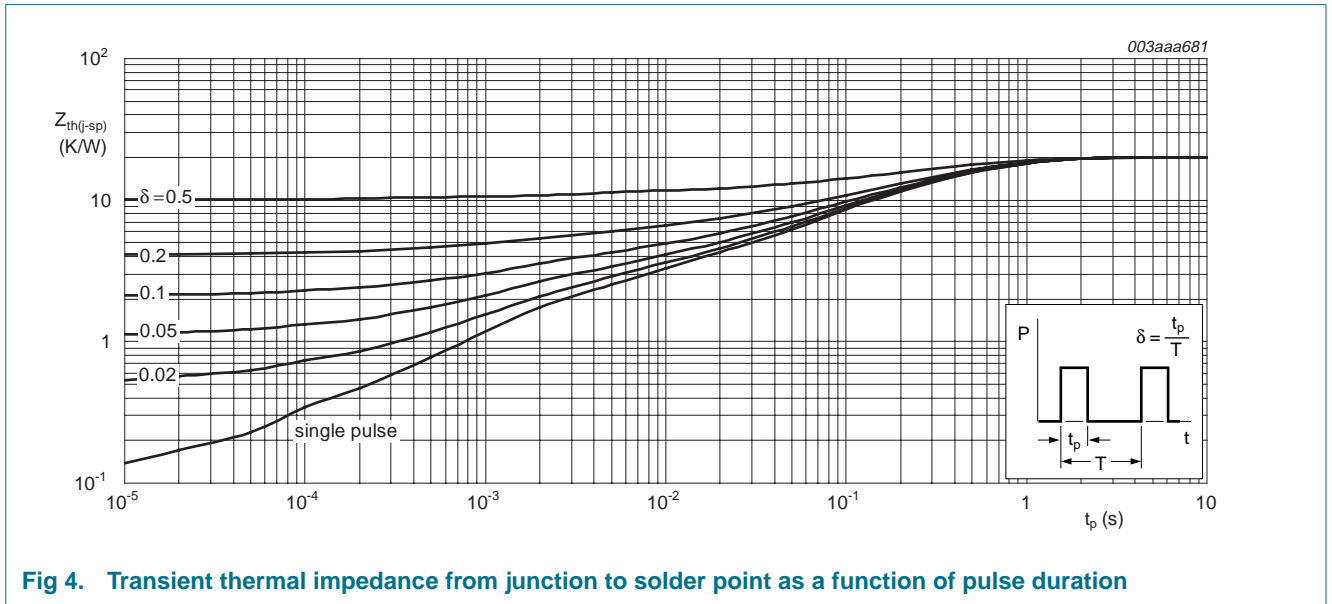


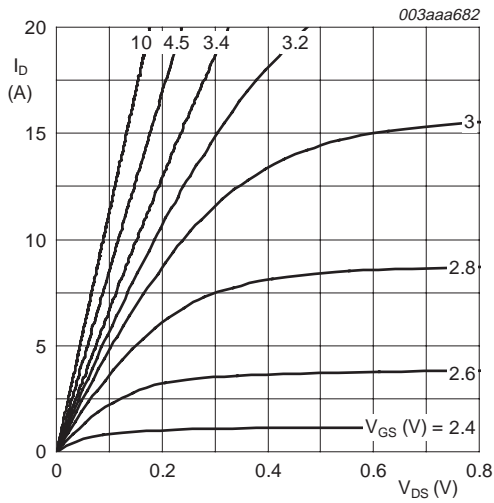
Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

6. Characteristics

Table 5. Characteristics

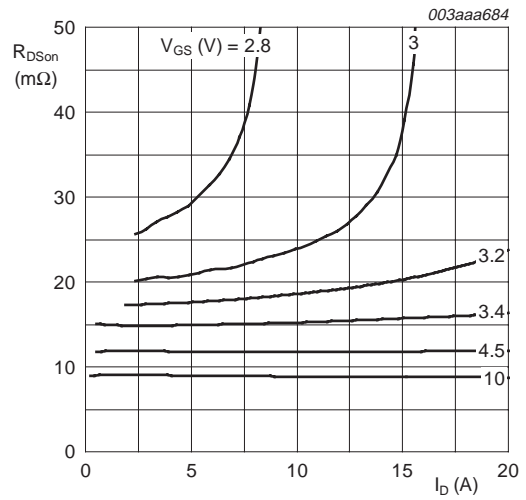
$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}; V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$ $T_j = -55\text{ °C}$	30 27	- -	- -	V V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}; V_{DS} = V_{GS}$; see Figure 9 and 10 $T_j = 25\text{ °C}$ $T_j = 150\text{ °C}$ $T_j = -55\text{ °C}$	1.3 0.8 -	1.7 - -	2.15 - 2.6	V V V
I_{DSS}	drain leakage current	$V_{DS} = 30\ \text{V}; V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$ $T_j = 150\text{ °C}$	- - -	- - -	1 100	μA μA
I_{GSS}	gate leakage current	$V_{GS} = \pm 16\ \text{V}; V_{DS} = 0\ \text{V}$	-	-	100	nA
R_G	gate resistance	$f = 1\ \text{MHz}; V_{GS(AC)} = 150\ \text{mV}$	-	1.6	-	Ω
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ \text{V}; I_D = 25\ \text{A}$; see Figure 6 and 8 $T_j = 25\text{ °C}$ $T_j = 150\text{ °C}$ $V_{GS} = 4.5\ \text{V}; I_D = 25\ \text{A}$; see Figure 6 and 8	- - -	7.1 12.1 10.1	8.9 15.1 12.5	m Ω m Ω m Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 15\ \text{A}; V_{DS} = 12\ \text{V}; V_{GS} = 4.5\ \text{V}$; see Figure 11 and 12	-	10.6	-	nC
Q_{GS}	gate-source charge		-	4.85	-	nC
Q_{GS1}	pre- $V_{GS(th)}$ gate-source charge		-	2.4	-	nC
Q_{GS2}	post- $V_{GS(th)}$ gate-source charge		-	2.45	-	nC
Q_{GD}	gate-drain charge		-	2.5	-	nC
$V_{GS(pl)}$	gate-source plateau voltage		-	3	-	V
C_{iss}	input capacitance	$V_{GS} = 0\ \text{V}; V_{DS} = 12\ \text{V}; f = 1\ \text{MHz}$; see Figure 14	-	1380	-	pF
C_{oss}	output capacitance		-	290	-	pF
C_{rss}	reverse transfer capacitance		-	135	-	pF
C_{iss}	input capacitance	$V_{GS} = 0\ \text{V}; V_{DS} = 0\ \text{V}; f = 1\ \text{MHz}$	-	1590	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12\ \text{V}; R_L = 0.8\ \Omega; V_{GS} = 4.5\ \text{V}$; $R_G = 5.6\ \Omega$	-	19	-	ns
t_r	rise time		-	22	-	ns
$t_{d(off)}$	turn-off delay time		-	19	-	ns
t_f	fall time		-	11	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 20\ \text{A}; V_{GS} = 0\ \text{V}$; see Figure 13	-	0.95	1.2	V
t_{rr}	reverse recovery time	$I_S = 15\ \text{A}; dI_S/dt = -100\ \text{A}/\mu\text{s}; V_{GS} = 0\ \text{V}$	-	34	-	ns
Q_r	recovered charge		-	14	-	nC



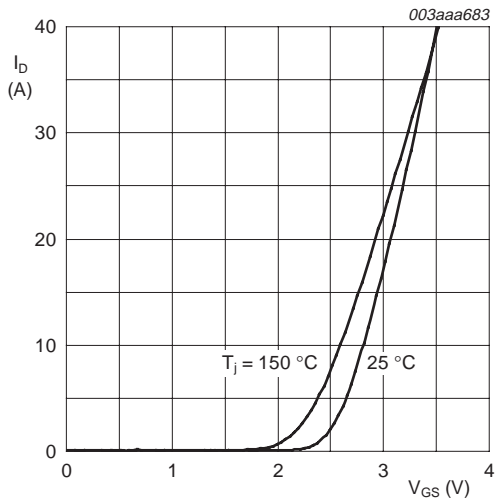
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



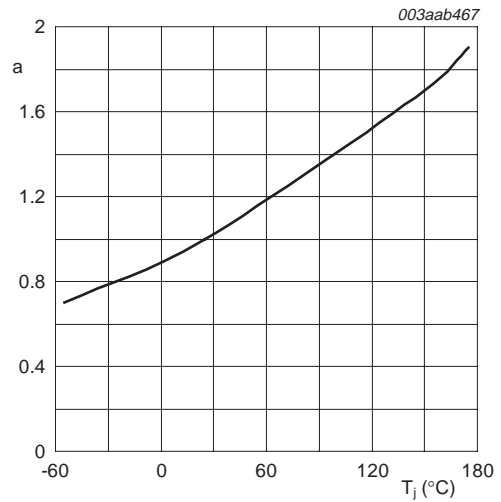
$T_j = 25^\circ\text{C}$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



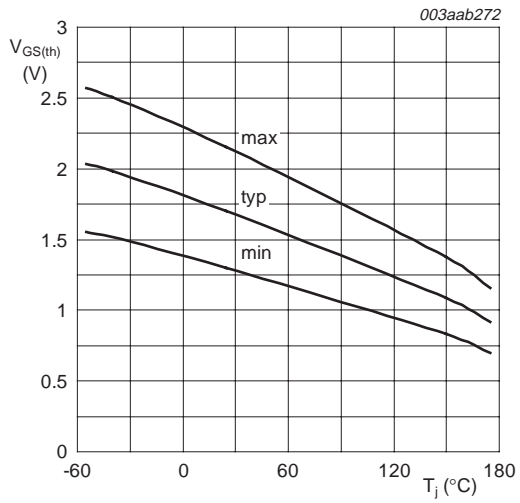
$T_j = 25^\circ\text{C}$ and 150°C ; $V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



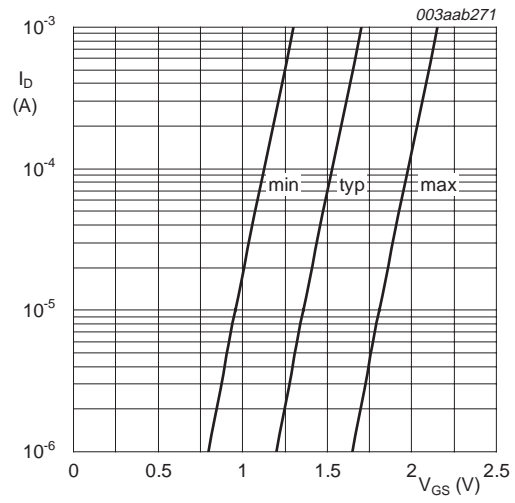
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



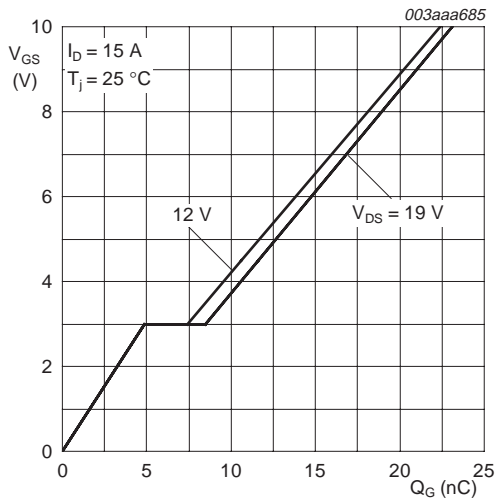
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



$T_j = 25 \text{ }^{\circ}C; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$I_D = 15 \text{ A}; V_{DS} = 12 \text{ V and } 19 \text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values

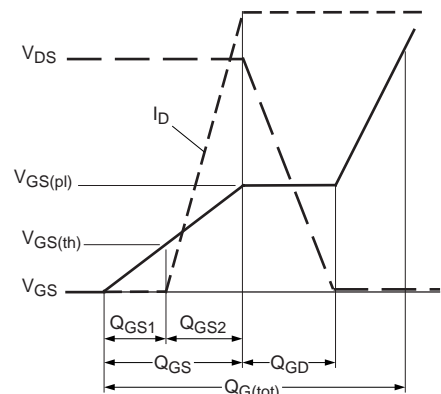
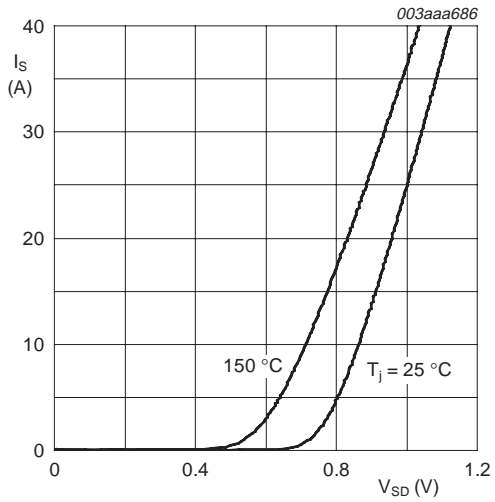
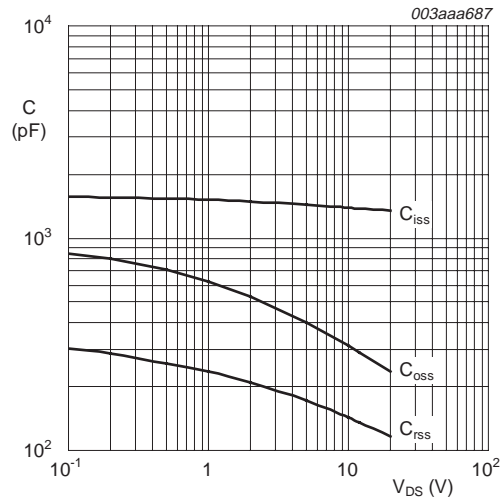


Fig 12. Gate charge waveform definitions



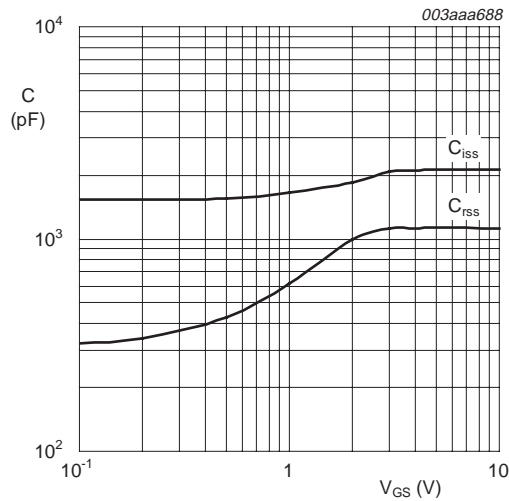
$T_j = 25\text{ °C}$ and 150 °C ; $V_{GS} = 0\text{ V}$

Fig 13. Source current as a function of source-drain voltage; typical values



$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{DS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 15. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



Fig 16. Package outline SOT96-1 (SO8)

8. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHK18NQ03LT_1	20061218	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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