FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12549-1E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89800 Series

MB89803/805/P808/PV800

■ DESCRIPTION

MB89800 series is a line of single-chip microcontrollers using the F²MC-8L* CPU core which can operate at low voltage but at high speed. In addition to an LCD controller/driver allowing 240-pixel display the microcontrollers contain a variety of peripheral functions such as timers, a UART, a serial interface, and an external interrupt. The configuration of the MB89800 series is therefore best suited to control of LCD display panels.

*: F²MC stands for FUJITSU Flexible Microcontroller.

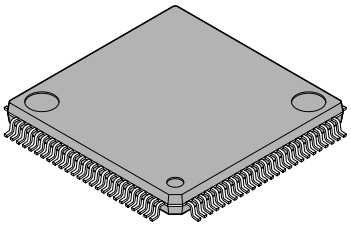
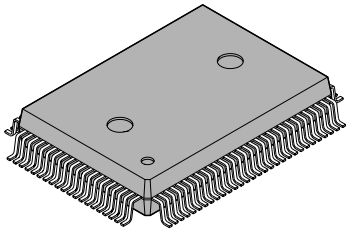
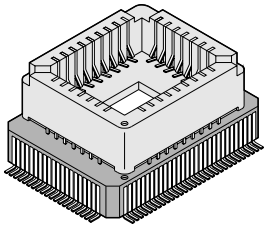
■ FEATURES

- Minimum execution time: 0.4 µs/10 MHz (Vcc = +5.0 V)
- F²MC-8L family CPU core

Instruction set optimized for controllers
- Multiplication and division instructions
- 16-bit arithmetic operations
- Test and branch instructions
- Bit manipulation instructions, etc.

(Continued)

■ PACKAGES

100 pin, Plastic LQFP	100 pin, Plastic QFP	100 pin, Ceramic MQFP
		
(FPT-100P-M05)	(FPT-100P-M06)	(MQP-100C-P01)

FUJITSU

(Continued)

- LCD controller/driver
  Max 70 segments/4 commons
  Divided resistor for LCD power supply
- Three types of timers
  8-bit PWM timer (also usable as a reload timer)
  8-bit pulse width count timer (also usable as a reload timer)
  20-bit time-base counter
- Two serial interfaces
  8-bit synchronous serial interface (Switchable transfer direction allows communication with various equipment.)
  UART (5-, 7-, 8-bit transfer capable)
- External interrupt: 2 channels
  Capable of wake-up from low-power consumption modes (with an edge detection function)
- Low-power consumption modes
  Stop mode (Oscillation stops to minimize the current consumption.)
  Sleep mode (The CPU stops to reduce the current consumption to approx. 1/3 of normal.)

■ PRODUCT LINEUP

Part number / Parameter	MB89803	MB89805	MB89P808	MB89PV800
Classification	Mass production product (mask ROM products)		One-time PROM product	Piggyback/evaluation product for evaluation and development
ROM size	8 K × 8 bits (internal mask ROM)	16 K × 8 bits (internal mask ROM)	48 K × 8 bits (internal PROM, programming with general-purpose EPROM programmer)	48 K × 8 bits (external ROM)
RAM size	256 × 8 bits	512 × 8 bits	2 K × 8 bits	
CPU functions	Number of instructions : 136 instructions Instruction bit length : 8 bits Instruction length : 1 byte to 3 bytes Data bit length : 1, 8, 16 bit length Minimum execution time : 0.4 µs/10 MHz (V_{CC} = 5.0 V) Interrupt processing time : 3.6 µs/10 MHz (V_{CC} = 5.0 V)			
Ports	I/O ports (N-ch open-drain) : 16 (All also serve as segment pins.)*1 I/O ports (N-ch open-drain) : 6 I/O ports (CMOS) : 6 (5 ports also serve as peripheral I/O.) Input ports : 4 (1 port also serves as an external interrupt input.) Total : 32 (Max)			
PWM timer	8-bit reload timer operation (toggled output capable) 8-bit resolution PWM operation Operating clock (pulse width count timer output, 0.4 µs, 6.4 µs, 25.6 µs/10 MHz)			
Pulse width count timer	8-bit reload timer operation 8-bit pulse width count operation (continuous measurement capable, “H” width, “L” width, or single-cycle measurement capable) Operating clock(0.4 µs, 1.6 µs, 12.8 µs/10 MHz)			
Serial I/O 8 bits	8-bit length One clock selectable from four transfer clocks(0.8 µs, 3.2 µs, 12.8 µs/10 MHz) LSB first/MSB first selectability			
UART	5-, 7-, 8- bit transfer capable, built-in baud-rate generator (Max 156250/10 MHz)			
LCD controller/ driver	Common output: 4 Segment output: 70 (Max) Operating mode: 1/2 bias • 1/2 duty, 1/3 bias • 1/3 duty, 1/3 bias • 1/4 duty LCD display RAM size: 70×4 bits Dividing resistor for LCD driving: Built-in(An external resistor selectable)			
External interrupt	2 channels (edge selectable) (1 channel also serves as a pulse width count timer input)			
Standby mode	Sleep mode, stop mode			
Process	CMOS			
Operating voltage*2	2.2 V to 6.0 V		2.7 to 6.0 V	
EPROM for use				MBM27C512-20TV (LCC package)

*1 : The function is selected by the mask option.

*2 : Varies with conditions such as the operating frequency. (See “■ELECTRICAL CHARACTERISTICS”.)

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89803	MB89805	MB89P808	MB89PV800
FPT-100P-M05	○	○	○	×
FPT-100P-M06	○	○	○	×
MQP-100C-P01	×	×	×	○

○ : Available × : Not available

Note : For more information about each package, see “ ■PACKAGE DIMENSIONS”.

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, it is necessary to confirm its differences from the product that will actually be used.
Take particular care on the following points:

- MB89803 register bank addresses upper than 0180H can not be used.
- The stack area, etc., is set at the upper limit of the RAM.

2. Current Consumption

- In the case of the MB89PV800, add the current consumed by the EPROM which is connected to the top socket.
- When operating at low speed, the current consumption in the one-time PROM or EPROM model is greater than on the mask ROM models. However, the current consumption in sleep/stop modes is the same. (For more information, see “■ELECTRICAL CHARACTERISTICS”.)

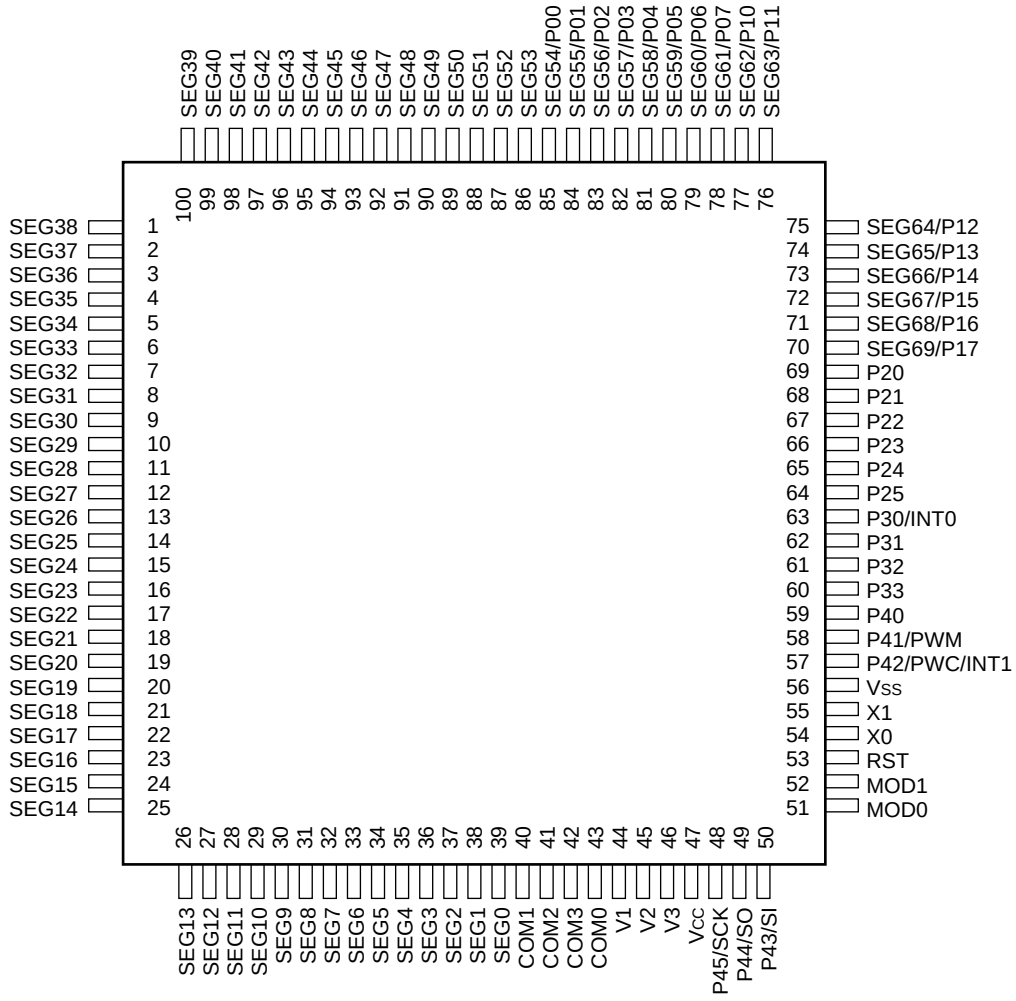
3. Mask Options

Functions that can be selected as options and how to designate these options vary by the product.
Before using options check “■MASK OPTIONS”.

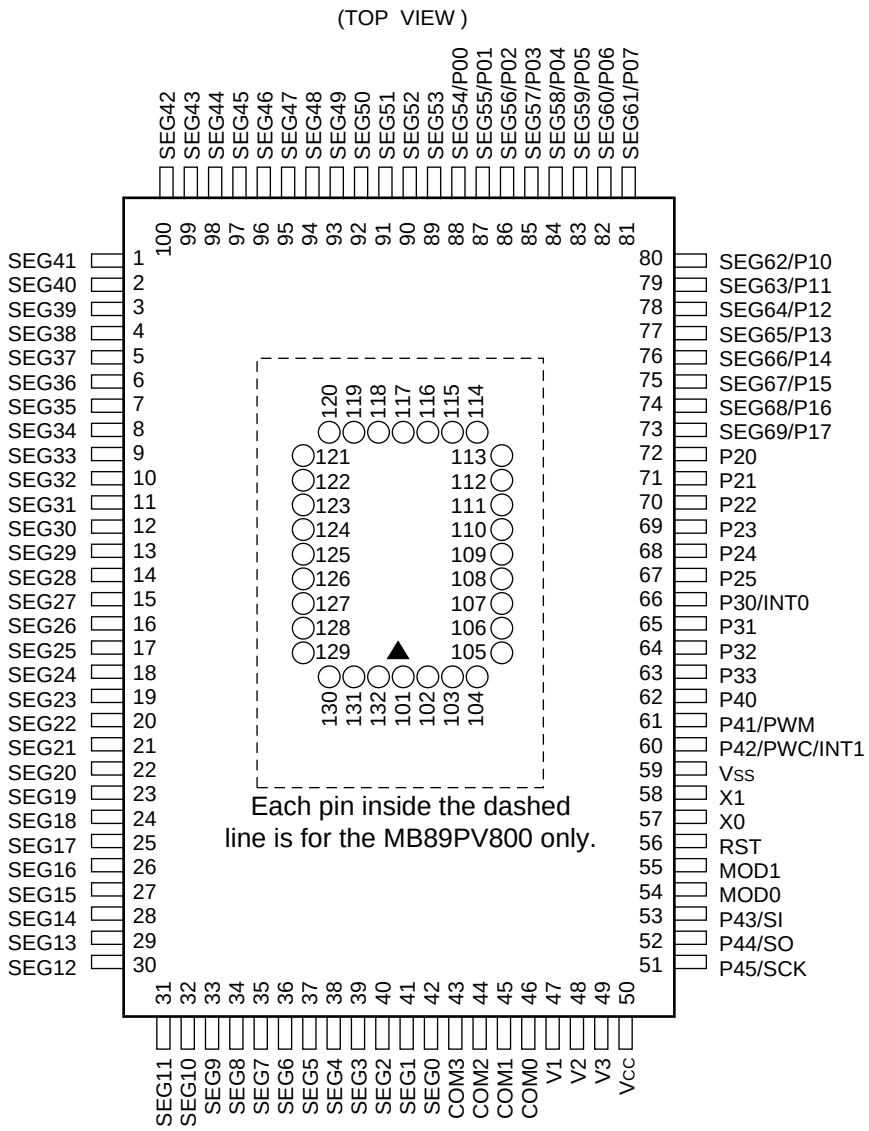
Note that the options are fixed especially in MB89PV800 and MB89P808.

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-100P-M05)



(MQP-100C-P01)
(FPT-100P-M06)

• Pin assignment on package top (MB89PV800 only)

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
101	N.C.	109	A2	117	N.C.	125	$\overline{OE}$
102	V_{PP}	110	A1	118	O4	126	N.C.
103	A12	111	A0	119	O5	127	A11
104	A7	112	N.C.	120	O6	128	A9
105	A6	113	O1	121	O7	129	A8
106	A5	114	O2	122	O8	130	A13
107	A4	115	O3	123	$\overline{CE}$	131	A14
108	A3	116	V_{SS}	124	A10	132	V_{CC}

N.C.: Internally connected. Do not use.

■ PIN DESCRIPTION

Pin no.		Pin name	Circuit type	Function
LQFP*1	MQFP/ QFP*2			
54	57	X0	A	Clock crystal oscillator pins
55	58	X1		
51	54	MOD0	B	Operating mode selection pin. Connect directly to V_{SS}.
52	55	MOD1		
53	56	$\overline{RST}$	C	This pin is an N-ch open-drain type with a pull-up resistor, and a hysteresis input type. “L” is output from this pin by an internal reset source (optional function). The internal circuit is initialized by the input of “L”.
85 to 78	88 to 81	P00/SEG54 to P07/SEG61	D	General-purpose N-ch open-drain I/O ports. Also serve as an LCD controller/driver segment output. The port and segment output are switched by mask option in 8-bit unit.
77 to 70	80 to 73	P10/SEG62 to P17/SEG69	D	General-purpose N-ch open-drain I/O ports. Also serve as an LCD controller/driver segment output. The port and segment output are switched by mask option in 4 to 1-bit unit.
69 to 64	72 to 67	P20 to P25	F	General-purpose N-ch open-drain I/O ports. A pull-up resistor option is provided.
63	66	P30/INT0	I	General-purpose input port. The input is CMOS input. Also serves as an external interrupt input (INT0), in this case, the input is hysteresis input. A pull-up resistor option is provided.
62 to 60	65 to 63	P31 to P33	H	General-purpose input ports. These pins are a CMOS input type. A pull-up resistor option is provided.
59	62	P40	E	General-purpose I/O port. A pull-up resistor option is provided.
58	61	P41/PWM	E	General-purpose I/O port. A pull-up resistor option is provided. Also serves as PWM timer toggle output (PWM).
57	60	P42/PWC/ INT1	E	General-purpose I/O port. A pull-up resistor option is provided. Also serves as pulse width count timer input (PWC) and an external interrupt input (INT1). The PWC and INT1 input is hysteresis input.
50	53	P43/SI	E	General-purpose I/O port. A pull-up resistor option is provided. Also serves as serial I/O and a UART data input (SI). The SI input is hysteresis input.
49	52	P44/SO	E	General-purpose I/O port. A pull-up resistor option is provided. Also serves as a serial I/O and a UART data output (SO).

*1 : FPT-100P-M05

*2 : FPT-100P-M06/MQP-100C-P01

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Pin no.		Pin name	Circuit type	Function
LQFP*1	MQFP/ QFP*2			
48	51	P45/SCK	E	General-purpose I/O port. A pull-up resistor option is provided. Also serves as a serial I/O and a UART clock I/O (SCK). The SCK input is hysteresis input.
39 to 1, 100 to 86	42 to 1, 100 to 89	SEG0 to SEG53	G	LCD controller/driver segment output pins
43 to 40	46 to 43	COM0 to COM3	G	LCD controller/driver common output pins
46 to 44	49 to 47	V3 to V1	—	LCD driving power supply pins
47	50	V_{CC}	—	Power supply pin
56	59	V_{SS}	—	Power supply (GND) pin

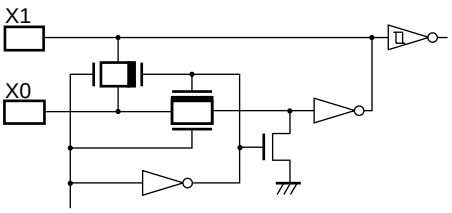
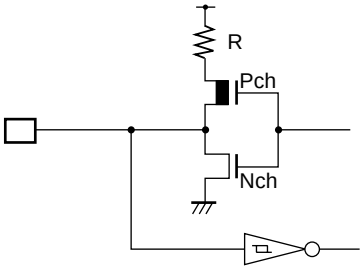
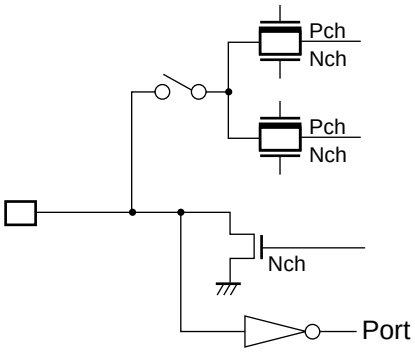
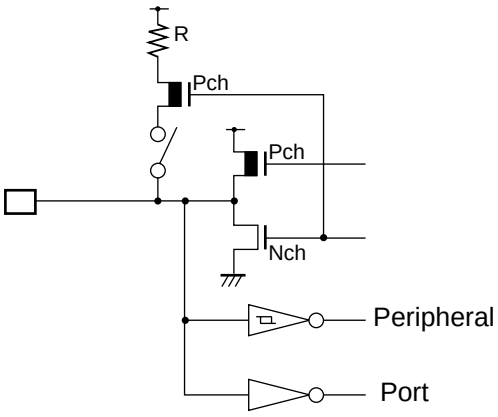
*1 : FPT-100P-M05

*2 : FPT-100P-M06/MQP-100C-P01

• **External EPROM pins (MB89PV800 only)**

Pin no.	Pin name	I/O	Function
102	V_{PP}	O	“H” level output pin
103 104 105 106 107 108 109 110 111	A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins
113 114 115	O1 O2 O3	I	Data input pins
116	V_{SS}	O	Power supply (GND) pin
118 119 120 121 122	O4 O5 O6 O7 O8	I	Data input pins
123	CE	O	ROM chip enable pin Outputs “H” during standby.
124	A10	O	Address output pin
125	OE	O	ROM output enable pin Outputs “L” at all times.
127 128 129	A11 A9 A8	O	Address output pins
130	A13	O	
131	A14	O	
132	V_{CC}	O	EPROM power supply pin
101 112 117 126	N.C.	—	Internally connected pins Be sure to leave them open.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Crystal oscillator circuit • At an oscillation feedback resistor of approximately 1 MΩ/5.0 V
B		• CMOS input
C		• At an output pull-up resistor (P-ch) of approximately 50 kΩ/5.0 V • Hysteresis input
D		• N-ch open-drain output • CMOS input • Segment output optional
E		• CMOS output • CMOS input • Hysteresis input (peripheral input) • Pull-up resistor optional

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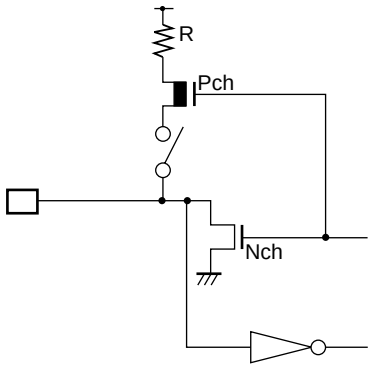
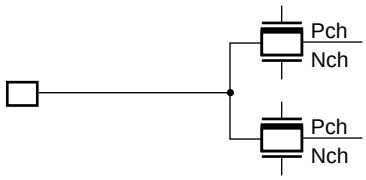
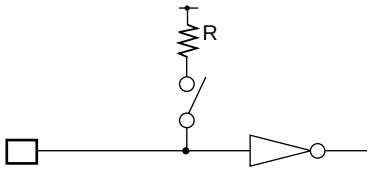
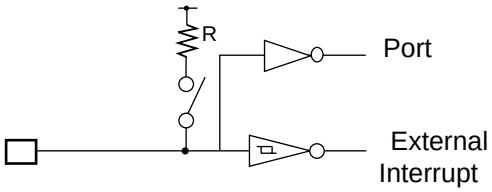
Type	Circuit	Remarks
F		• Nch open-drain output • CMOS input • Pull-up resistor optional
G		• LCDC output
H		• CMOS input • Pull-up resistor optional
I		• CMOS input (port) , Hysterisis input (interrupt) • Pull-up resistor optional

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in “■ELECTRICAL CHARACTERISTICS” is applied between V_{CC} and V_{SS}.
When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

4. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 Hz to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

5. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset (optional) and wake-up from stop mode.

■ PROGRAMMING TO THE EPROM ON THE MB89P808

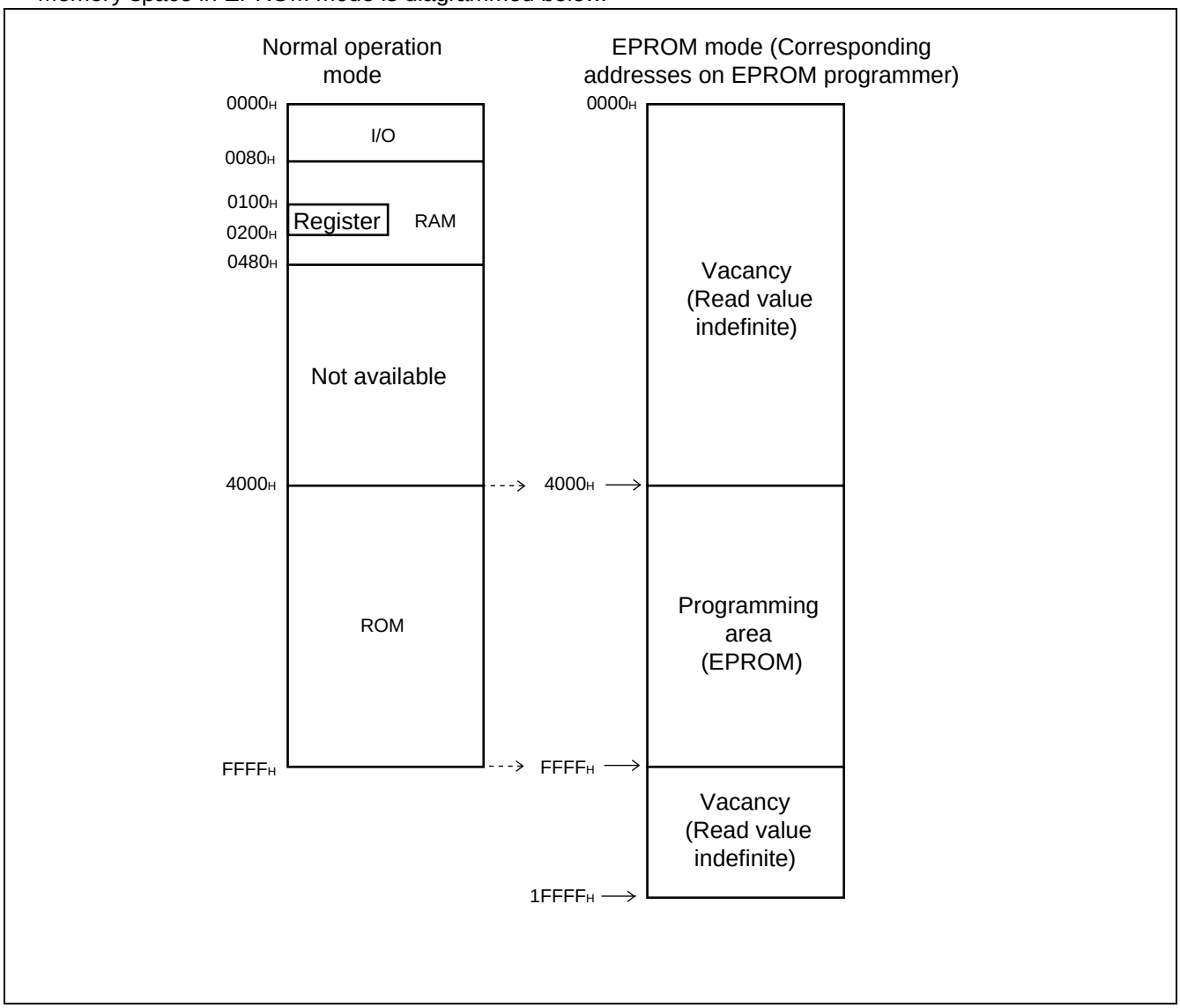
The MB89P808 is an OTPROM (one-time PROM) version for the MB89800 series.

1. Features

- 48-Kbyte PROM on chip
- Options can be set using the EPROM programmer.
- Equivalency to the MBM27C1001A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in EPROM mode is diagrammed below.



3. Programming to the EPROM

In EPROM mode, the MB89P808 functions equivalent to the MBM27C1001A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

- Programming procedure

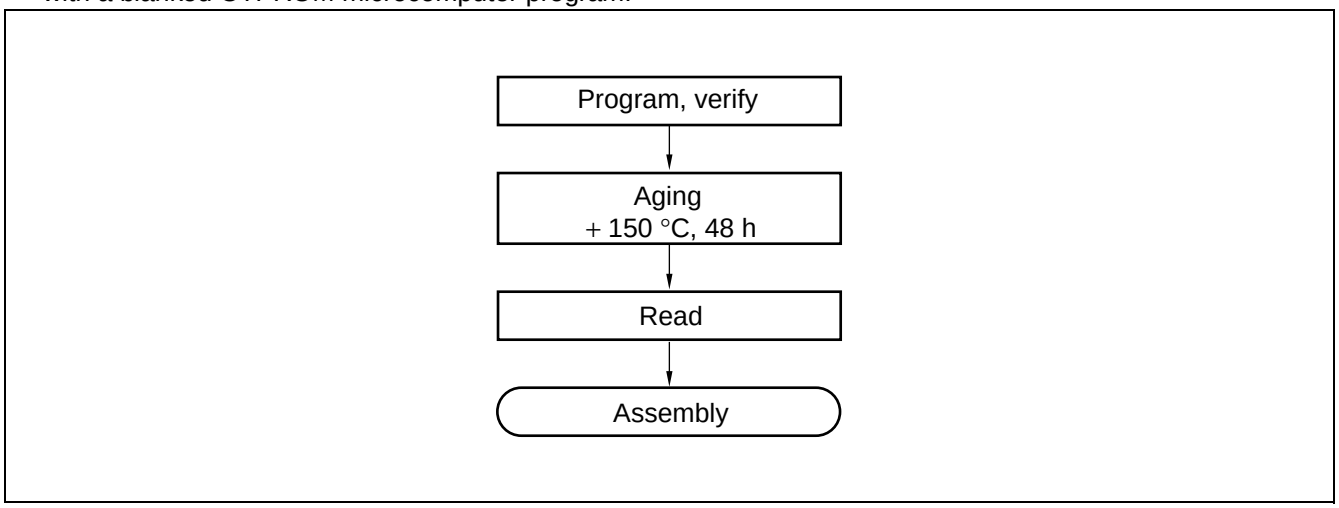
(1) Set the EPROM programmer to the MBM27C1001A.

(2) Load option data into addresses 4000H to FFFFH of the EPROM programmer.

(3) Program with the EPROM programmer.

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product for a product with a blanked OTPROM microcomputer program.



5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

6. EPROM Programmer Socket Adapter

Package	Compatible socket adapter
FPT-100P-M05	ROM-100SQF-32DP-8LA3
FPT-100P-M06	ROM-100QF-32DP-8LA2

Inquiry: Sunhayato Co., Ltd.: TEL +81-3-3984-7791

Note : With some EPROM programmers, stability of programming performance is enhanced by placing an 0.1 µF capacitor between the V_{PP} and V_{SS} pins or the V_{CC} and V_{SS} pins.

■ PROGRAMMING TO THE EPROM WITH PIGGY-BACK/EVALUATION CHIPS

1. EPROM for Use

MBM27C512-20TV

2. Programming Socket Adapter

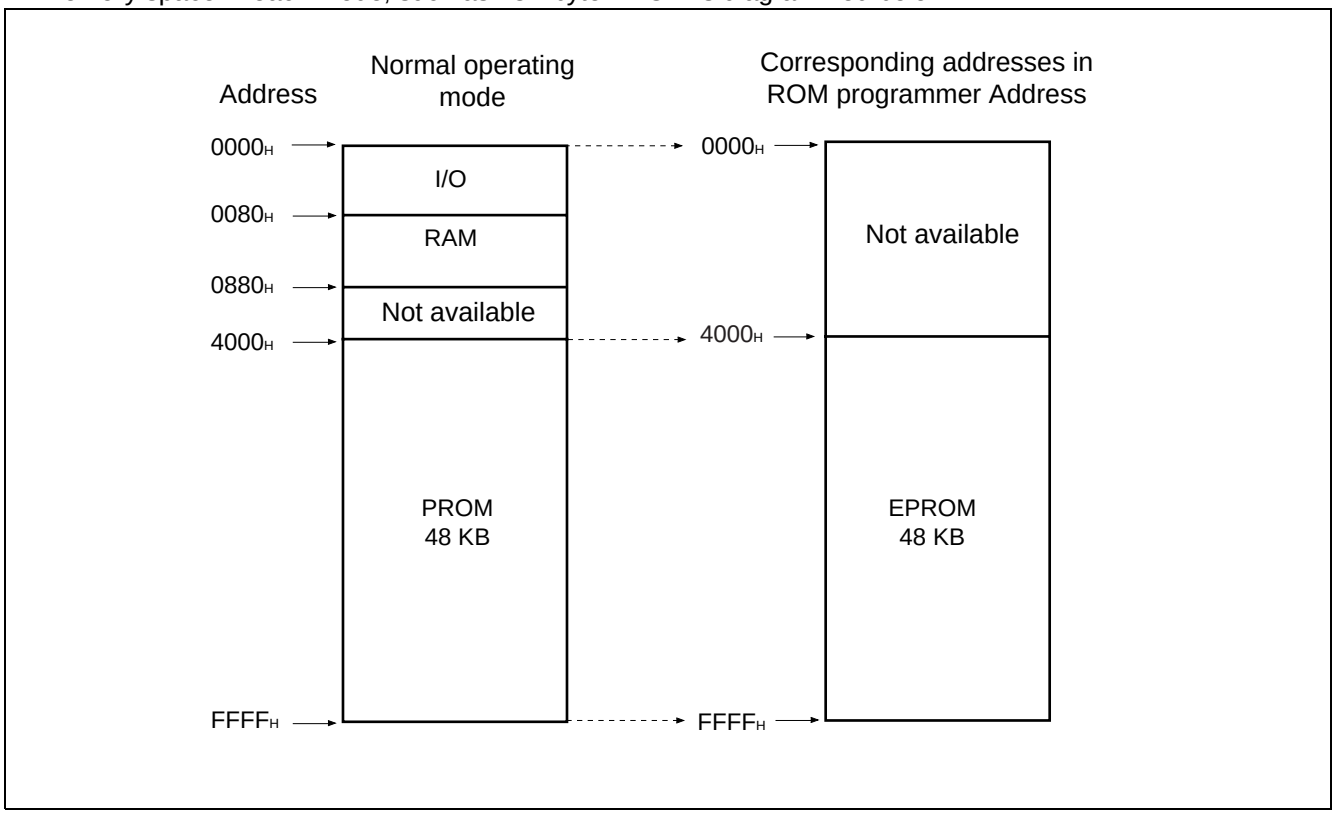
To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) listed below.

Package	Adapter socket part number
LCC-32 (Rectangle)	ROM-32LC-28DP-YG

Inquiry: Sunhayato Co., Ltd.: TEL +81-3-3984-7791

3. Memory Space

Memory space in each mode, such as 48 Kbyte PROM is diagrammed below.



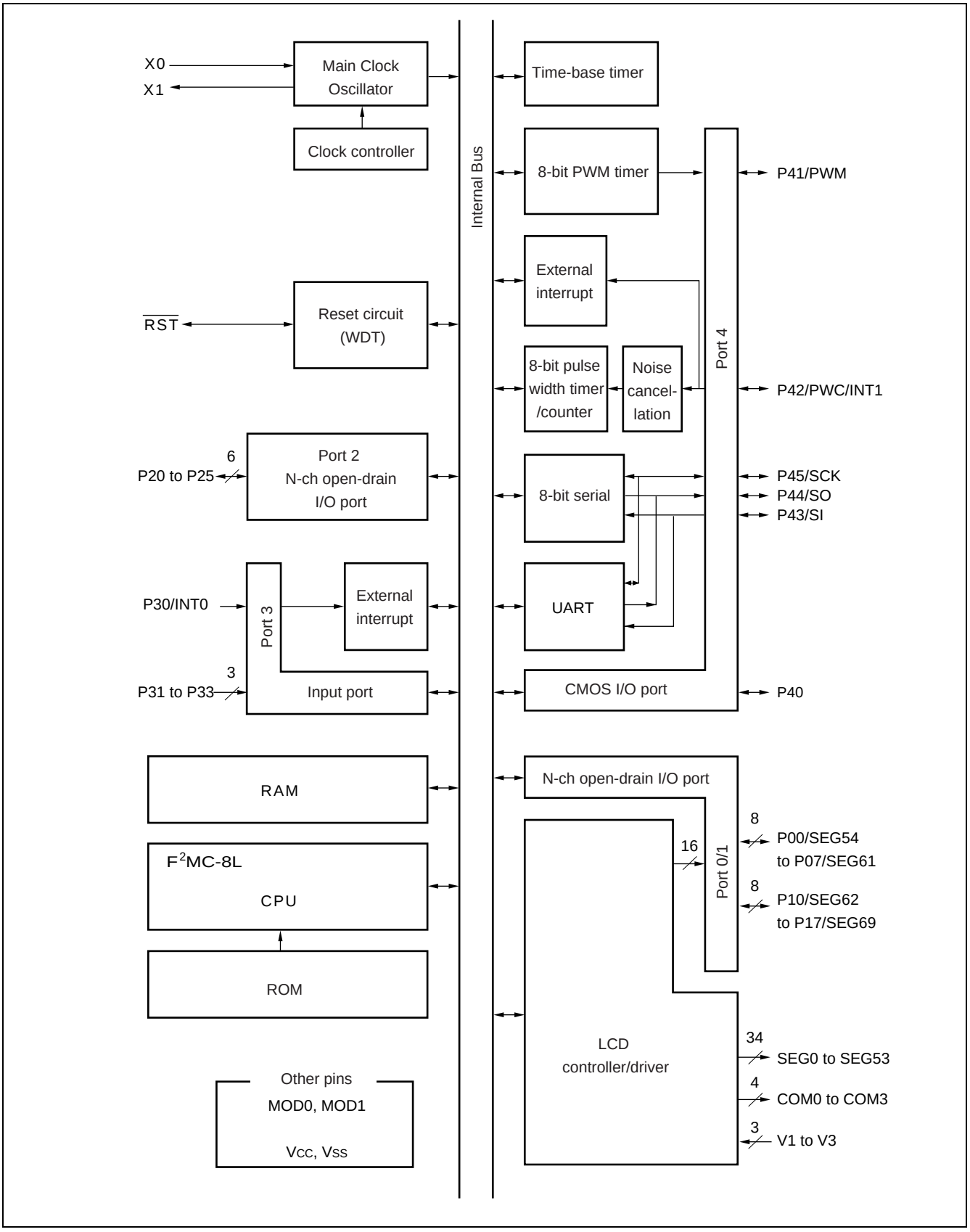
4. Programming to the EPROM

(1) Set the EPROM programmer to the MBM27C512.

(2) Load program data into the EPROM programmer at 4000_H to $FFFF_H$.

(3) Program to 4000_H to $FFFF_H$ with the EPROM programmer.

■ BLOCK DIAGRAM

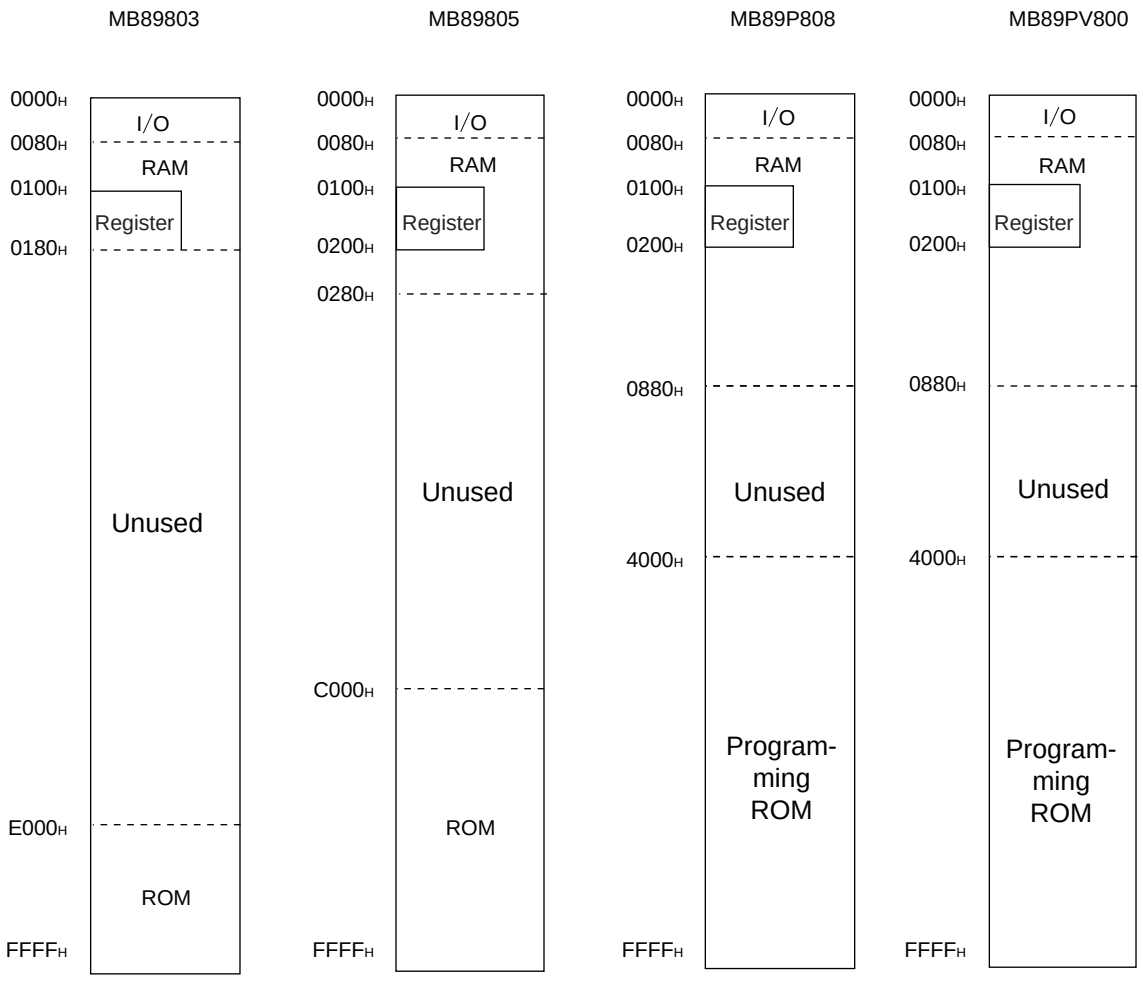


■ CPU CORE

1. Memory Space

The microcontrollers of the MB89800 series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89800 series is structured as illustrated below.

• Memory space



2. Registers

The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided :

Program counter (PC) : A 16-bit register for indicating instruction storage positions

Accumulator (A) : A 16-bit temporary register for storing arithmetic operations, etc.
When the instruction is an 8-bit data processing instruction, the lower byte is used.

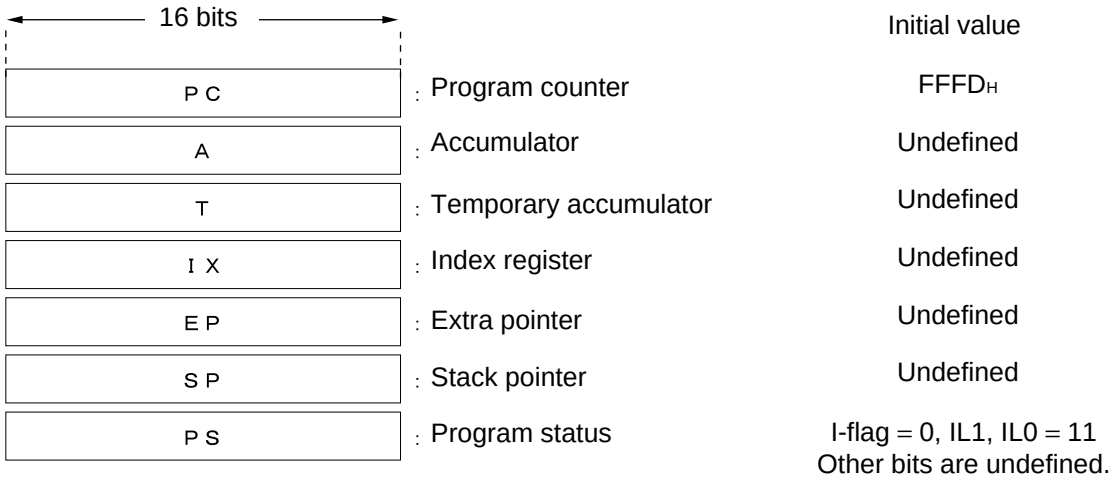
Temporary accumulator (T) : A 16-bit register which performs arithmetic operations with the accumulator.
When the instruction is an 8-bit data processing instruction, the lower byte is used.

Index register (IX) : A 16-bit register for index modification

Extra pointer (EP) : A 16-bit pointer for indicating a memory address

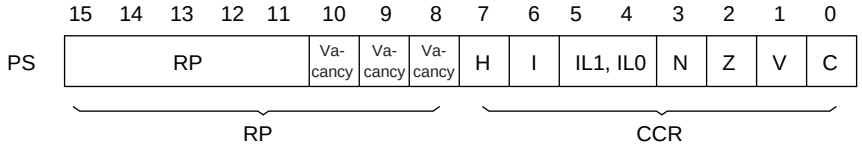
Stack pointer (SP) : A 16-bit register for indicating a stack area

Program status (PS) : A 16-bit register for storing a register pointer and a condition code



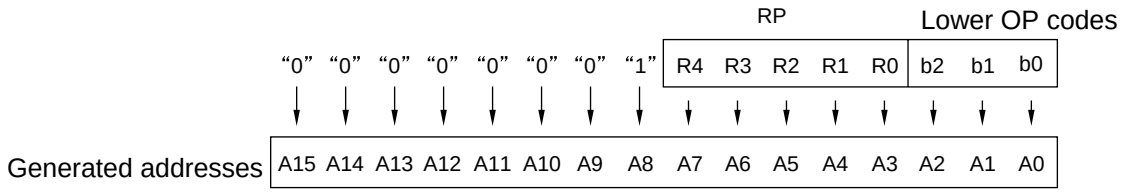
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

• Structure of the Program Status Register



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

- Rule for conversion of actual addresses of the general-purpose register area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag : Set to 1 when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

I-flag : Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.

IL1, 0 : Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High ↕ Low = no interrupt
0	1		
1	0	2	
1	1	3	

N-flag : Set to 1 if the highest bit is set to 1 as the result of an arithmetic operation. Cleared to 0 when the bit is set to 0.

Z-flag : Set to 1 when an arithmetic operation results in 0. Cleared to 0 otherwise.

V-flag : Set to 1 if the complement on 2 overflows as a result of an arithmetic operation. Cleared to 0 if the overflow does not occur.

C-flag : Set to 1 when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to 0 otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

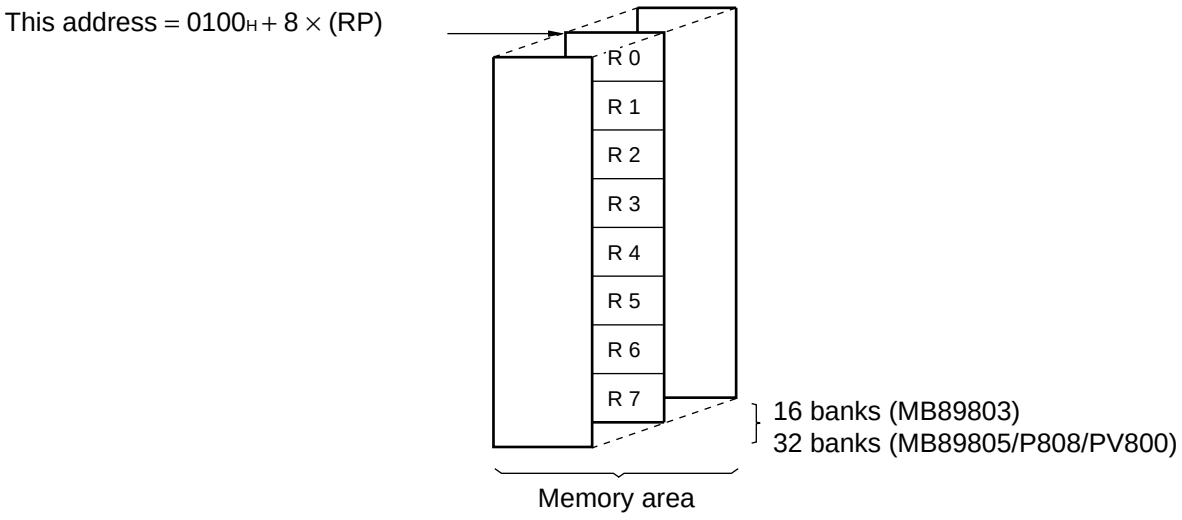
General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 16 banks can be used on the MB89803 (RAM 256 × 8 bits). The bank currently in use is indicated by the register bank pointer (RP).

Note : The number of register banks that can be used varies with the RAM size.

MB89803	0100h to 017Fh	16 banks
MB89805	0100h to 01FFh	32 banks
MB89P808	0100h to 01FFh	32 banks
MB89PV800	0100h to 01FFh	32 banks

• Register bank configuration



■ I/O MAP

Address	Read/write	Register name	Register description
00H	(R/W)	PDR0	Port 0 data register
01H	Vacancy		
02H	(R/W)	PDR1	Port 1 data register
03H	Vacancy		
04H	(R/W)	PDR2	Port 2 data register
05H	Vacancy		
06H	Vacancy		
07H	Vacancy		
08H	(R/W)	STBC	Standby control register
09H	(R/W)	WDTC	Watchdog timer control register
0AH	(R/W)	TBCR	Time-base timer control register
0BH	Vacancy		
0CH	(R)	PDR3	Port 3 data register
0DH	Vacancy		
0EH	(R/W)	PDR4	Port 4 data register
0FH	(W)	DDR4	Port 4 data direction register
10H	Vacancy		
11H	Vacancy		
12H	(R/W)	CNTR	PWM timer control register
13H	(W)	COMR	PWM timer compare register
14H	(R/W)	PCR1	PWC pulse width control register 1
15H	(R/W)	PCR2	PWC pulse width control register 2
16H	(R/W)	RLBR	PWC reload buffer register
17H	(R/W)	NCCR	PWC noise cancellation control register 1
18H	Vacancy		
19H	Vacancy		
1AH	Vacancy		
1BH	Vacancy		
1CH	(R/W)	SMR	Serial mode register
1DH	(R/W)	SDR	Serial data register
1EH	Vacancy		
1FH	Vacancy		

(Continued)

(Continued)

Address	Read/write	Register name	Register description
20H	(R/W)	SMC1	UART serial mode control register 1
21H	(R/W)	SRC	UART serial rate control register
22H	(R/W)	SSD	UART serial status/data register
23H	(R/W)	SIDR/SODR	UART serial data register
24H	(R/W)	SMC2	UART serial mode control register 2
25H	Vacancy		
26H	Vacancy		
27H	Vacancy		
28H	Vacancy		
29H	Vacancy		
2AH	Vacancy		
2BH	Vacancy		
2CH	Vacancy		
2DH	Vacancy		
2EH	Vacancy		
2FH	Vacancy		
30H	(R/W)	EIC1	External interrupt 1 control register 1
31H to 4FH	Vacancy		
50H to 72H	(R/W)	VRAM	Display data RAM
79H	(R/W)	LCR1	LCD controller/driver control register
7AH	(R/W)	SEGR	Segment output selection register
7BH	Vacancy		
7CH	(W)	ILR1	Interrupt level setting register 1
7DH	(W)	ILR2	Interrupt level setting register 2
7EH	(W)	ILR3	Interrupt level setting register 3
7FH	Vacancy		

R/W = Available Read and Write
R = Read only
W = Write only

Note : Do not use vacancies.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = 0.0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	
LCD power supply voltage	V_3	V_{SS} – 0.3	V_{SS} + 7.0	V	V3 to V1 Pin
Input voltage	V_{I1}	V_{SS} – 0.3	V_{CC} + 0.3	V	With pull-up resistor of P20 to P25 in selecting. Must not exceed V_{SS} + 7.0 V.
	V_{I2}	V_{SS} – 0.3	V_{SS} + 7.0	V	Without pull-up resistor of P20 to P25 in selecting.
	V_{I3}	V_{SS} – 0.3	V_3+ 0.3	V	Adapt to P00 to P07 and P10 to P17 in MB89P808 and MB89PV800. Must not exceed V_{SS} + 7.0 V.
	V_{I4}	V_{SS} – 0.3	V_{CC} + 0.3	V	Other pins. Must not exceed V_{SS} + 7.0 V.
Output voltage	V_{O1}	V_{SS} – 0.3	V_{CC} + 0.3	V	With pull-up resistor of P20 to P25 in selecting. Must not exceed V_{SS} + 7.0 V.
	V_{O2}	V_{SS} – 0.3	V_{SS} + 7.0	V	Without pull-up resistor of P20 to P25 in selecting.
	V_{O3}	V_{SS} – 0.3	V_3 + 0.3	V	Adapt to P00 to P07 and P10 to P17 in MB89P808 and MB89PV800. Must not exceed V_{SS} + 7.0 V.
	V_{O4}	V_{SS} – 0.3	V_{CC} + 0.3	V	Other pins. Must not exceed V_{SS} + 7.0 V.
“L” level output current	I_{OL}	—	+ 10	mA	Except power supply pins
“L” level average output current	I_{OLAV}	—	+ 4	mA	Average value (operating current×operating duty) , adapt to all pins except for power supply.
Total “L” level output current	ΣI_{OL}	—	+ 40	mA	
“H” level output current	I_{OH}	—	– 5	mA	Except power supply pins
“H” level average output current	I_{OHAV}	—	– 2	mA	Average value (operating current×operating duty) , adapt to all pins except for power supply.
Total “H”level output current	ΣI_{OH}	—	– 10	mA	
Power consumption	Pd	—	+ 300	mW	
Operating temperature	T_A	– 40	+ 85	°C	
Storage temperature	Tstg	– 55	+ 150	°C	

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

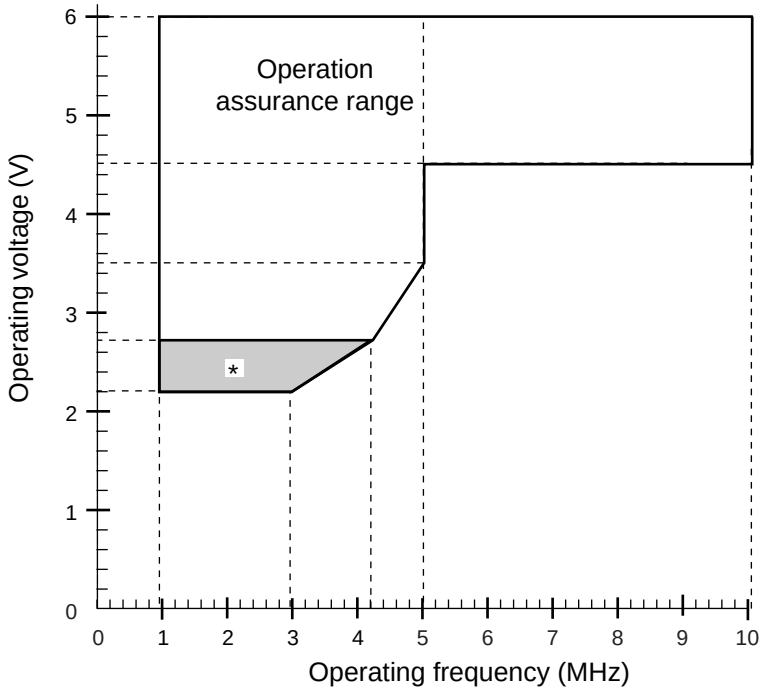
2. Recommended Operating Conditions

(V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	2.2*	6.0*	V	Normal operation assurance range
		1.5	6.0	V	Retains the RAM state in stop mode
LCD power supply voltage	V_3	V_{SS}	6.0	V	V3 pin The optimum value is dependent on the element in use.
Operating temperature	T_A	– 40	+ 85	°C	

* : The minimum operating power supply voltage varies with the operating frequency.

Operation Voltage – Operating frequency



* : The shaded area is assured only for the MB89803/805.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(V_{CC} = V_3 = +5.0 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	P00 to P07, P10 to P17, P20 to P25, P30 to P33, P40 to P45	—	0.7 V_{CC}*1	—	V_{CC} + 0.3	V	CMOS input
	V_{IHS}	$\overline{RST}$, MOD0 to MOD1, INT0, SCK, SI, PWC/ INT1	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	CMOS hysterisis input
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17, P20 to P25, P30 to P33, P40 to P45	—	V_{CC} – 0.3	—	0.3 V_{CC}*1	V	CMOS input
	V_{ILS}	$\overline{RST}$, MOD0 to MOD1, INT0, SCK, SI, PWC/ INT1	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	CMOS hysterisis input
Open-drain output pin application voltage	V_{D1}	P20 to P25	Without pull-up resistor	V_{SS} – 0.3	—	V_{SS} + 6.0	V	
	V_{D2}	P00 to P07, P10 to P17	—	V_{SS} – 0.3	—	V_{SS} + 6.0	V	Adapt to MB89803/805
				V_{SS} – 0.3	—	V_3*1	V	Adapt to MB89PV800/ P808
"H"level output voltage	V_{OH}	P40 to P45	I_{OH} = – 2 mA	2.4	—	—	V	
"L"level output voltage	V_{OL1}	P00 to P07, P10 to P17, P20 to P25, P40 to P45	I_{OL} = 1.8 mA	—	—	0.4	V	
	V_{OL2}	$\overline{RST}$	I_{OL} = 4.0 mA	—	—	0.4	V	

(Continued)

(V_{CC} = V_3 = +5.0 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Sym-bol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input leakage current (Hi-z output leakage current)	I_{LI1}	MOD0, MOD1, P30 to P33, P40 to P45	0.45 V < V_I < V_{CC} Without pull-up resistor	—	—	± 5	µA	
		P00 to P07, P10 to P17	0.45 V < V_I < V_{CC}	—	—	± 5	µA	Adapt to MB89PV800/ P808
	I_{LI2}	P20 to P25	0.45 V < V_I < 6 V Without pull-up resistor	—	—	± 1	µA	
		P00 to P07, P10 to P17	0.45 < V_I < 6 V	—	—	± 1	µA	Adapt to MB89803/805
Pull-up Resistance	R_{PULL}	P20 to P25, P30 to P33, P40 to P45, $\overline{RST}$	V_I = 0 V With pull-up resistor	25	50	100	kΩ	
Common output impedance	R_{VCOM}	COM0 to COM3	V1 to V3 = + 5.0 V	—	—	2.5	kΩ	
Segment output impedance	R_{VSEG}	SEG0 to SEG49	V1 to V3 = + 5.0 V	—	—	15	kΩ	
LCD divided resistance	R_{LCD}	—	V3 to V_{SS}	30	60	120	kΩ	
LCD leakage current	I_{LCDL}	V1 to V3, COM0 to COM3, SEG0 to SEG69	—	—	—	± 1	µA	
Power supply current*2	I_{CC1}	V_{CC}	RUN mode Fc = 5 MHz t_{inst} = 0.8 µs	—	4.5	6	mA	Adapt to MB89803/805/ PV800
				—	9	15	mA	Adapt to MB89P808
			RUN mode Fc = 10 MHz t_{inst} = 0.4 µs	—	9	12	mA	Adapt to MB89803/805/ PV800
				—	13	20	mA	Adapt to MB89P808

(Continued)

(Continued)

(V_{CC} = V_3 = +5.0 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*2	I_{CC2}	V_{CC}	RUN mode Fc = 5 MHz t_{inst} = 12.8 µs	—	0.6	0.9	mA	Adapt to MB89803/805/ PV800
				—	3.5	7	mA	Adapt to MB89P808
			RUN mode Fc = 10 MHz t_{inst} = 6.4 µs	—	1.2	1.8	mA	Adapt to MB89803/805/ PV800
				—	4	8	mA	Adapt to MB89P808
	I_{CCS1}	V_{CC}	Sleep mode Fc = 5 MHz t_{inst} = 0.8 µs	—	1.5	2	mA	
			Sleep mode Fc = 10 MHz t_{inst} = 0.4 µs	—	3	4	mA	
	I_{CCS2}	V_{CC}	Sleep mode Fc = 5 MHz t_{inst} = 12.8 µs	—	0.4	0.8	mA	
			Sleep mode Fc = 10 MHz tinst = 6.4 µs	—	0.8	1.6	mA	
	I_{CCH}	V_{CC}	Stop mpde T_A = +25 °C	—	0.1	1	µA	Adapt to MB89803/805
				—	0.1	10	µA	Adapt to MB89P808/ PV800
Input capacitance	C_{IN}	Except V_{CC} and V_{SS}	—	—	10	—	pF	

*1 : The input voltage to P00 to P07 and P10 to P17 for the MB89P800/PV808 must not exceed the LCD power supply voltage (V3 pin voltage).

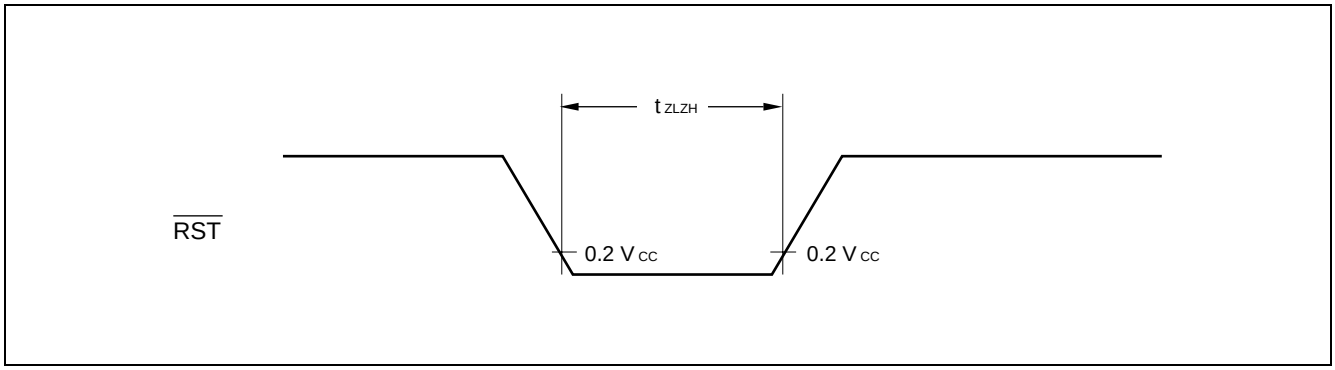
*2 : The measurement condition of power supply current is as follows: the external clock, open output pins and the external LCD dividing resistor. In the case of the MB89PV800, the current consumed by the connected EPROM and ICE is not included.

4. AC Characteristics

(1) Reset Timing

(V_{CC} = +5.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	48 t_{XCYL}	—	ns	

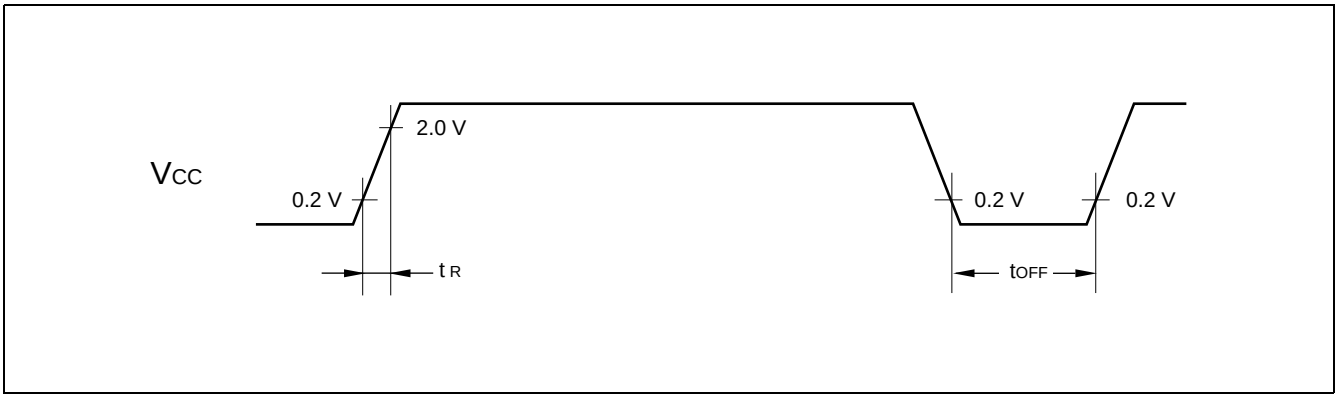


(2) Power-on Reset

(V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	50	ms	Power-on reset function only
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operation

Note : Make sure that power supply rises within the selected oscillation stabilization time.
If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.



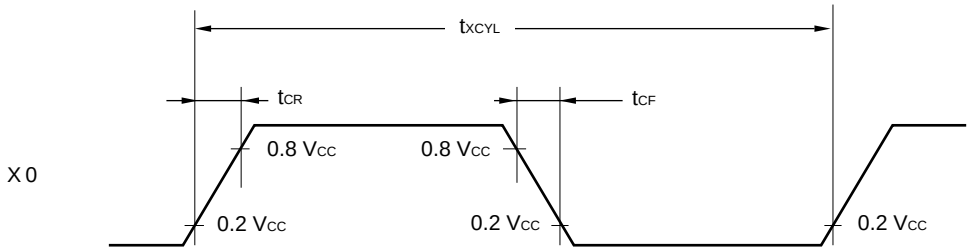
(3) Clock Timing

(V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_C	X0, X1	—	1	—	10	MHz	
Clock cycle time	t_{XCYL}			100	—	1000	ns	Crystal or ceramic resonator
Input clock duty ratio*	duty	X0		30	—	70	%	External clock
Input clock rising/falling time	t_{CR} t_{CF}			—	—	10	ns	External clock

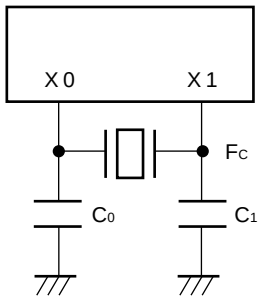
* : duty = P_{WH} /t_{HCYL}

• X0 and X1 timing and conditions

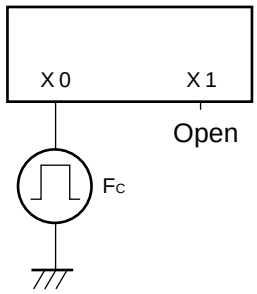


• Clock conditions

When a crystal or ceramic resonator is used



When an external clock in use



(4) Instruction Cycle

(V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Minimum execution time (Instruction cycle)	t_{inst}	4/F_C	64/F_C	µs	64/F_C, 16/F_C, 8/F_C, 4/F_C

(5) Serial I/O Timing

(V_{CC} = +5.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Vlue		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK	Internal shift clock mode	2 t_{inst}*	—	µs	
SCK↓→SO time	t_{SLOV}	SCK, SO		– 200	+200	ns	
Valid SI → SCK↑	t_{IVSH}	SI, SCK		0.5 t_{inst}*	—	µs	
SCK↑→valid SI hold time	t_{SHIX}	SCK, SI		0.5 t_{inst}*	—	µs	
Serial clock “H” pulse width	t_{SHSL}	SCK	External shift clock mode	t_{inst}*	—	µs	
Serial clock “L” pulse width	t_{SLSH}			t_{inst}*	—	µs	
SCK↓→SO time	t_{SLOV}	SCK, SO		0	200	ns	
Valid SI → SCK↑	t_{IVSH}	SI, SCK		0.5 t_{inst}*	—	µs	
SCK↑→valid SI hold time	t_{SHIX}	SCK, SI		0.5 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle”.

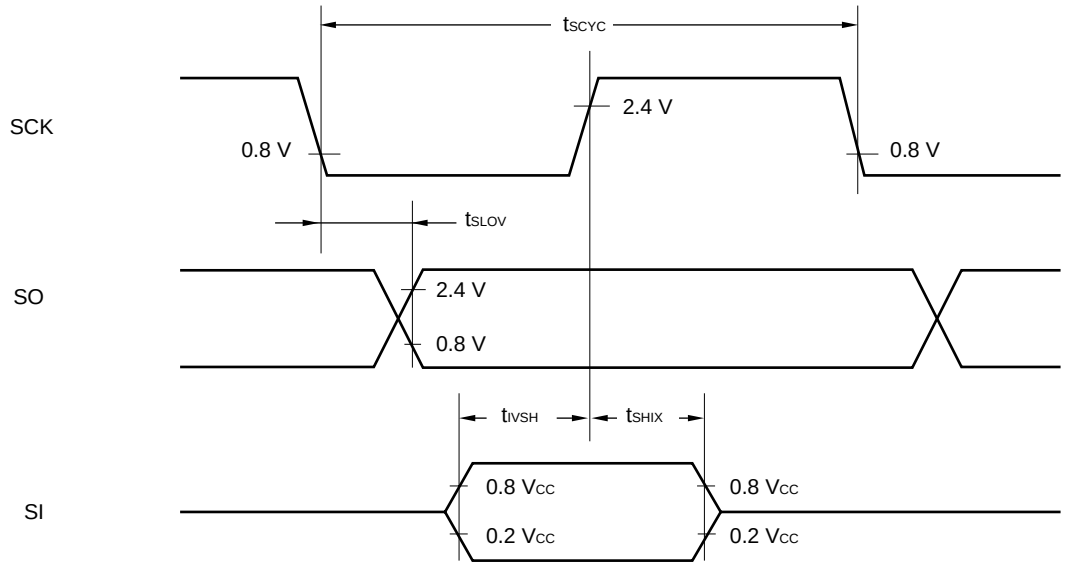
(6) UART Timing

(V_{CC} = +5.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

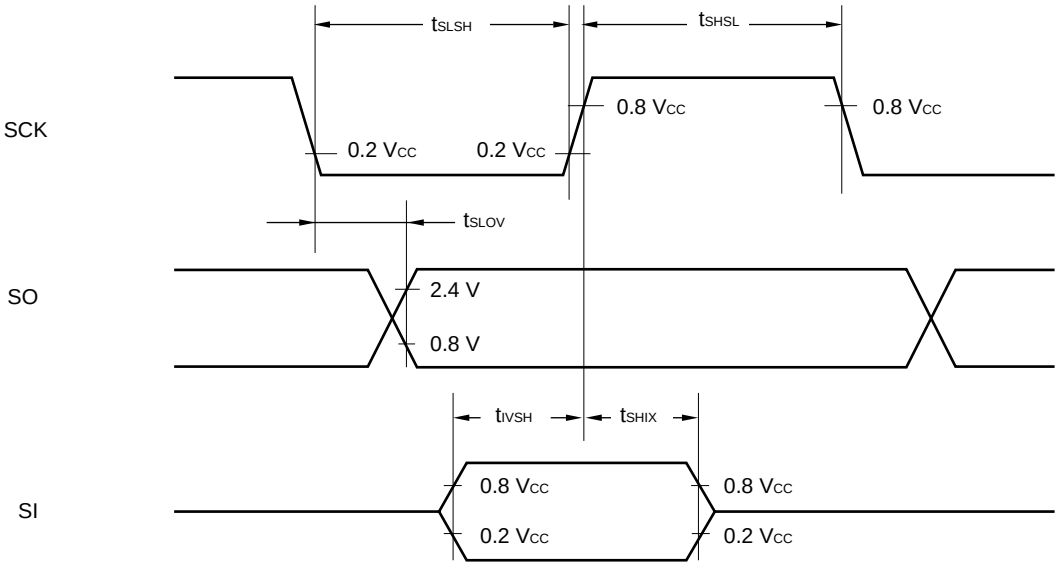
Parameter	Symbol	Pin name	Condition	Vlue		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK	Internal shift clock mode	2 t_{inst}*	—	µs	
SCK↓→SO time	t_{SLOV}	SCK, SO		– 200	+200	ns	
Valid SI → SCK↑	t_{IVSH}	SI, SCK		0.5 t_{inst}*	—	µs	
SCK↑→valid SI hold time	t_{SHIX}	SCK, SI		0.5 t_{inst}*	—	µs	
Serial clock “H” pulse width	t_{SHSL}	SCK	External shift clock mode	t_{inst}*	—	µs	
Serial clock “L” pulse width	t_{SLSH}			t_{inst}*	—	µs	
SCK↓→SO time	t_{SLOV}	SCK, SO		0	200	ns	
Valid SI → SCK↑	t_{IVSH}	SI, SCK		0.5 t_{inst}*	—	µs	
SCK↑→valid SI hold time	t_{SHIX}	SCK, SI		0.5 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle”.

• Internal shift clock mode



• External shift clock mode

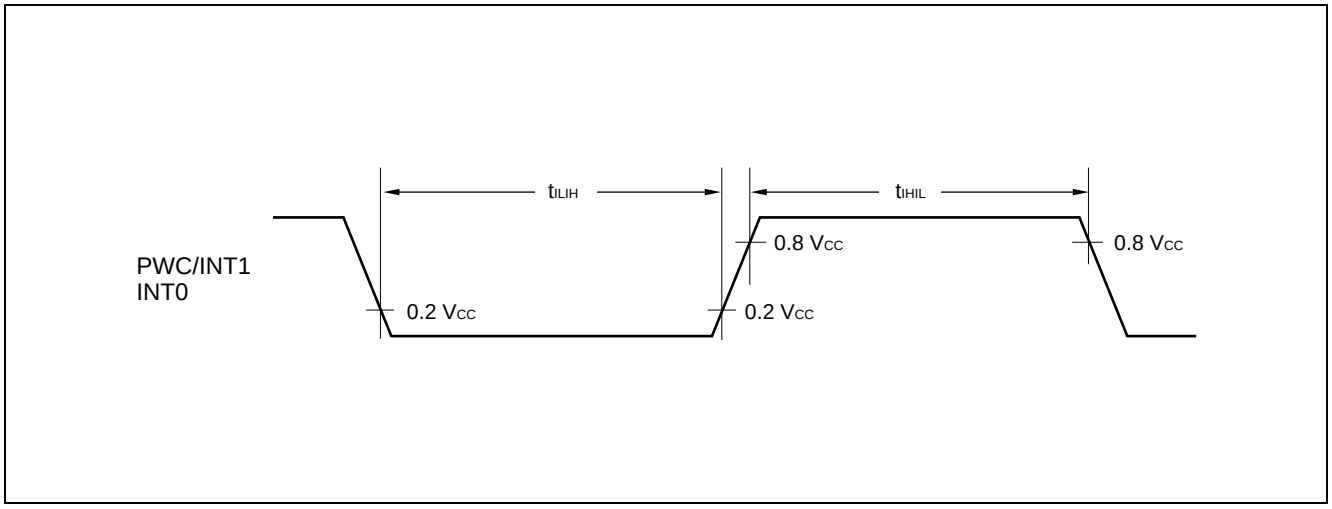


(7) Peripheral Input Timing

(V_{CC} = +5.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

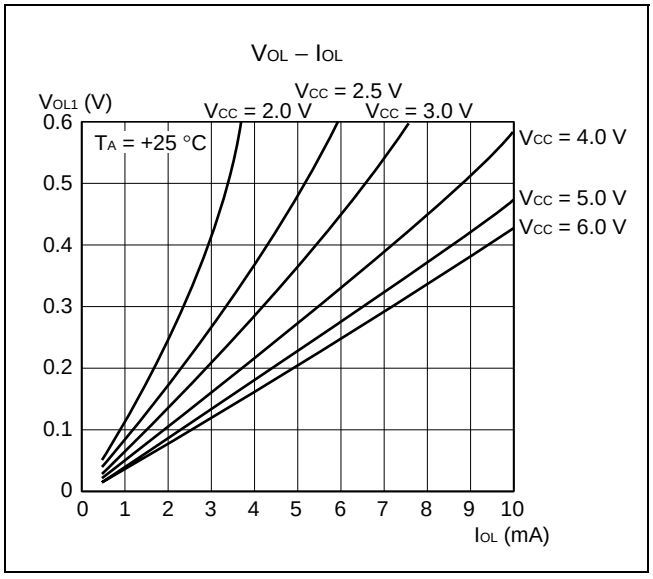
Parameter	Sym-bol	Pin name	Condi-tion	Vlue		Unit	Remarks
				Min	Max		
Peripheral input “H” level pulse width	t_{ILIH}	PWC/INT1 INT0	—	2 t_{inst} *	—	µs	
Peripheral input “L” level pulse width	t_{IHIL}			2 t_{inst} *	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle”.

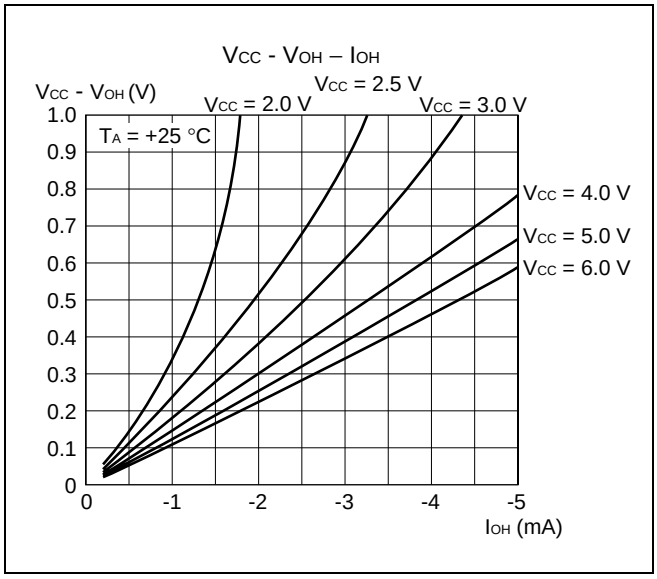


■ EXAMPLE CHARACTERISTICS

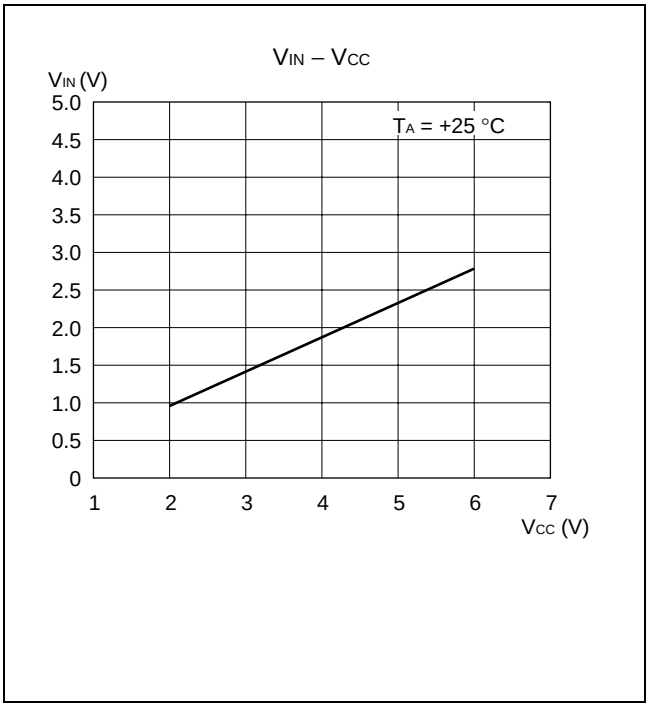
(1) ”L” Level Output Voltage



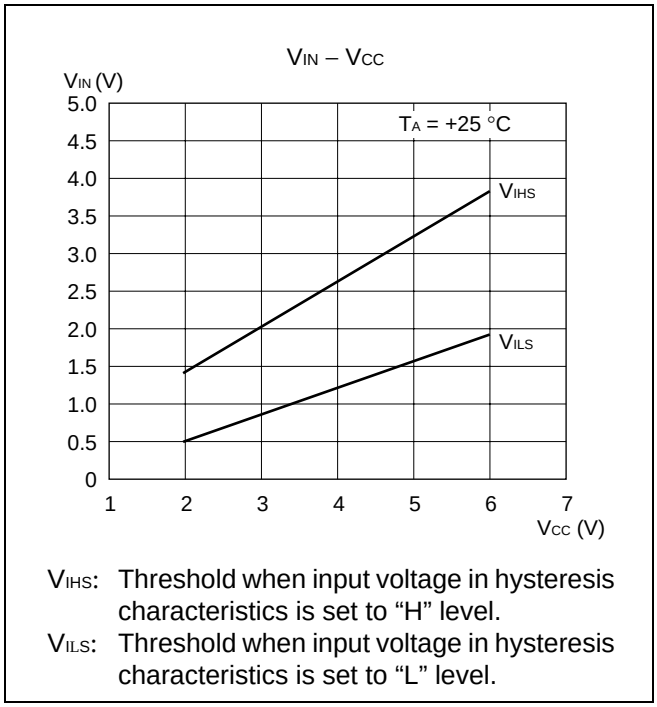
(2) “H” Level Output Voltage



((3) “H” Level Input Voltage/ “L” Level Input Votage (CMOS Input)



(4) “H” Level Input Voltage / ”L” Level Input Voltage (CMOS Hysterisis Input)

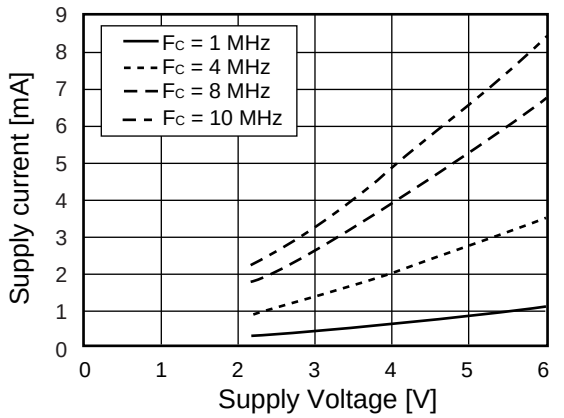


V_{IHS}: Threshold when input voltage in hysteresis characteristics is set to “H” level.

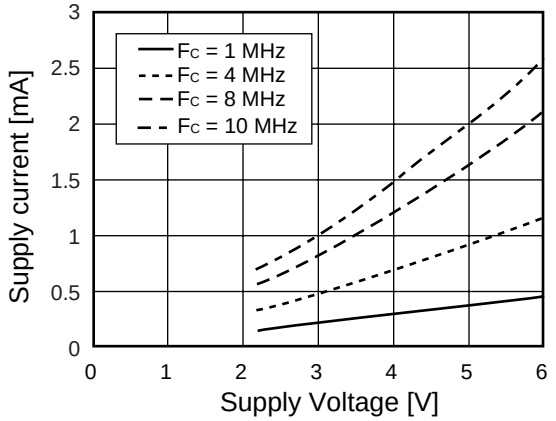
V_{ILS}: Threshold when input voltage in hysteresis characteristics is set to “L” level.

(5) Power Supply Current (External Clock)

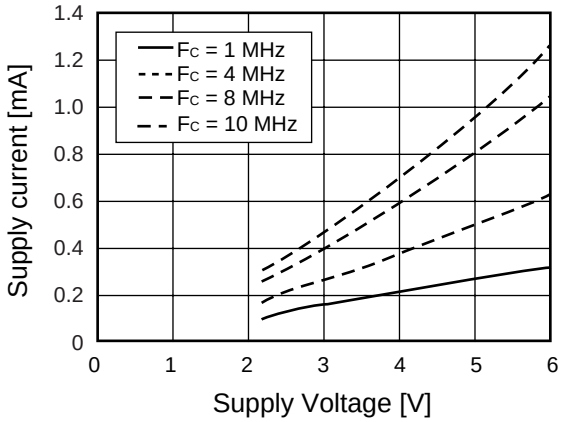
MB89805 ICC1 Example Characteristics
T_A = +25 °C



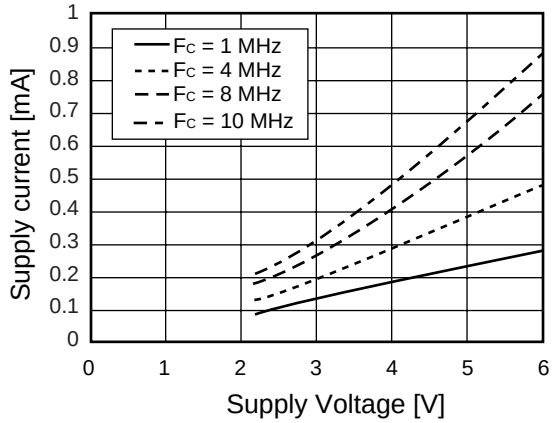
MB89805 ICCS1 Example Characteristics
T_A = +25 °C



MB89805 ICC2 Example Characteristics
T_A = +25 °C

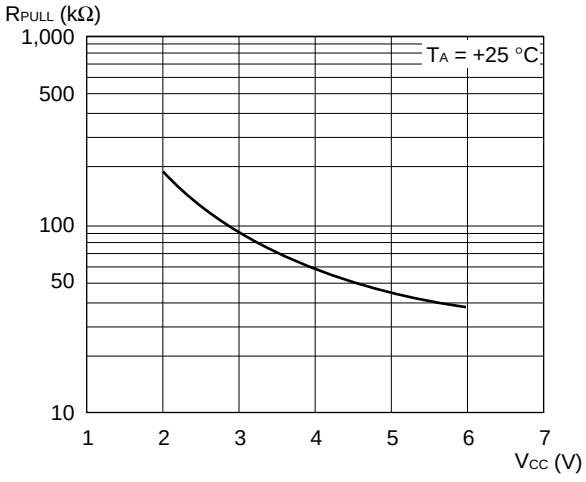


MB89805 ICCS2 Example Characteristics
T_A = +25 °C



(6) Pull-up Resistor Value

R_{PULL} – V_{CC}



■ MASK OPTIONS

No	Part number	MB89803/805	MB89P808, MB89PV800
	Method of specification	Mask Option	Fixed
1	Pull-up resistors P20 to P25, P30 to P33, P40 to P45	Selectable by pin	No
2	Power-on reset With power-on reset Without power-on reset	Selectable	With power-on reset
3	Oscillation stabilization time*1 Approx. $2^{17}/F_C$ (Approx. 13.1 ms) Approx. $2^{13}/F_C$ (Approx. 0.81 ms)	Selectable	$2^{17}/F_C$
4	Reset pin output With reset output Without reset output	Selectable	With reset output
5	Segment output switching 70 segments : No port selection 69 segments : Selection of P17 68 segments : Selection of P17 to P16 66 segments : Selection of P17 to P14 62 segments : Selection of P17 to P10 54 segments : Selection of P17 to P10, P07 to P00	Selectable*2	Selectable*3

*1 : The oscillation settling time is generated by dividing the oscillation clock frequency. Since the oscillation period is not stable immediately after oscillation has been started, therefore, the oscillation settling time in the above list should be regarded as a reference.

*2 : Port selection must be same setting of the segment output selection register of LCD controller.

*3 : Note that, when ports are set, the input voltage value for the port pins are different from those for mask ROM products.
Ports are set by the register setting of the segment output selection register of LCD controller.

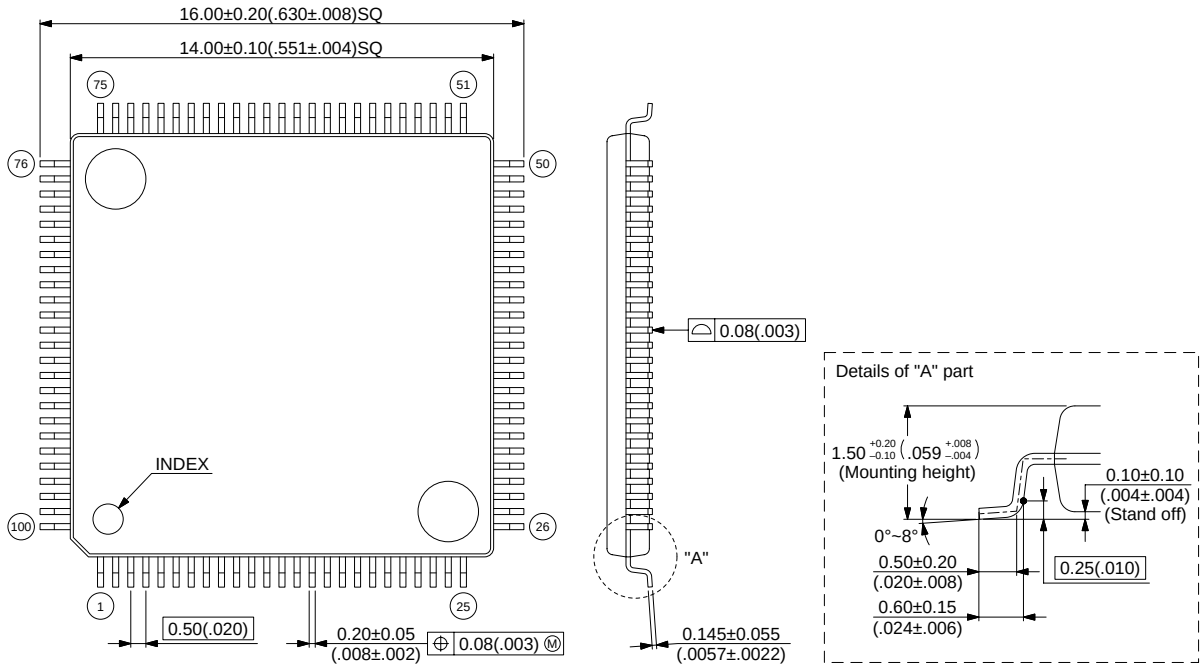
■ ORDERING INFORMATION

Part Number	Package	Remarks
MB89803PF MB89805PF MB89P808PF	100-pin Plastic QFP (FPT-100P-M06)	
MB89803PFV MB89805PFV MB89P808PFV	100-pin Plastic LQFP (FPT-100P-M05)	
MB89PV800CF	100-pin Ceramic MQFP (MQP-100C-P01)	

■ PACKAGE DIMENSIONS

100-pin Plastic LQFP
(FPT-100P-M05)

Note : Pins width and pins thickness include plating thickness.

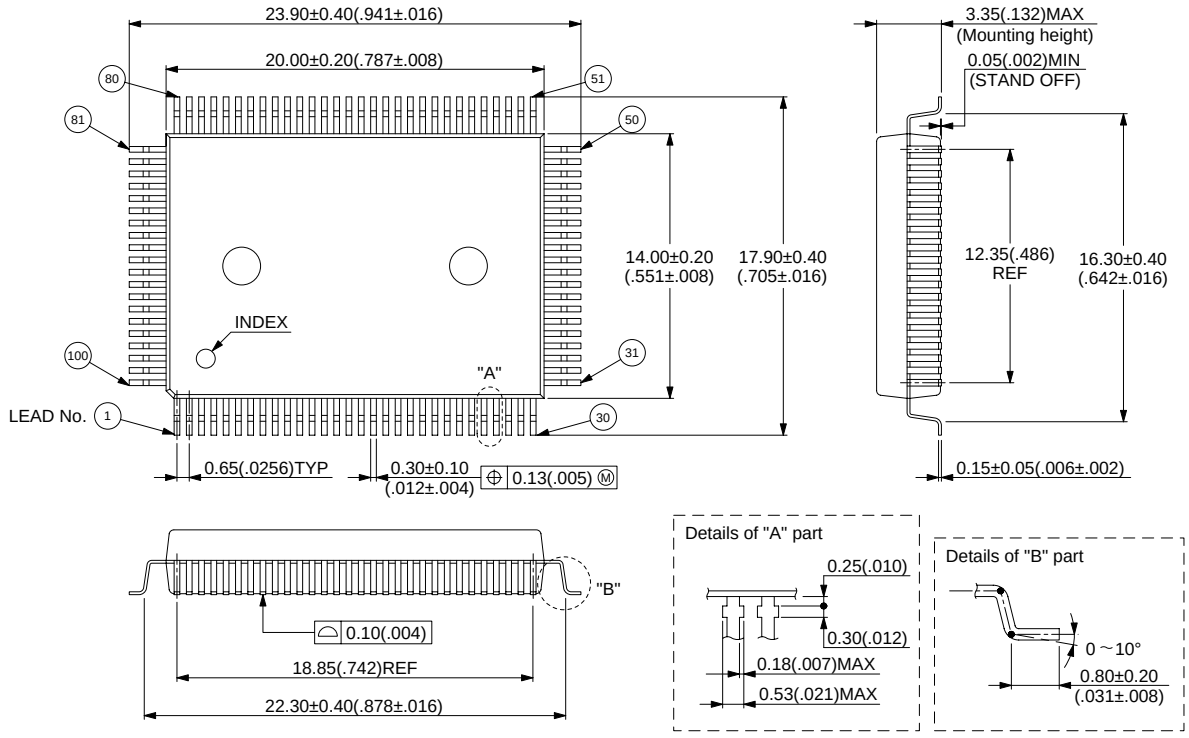


Dimensions in mm (inches)

(Continued)

100-pin Plastic QFP
(FPT-100P-M06)

Note : Pins width and pins thickness include plating thickness.

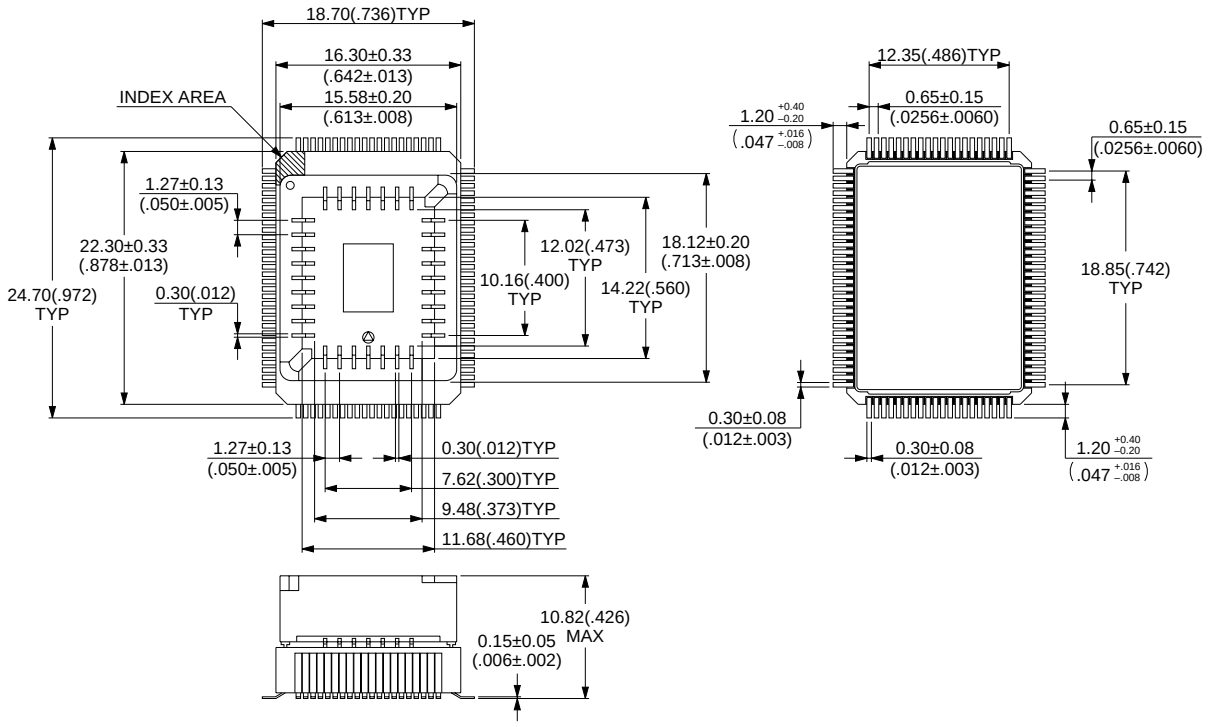


Dimensions in mm (inches)

(Continued)

(Continued)

100-pin Ceramic MQFP
(MQP-100C-P01)



Dimensions in mm (inches)

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