88EM8010/88EM8011

Power Factor Correction Controller

Datasheet

Customer Use Only

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PRODUCT OVERVIEW

The Marvell® 88EM8010/88EM8011 device is a high performance Power Factor Correction (PFC) Controller for boost applications. The device is used for universal PFC front-end boost converters in system or standalone products.

Both devices work at fixed frequencies. 88EM8010 at 60kHz while 88EM8011 at 120kHz.

Marvell advanced mixed signal technology ensures low Total Harmonic Distortion (THD). The IC operates under average Continuous Conduction Mode (CCM).

The 88EM8010/88EM8011 PFC controller improves the steady state and transient performance through Marvell's innovative Digital Signal Processing (DSP) solution. The proprietary adaptive over-current protection has the ability to ensure almost constant power constraint and provides safety provisions including open loop and over voltage protection protocols.

The internal voltage loop compensation and current loop control guarantees system stability and thus reduces the external component count and costs.

The 8-pin SOIC package further facilitates the application design process, saving board space. The resultant simple system design and minimum cost makes 88EM8010/88EM8011 the ideal choice for PFC controllers.

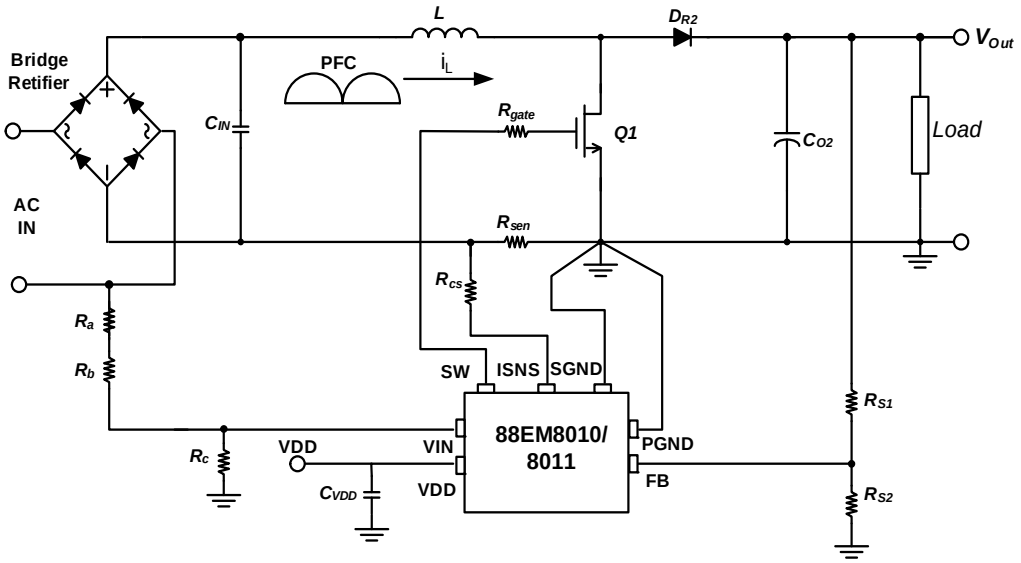
General Features

- **Patented DSP control with adaptive loop coefficient**
- **Continuous Conduction Mode (CCM) operation**
- **Average current mode control**
- **Adaptive control loop achieves high power factor for a wide range of voltage and load conditions**
- **Adaptive over current protection for universal voltage**
- Fixed frequency of operation
- High power factor and low harmonic distortion for a wide range of load conditions
- Up to 2A driver capability
- Minimal external components required
- Under voltage lockout (UVLO)
- Over voltage protection (OVP)
- Thermal shutdown
- Input line frequency range from 45Hz to 65Hz

Applications

- Universal front-end PFC boost controller
- AC/DC adaptors and battery chargers
- Electronic Ballasts front-end with PFC

Figure 1: PFC Boost Circuit Diagram



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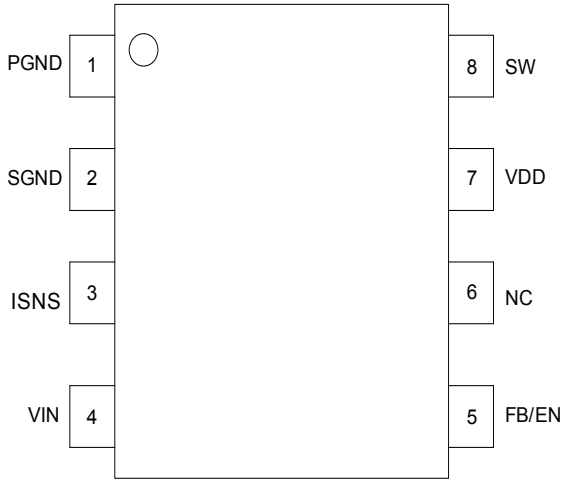
1 Signal Description

1.1 Pin Configurations

Figure 2: SOIC-8 Pin Diagram (Top View)



1.2 Pin Descriptions

Table 1: Pin Descriptions

Pin #	Pin Name	Pin Type	Pin Description
1	PGND	Ground	Power Ground
2	SGND	Ground	Signal Ground
3	ISNS	Input	Current Sense
4	VIN	Input	Voltage Input
5	FB/EN	Input	Feedback/Enable/Shutdown
6	NC	NC	No Connect
7	VDD	Supply	IC Supply Voltage
8	SW	Output	Switch

Table 2: Pin Descriptions

Pin #	Pin Name	Description
1	PGND	**Power Ground** Connected to the source of the primary MOSFET. The PCB trace from the power ground to the source of the MOSFET must be kept as short as possible. To avoid any switching noise interruption on signal processing, PGND and SGND remain separate inside the IC.
2	SGND	**Signal Ground** Must be connected to the power ground with Kelvin sensing connection, so that SGND has dedicated trace and connections and provides noiseless environment for the signal processing.
3	ISNS	**Current Sense** Sense resistor varies for different loads. Pin used for current shaping and for over current protection. Please refer to Section 5, Design and Applications Information, on page 27.
4	VIN	**Voltage Input** • Connects to resistive divider at input AC line “phase” to GND. Voltage applied is a half rectified sine wave scaled down by the input resistive divider. • Voltage input pin is a high impedance input pin. An impedance of 2M (typical) is recommended to be designed from the input AC “phase” to GND in order to reduce the standby power. Higher impedance is preferred with the right PCB design on this pin signal. • Voltage is compared with a threshold reference (V_{VIN_BR}) to detect the zero-cross location of the input sine wave and synthesize (regenerate) the input sine wave. This sine wave is used to generate the current reference. • Brown-out protection[1] function is also provided by this pin. A resistor devider with a 100:1 ratio from the highside resistor to the lowside resistor is corresponding to the “brown-out protection” input voltage as 50V (RMS). Increasing that raio will increase the “brown-out voltage”. Please refer to footnote[1] for further explaination.
5	FB/EN	**Feedback** The output voltage is scaled to 2.5V with 100% rated value. Transition from soft start to normal regulation at 87.5% rated V_{FB}. Over voltage shutdown SW gate signal at 107% rated V_{FB} and recover once below V_{FB_OVP}. There is another threshold ($V_{FB\_OVP\_LATCH}$) as 3.77V on the FB pin. When FB Voltage reaches $V_{FB\_OVP\_LATCH}$, SW signal is shutdown and latched until another VDD power on reset. **EN: Enable/Shutdown** • At V_{FB}>V_{FB_EN} (Table 5) IC is enabled. • Pulling this pin to V_{FB} < V_{FB_SHDN} (Table 5) disables the chip back to sleep mode Note: A 200k resistor inside IL between FB pin to SGND. This should be included in the calculation for the design of the output voltage feedback resistor devider.
6	NC	**No Connect** **Float this pin.**
7	VDD	**IC Supply Voltage** Nominal voltage is 12V (typical) and the Under Voltage Lockout (UVLO) for V_{DD} <V_{DD_UVLO} (Table 5). When V_{DD} < V_{DD_UVLO}, IC is shut down. Start voltage of IC is V_{DD_ON} (Table 5) and maximum voltage is 16V (Table 5). It should be clamped by a Zener for protection in the system design.
8	SW	**Switch** PWM gate signal for the boost switch. Connects to the gate of external boost MOSFET. It is the DSP core output for ON/OFF time buffered through the internal adaptive driver.

1. Brown-out voltage is determined by R_a , R_b, and R_c as shown in Figure 1. Please refer to Section 5.1 for a further understanding.

2 Electrical Specifications

2.1 Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings[1]

NOTE: Stresses above those listed in Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Symbol	Parameter	Min	Max	Units
V_{DD}	Power Supply (Voltage to PGND=SGND)	-0.3	18	V
V_{Isns}	Voltage at ISNS pin	-0.5	3	V
V_{VIN}	Voltage at VIN pin	-0.3	5.5	V
V_{FB}	Voltage at FB pin	-0.3	5.5	V
V_{SW}	Output Driver Voltage		18	V
θ_{JA}	Thermal Resistance SOIC-8		156.5	°C/W
	Thermal Resistance DIP-8		89.5	°C/W
T_A	Operating Ambient Temperature Range[2]	-40	85	°C
T_J	Maximum Junction Temperature		125	°C
T_{STOR}	Storage Temperature Range	-65	150	°C
V_{ESD}	ESD Rating[3]		2	kV

1. Exceeding the absolute maximum rating may damage the device.
2. Specifications over the -40°C to 85°C operating temperature ranges are assured by design, characterization and correlation with statistical process controls.
3. Devices are ESD sensitive. Handling precautions recommended. Human Body model, 1.5kΩ in series with 100pF.

2.2 Recommended Operating Conditions

Table 4: Recommended Operating Conditions[1]

Symbol	Parameter	Min	Typ	Max	Units
T_A	Operating Ambient Temperature[2]	-40		85	°C
T_J	Junction Temperature	-20		125	°C

1. This device is not guaranteed to function outside the specified operating temperature range.
2. Over the –40°C to 85°C operating temperature ranges are assured by design, characterization, and correlation with statistical process controls.

2.3 Electrical Characteristics

Table 5: Electrical Characteristics

NOTE: A 12V supply voltage is applied and the ambient temperature (T_A) = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD} Supply						
V_{DD}	Supply Voltage		7.0	12	16	V
V_{DD_ON}	V_{DD} Power On Threshold	First time power on operation		11.9	12.22	V
V_{DD_UVLO}	V_{DD} Power Off Threshold (UVLO)	After V_{DD} is powered up and running		7.0	7.2	V
$V_{DD\_UVLO\_HYS}$	V_{DD_UVLO} Hysteresis		4.7		5.3	V
I_{DD_QST}	V_{DD} Quiescent Current[1]	V_{DD} = 12V			95	µA
I_{DD_OP}	V_{DD} Operating Current	V_{DD} = 12V; C_{Gate} = 1nF F_{SW} = 118kHz V_{IN}= 0		5.2	6.2	mA
Thermal Shutdown						
T_{SD}	Thermal Shutdown		150			°C
T_{SD_HYS}	Hysteresis for Thermal Shutdown		25			°C
Gate Driver						
V_{G_HI}	Minimum Gate High Voltage[2]	V_{DD} = 12V C_{Gate} = 1nF Sourcing 500mA	10.0			V
V_{G_LO}	Maximum Gate Low Voltage[3]	V_{DD} = 12V C_{Gate} = 1nF Sinking 500mA			2.0	V
R_{DSON}	Gate Drive Resistance	Sourcing 75mA T=25°C		2.4		Ω
	Gate Drive Resistance	Sinking 20mA T=25°C		2.0		Ω
I_{SW_PK}	Driver Peak Current	C_{Gate} = 10 nF V_{DD} = 12 V	2.0			A
t_R	Rise Time	C_{Gate} = 1 nF		35		ns
		C_{Gate} = 10 nF		125		ns
t_F	Fall Time	C_{Gate} = 1 nF		35		ns
		C_{Gate} = 10 nF		145		ns

Table 5: Electrical Characteristics

NOTE: A 12V supply voltage is applied and the ambient temperature (T_A) = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
D_{MAX}	Maximum Duty Cycle				97	%
Feedback/Overvoltage						
V_{FB_REG}	Normal Regulation Reference	IC powered on		2.55		V
V_{FB_EN}	V_{FB} at Enable Threshold	IC powered on by V_{DD_ON}. Transition from sleep mode to IC enable at Enable Threshold of V_{FB_EN}		0.278		V
V_{FB_SHDN}	V_{FB} at Shutdown Threshold	IC powered on by V_{DD_ON}. Transfe from IC enable to sleep mode at Shutdown Threshold of V_{FB_SHDN}		0.248		V
$V_{FB\_EN\_HYS}$	V_{FB} at Enable Hysteresis			0.03		V
V_{FB_OVP}	Over Voltage Protection Threshold	At 107% of V_{FB_REG}.	2.67	2.71	2.75	V
$V_{FB\_OVP\_HYS}$	Over Voltage Protection Hysteresis		0.102		0.108	V
$V_{FB\_OVP\_LATCH}$	Over Voltage Protection Latch			3.77		V
Current Sensing and Current Protection[4]						
V_{IOVER_TH1}	Over Current Threshold Zone 1[5]	Peak value of half-sine voltage at V_{IN}: $1.26<V_{IN}<1.89V_{pk}$[6]		397		mV
V_{IOVER_TH2}	Over Current Threshold Zone 2[5]	Peak value of half-sine voltage at V_{IN}: $1.89<V_{IN}<2.59V_{pk}$[7]		329		mV
V_{IOVER_TH3}	Over Current Threshold Zone 3[5]	Peak value of half-sine voltage at V_{IN}: $2.59< V_{IN}<3.43V_{pk}$[8]		269		mV
V_{IOVER_TH4}	Over Current Threshold Zone 4[5]	Peak value of half-sine voltage at V_{IN}: $3.43<V_{IN}<3.85V_{pk}$[9]		202		mV
88EM8010 Switching Frequency Oscillator						
F_{SW}	Frequency			59		kHz
88EM8011 Switching Frequency Oscillator						
F_{SW}	Frequency		100.3	118	135.7	kHz

1. Quiescent Current: V_{DD} power supply current before V_{DD} first time reaches V_{DD_On}.

2. Considering the voltage drop on the internal driver MOSFET during current sourcing.
3. Considering the voltage drop on the internal driver MOSFET during current sinking.
4. To achieve almost constant power limit for the universal input range, current protection self-adjusts thresholds in four zones of input voltage levels. A margin of 50% compared to the rated current is considered for the threshold current values.
5. Threshold of negative voltage drop across R_{sns} due to instantaneous current
6. With input divider ratio of 1/100, these values are equivalent to 90 V_{rms}<V_{line}<135 V_{rms}.
7. With input divider ratio of 1/100, these values are equivalent to 135 V_{rms}<V_{line}<185 V_{rms}.
8. With input divider ratio of 1/100, these values are equivalent to 185 V_{rms}<V_{line}<245 V_{rms}.
9. With input divider ratio of 1/100, these values are equivalent to 245 V_{rms}<V_{line}<275 V_{rms}.

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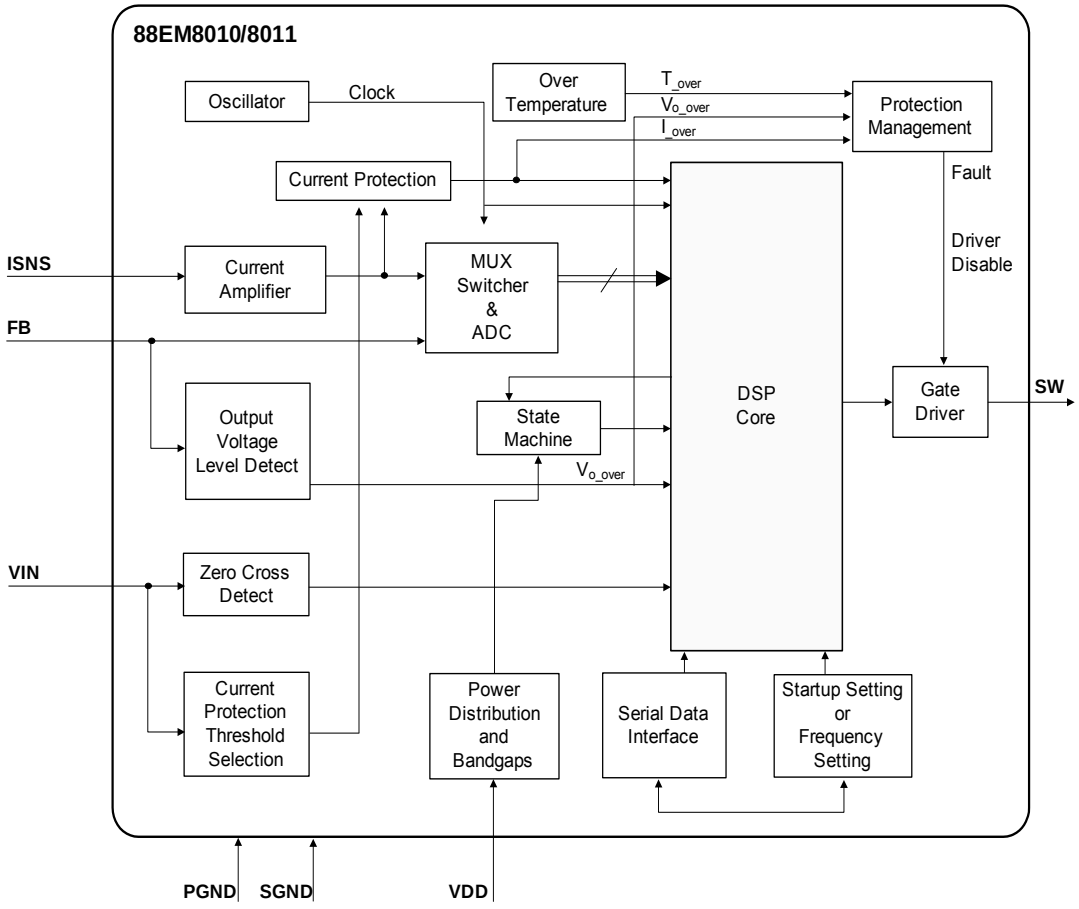
3 Functional Description

3.1 Overview

The 88EM8010/88EM8011 is a high performance, low-cost with minimum component count Power Factor Correction (PFC) Controller. The device is used for Universal PFC front-end boost converters in systems or standalone products. The high performance of 88EM8010/88EM8011 is accompanied with its small system size and simplicity of application. Figure 3 shows the top level block diagram.

Figure 3: Top Level Block Diagram



3.2 Signal Process and Functions

The 88EM8010/88EM8011 boost power board includes three inputs:

- Resistive divider signal from AC line voltage
- Feedback from the output DC bus
- Voltage across the current sense resistor

The input phase voltage to ground (half rectified sine wave) scaled down by the input resistive divider is applied to pin V_{IN}. This signal used for estimation of the AC line voltage and regeneration of the AC sine wave. It is also used for voltage level detection that produces adaptive multiple thresholds for the over current limit and guarantees a constant power limit from the AC source.

Signal from the DC bus voltage through the output resistor devider and Analog-to-Digital Converter (ADC) provides the feedback data for the voltage PI control loop.

HF switching current pulse signal is retrieved from the voltage drop across the current sense resistor. Current sensing signal is negative to the ground. This signal after HF noise filter and fixed gain amplification, is transferred through the ADC to the digital current loop and the current error amplifier. The reference current for the current control PI loop is provided by multiplying the voltage error amplifier output and the regenerated sinusoidal line voltage information.

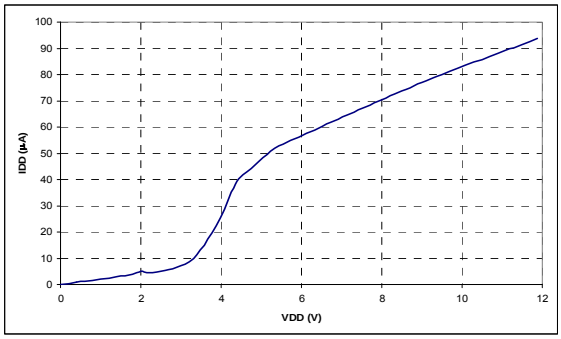
4 Functional Characteristics

The following applies unless otherwise noted: V_{IN} = 60Hz half-wave sinusoidal from 0V to the peak voltage (V_{PK}) given in the test conditions of each graph. T_A = 25°C.

All measurement readings are typical.

4.1 V_{DD} Characteristics

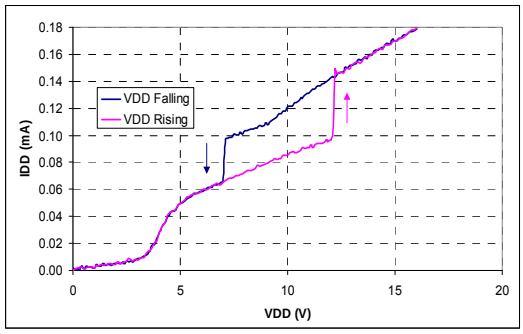
Figure 4: I_{DD} Quiescent (I_{DD_QST}) vs. V_{DD}



Test Conditions:

- V_{IN} = 0V
- F_{SW} = 118kHz
- V_{FB} = 0V
- C_{Gate} = 1nF
- V_I_{sns} = 0V

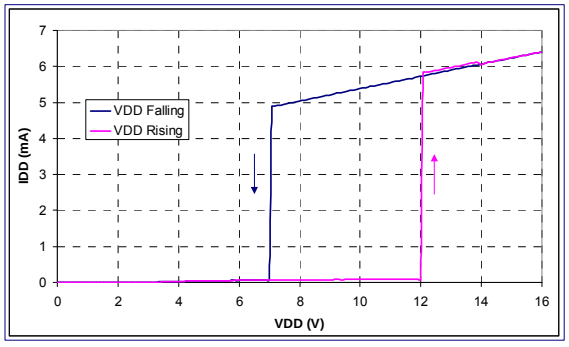
Figure 5a: I_{DD} vs. V_{DD} (V_{DD_ON})



Test Conditions:

- V_{IN} = 0V
- F_{SW} = 118kHz
- **V_{FB} = 0V**
- C_{Gate} = 1nF
- V_I_{sns} = 0V

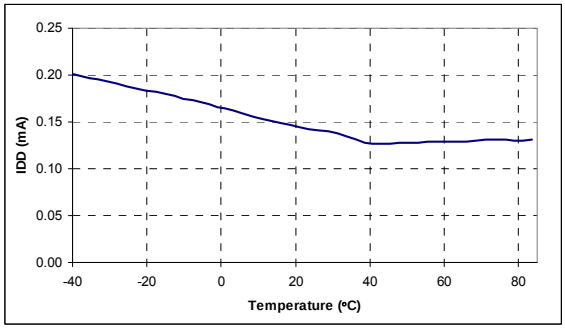
Figure 5b: I_{DD} vs. V_{DD} (V_{DD_ON}), V_{FB} Enable



Test Conditions:

- V_{IN} = 0V
- F_{SW} = 118kHz
- **V_{FB} = 2.4V**
- C_{Gate} = 1nF
- V_I_{sns} = 0V

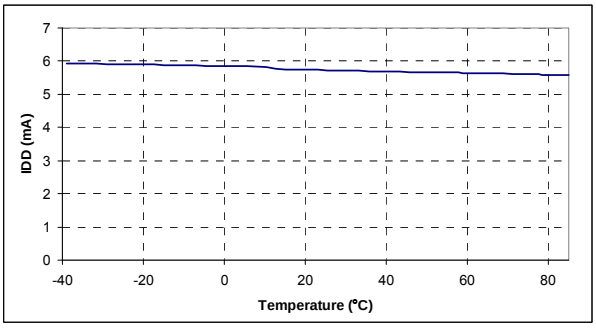
Figure 6a: I_{DD} Sleep (I_{DD_OP}) vs. Temperature



Test Conditions:

- V_{DD} = 12V
- V_{IN} = 0V
- F_{SW} = 118kHz
- **V_{FB} = 0V**
- C_{Gate} = 1nF
- V_I_{sns} = 0V

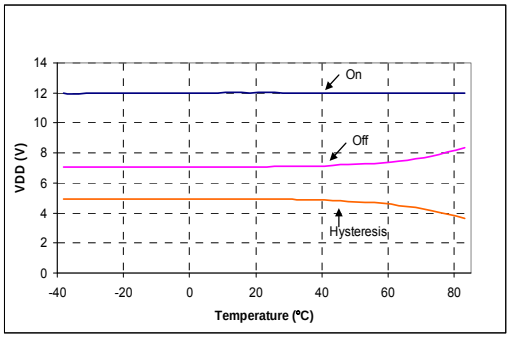
Figure 6b: I_{DD} Operation (I_{DD_OP}) vs. Temperature



Test Conditions:

- V_{DD} = 12V
- V_{IN} = 0V
- F_{SW} = 118kHz
- **V_{FB} = 2.4V**
- C_{Gate} = 1nF
- V_I_{sns} = 0V

Figure 7: V_{DD} On/Off vs. Temperature

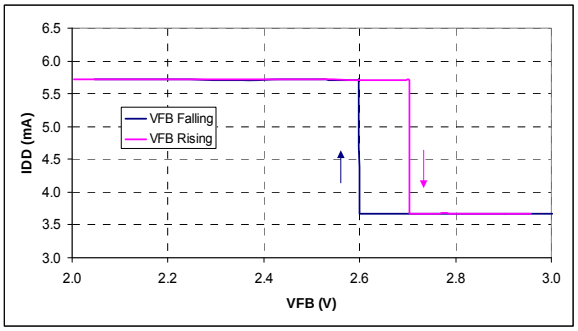


Test Conditions:

- V_{IN} = 0V
- F_{SW} = 118kHz
- F_{FB} = 2.4V
- C_{Gate} = 1nF
- V_I_{sns} = 0V

4.2 V_{FB} Characteristics for Over Voltage Protection

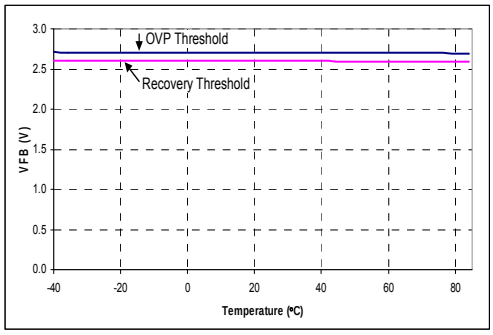
Figure 8: I_{DD} vs. V_{FB} (OVP)



Test Conditions:

- V_{DD} = 12V
- V_{IN} = 0V
- F_{SW} = 118kHz
- C_{Gate} = 1nF
- V_I_{sns} = 0V

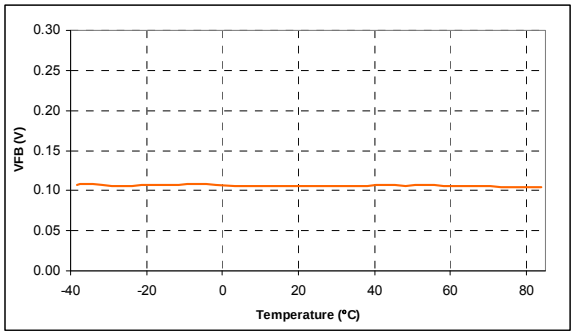
Figure 9: V_{FB_OVP} vs. Temperature



Test Conditions:

- V_{DD} = 12V
- V_{IN} = 0V
- F_{SW} = 118kHz
- C_{Gate} = 1nF
- V_I_{sns} = 0V

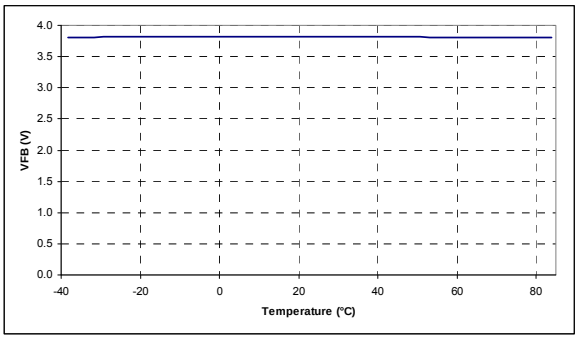
Figure 10: V_{FB_OVP} Hysteresis vs. Temperature



Test Conditions:

- V_{DD} = 12V
- V_{IN} = 0V
- F_{SW} = 118kHz
- C_{Gate} = 1nF
- V_I_{sns} = 0V

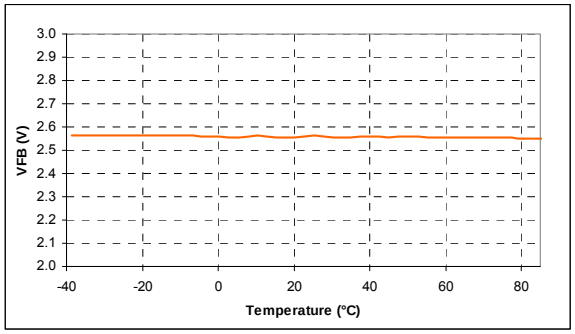
Figure 11: $V_{FB\_OVP\_LATCH}$ vs. Temperature



Test Conditions:

- V_{DD} = 12V
- V_{IN} = 0V
- F_{SW} = 118kHz
- C_{Gate} = 1nF
- V_I_{sns} = 0V

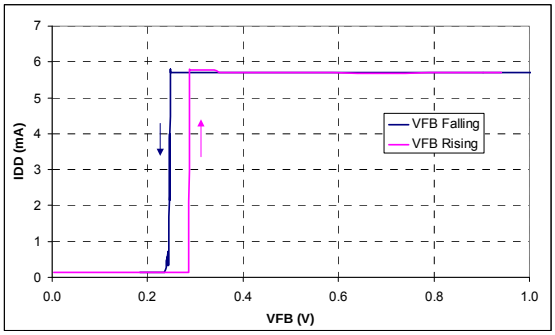
Figure 12: Normal Regulation Reference (V_{FB_REG}) vs. Temperature



Test Conditions:

- V_{DD} = 12V
- V_{IN} = 2V
- F_{SW} = 118kHz
- C_{Gate} = 1nF
- V_I_{sns} = 0V

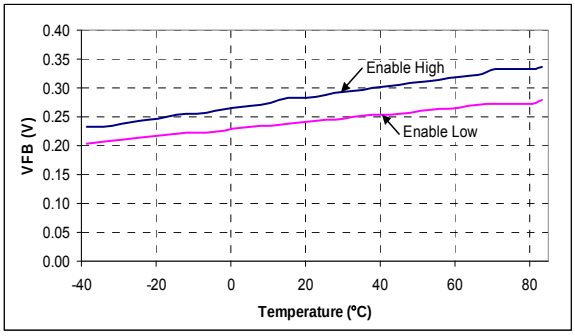
Figure 13: I_{DD} vs. V_{FB} (Enable)



Test Conditions:

- V_{DD} = 12V
- V_{IN} = 0V
- F_{SW} = 118kHz
- C_{Gate} = 1nF
- V_I_{sns} = 0V

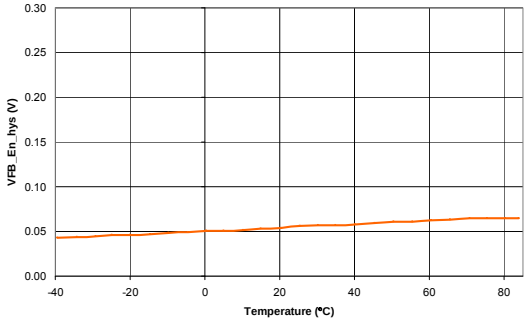
Figure 14: V_{FB_EN} (Enable) vs. Temperature



Test Conditions:

- V_{DD} = 12V
- V_{IN} = 0V
- F_{SW} = 118kHz
- C_{Gate} = 1nF
- V_I_{sns} = 0V

Figure 15: V_{FB_EN} Hysteresis vs. Temperature

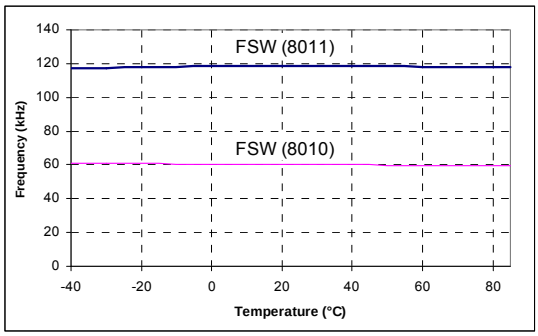


Test Conditions:

- V_{DD} = 12V
- V_{IN} = 0V
- F_{SW} = 118kHz
- C_{Gate} = 1nF
- V_I_{sns} = 0V

4.3 Switching Frequency Characteristics

Figure 16: Switching Frequency vs. Temperature

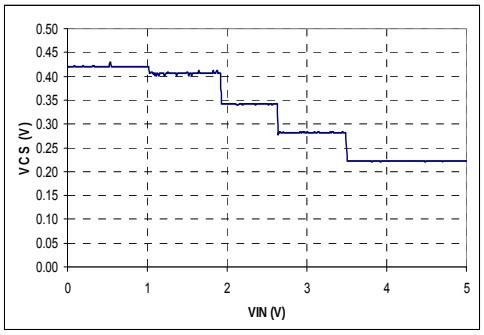


Test Conditions:

- V_{DD} = 12V
- V_{IN} = 0V
- V_{FB} = 2.4V
- C_{Gate} = 1nF
- V_I_{sns} = 0V

4.4 Over Current Threshold Characteristics

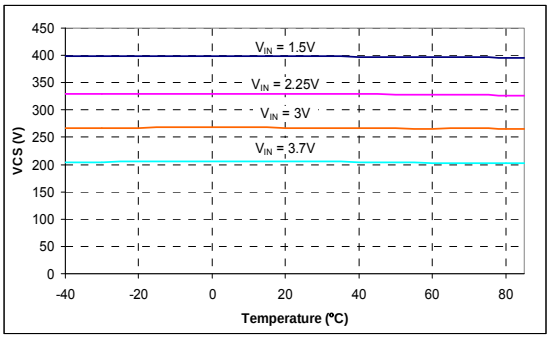
Figure 17: Over Current (V_{IOVER}) vs. Input Voltage V_{IN} Peak Value)



Test Conditions:

- V_{DD} = 12V
- F_{SW} = 118kHz
- V_{FB} = 2.4V
- C_{Gate} = 1nF
- V_I_{sns} = 0V

Figure 18: Over Current (V_{IOVER}) vs. Temperature



Test Conditions:

- V_{DD} = 12V
- F_{SW} = 118kHz
- V_{FB} = 2.4V
- C_{Gate} = 1nF
- V_I_{sns} = 0V

5 Design and Applications Information

The boost converter is the most popular topology for two stage front-end PFC pre-regulator system. The 88EM8010/88EM8011 chip control algorithm uses Average Current Mode Control for power factor correction applications based on Boost topology with low harmonic distortion and good noise immunity. The IC senses the output voltage and forces it to follow the reference voltage to produce a stable DC output voltage matching the design requirement. It also senses the inductor current and forces the average signal of the inductor current to follow the sinusoidal current reference, therefore achieving unity power factor.

Marvell's innovative PFC control technology improves the performance of the Boost converter used in PFC applications. The 88EM8010/88EM8011 provides the higher drive current capability than that of the competitors' ICs. The 88EM8010/8011 also achieves high power factor/low THD at high line low load condition which is benefited from Marvell mixed signal technology. The Boost PFC solution based on the 88EM8010/88EM8011 provides customers with the simplest structure, lowest cost and best performance compared with the other industry solutions currently on the market.

The following sections provide guidelines for the application design, component selection, and board layout in order to improve front-end Boost PFC performance. There are three analog input signals listed below are required from the power train to the controller IC 88EM8010/88EM8011.

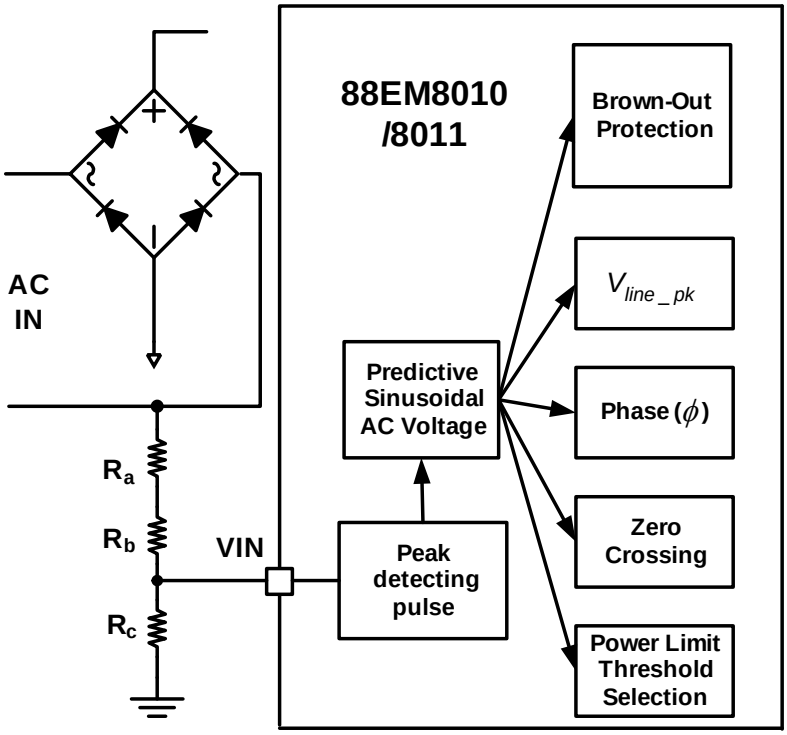
1. Input voltage signal at VIN pin is a half sinusoidal waveform. It is fed into the VIN pin through the input voltage resistor divider. This is for the line frequency zero-cross detection for PFC.
2. Output voltage signal at FB pin is the output voltage through the resistor divider to feedback on FB pin. This is for the voltage loop regulation.
3. Current sensing signal through the sensing resistor to the ISNS pin. This is for the average current mode control to achieve a good sinusoidal current waveform and high power factor.

The output signal from the 88EM8010/88EM8011 is the PWM gate drive signal from the SW pin. The switching frequency on the 88EM8010 device is fixed to 60kHz (typical) while the 88EM8011 is fixed to 120kHz (typical). Both device tolerances are shown in Table 5, Electrical Characteristics, on page 15.

5.1 Input Voltage Resistor Divider on VIN Pin

An accurate peak detection signal and zero-cross detection for regenerating the input sinusoidal voltage is the most important issue for a proper current shaping and total harmonic distortion (THD) improvement. If the threshold reference is too high, near the peak area, the calculation may lose accuracy because of the low slope. On the other hand, if the threshold reference is too low due to the possible distortions near the zero-crossing, there could be an error on zero-cross detection. For a universal input voltage range (85VAC~270VAC) the optimum accuracy would be achieved if the threshold level is around 30 degree of the line cycle.

Figure 19: Internal Block for Zero-cross Detection, Brown-out Protection



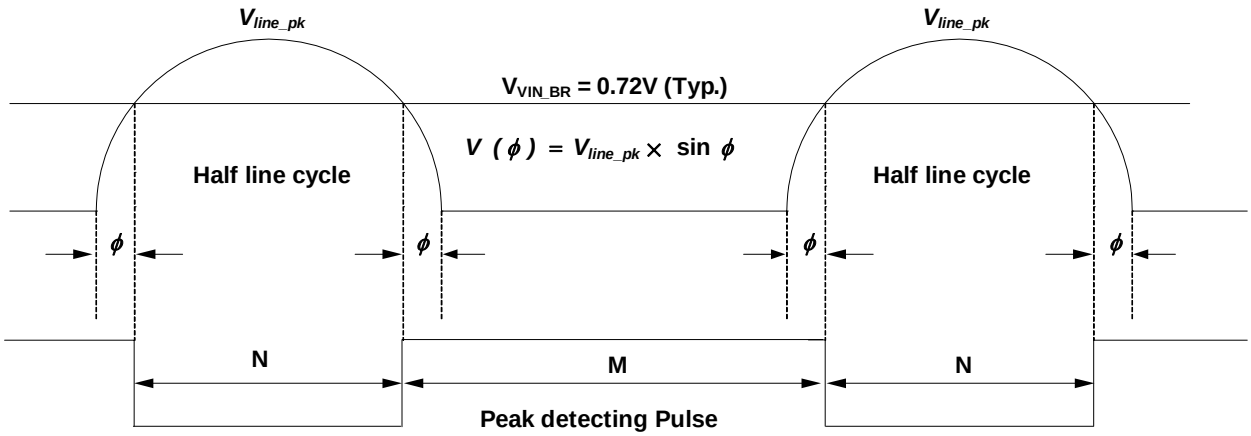
To get a proper sinusoidal AC voltage, UVLO, and peak voltage detection, we need to choose the right value for the sensing resistors: R_a, R_b, and R_c (See Figure 19). If the value is too small there will be higher power loss and if the value is too big the resistor will not properly work due to the picking noise of the VIN signal. The recommended values are shown below:

$$\frac{R_a + R_b}{R_c} = \frac{100}{1} = \frac{1.8M\Omega}{18k\Omega}$$

Equation (1)

For the input voltage resistor divider, the appropriate combination based on the voltage / power rating of the resistors should also be considered.

Figure 20: Peak Detecting Signal for Predictive Sinusoidal AC Voltage



As can be seen in Figure 20, the internal peak detecting circuit generates peak detecting pulse through the inside comparator which has a threshold voltage of 0.72V (typical). Processing of this pulse in DSP core calculates the mid-point (peak point) and the zero-crossing point of the sinusoidal waveform. The phase angle of ϕ is calculated using the width of the high and low signal M&N.

$$N = (\pi - 2\phi) \quad \text{Equation (2)}$$

$$M = (\pi + 2\phi) \quad \text{Equation (3)}$$

$$\phi = \frac{(M - N)}{4} \quad \text{Equation (4)}$$

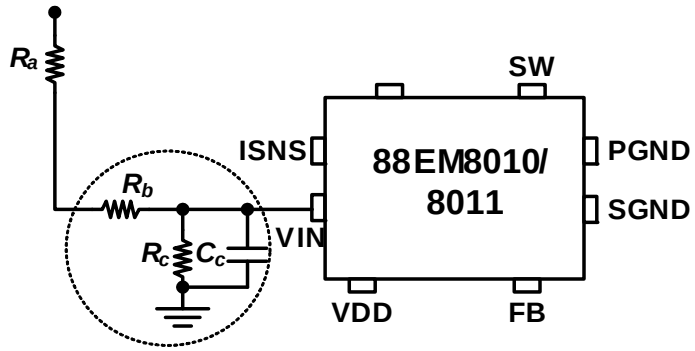
Peak value of the sinusoidal waveform is introduced by the relation:

$$V_{\text{line\_pk}} = \frac{V(\phi)}{\sin(\phi)} \quad \text{Equation (5)}$$

The signal that appears on the VIN pin is a half sinusoidal voltage waveform and its peak line value has to be higher than V_{VIN_BR} of 0.72V (typical) for normal operation. Whenever the V_{VIN_BR} is less than 0.72V at the peak line value, it is considered as a Brown-out condition. The IC only generates 6% duty during the brown-out condition. To adjust the brown-out protection point, the resistance value of R_a, R_b and R_c can be changed. With the recommended resistor values in Equation (1) the brown-out protection voltage is 72V peak value, which is around a 50V RMS value for the input line voltage.

The layout of R_b, R_c and C_c should be kept as close as possible to the VIN pin, as shown in Figure 21 in order to have a proper layout on the input voltage resistor divider and to avoid noise picking. It is also recommended that a 0.1nF–10nF capacitor is connected between the VIN pin and ground with the layout also close to this pin.

Figure 21: Input Voltage Resistor Divider Layout Guidelines



Keep layout of R_b, R_c and C_c as close as possible to Vin pin to have high noise immunity

5.2 Voltage Loop & Output Voltage Feedback on FB Pin

The 88EM8010/88EM8011 IC integrates the voltage loop into digital DSP core. This internal voltage loop has the lower corner frequency for the PFC requirement. The FB pin is the internal voltage loop feedback signal input. The voltage reference of the IC is 2.5V for the rated output voltage.

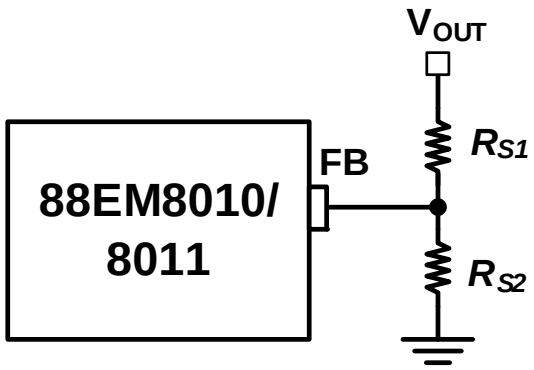
It is well known that the front-end PFC with Boost topology has to maintain low enough bandwidth (less than 20Hz) in order to achieve a good sinusoidal current waveform and power factor under a wide input voltage and load condition. In order to achieve a good sinusoidal current waveform and power factor, the voltage loop regulation coefficient should also be designed properly corresponding to the different input voltages. The adaptive voltage loop coefficient is designed inside the IC to select different voltage regulation parameters corresponding to the different input voltage. This achieves a much better power factor and sinusoidal current waveform compared to any of PFC power system on the market now.

The design of $R_{S1}$and R_{S2}, as shown in Figure 22, is based on the rated output voltage and the power loss of the resistor divider. In order to keep low power consumption on the resistor divider and good signal to noise immunity, a total resistance of several MΩ is recommended for the pair of resistors R_{S1} and R_{S2}. Because there is a 200kΩ resistor inside of the IC between the FB pin to the SGND, the value of R_{S1} and R_{S2} is designed based on Equation (6) as:

$$\frac{V_{ref}}{R_{s2}} + \frac{V_{ref}}{R_0} = \frac{V_{out} - V_{ref}}{R_{s1}} \qquad \text{Equation (6)}$$

Where V_{ref} is 2.5V and R_0 is 200kΩ.

Figure 22: Output Voltage Resistor Divider



5.3 Current Sensing and Over Current Protection

5.3.1 Current Sensing through ISNS Pin

The voltage drop on the current sense resistor should be kept very small in order to reduce the power consumption on the sense resistor (R_{sen}). The voltage drop (V_{sen}) across resistor (R_{sen}) represents the Boost current signal. As shown in Figure 23. V_{sen} is feedback to the ISNS pin through a resistor R_{CS}, which is around 200Ω. This resistor is necessary for the protection of the ISNS pin during inrush and lightning surge condition.

The resistor (R_{sen}) should be designed and calculated such as the example in Table 6 where R_{sen} is designed for a 64W Boost converter. The specification are: output power = 64W, input voltage range = 85-264V, output voltage = 450V, 30% margin of over current on top of the normal current.

Figure 23: Current Sensing Circuit

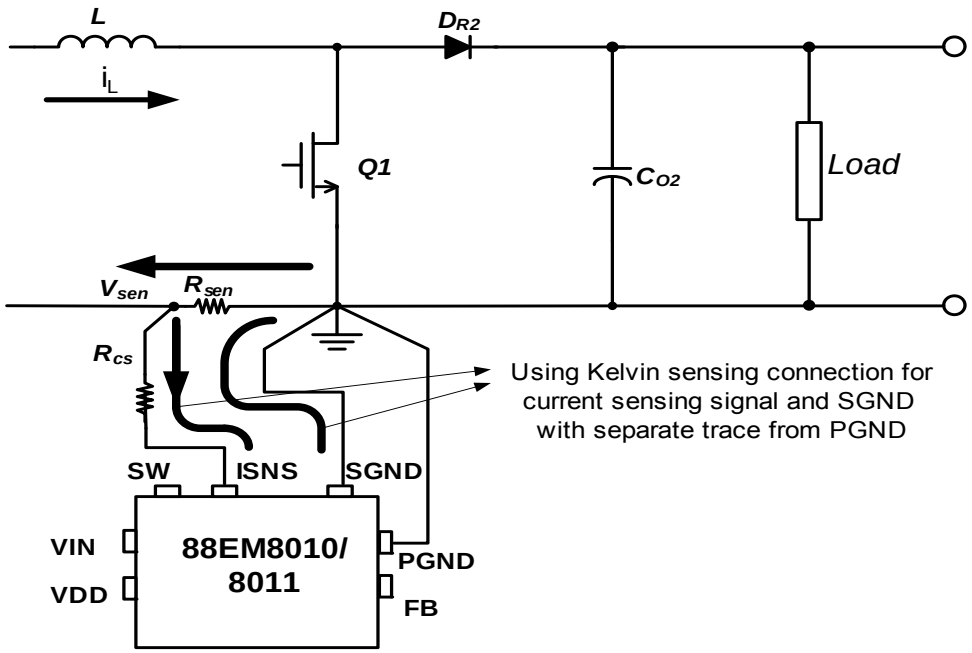


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Table 6: Current Sensing Resistor Selection

Input Power	P_{IN}	64W
Minimum Input Voltage	V_{INMIN}	85V
Maximum Average Input Current	$I_{INMAX} = \sqrt{2} \times \frac{P_{IN}}{V_{INMIN}}$	1.06A
Assume 30% Switching Frequency Ripple	$\Delta ripple = I_{INMAX} \times 30\,\%$	0.32A
Peak Current with Ripple	$i_{peak} = I_{INMAX} + \Delta ripple$	1.38A
Over Current Threshold Zone 1 (Table 5)	$V_{IOVERTH1}$	0.391V
Over Current Margin	I_{MARGIN}	30%
Current Sensing Resistor Calculation	$R_{sns} = \frac{V_{IOVERTH1}}{i_{peak} \times (1 + I_{MARGIN})}$	0.22Ω
Current Sensing Resistor Selection	R_{sns}	0.25Ω

Table 7 shows the reference value of the current sensing resistor. In the practical design, the current sensing resistor value could be fine tuned around the value shown in the table based on the specification and the primary inductance of the Boost transformer.

Table 7: Current Sensing Resistor Selection Reference

Input Power (W)	32	64	125	250
Current Sensing Resistor (Ω)	0.40–0.50	0.20–0.25	0.10–0.125	0.05–0.06

As the layout guideline, the current sensing signal should use Kelvin sensing connection, as shown in Figure 23. It means the SGND should layout as a separate trace from the PGND to avoid any heavy current and spike current sharing on that trace. The V_{sen} net should be layout as close as possible to the R_{sen} resistor. The same time, the R_{sen} resistor should be layout as close as possible to the ground as shown in Figure 23.

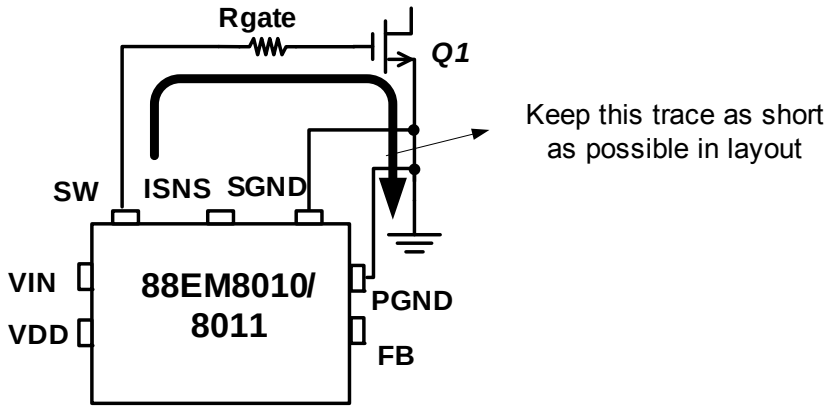
5.3.2 Over Current Limitation

An adaptive current protection threshold is designed in the IC corresponding to the different input voltage in order to get the cycle by cycle current protection to avoid the transformer saturation. The four level threshold is shown in the electrical characteristic table. The universal input voltage is identified into four range from 90V to 275V. With the input voltage resistor divider ratio value as 100:1, these four ranges are 90–135V, 135–185V, 185–245V and 245V to 275V. If the resistor divider ratio value is increased from 100:1 to a higher value, these ranges will shift to the higher voltage side. On the other hand, if the resistor divider ratio value is decreased from 100:1 to a lower value, these ranges will shift to the lower voltage side. Therefore, the customer has the flexibility to adjust these ranges during the design by tuning the input voltage resistor divider ratio around the default value as 100:1.

5.4 SW Pin to MOSFET Gate

The 88EM8010/88EM8011 provides a maximum 2A drive current, which is the strongest drive to date in comparison with the competition on the market. A default resistor of 10Ω is designed to go between the SW pin and the gate of the external MOSFET. The gate driver loop is subject to fast rise and the layout trace should be kept as short as possible in order to minimize the parasitic inductance, as shown in Figure 24.

Figure 24: SW Pin Layout Guidelines



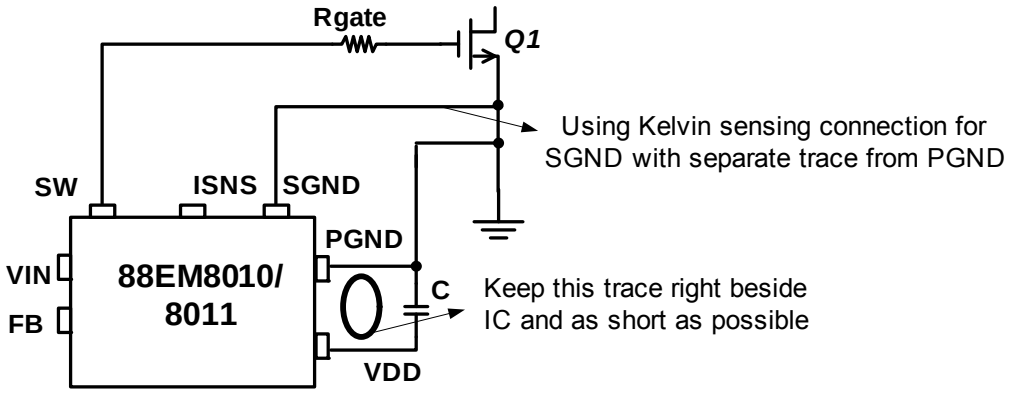
5.5 VDD, Signal Ground (SGND) and Power Ground (PGND)

VDD is the IC power supply pin. It has a typical value of 12V and a maximum operating voltage of 16V. A Zener circuit below 16V is recommended in order to guarantee that the voltage on VDD will not go any higher than 16V. The IC begins to function when VDD powers on at 12V. Once the IC powers on, it keeps functioning as long as the VDD is higher than V_{DD_UVLO}, which is 7V (typical). In a practical design, an electrolytic capacitor is recommended to connect between VDD and ground in order to retain the IC functionality during startup. That capacitor will need to keep the VDD higher than 7V before the bias transformer winding takes over and provides enough energy for the power IC.

A 0.01–0.1μF ceramic capacitor is strongly recommended to be placed between the VDD and IC ground with the layout trace as close to the IC as possible. This capacitor is used for decoupling the noise to VDD and clamping the VDD voltage during the switching of the internal driver circuit.

SGND is directly connected to the system ground by a Kelvin connection trace. The system ground is the source of the MOSFET, as shown in Figure 25. PGND connects to the system ground separately and can not share the same trace with SGND. This is due to pulse current on PGND while driving the external MOSFET on and off. This pulse current produces pulse voltage drops on the PGND trace and may cause the current sensing signal to be distorted if the SGND shares the same trace.

Figure 25: VDD Decoupling Capacitor and Ground Layout Guidelines



5.6 Boost PFC Schematics

Figure 26: 64W/450V Front-End Boost PFC Schematic

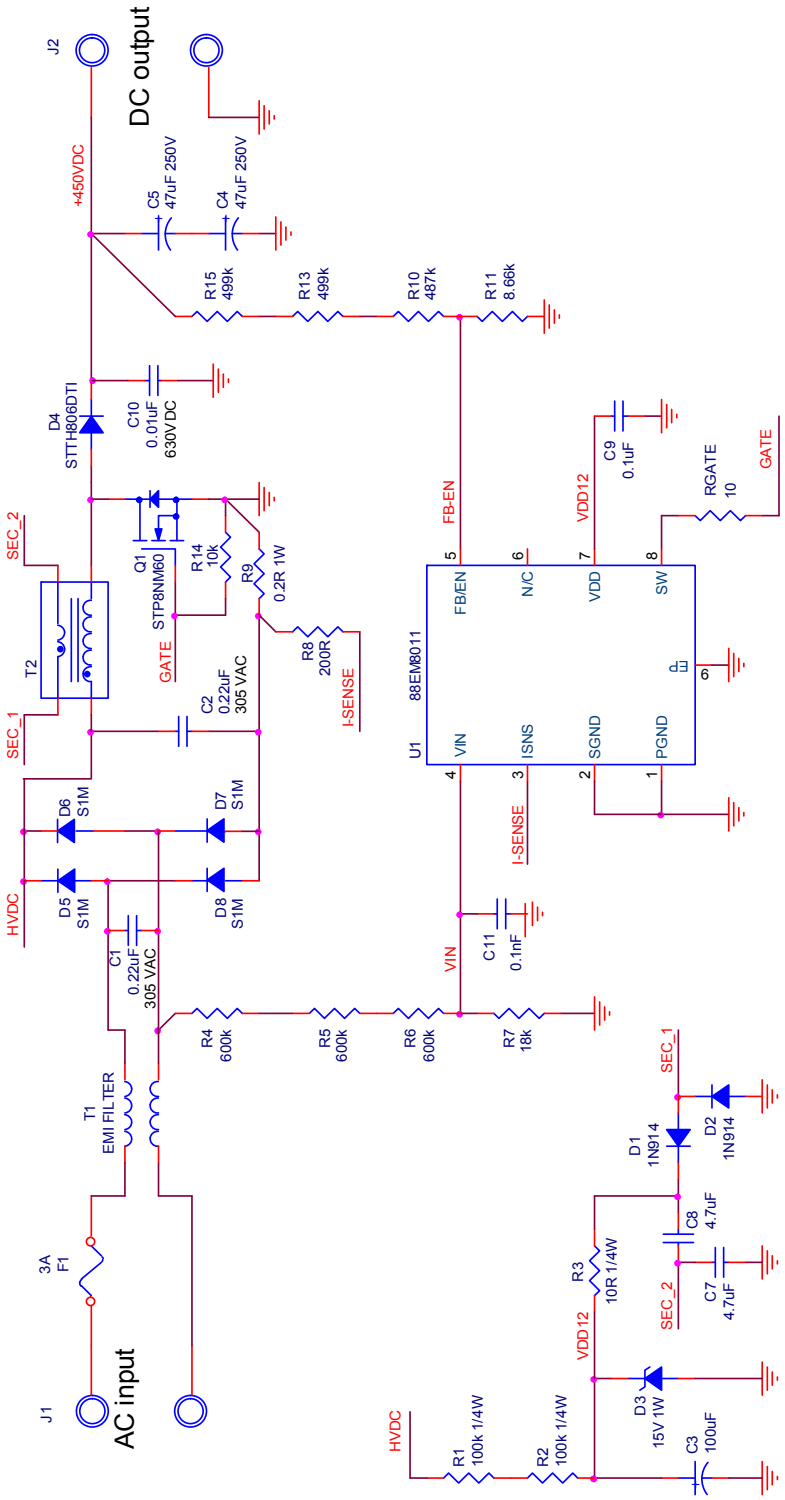
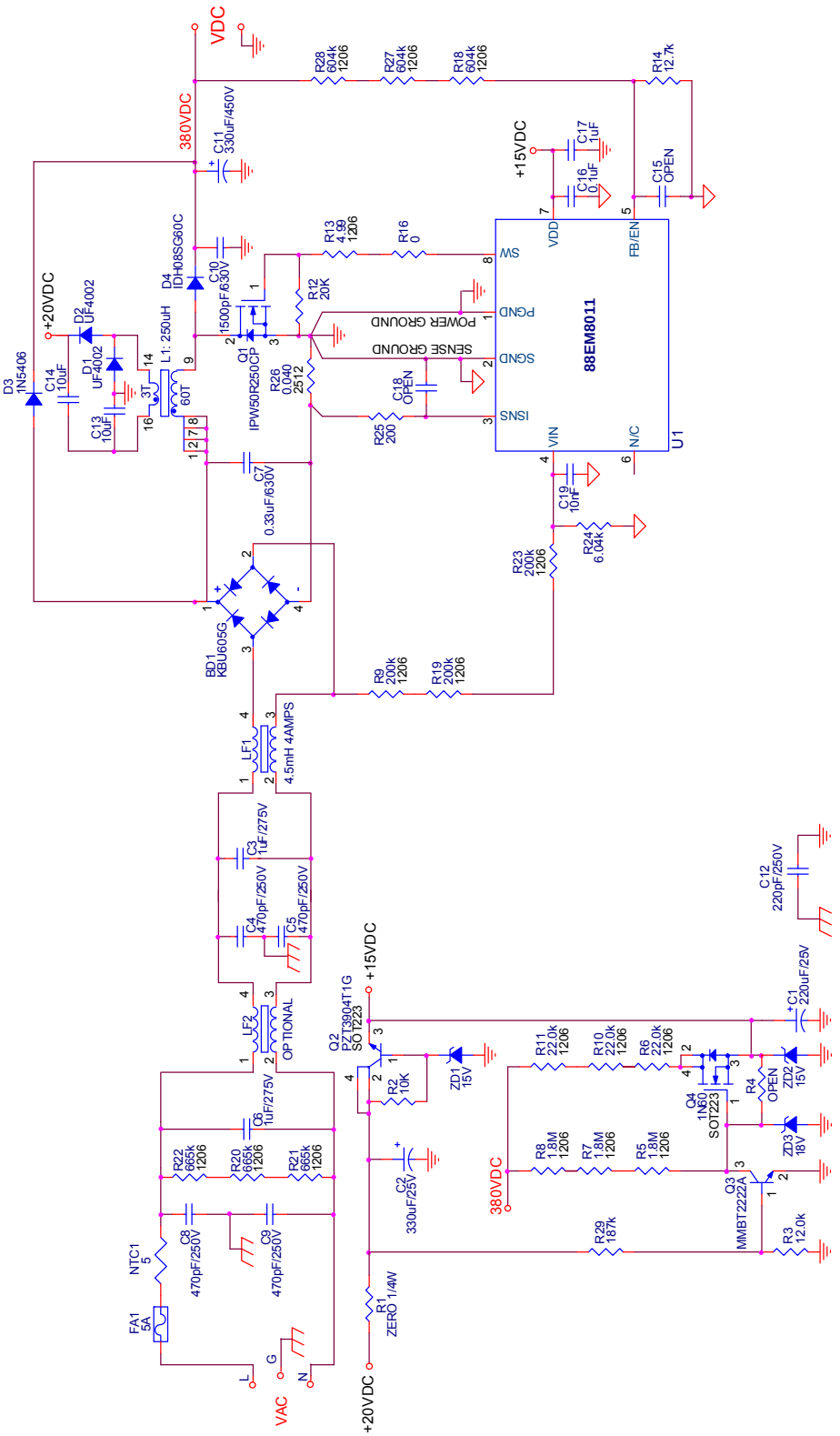
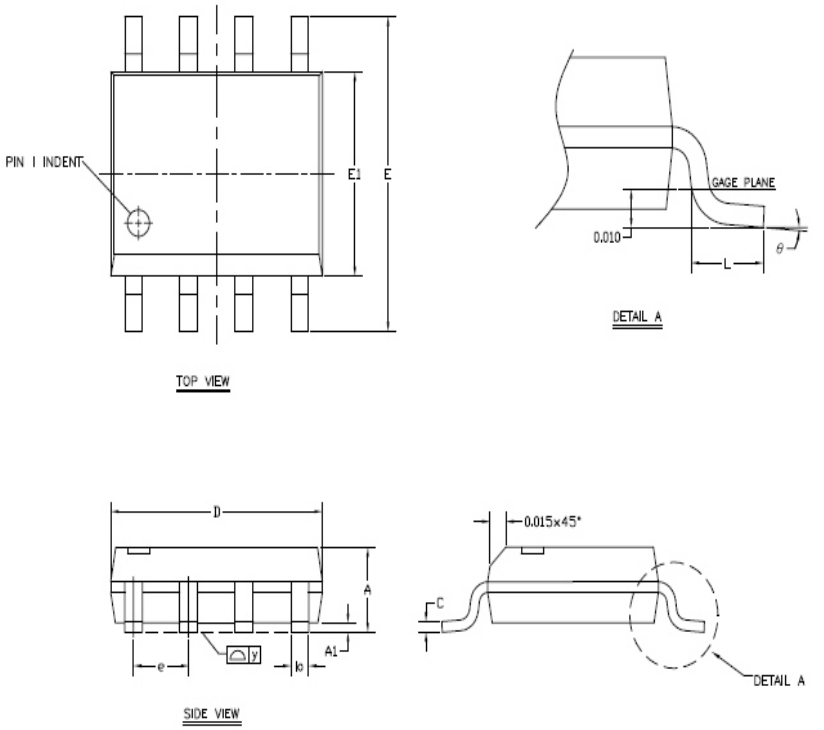


Figure 27: 300W/380V Front-End Boost PFC Schematic



6.1 Mechanical Drawings

Figure 28: 8-Pin SOIC Mechanical Drawing



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.30	—	1.75	0.051	—	0.069
A1	0.10	—	0.25	0.004	—	0.010
b	0.33	0.42	0.51	0.013	0.016	0.020
C	0.18	0.20	0.25	0.007	0.008	0.010
D	4.80	4.85	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27 BSC			0.050 BSC		
L	0.40	—	1.27	0.016	—	0.050
y	—	—	0.10	—	—	0.004
θ	0°	—	8°	0°	—	8°

NOTE :
1. CONTROLLING DIMENSION : INCH
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT NOT EXCEED 0.006"[0.15mm] PER END.
3. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.003"[0.08mm] TOTAL IN EXCEED OF THE "b" IMENSION AT MAXIMUM MATERIAL CONDITION.

Notes:

- All dimensions in mm.
- See Section 7, Part Order Numbering/Package Marking, on page 39 for package marking and pin 1 location.

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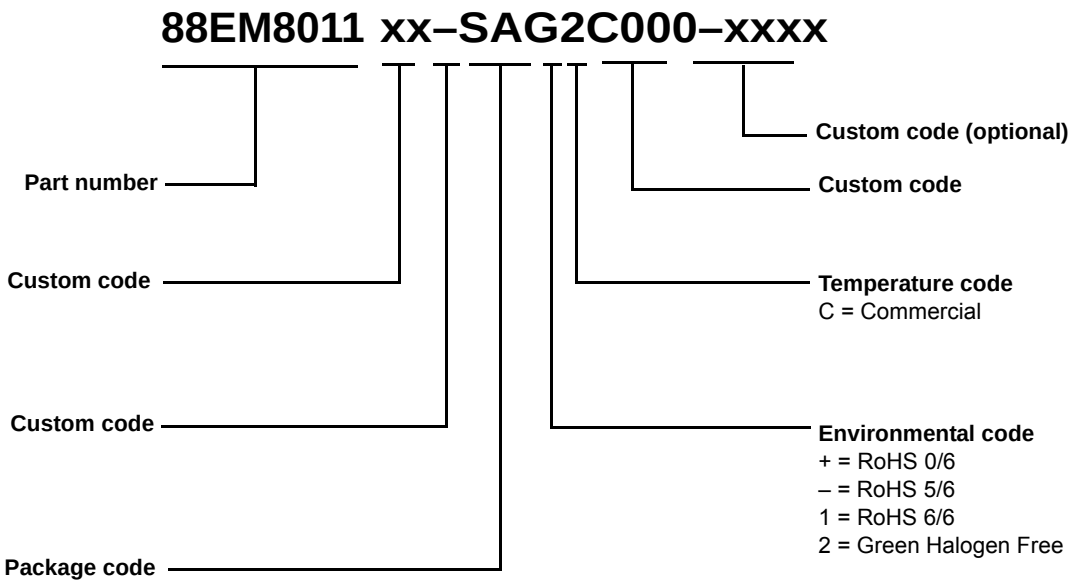
7 Part Order Numbering/Package Marking

7.1 Part Order Numbering

Figure 29 shows the part order numbering scheme. For complete ordering information, contact your Marvell FAE or sales representative.

Figure 29: 88EM8010/88EM8011 Sample Ordering Part Number



The standard ordering part number for the respective solution is shown in Table 8.

Table 8: 88EM8010/88EM8011 Part Order Options[1]

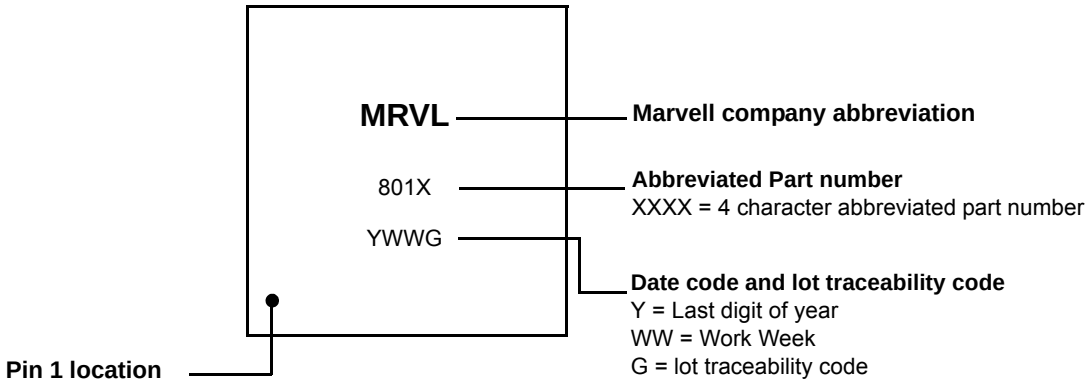
Package Type	Part Order Number
8-Pin SOIC	88EM8010xx-SAG2C000-xxxx
8-Pin SOIC	88EM8010xx-SAG2C000-T (Tape and Reel)
8-Pin SOIC	88EM8011xx-SAG2C000-xxxx
8-Pin SOIC	88EM8011xx-SAG2C000-T (Tape and Reel)

1. Please note that the 88EM8010 device is 60kHz and the 88EM8011 device is 120kHz.

7.2 Package Markings

Figure 30 shows a sample package marking and pin 1 location.

Figure 30: Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings are approximate.

G Revision History

Table 9: Revision History

Document Type	Document Revision
88EM8010/88EM8011 (Document = Rev. B)	
	■ Break-out 8010 (60kHz) and 8011 (120kHz) ■ Edits to Signals - Pin Descriptions ■ EC Table edits - change in values ■ Reworked Applications section

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