	PS-AT65609EHW
ATMEL ®	Revision A

MICROCIRCUIT, DIGITAL, MEMORY,

8K x 8-Bit, 5V Very Low Power CMOS SRAM,

MONOLITHIC SILICON

Revision	Written by	Approved by	Date
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DOCUMENTATION CHANGE NOTICE

Date	Revision	Change Description
06/11/2009	A	First release

SUMMARY

FIGURES

TABLES

1 GENERAL

1.1 Scope

This specification details the ratings, physical and electrical characteristics, tests and inspection data of the 8K x 8-Bit SRAM named AT65609EHW. It also defines the specific requirement for space and military applications with high reliability.

1.2 Identification

Part number	Description	Access Time	Case	Level
AT65609EHW-CI40MQ	8K x 8-Bit SRAM	40 ns	28-lead DIL side-brazed 600 Mils	Mil Level B
AT65609EHW-CI40SV	8K x 8-Bit SRAM	40 ns	28-lead DIL side-brazed 600 Mils	Space Level B
AT65609EHW-CI40SR	8K x 8-Bit SRAM	40 ns	28-lead DIL side-brazed 600 Mils	Space Level B RHA

1.3 Absolute maximum ratings

Supply voltage range (V_{CC})... -0.5V to 7.0V DC[*]
DC Input voltage range (V_{IN})... GND-0.3V to V_{CC} + 0.3V[*]
DC Output voltage range (V_{OUT}) .... GND-0.3V to V_{CC} + 0.3V[*]
Power dissipation (Pd) .... 0,6 W
Storage temperature.. -65°C to 150°C[*]
Maximum junction temperature (T_J).................................... 175°C
Thermal resistance junction to case (Θjc) : . ... 7°C/W
Lead temperature (soldering @ 1/16 in, 10 s) .... 300°C

NOTE [*] : Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. **Exposure between recommended DC operating and absolute maximum rating conditions for extended periods may affect device reliability.**

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})... 4.5V DC to 5.5V DC
Ambient operating temperature (T_A) .... -55°C to 125°C
Storage temperature... 30°C, 20 to 65% RH, dust free, original packing

1.5 Radiation features

Tested up to a Total Dose of .... 300 krads (Si)
(according to MIL STD 883 Method 1019)

No Single Event Latch-up below a LET Threshold of .... 80 MeV/mg/cm^2 @ 125°C

1.6 Handling precautions

These components are susceptible to be damaged by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacturing, testing, shipment and any handling (MIL STD 883 Method 3015.3)

ESD (HBM) .... > 4000 V
ESD (CDM) .... > 1000 V

2 APPLICABLE DOCUMENTS

MIL-PRF-38535 .... Integrated Circuits, Manufacturing, General Specification for.
MIL-STD-883 .... Test Method Standard Microcircuits.
ASTM Standard F1192-95 .... Standard guide for the measurement of single event
phenomena from heavy ion irradiation of semiconductor
devices
JEDEC Standard EIA/JESD78 .... IC latch-up test
ATMEL Aerospace Products Quality Flows

In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence.

3 REQUIREMENTS

3.1 Design, construction, and physical dimensions.

The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.1.1 Timing waveforms

The timing waveforms shall be as specified in Timing waveforms section page 19.

3.1.2 Package type

The package shall be a DIL side-brazed 600 Mils, 28 leads as specified in Package drawing section page 24. The case shall be hermetically sealed and have a ceramic body. The leads shall be brazed.

3.1.3 Terminal connections

The terminal connections shall be as specified in Terminal connections section page25.

3.1.4 Block diagram

The block diagram and the truth table shall be as specified in Block diagram and truth table section page 26.

3.2 Marking

Each component shall be marked in respect of:
(a) Lead Identification
(b) Component Number
(c) Traceability Information
(d) Manufacturer's Component Number

3.2.1 Lead Identification

An index shall be located at the top of the package in the position defined in Package drawing section page 24.

3.2.2 Component Number

Each component shall bear the component number which shall be constituted and marked as follows :

AT65609EHW – CI 40 SV

Product identification
Package (CI = 28-lead DIL side-brazed)
Speed (40 = 40 ns)
Level (MQ=Military Level B, SV=Space Level B, SR=Space Level B RHA)
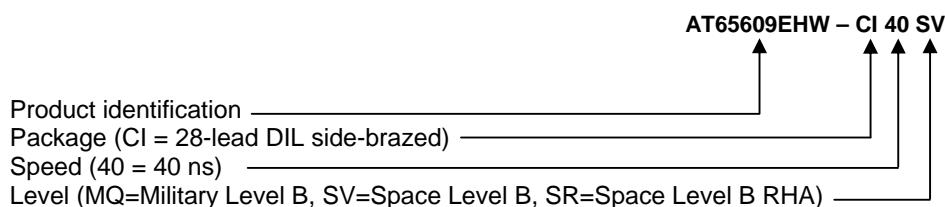
3.2.3 Traceability Information

Each component shall be marked in respect of traceability information : lot number and date code.

3.3 Electrical characteristics

The parameters to be measured with respect of electrical characteristics are scheduled in Electrical and timing characteristics section page 9. The measurements shall be performed at T_{amb}=22 ± 3°C, T_{high}=125 (+0/-5)°C and T_{low} = -55 (+5/-0)°C respectively.

3.4 Burn-in test

3.4.1 Electrical circuit

Circuit for use in performing the power burn-in is shown in Power burn-in and operating life test section page 27, in accordance with the intent specified in test method 1015 of MIL-STD-883.

3.4.2 Parameters drift value

For space level, the parameter drift values applicable to burn-in are specified in Parameter drift values section page 18. Unless otherwise stated, measurements shall be performed at +22 +/- 3°C.
The parameter drift values (Δ), applicable to the parameters scheduled, shall not be exceeded.
In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Electrical and timing characteristics section page 9 shall not be exceeded.
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3.5 Environmental and Endurance Tests

3.5.1 Electrical Circuit for Operating Life Test

The circuit for operating life testing shall be as specified for power burn in Power burn-in and operating life test section page 27.

3.5.2 Electrical Measurements at Completion of Environmental and endurance tests

The parameters to be measured are scheduled in Electrical and timing characteristics section page 9.
Unless otherwise stated, the measurements shall be performed at t_{amb} = 22 +/-3°C.

3.5.3 Conditions for Operating Life Test

The conditions for operating life testing shall be the same as those specified for power burn in.

3.6 Total dose irradiation testing

3.6.1 Bias Conditions

Continuous bias shall be applied during irradiation testing as shown in Total dose radiation test. section page 29.

3.6.2 Electrical Measurements

The parameters to be measured prior to, during and on completion of irradiation texture are scheduled in Electrical and timing characteristics section page 9.

4 QUALITY ASSURANCE PROVISIONS

4.1 Wafer lot validation

Compliant with ATMEL Quality Management System.
For space level, Wafer Lot is accepted by a SEM performed according to AEQC0016 (AEQC0016 referred to MIL-Std-883 method 2018 and 21400 ESCC specification).

4.2   Sampling and inspection.

Sampling and inspection procedures shall be in accordance with MIL-PRF-38535.

4.3   Screening.

Screening equivalent to MIL-PRF-38535. Screening shall be conducted on all devices prior to qualification and technology conformance inspection

• The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in accordance with MIL-PRF-38535.

• Additional screening for space application devices shall be as specified in MIL-PRF-38535, appendix B.

4.4   Quality conformance inspection

Qualification inspection for high reliability and space level devices shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections.

4.4.1   Group A inspection.

• Tests shall be as specified in Electrical and timing characteristics section page 9.
• Subgroups 5 and 6 of table I of method 5005 of MIL STD 883 shall be omitted.
• Subgroups 7 and 8 of table I of method 5005 of MIL STD 883 shall include verifying the functionality of the device.
• O/V (latch up) tests shall be measured only for the initial qualification and after any process or design changes which may affect the performance of the device.
• Capacitance measurement shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is five devices with no failure, and all input and output terminals tested.

4.4.2   Group C inspection.

The group C inspection end-point electrical parameters shall be as specified in in Electrical and timing characteristics section page 9.

4.4.3   Group D inspection.

The group D inspection end-point electrical parameters shall be as specified in Electrical and timing characteristics section page 9.

4.5   Delta measurements

Delta measurements, as specified in Parameter drift values section page 18, shall be made and recorded before and after the required burn-in screens to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in Parameter drift values section page 18. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7 and 9.

5   PACKAGING

5.1   Packaging requirements

The requirements for packaging shall be in accordance with MIL-PRF-38535.

6 ANNEXES

6.1 Electrical and timing characteristics

TABLE 1 - Electrical performances characteristics.

Test	Symbol	Test method Mil-Std-883	Conditions -55°C ≤ T_C ≤ +125°C +4.5 V ≤ Vcc ≤ +5.5 V unless otherwise specified	Limits		Unit
				Min	Max	
Functional test 1 Nominal inputs	-	3014	Verify truth table Note 1	-	-	-
Functional test 2 Worst case inputs	-	3014	Verify truth table Note 1	-	-	-
Functional test 3 Worst case outputs	-	3014	Verify truth table Note 1	-	-	-
Functionnal test 4 Nominal inputs	-	3014	Verify truth table Note 1	-	-	-
Input clamp voltage to Vss	VIC	3008	Iin = -100 µA Vcc open, Vss=0	-2	-0.2	V
Low level input current	IIL	3009	Vcc=5.5V Vin=0V	-10	-	µA
High level input current	IIH	3010	Vcc=5.5V Vin=5.5V	-	10	µA
High impedance output leakage current Third state 1, low level	IOZL1		Vin($\overline{CS1}$) = 4.5V Vin($\overline{WE}$, $\overline{OE}$) = 4.5V Vin(CE) = 0V Vcc=5.5V Vout=0V	-10	-	µA
High impedance output leakage current Third state 2, low level	IOZL2	-	Vin($\overline{CS1}$) = 0V Vin($\overline{WE}$, $\overline{OE}$) = 4.5V Vin(CE) = 4.5V Vcc=5.5V Vout=0V	-10	-	µA
High impedance output leakage current Third state 1, high level	IOZH1	-	Vin($\overline{CS1}$) = 4.5V Vin($\overline{WE}$, $\overline{OE}$) = 4.5V Vin(CE) = 0V Vcc=5.5V Vout=5.5V	-	10	µA
High impedance output leakage current Third state 2, high level	IOZH2	-	Vin($\overline{CS1}$) = 0V Vin($\overline{WE}$, $\overline{OE}$) =4.5V Vin(CE) = 4.5V Vcc=5.5V Vout=5.5V	-	10	µA
Low level output voltage	VOL	3007	IOL=8mA Vcc=4.5V Note 2		0.4	V
High level output voltage	VOH	3006	IOH=-4mA Vcc=4.5V Note 3	2.4		V
Standby Supply Current	ICCSB	3005	$\overline{CS1}$> VIH or CE< VIL and $\overline{CS1}$< VIL		5	mA
Standby Supply Current	ICCSB1	3005	$\overline{CS1}$> Vcc-0.3V or CE<GND+0.3V and $\overline{CS1}$< 0.2V Note 4		3	mA

Test	Symbol	Test method Mil-Std-883	Conditions -55°C ≤ T_C ≤ +125°C +4.5 V ≤ Vcc ≤ +5.5 V unless otherwise specified	Limits		Unit
				Min	Max	
Dynamic Operating Current	ICCOP	3005	F=1/TAVAV, Iout=0 mA, $\overline{WE} = \overline{OE}$ =Vcc, Vin = GND or Vcc, Vcc max, $\overline{CS1}$ = VIL, CE= VIH, Pattern = ICCACT		80	mA
Data Retention Current	ICCDR1	3005	$\overline{CS1}$ = Vcc or CE = $\overline{CS1}$ = GND, Vin = GND/Vcc, Vcc = 2V Note 4		1.5	mA
Vcc for data retention	VCCDR	-	Note 5	2.0		V
Operation Recovery Time	TR	-		TAVAV		ns
Chip deselect to data retention	TCDR	-	Note 5	0.0		ns
Input capacitance	Cin	3012	Vin = 0 V T_C = 25°C f_{IN} = 1.0 MHz Note 9		8	pF
Output capacitance	Cout	3012	Vout = 0 V T_C = 25°C f_{IN} = 1.0 MHz Note 9		8	pF

TABLE 2 - Write Cycle Timing.

Symbol	Test	Test method Mil-Std-883	Conditions -55°C ≤ T_C ≤ +125°C +4.5 V ≤ Vcc ≤ +5.5 V unless otherwise specified	Limits		Unit
				Min	Max	
T_{AVAW}	Write cycle time	3003	Vcc = 4.5V & 5.5V Notes 1,6	40		ns
T_{AVWL}	Address set-up time	3003	Vcc = 4.5V & 5.5V Notes 1,6	0		ns
T_{AVWH}	Address valid to end of write	3003	Vcc = 4.5V Notes 1,6	35		ns
T_{DVWH}	Data set-up time	3003	Vcc = 4.5V Notes 1,7	22		ns
T_{E1LWH}	$\overline{CS1}$ low to write end	3003	Vcc = 4.5V Notes 1,6	35		ns
T_{E2HWH}	CE high to write end	3003	Vcc = 4.5V Notes 1,6	35		ns
T_{WLQZ}	Write low to high Z	3003	Vcc = 4.5V & 5.5V Note 8		17	ns
T_{WLWH}	Write pulse width	3003	Vcc = 4.5V Notes 1,7	35		ns
T_{WHAX}	Address hold from to end of write	3003	Vcc = 4.5V & 5.5V Notes 1,6	3		ns
T_{WHDX}	Data hold time	3003	Vcc = 4.5V & 5.5V Notes 1,7	0		ns
T_{WHQX}	Write high to low Z	3003	Vcc = 4.5V & 5.5V Note 8	0		ns

TABLE 3 - Read Cycle Timing.

Symbol	Test	Test method Mil-Std-883	Conditions -55°C ≤ T_C ≤ +125°C +4.5 V ≤ Vcc ≤ +5.5 V unless otherwise specified	Limits		Unit
				Min	Max	
T_{AVAV}	Read cycle time	3003	Vcc = 4.5V & 5.5V Notes 1,6	40		ns
T_{AVQV}	Address access time	3003	Vcc = 4.5V & 5.5V Notes 1,7		40	ns
T_{AVQX}	Address valid to low Z	3003	Vcc = 5.5V Notes 1,6	3		
T_{E1LQV}	Chip-select1 access time	3003	Vcc = 4.5V Notes 1,7		40	ns
T_{E1LQX}	$\overline{CS1}$ low to low Z	3003	Vcc = 4.5V & 5.5V Note 8	3		ns
T_{E1HQZ}	$\overline{CS1}$ high to high Z	3003	Vcc = 4.5V & 5.5V Note 8		15	ns
T_{E2HQV}	Chip-select2 access time	3003	Vcc = 4.5V Notes 1,7		40	ns
T_{E2HQX}	CE high to low Z	3003	Vcc = 4.5V & 5.5V Note 8	3		ns
T_{E2LQZ}	CE low to high Z	3003	Vcc = 4.5V & 5.5V Note 8		15	ns
T_{GLQV}	Ouput Enable access time	3003	Vcc = 4.5V Notes 1,7		15	ns
T_{GLQX}	$\overline{OE}$ low to low Z	3003	Vcc = 4.5V & 5.5V Note 8	0		ns
T_{GHQZ}	$\overline{OE}$ high to high Z	3003	Vcc = 4.5V & 5.5V Note 8		10	ns

NOTES

1) Functional go-no-go test with the following test sequences :

FUNCTIONAL TEST 1

Pattern	Timing (ns) (a,c)	VCC (V)	VSS (V)	VIL (V)	VIH (V)	IOL (mA)	IOH (mA)	Vout comp (V)
March	105	4.5-5.5	0	0	3	0.5	-0.5	1.5
Checkerboard	105	4.5-5.5	0	0	3	0.5	-0.5	1.5
Imag	105	4.5-5.5	0	0	3	0.5	-0.5	1.5
Genbl	105	4.5	0	0	3	0.5	-0.5	1.5

FUNCTIONAL TEST 2

Pattern	Timing (ns) (a,c)	VCC (V)	VSS (V)	VIL (V)	VIH (V)	IOL (mA)	IOH (mA)	Vout comp (V)
March	105	6	0	-0.3	6.3	0.5	-0.5	1.5
March	105	4	0	-0.3	4.3	0.5	-0.5	1.5
March	105	5.5	0	0	2.2	0.5	-0.5	1.5
March	105	4.5	0	0.8	0	0.5	-0.5	1.5

FUNCTIONAL TEST 3

Pattern	Timing (ns) (a,c)	VCC (V)	VSS (V)	VIL (V)	VIH (V)	IOL (mA)	IOH (mA)	Vout comp (V)
March	105	4.5	0	0	3	8	-4	(b)

FUNCTIONAL TEST 4

Pattern	Timing (ns) (a,c)	VCC (V)	VSS (V)	VIL (V)	VIH (V)	IOL (mA)	IOH (mA)	Vout comp (V)
March	100	4.5 and 5.5V	0	0	3	0.5	-0.5	1.5
Comarch	100	4.5 and 5.5V	0	0	3	0.5	-0.5	1.5
Imag	100	4.5 and 5.5V	0	0	3	0.5	-0.5	1.5
Checkerboard	100	4.5 and 5.5V	0	0	3	0.5	-0.5	1.5

a) a write cycle is followed by a read cycle. The time between start of write and start of read per the truth table is the specified "timing" parameter. $t_r = t_f = 5$ ns maximum

b) 0.4V for low output level, 2.4V for high output level

c) Ouput load 1 TTL gate equivalent + $C_L < 30$ pF

2) Select address inputs to produce a low level at the pin under test.

3) Select address inputs to produce a high level at the pin under test.

4) Measurements are performed with the memory loaded with a background of zeros, then with a background of ones, for all inputs high, then low. Only the worst case is recorded.

5) Data retention procedure :

   a) Write memory with CHECKERBOARD pattern
   b) Power down to VCC = 2V for 250ms
   c) Restore VCC to 4.5V, wait tr, read memory and compare with original pattern

   d) Repeat the procedure with $\overline{CHECKERBOARD}$ pattern

6) Parameter tested go-no-go during functional test 4.

7) Parameter measured during functional test 4 using pattern March at 4.5V and 5.5V.

8) Guaranteed with output loading 5pF but not tested. Characterized at initial design and after major process changes.

9) Guaranteed but not tested

10) The following pattern definitions apply :

   a) ICCACT
      Write loop pattern between Nmin and Nmax

b) MARCH

```
┌─────────────────────────────────┐
│ Memory size   8192              │
│ Data          1010 1010         │
│ Nmin          0                 │
│ Nmax          8191              │
└─────────────────────────────────┘
              │
              ▼
   ┌─────────────────────────┐
   │  Write background data  │
   └─────────────────────────┘
              │
              ▼
        ┌───────────┐
        │   N = 0   │
        └───────────┘
              │
  ┌───────────┤
  │           ▼
  │  ┌─────────────────────┐
  │  │  Read and compare   │
  │  └─────────────────────┘
  │           │
  │           ▼
  │     ┌───────────────┐
  │     │  Write datab  │
  │     └───────────────┘
  │           │
  │           ▼
  │     ┌───────────────┐
  │     │  Increment N  │
  │     └───────────────┘
  │           │
  │   N       ▼
  └──────◇ N > Nmax ◇
              │
            YE│
              ▼
        ┌─────────────┐
        │  N = Nmax   │
        └─────────────┘
              │
  ┌───────────┤
  │           ▼
  │  ┌─────────────────────┐
  │  │  Read and compare   │
  │  └─────────────────────┘
  │           │
  │           ▼
  │     ┌───────────────┐
  │     │  Write datab  │
  │     └───────────────┘
  │           │
  │           ▼
  │     ┌───────────────┐
  │     │  Decrement N  │
  │     └───────────────┘
  │           │
  │   N       ▼
  └──────◇ N < 0 ◇
              │
            YE│
              ▼
        ┌─────────┐
        │   END   │
        └─────────┘
```

c) Checkerboard

```
┌─────────────────────────────┐
│ Memory size     8192         │
│ Data            1010 1010    │
│ Nmin            0            │
│ Nmax            8191         │
└─────────────────────────────┘
              │
              ▼
┌─────────────────────────────┐
│ Write data or datab          │
│ if Xo = Yo in Nmin           │
└─────────────────────────────┘
              │
              ▼
┌─────────────────────────────┐
│ Write data or datab          │
│ if Xo = Yo in N+1            │
└─────────────────────────────┘
              │
              ▼
        ◇ N = Nmax ◇  ── NO
              │ YES
              ▼
┌─────────────────────────────┐
│ Read and compare             │
│ Data or datab                │
│ if Xo = Yo in Nmin           │
└─────────────────────────────┘
              │
              ▼
┌─────────────────────────────┐
│ Read and compare             │
│ Data or datab                │
│ If Xo = Yo in N+1           │
└─────────────────────────────┘
              │
              ▼
        ◇ N = Nmax ◇  ── NO
              │ YES
              ▼
         ┌────────┐
         │  END   │
         └────────┘
```

d) Imag

```
Write Background Data ──────────────────────────┐
          │                                      │
          ▼                                      ▼
       N = 0                                  N = Nmax
          │                                      │
          ▼                                      ▼
   Read Cell N Data                        Read Cell N Datab
          │                                      │
          ▼                                      ▼
   Write Cell N Datab                      Write Cell N Data
          │                                      │
          ▼                                      ▼
   Write Cell N Data                       Write Cell N Datab
          │                                      │
          ▼                                      ▼
   Write Cell n Datab                      Write Cell N Data
          │                                      │
          ▼                                      ▼
    Increment N                             Decrement N
          │                                      │
          ▼                                      ▼
   NO ◄ N > Nmax                            N < 0 ► (YES)
          │ YES                                  │ YES
          ▼                                      ▼
   Read Cell N Datab                       Read Cell N Data
          │                                      │
          ▼                                      ▼
   Write Cell N Data                       Write Cell N Datab
          │                                      │
          ▼                                      ▼
   Write Cell N Datab                      Write Cell N Data
          │                                      │
          ▼                                      ▼
    Increment N                             Decrement N
          │                                      │
          ▼                                      ▼
   NO ◄ N > Nmax                            N < 0 ► (YES)
          │ YES                                  │ YES
          └──────────────────────────►         END
```

Memory Size : 8192
Data   : 1010 1010
Nmax   : 8191

e) Comarch
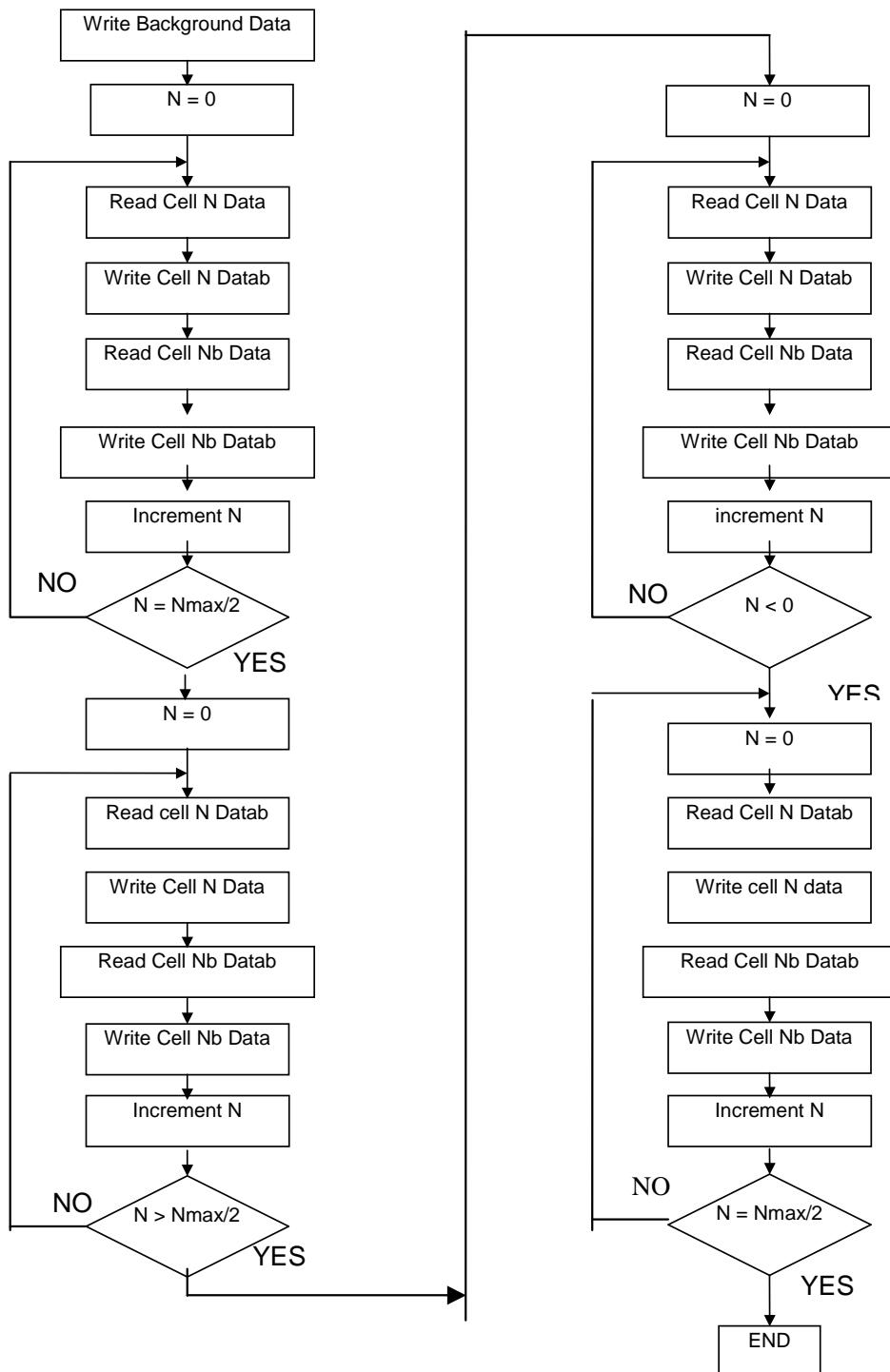
Memory size : 8192
Data : 1010 1010
Nmax : 8191

f) Genbl

Write 0 background
Write 1 background

Read 1 background with $\overline{OE}$ = VIL

Read 1 background with $\overline{OE}$ = VIH (must be fail)

6.2 Parameter drift values

TABLE 4 - Parameter drift values

Test	Symbol	Test method Mil-Std-883	Conditions	Drift limits	Unit
Low level Input current	I_{IL}	As per table 1	As per table 1	1	μA
High level Input current	I_{IH}	As per table 1	As per table 1	1	μA
Output leakage Low current	I_{OZL}	As per table 1	As per table 1	1	μA
Output leakage High current	I_{OZH}	As per table 1	As per table 1	1	μA
Stand-by supply current	I_{CCSb}	As per table 1	As per table 1	0.5	mA
Stand-by supply current	I_{CCSb1}	As per table 1	As per table 1	0.3	mA
Data retention current	I_{ccdr1}	As per table 1	As per table 1	0.15	mA

NOTE: the above parameter shall be recorded before and after burn-in and life test to determine the delta.

6.3 Timing waveforms

6.3.1 AC Test Conditions:

Input Pulse Levels: .... **GND to 3.0 V**

Input Rise/Fall Times: ....**5 ns**

Input Timing Reference Levels: **1.5V**

Output Loading IOL/IOH (see Figure 1a and Figure 1b): **30pF**

6.3.2 AC Test Loads Waveforms

FIGURE 1 - Output loads
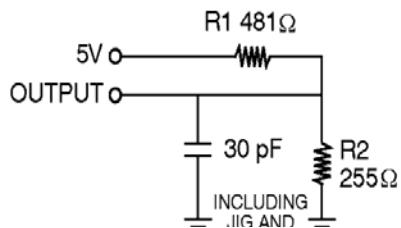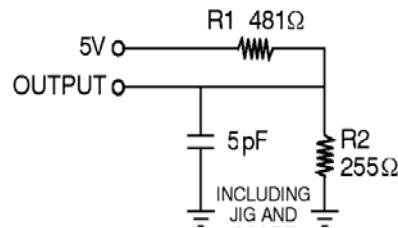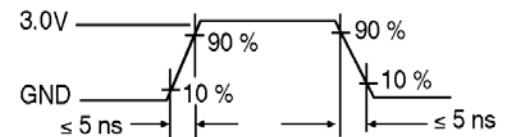
Figure 1a   Figure 1b   Figure 2

Equivalent to : THEVENIN EQUIVALENT
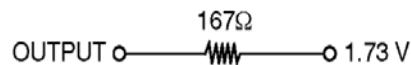
6.3.3 Data Retention Mode

Atmel CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules ensure data retention:

1. During data retention chip select $\overline{CS1}$ must be held high within VCC to VCC -0.2V or, chip select CE must be held down within GND to GND +0.2V.

2. Output Enable ($\overline{OE}$) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.

3. During power up and power-down transitions $\overline{CS1}$ and $\overline{OE}$ must be kept between VCC + 0.3V and 70% of VCC, or with CE between GND and GND -0.3V.

4. The RAM can begin operation > TR ns after VCC reaches the minimum operation voltages (4.5V).

FIGURE 2 - Data retention timing waveform
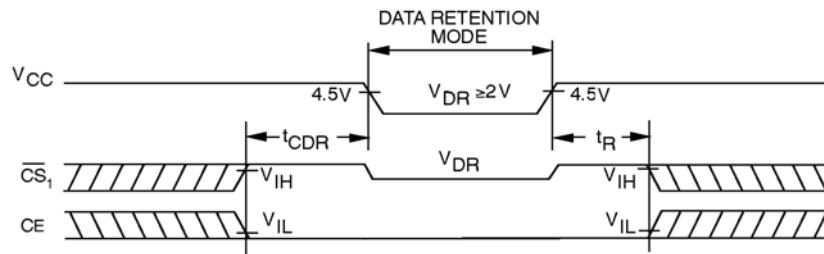
6.3.4 Write cycles

FIGURE 3 - Write cycle timings waveforms

Figure 3a - Write Cycle 1
$\overline{WE}$ controlled, $\overline{OE}$ High During Write
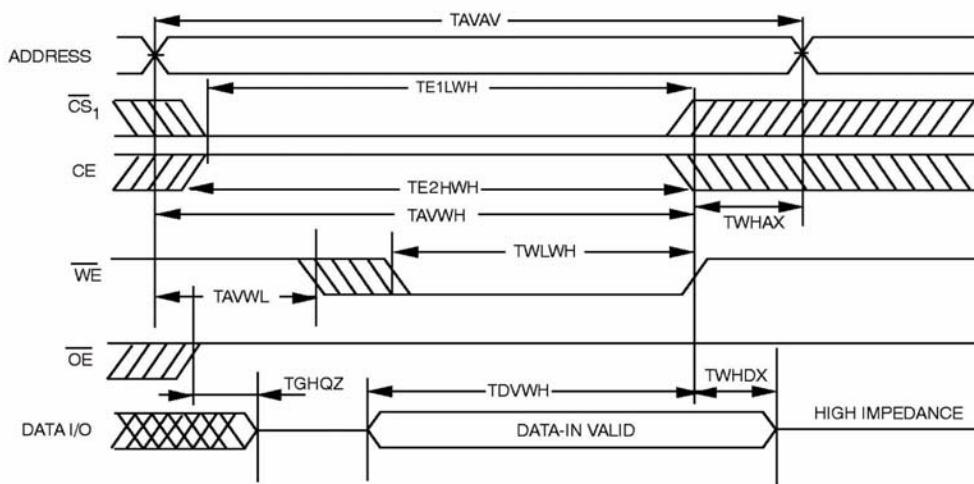
Figure 3b - Write Cycle 2
$\overline{WE}$ controlled, $\overline{OE}$ Low
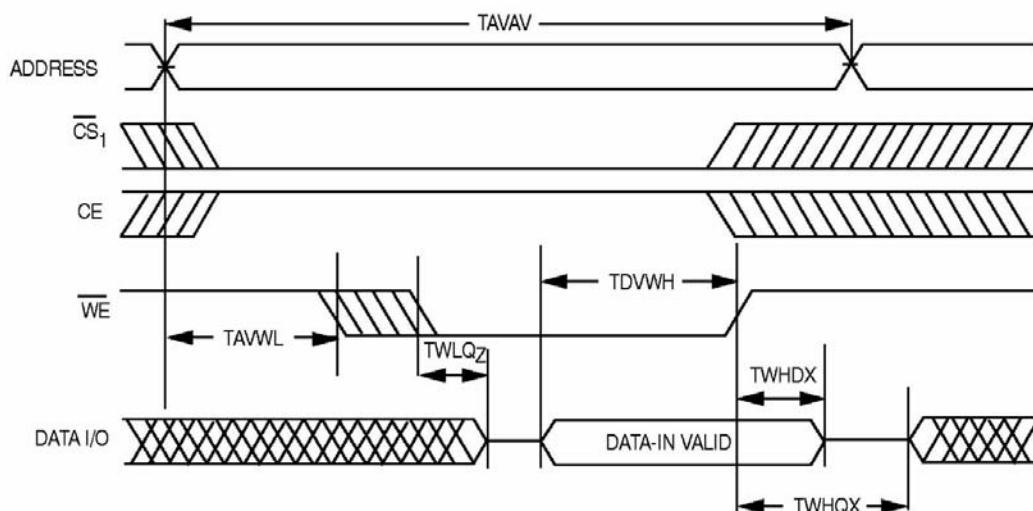
Figure 3c - Write Cycle 3
$\overline{CS1}$ or CE controlled
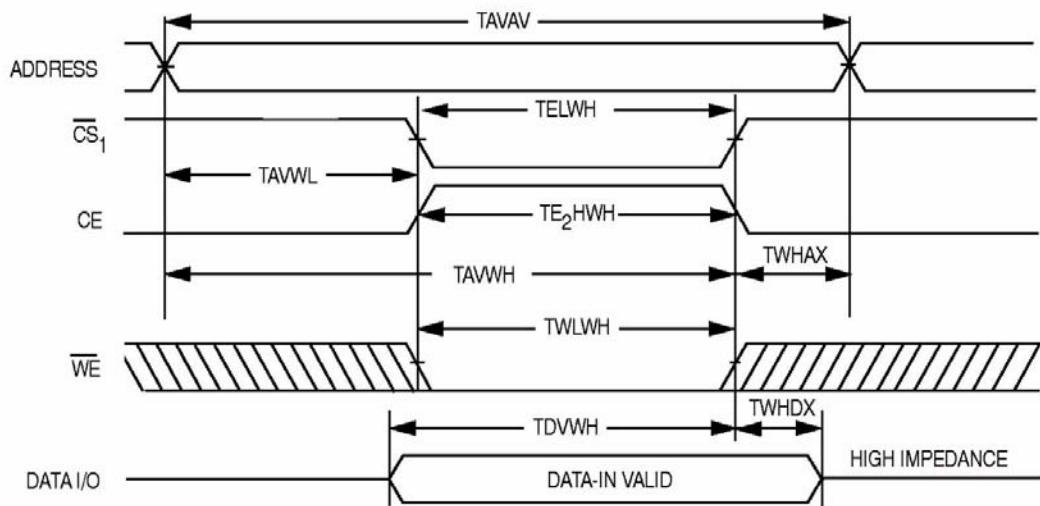
NOTE : The internal write time of the memory is defined by the overlap of $\overline{CS1}$ Low and CE HIGH and $\overline{WE}$ LOW. Both signals must be actived to initiate a write and either signal can terminate a write by going in actived. The data input setup and hold timing should be referenced to the actived edge of the signal that terminates the write. Data out is high impedance if $\overline{OE}$ = V_{IH}.

6.3.5 Read cycles

FIGURE 4 - Read cycle timings waveforms

Figure 4a - Read Cycle 1

Address Controlled ($\overline{CS1}$ = $\overline{OE}$ Low, CE = $\overline{WE}$ High)
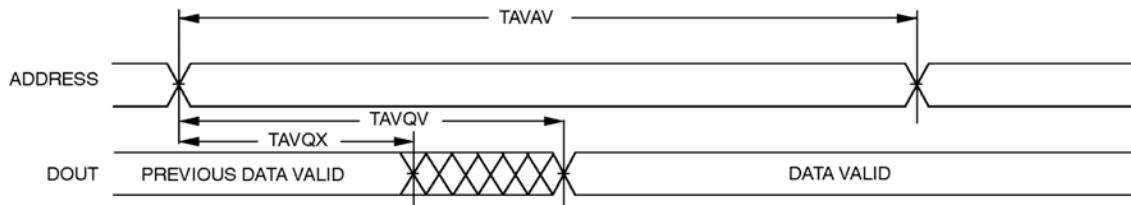
Figure 4b - Read Cycle 2

$\overline{CS1}$ Controlled (CE = $\overline{WE}$ High)
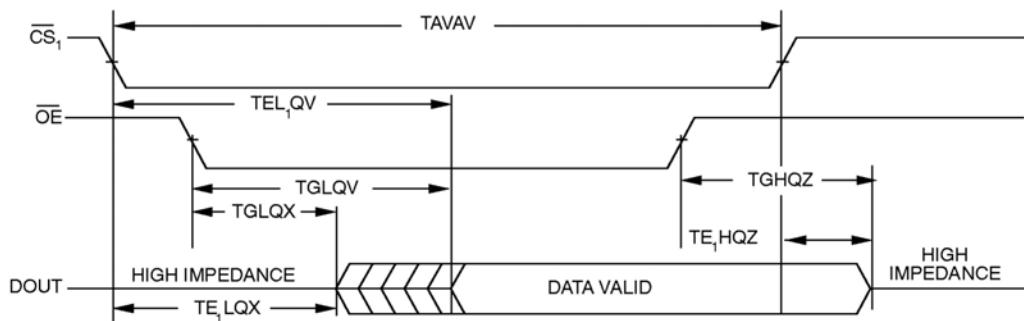
Figure 4c - Read Cycle 3

CE Controlled ($\overline{WE}$ High, $\overline{CS1}$ Low)
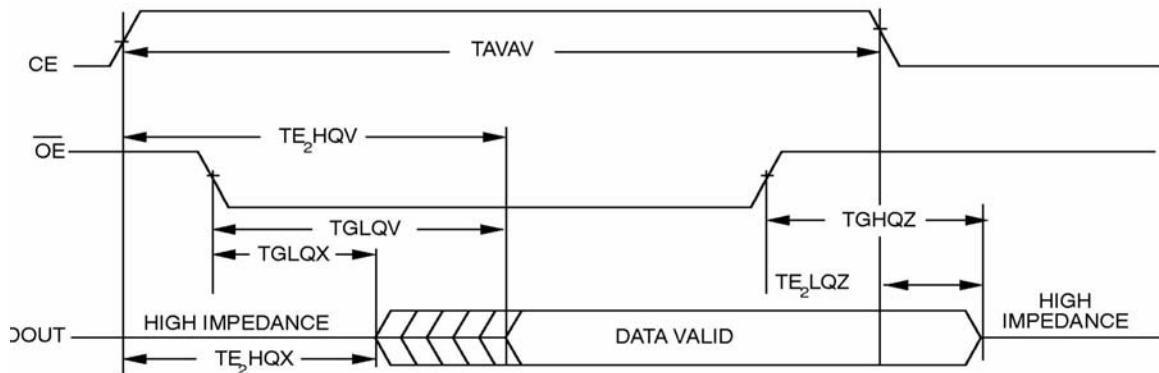
6.4 Case outline

6.4.1 Package drawing

FIGURE 5 - 28 leads DIL side-brazed 600 Mils package
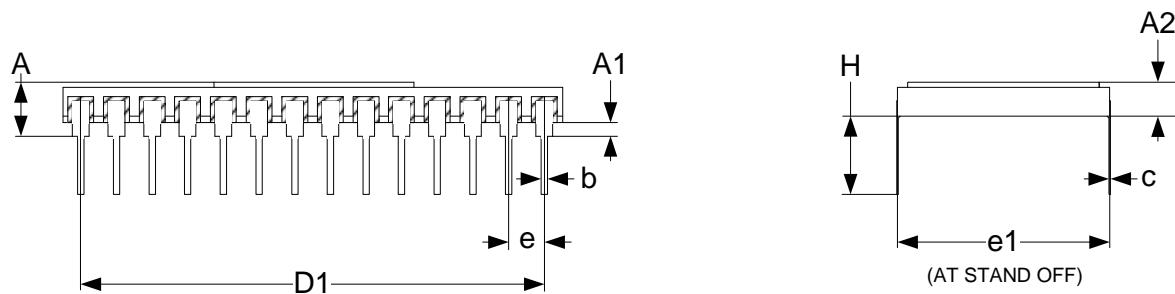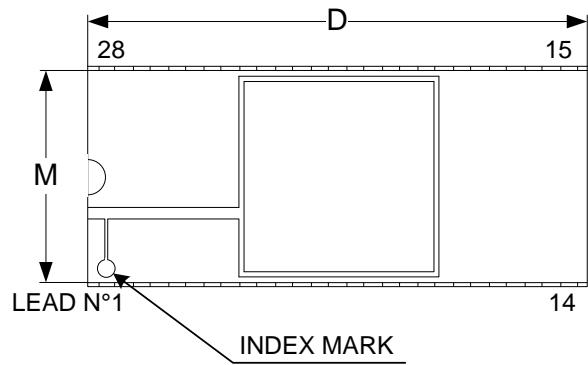
Ref	Millimeters			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	3.73	3.99	4.24	0.147	0.157	0.167
A1	1.02	1.27	1.52	0.040	0.050	0.060
A2	2.47	2.73	2.98	0.0974	0.1074	0.1174
b	0.41	0.46	0.51	0.016	0.018	0.020
c	0.23	0.25	0.30	0.009	0.010	0.012
D	35.20	35.56	35.92	1.386	1.400	1.414
D1	32.89	33.02	33.15	1.295	1.300	1.305
e	2.41	2.54	2.67	0.095	0.100	0.105
e1	14.99	15.24	15.49	0.590	0.600	0.610
H			5.51			0.217
M	14.86	15.11	15.37	0.585	0.595	0.605

6.4.2 Terminal connections

TABLE 5 - Terminal connections

Case outline			
Pin Number	Name	Pin Number	Name
1	NC	15	I/O3
2	A12	16	I/O4
3	A7	17	I/O5
4	A6	18	I/O6
5	A5	19	I/O7
6	A4	20	$\overline{CS1}$
7	A3	21	A10
8	A2	22	$\overline{OE}$
9	A1	23	A11
10	A0	24	A9
11	I/O0	25	A8
12	I/O1	26	CE
13	I/O2	27	$\overline{WE}$
14	GND	28	V_{CC}

Name	Description
A0 - A12	Addresses
CE	Chip Enable
$\overline{CS1}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 – I/O7	Data Inputs/Outputs
NC	Not connected
V_{CC}	Power
GND	Ground

6.5   Block diagram and truth table

FIGURE 6 - Block diagram
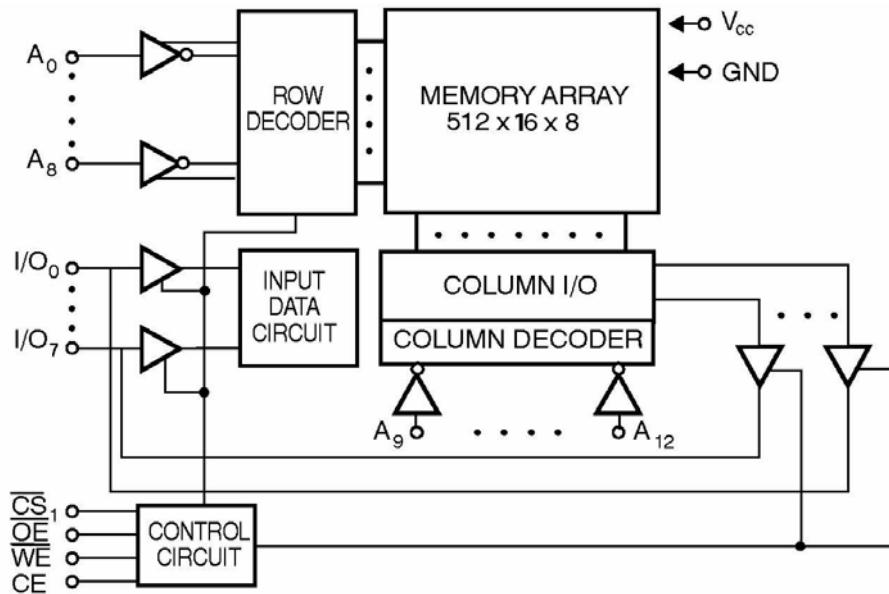
TABLE 6 - Truth table

$\overline{CS1}$	CE	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	X	Z	Deselect / Power-Down
X	L	X	X	Z	Deselect / Power-Down
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	Z	Ouput Disable

Note: L=low, H=high, X=low or high, Z=high impedance

6.6 Power burn-in and operating life test

TABLE 7 - Burn-in and life test conditions

Characteristics	Symbol	Conditions	Unit
Ambient Temperature	Tamb	125 (+0/-5)	°C
Address inputs	Vin	S3 to S15 (note 1)	Vac
Select pins	$\overline{CS1}$	0	V
	CE	Vcc	V
Control inputs	$\overline{OE}$, $\overline{WE}$	S1 and S2 (note 2)	Vac
Inputs/Outputs	Vin	S16 and S17	Vac
Pulse frequency	S3	330 +/- 20%	kHz
Positive Supply Voltage	VCC	5.7V (+0.1 /-0.1)	V
Negative Supply Voltage	GND	0	V

NOTES :

1/ $S_n = \dfrac{1}{2}.S_{n-1}$ for n>=3

2/ Control Input
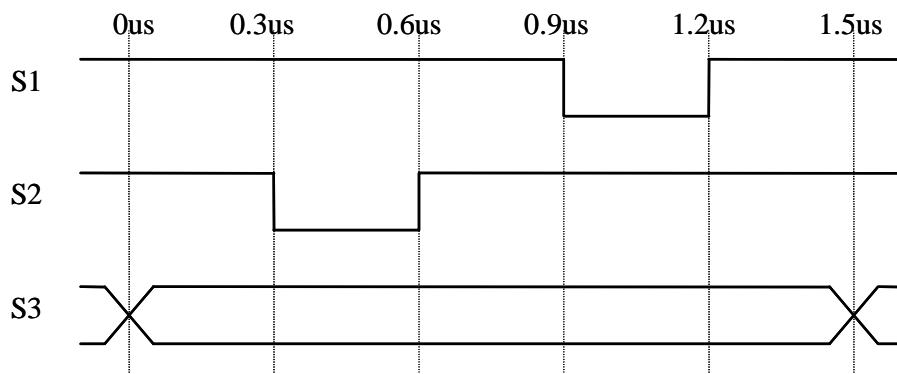
3/ All Inputs and Outputs shall be connected through a serial protection resistor/load of 1 kOhm as follows :

FIGURE 7 - Electrical circuit for burn-in and operating life test

	1 NC	VCC 28	Vcc
S15	2 A12	WE 27	S2
S10	3 A7	CE 26	Vcc
S9	4 A6	A8 25	S11
S8	5 A5	A9 24	S12
S7	6 A4	A11 23	S14
S6	7 A3	OE 22	S1
S5	8 A2	A10 21	S13
S4	9 A1	CS1 20	GND
S3	10 A0	I/O7 19	S17
S16	11 I/O0	I/O6 18	S16
S17	12 I/O1	I/O5 17	S17
S16	13 I/O2	I/O4 16	S16
GND	14 GND	I/O3 15	S17

65609EHW
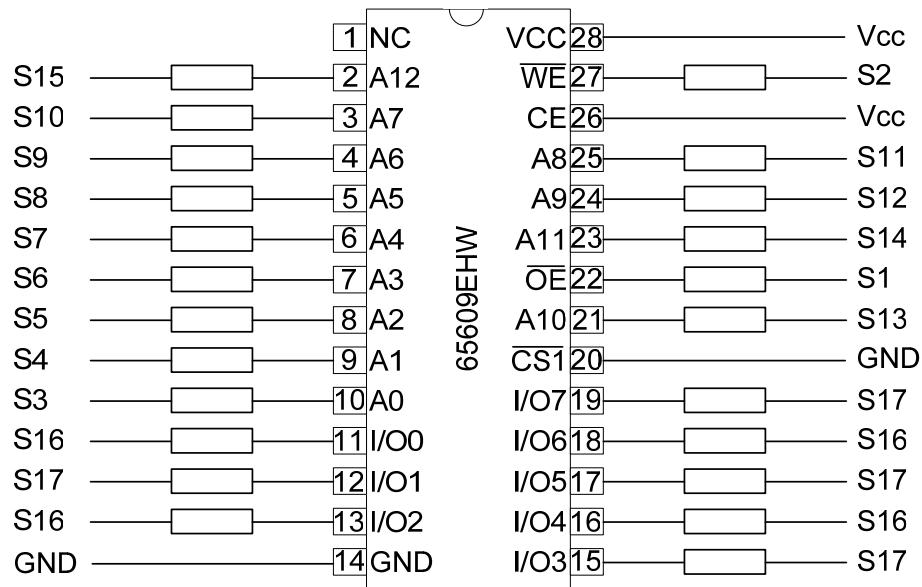
6.7 Total dose radiation test.

FIGURE 8 - Electrical circuit for total dose radiation test.

Continuous bias shall be applied during irradiation testing as specified below, through a serial protection resistor/load of 5.6 kOhm.
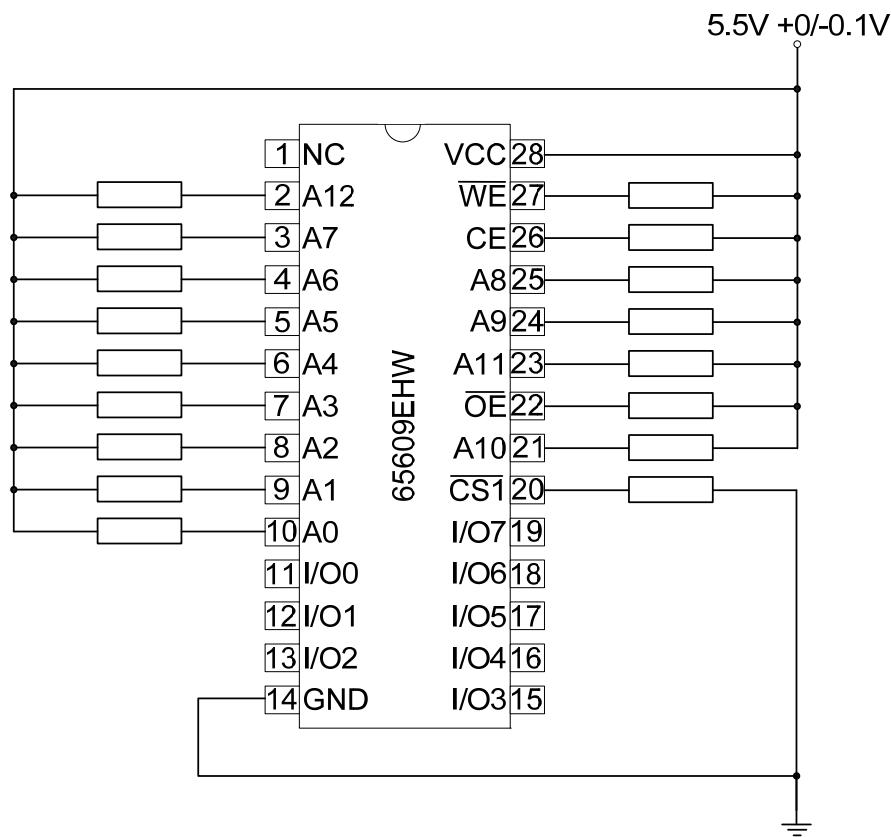
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