2.8-W Stereo Fully Differential Audio Power Amplifier

DESCRIPTION

The EUA4996 is a stereo fully-differential audio amplifier, capable of delivering 2.8W/channel of continuous output power to a 3Ω load with 10% THD+N from a 5V power supply.

The EUA4996 features independent shutdown control for each channel. The feedback resistors are internal, allowing the gain to be set with only two input resistors per channel. High PSRR and fully differential architecture provide increased immunity to noise and RF rectification, and a fast startup time with minimal pop, making the EUA4996 idea for notebook PC, smart phone applications.

FEATURES

- Output Power
  - 2.8W/Ch Into 3Ω at 5V, THD=10% (Typ.)
  - 1.99W/Ch Into 4Ω at 5V, THD=1% (Typ.)
  - 1.27W/Ch Into 8Ω at 5V, THD=1% (Typ.)
- Wide Supply Voltage: 2.5V to 5.5V
- Independent Shutdown Control for Each Channel
- High PSRR : 86dB
- Fast 23ms Startup Time with Minimal POP
- Low 8mA Quiescent Current at 5V Supply and 1μA Shutdown Current
- Thermal Protection
- 4mm × 4mm TQFN-16 Package
- RoHS Compliant and 100% Lead(Pb)-Free

APPLICATIONS

- Notebook PCs
- Smart Phones

Typical Application Circuit

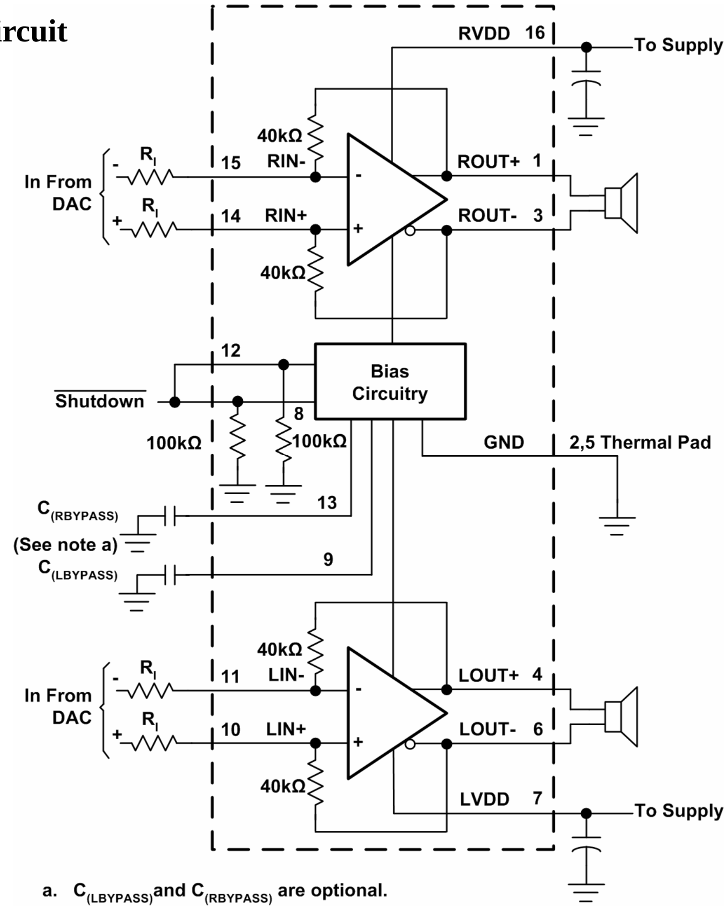
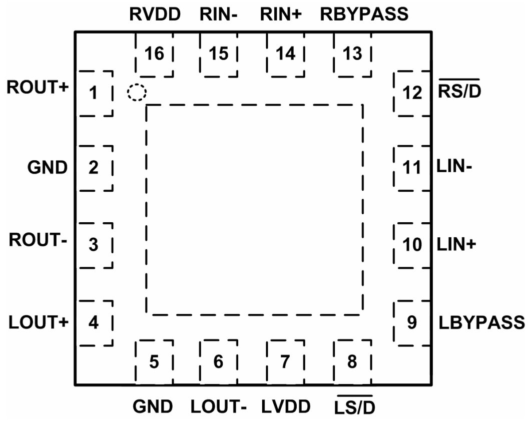


Figure 1.

Pin Configurations

Package Type	Pin Configurations
TQFN-16	

Pin Description

PIN	TQFN-16	I/O	DESCRIPTION
ROUT+	1	O	Right channel positive BTL output
GND	2,5	I	High current ground
ROUT-	3	O	Right channel negative BTL output
LOUT+	4	O	Left channel positive BTL output
LOUT-	6	O	Left channel negative BTL output
LVDD	7	I	Left channel power supply. Must be tied to RVDD for stereo operation.
$\overline{\text{LS/D}}$	8	I	Left channel shutdown terminal (active low logic)
LBYPASS	9	-	Left channel mid-supply voltage. Adding a bypass capacitor improves PSRR
LIN+	10	I	Left channel positive differential input
LIN-	11	I	Left channel negative differential input
$\overline{\text{RS/D}}$	12	-	Right channel shutdown terminal (active low logic)
RBYPASS	13	-	Right channel mid-supply voltage. Adding a bypass capacitor improves PSRR
RIN+	14	I	Right channel positive differential input
RIN-	15	I	Right channel negative differential input
RVDD	16	I	Power supply

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUA4996JIR1	TQFN-16	xxxxx A4996	-40°C to 85°C

EUA4996 □ □ □ □

- Lead Free Code
  1: Lead Free 0: Lead
- Packing
  R: Tape & Reel
- Operating temperature range
  I: Industry Standard
- Package Type
  J: TQFN

Absolute Maximum Ratings

- Supply voltage, V_{DD} -- 6V
- Input voltage, V_I -- -0.3 V to V_{DD} +0.3V
- Storage temperature rang, T_{stg} -- -65°C to 150°C
- Junction Temperature -- 150°C

Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply Voltage, V_{DD}	2.5		5.5	V
High-level input voltage, V_{IH}	1.55			V
Low-level input voltage, V_{IL}			0.5	
Operating free-air temperature, T_A	-40		85	°C

Electrical Characteristics, T_A=25°C

Symbol	Parameter	Conditions		EUA4996 Min	Typ	Max.	Unit
V_{OS}	Output offset voltage (measured differentially)	V_I=0V differential, Gain=1V/V, V_{DD}=5.5V		-9	0.8	9	mV
PSRR	Power supply rejection ratio	V_{DD}=2.5V to 5.5V			-87		dB
V_{IC}	Common mode input range	V_{DD}=2.5V to 5.5V		0.5		V_{DD}-0.8	V
CMRR	Common mode rejection range	V_{DD}=2.5V, V_{IC}=0.5V to 1.7V			-63		dB
		V_{DD}=5.5V, V_{IC}=0.5V to 4.7V			-63		
	Low-output swing	R_L=3Ω, Gain=1V/V V_{IN+}=V_{DD}, V_{IN-}=0V or V_{IN+}=0V, V_{IN-}=V_{DD}	V_{DD}=5.5V		0.55		V
			V_{DD}=3.6V		0.42		
			V_{DD}=2.5V		0.34	0.4	
	High-output swing	R_L=3Ω, Gain=1V/V V_{IN+}=V_{DD}, V_{IN-}=0V or V_{IN-}=V_{DD}, V_{IN+}=0V	V_{DD}=5.5V		4.9		V
			V_{DD}=3.6V		3.1		
			V_{DD}=2.5V	1.9	2.1		
$\|I_{IH}\|$	High-level input current, $\overline{\text{Shutdown}}$	V_{DD}=5.5V, V_I=5.8V			58	100	µA
$\|I_{IL}\|$	Low-level input current, $\overline{\text{Shutdown}}$	V_{DD}=5.5V, V_I=-0.3V			3	100	µA
I_Q	Quiescent current	V_{DD}=2.5V to 5.5V, with load			8		mA
$I_{(SD)}$	Supply current	V($\overline{\text{Shutdown}}$)≤0.5V, V_{DD}=2.5V to 5.5V, R_L= 3Ω			0.08	1	µA
	Gain	R_L= 3Ω		$\frac{38k\Omega}{RI}$	$\frac{40k\Omega}{RI}$	$\frac{42k\Omega}{RI}$	V/V
	Resistance from shutdown to GND				100		kΩ

Operating Characteristics, T_A=25°C, Gain=1V/V

Symbol	Parameter	Conditions			EUA4996 Min	EUA4996 Typ	EUA4996 Max.	Unit
P_O	Output power	THD+N=1%, f=1kHz,R_L=3Ω		V_{DD}=5V		2.25		W
				V_{DD}=3.6V		1.13		
				V_{DD}=2.5V		0.46		
		THD+N=1%, f=1kHz,R_L=4Ω		V_{DD}=5V		1.99		
				V_{DD}=3.6V		1		
				V_{DD}=2.5V		0.42		
		THD+N=1%, f=1kHz,R_L=8Ω		V_{DD}=5V		1.27		
				V_{DD}=3.6V		0.65		
				V_{DD}=2.5V		0.29		
THD+N	Total harmonic distortion plus noise	f=1kHz ,R_L=3Ω	P_O=2W	V_{DD}=5V		0.16		%
			P_O=1W	V_{DD}=3.6V		0.19		
			P_O=300mW	V_{DD}=2.5V		0.08		
		f=1kHz ,R_L=4Ω	P_O=1.8W	V_{DD}=5V		0.09		
			P_O=0.7W	V_{DD}=3.6V		0.06		
			P_O=300mW	V_{DD}=2.5V		0.07		
		f=1kHz ,R_L=8Ω	P_O=1W	V_{DD}=5V		0.04		
			P_O=0.5W	V_{DD}=3.6V		0.04		
			P_O=200mW	V_{DD}=2.5V		0.05		
K_{SVR}	Supply ripple rejection ratio	V_{DD}=3.6V, Inputs ac-grounded with C_i=2µF, $V_{(Ripple)}$=200mVpp		f = 217Hz		-86		dB
				f = 1kHz		-80		
	Crosstalk	V_{DD}=5V, R_L=3Ω, f=1kHz ,P_O=1W				-99		dB
SNR	Signal-to-noise ratio	V_{DD}=5V, P_O=2W,R_L=3Ω,f=1kHz,Gain=1V/V				106		dB
Vn	Output voltage noise	V_{DD}=3.6V, f=20Hz to 20kHz, Gain=1V/V ,Inputs ac-grounded with C_I=0.22µF		No weighting		12		µV_{RMS}
				A weighting		8.7		
CMRR	Common mode rejection ratio	V_{DD}=3.6V,V_{IC}=200mV_{PP}		f=217Hz		-60		dB
Z_I	Input impedance				38	40	42	kΩ
	Start-up time from shutdown	V_{DD}=3.6V, C_{BYPASS}=0.1µF				23		ms

Note: The thermal performance of the TQFN package when used with the exposed- DAP connected to a thermal plane is sufficient for driving 4Ω or 3Ω loads.

Typical Operating Characteristics

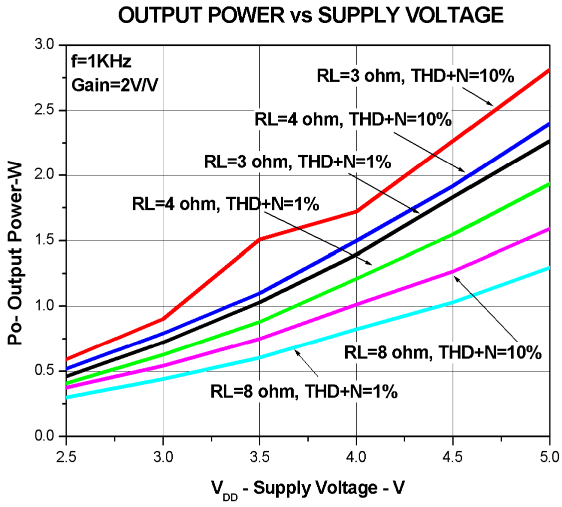


Figure 2

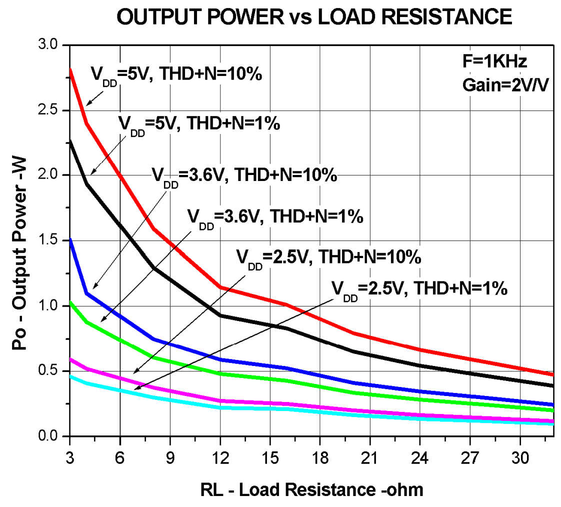


Figure 3

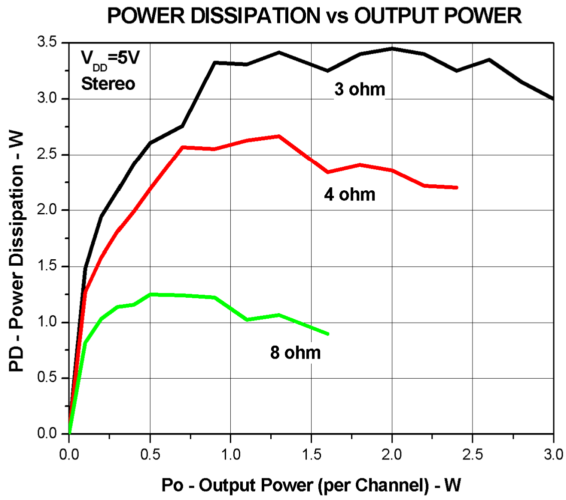
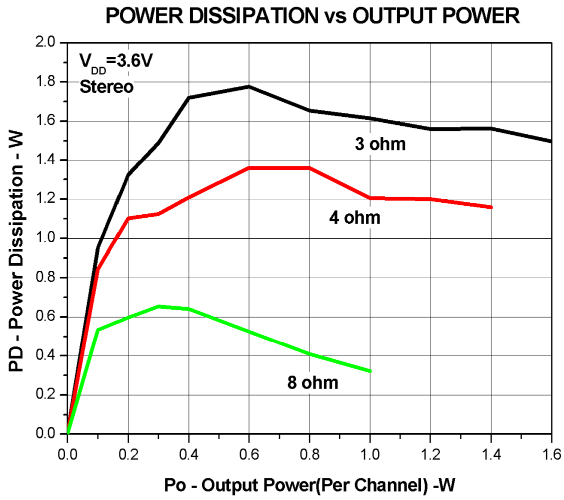


Figure 4



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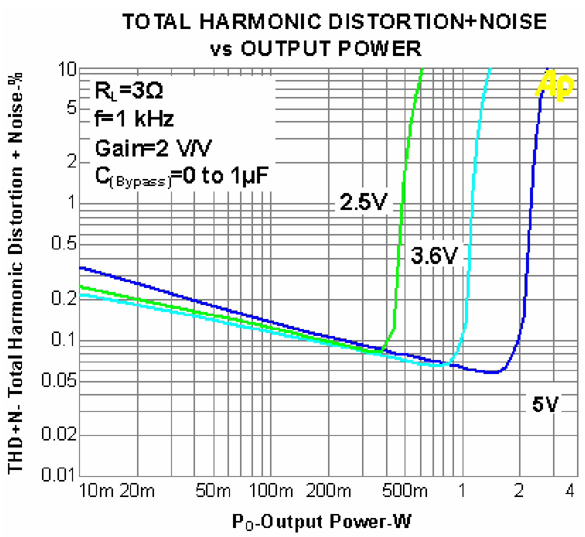

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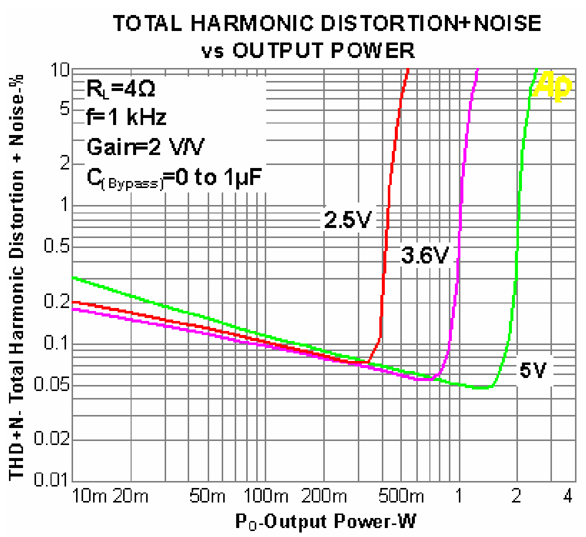
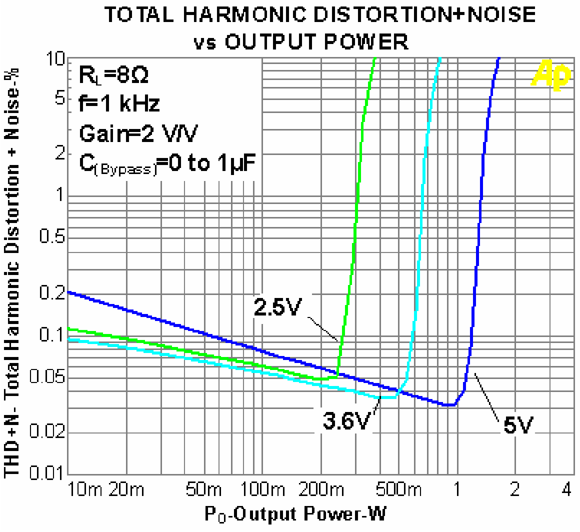


Figure 7

Typical Operating Characteristics (continued)



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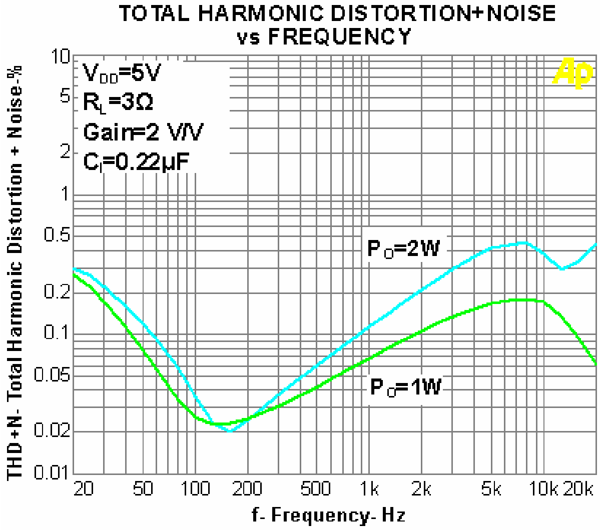

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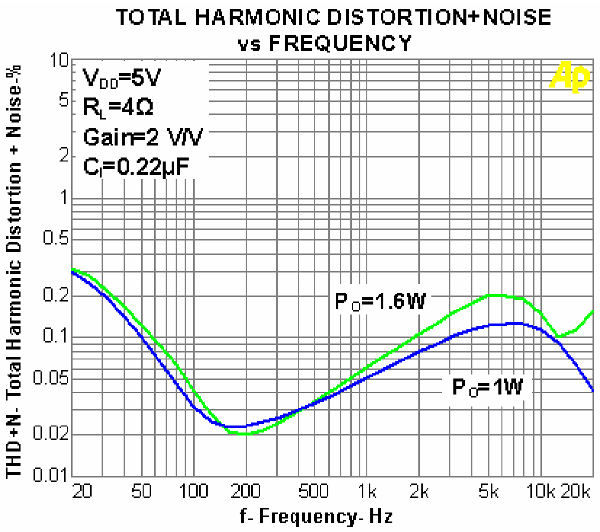


Figure 10

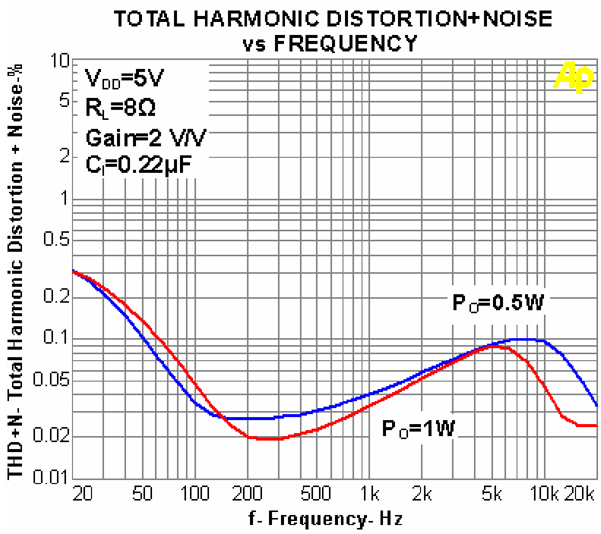
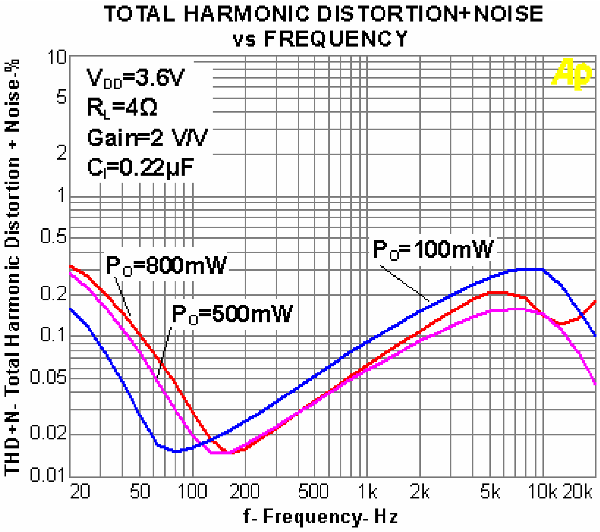


Figure 11



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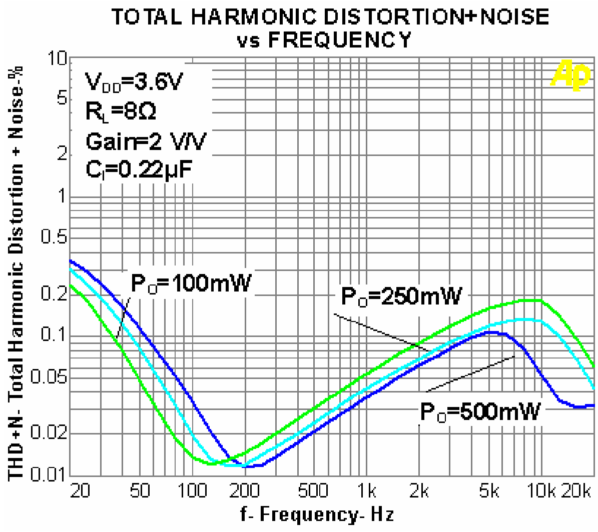


Figure 13

Typical Operating Characteristics (continued)

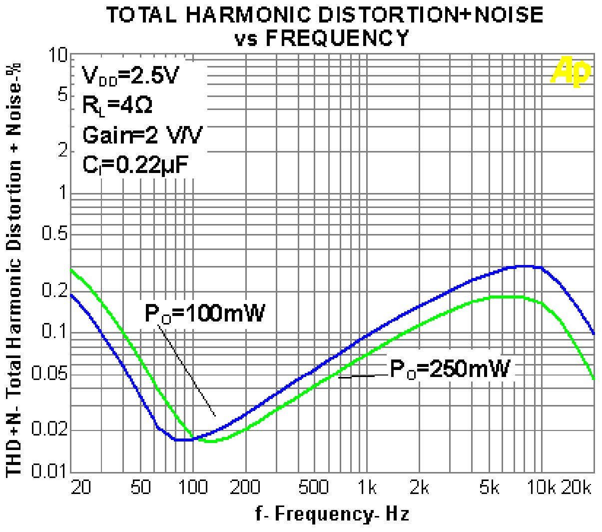


Figure 14

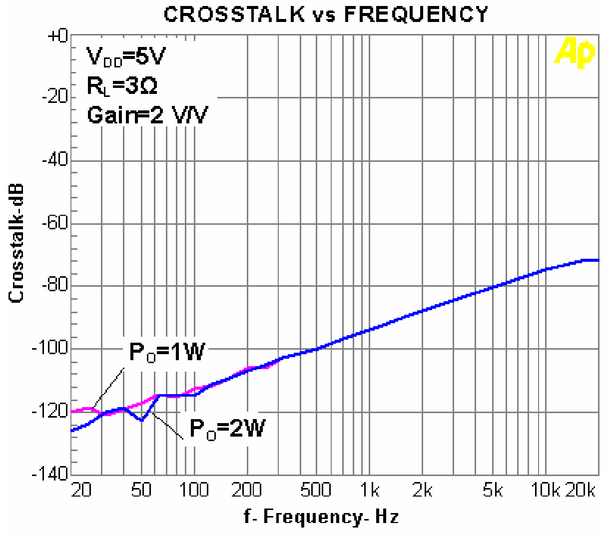


Figure 15

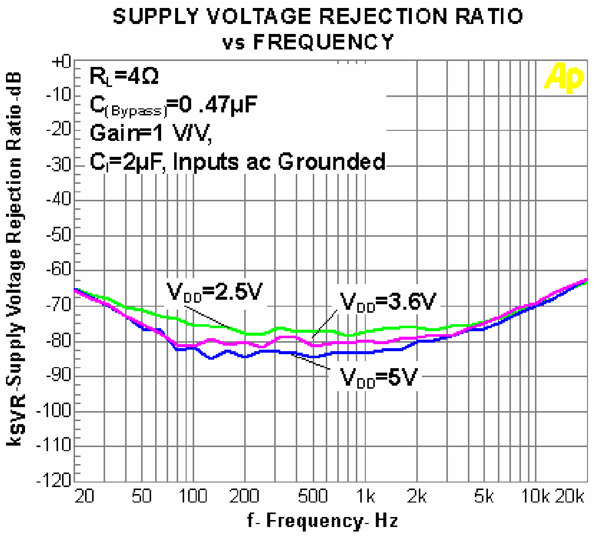


Figure 16

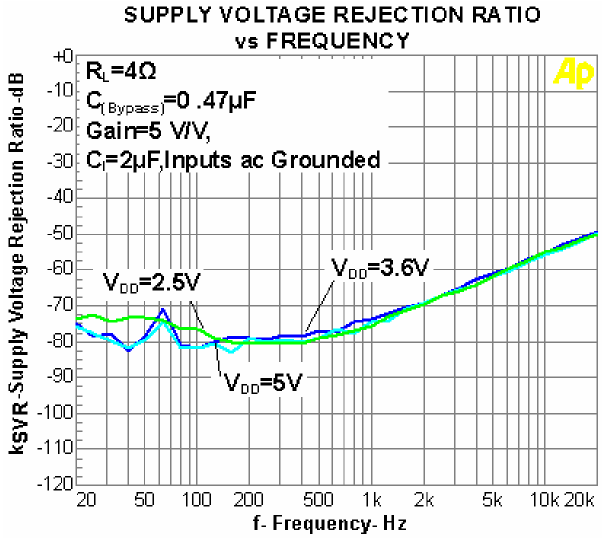


Figure 17

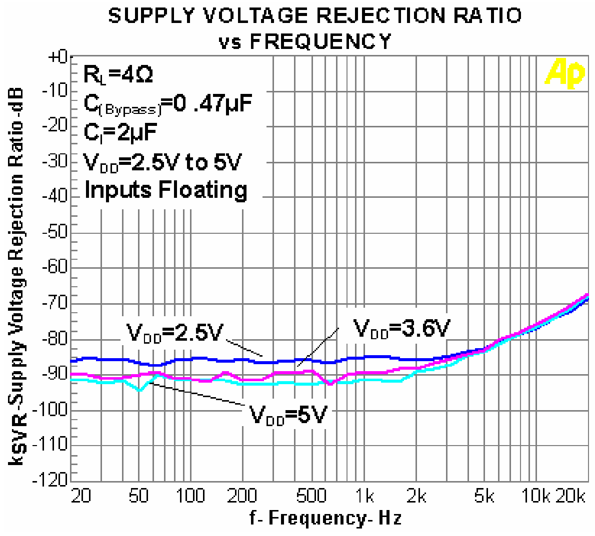


Figure 18

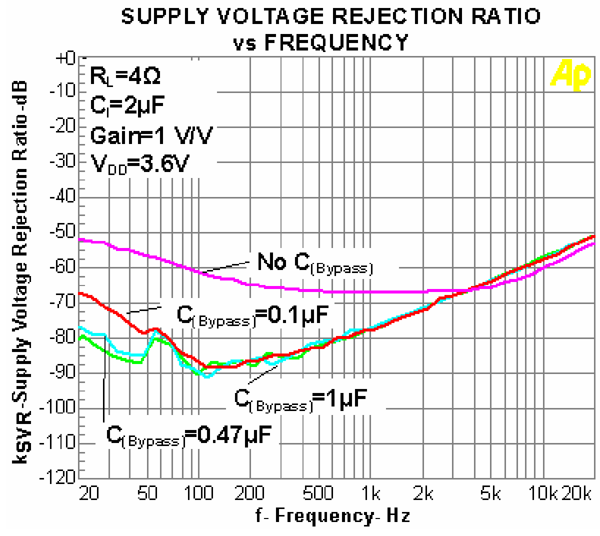


Figure 19

Typical Operating Characteristics (continued)

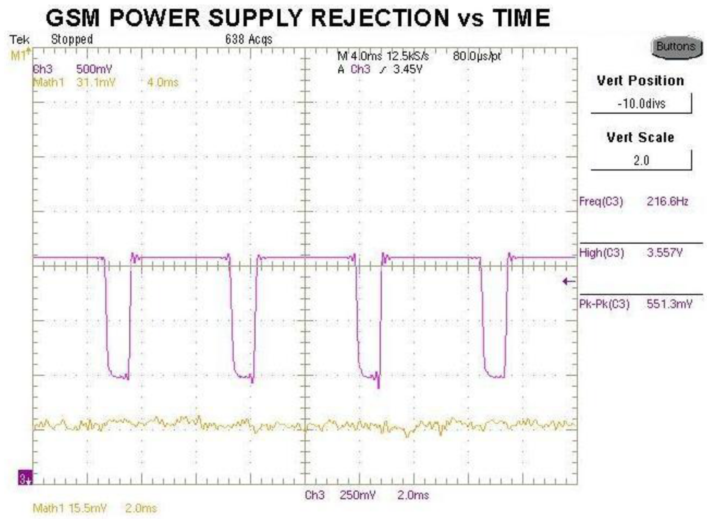


Figure 20

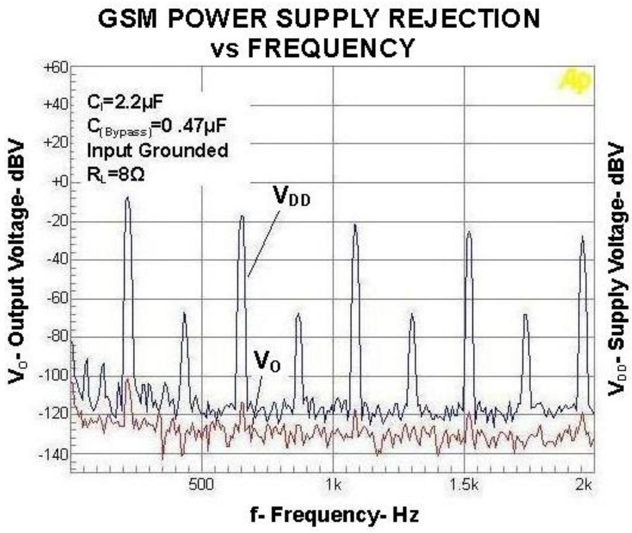


Figure 21

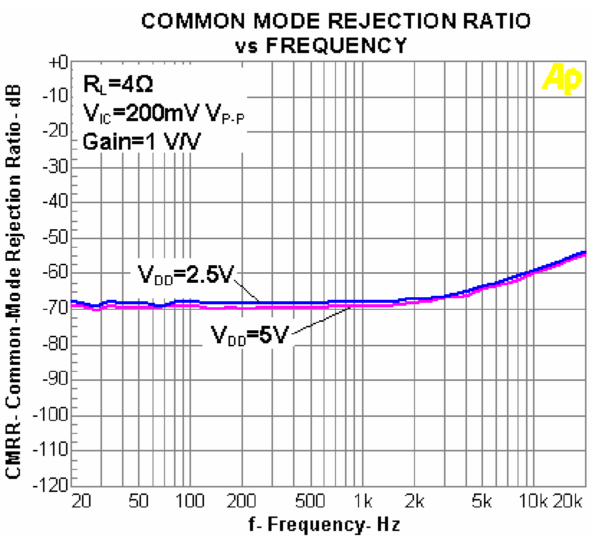


Figure 22

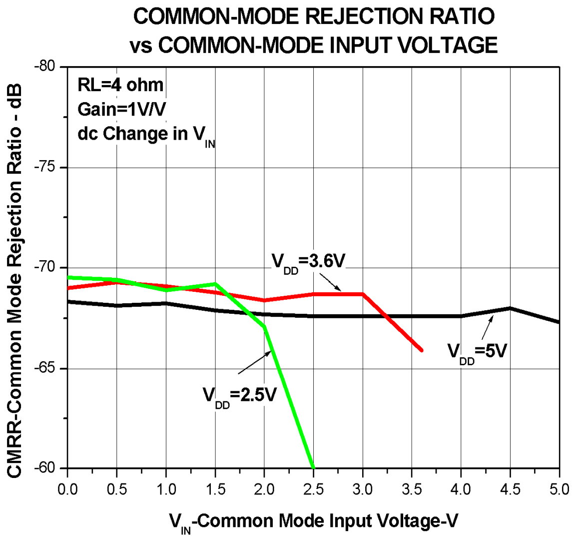


Figure 23

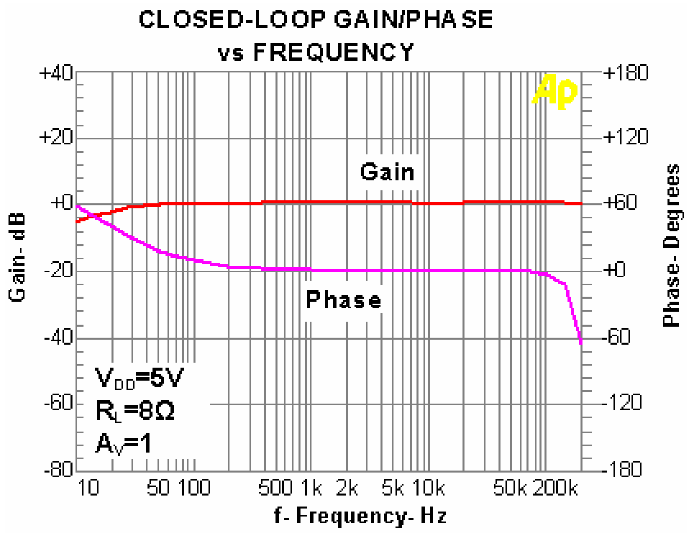


Figure 24

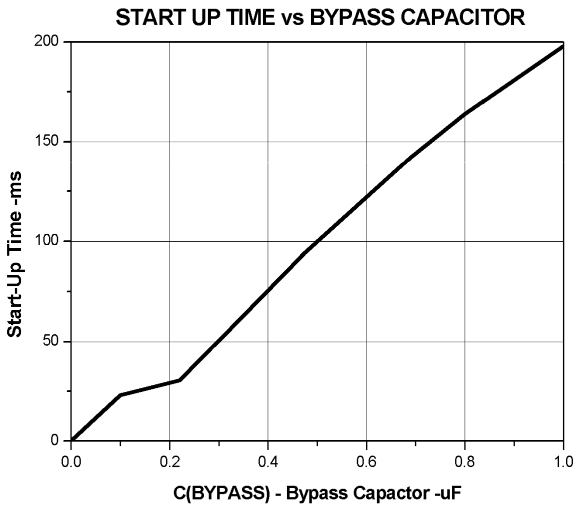


Figure 25

Application Information

Fully Differential Amplifier

The EUA4996 is a fully differential amplifier that features differential inputs and outputs. The EUA4996 also includes a common mode feedback loop that controls the output bias value to average it at $V_{CC}/2$ for any DC common mode input voltage. This allows the device to always have a maximum output voltage swing, and by consequence, maximize the output power. Moreover, as the load is connected differentially, compared to a single-ended topology, the output is four times higher for the same power supply voltage. The fully differential EUA4996 can still be used with a single-ended input; however, the EUA4996 should be used with differential inputs when in a noisy environment, like a wireless handset, to ensure maximum noise rejection.

Advantages of Fully Differential Amplifiers

The advantages of a full-differential amplifier are:

- Very high PSRR (Power Supply Rejection Ratio).
- High common mode noise rejection.
- Virtually zero pop without additional circuitry, giving an faster start-up time compared to conventional single-ended input amplifiers.
- No input coupling capacitors required thanks to common mode feedback loop.
- Midsupply bypass capacitor not required.

Application Schematics

Figure 26 through Figure 27 show application schematics for differential and single-ended inputs. Typical values are shown in Table1.

Table1. Typical Component Value

Component	Value
R_I	40kΩ
$C_{(BYPASS)}$	0.22μF
C_S	1μF
C_I	0.22μF

Power Dissipation

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. The maximum power dissipation for a given application can be derived from the power dissipation graphs of from equation1.

$$P_{DMAX} = 4*(V_{DD})^2/(2\pi^2 R_L) \text{ ------------(1)}$$

It is critical that the maximum junction temperature T_{JMAX} of 150°C is not exceeded. T_{JMAX} can be determine from the power derating curves by using P_{DMAX} and the PC board foil area. By adding additional copper foil, the thermal resistance of the application can be reduced, resulting in higher $P_{DMAX.}$ Additional copper foil can be added to any of the leads connected to the EUA4996. If T_{JMAX} still exceeds 150°C, then additional changes must be made. These changes can include reduced supply voltage, higher load impedance, or reduced ambient temperature. Internal power dissipation is a function of output power.

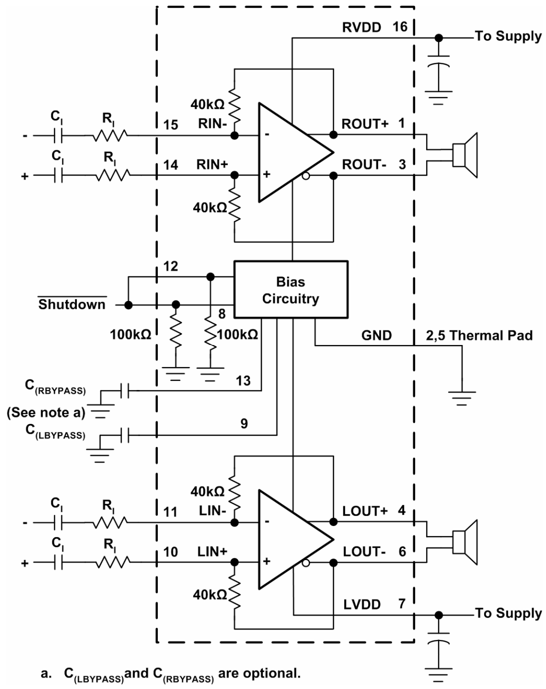


Figure 26.Differential Input Application Schematic Optimized with Input Capacitors

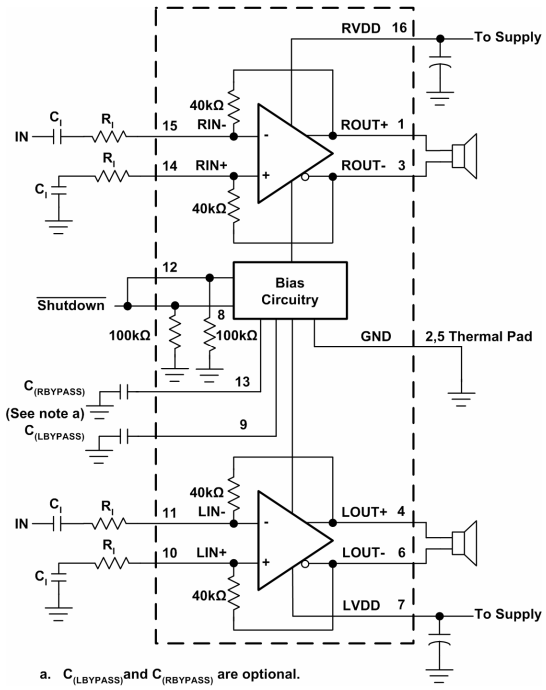


Figure 27.Single-Ended Input Application Schematic

Proper Selection of External Components

Gain-Setting Resistor Selection

The input resistor (R_I) can be selected to set the gain of the amplifier according to equation2.

$$Gain = R_F / R_I \qquad (2)$$

The internal feedback resistors (R_F) are trimmed to 40kΩ.

Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and the cancellation of the second harmonic distortion diminishes if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized.

Bypass Capacitors (C_{BYPASS}) and Start-up Time

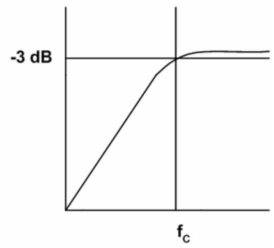
The internal voltage divider at the Bypass pin of this device sets a mid-supply voltage for internal references and sets the output common mode voltage to $V_{DD}/2$. Adding a capacitor to this pin filters any noise into this pin and increases k_{SVR}. $C_{(BYPASS)}$ also determines the rise time of V_{O+} and V_{O-} when the device is taken out of shutdown. The larger the capacitor, the slower the rise time. IF Bypass Capacitors are used, it is necessary to use separate bypass capacitors for each bypass pin.

Input Capacitor (CI)

The EUA4996 does not require input coupling capacitors if using a differential input source that is biased from 0.5V to V_{DD} -0.8V. Use 1% tolerance or better gain-setting resistors if not using input coupling capacitors.

In the single-ended input application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation3.

$$f_C = \frac{1}{2\pi R_I C_I} \qquad (3)$$



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit.

Consider the example where R_I is 10kΩ and the specification calls for a flat bass response down to 100Hz. Equation 3 is reconfigured as equation4.

$$C_I = \frac{1}{2\pi R_I f_C} \qquad (4)$$

In this example, C_I is 0.16µF, so one would likely choose a value in the range of 0.22µF to 0.47µF.

Ceramic capacitors should be used when possible, as they are the best choice in preventing leakage current. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

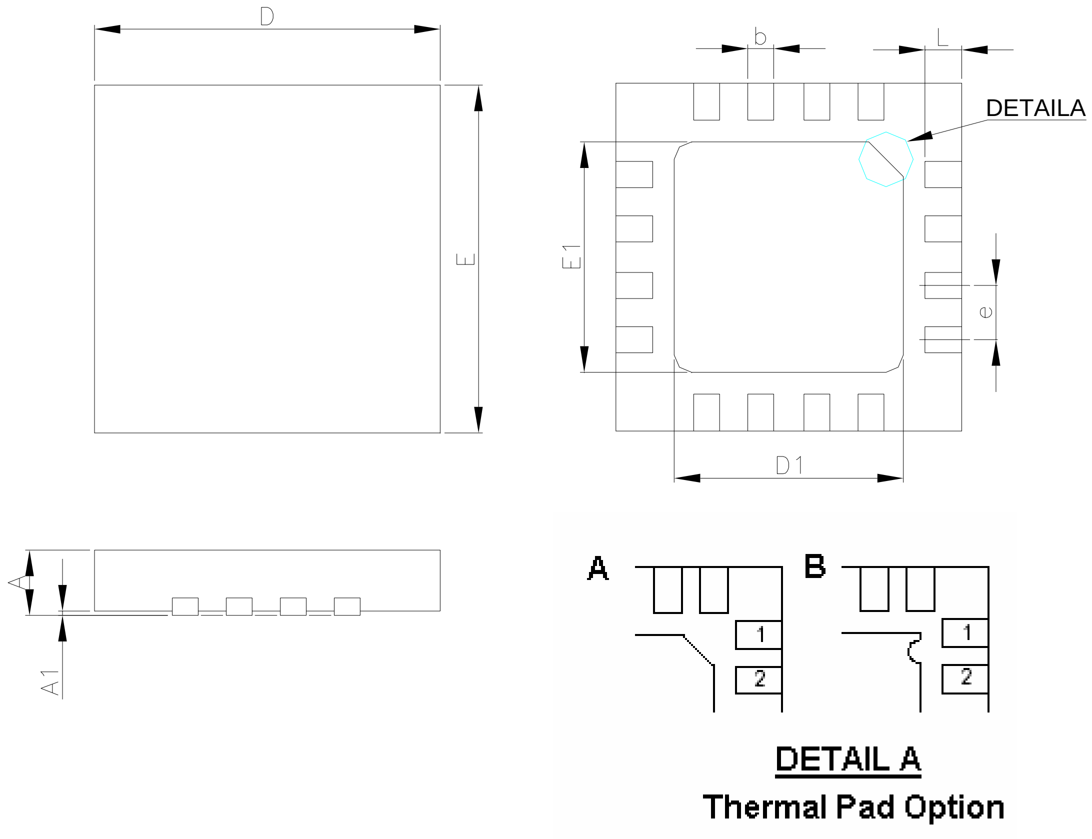
Decoupling Capacitor (CS)

The EUA4996 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1µF to 1 µF, placed as close as possible to the device V_{DD} lead works best. For filtering lower frequency noise signals, a 10-µF or greater capacitor placed near the audio power amplifier also helps, but is not required in most applications because of the high PSRR of this device.

Each V_{DD} pin must have a separate power supply decoupling capacitor. Additionally, the left and high channel V_{DD} pins must be tied together on the PCB.

Package Information

TQFN-16



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
b	0.25	0.35	0.009	0.014
E	3.90	4.10	0.153	0.161
D	3.90	4.10	0.153	0.161
D1	2.50		0.098	
E1	2.50		0.098	
e	0.65		0.026	
L	0.30	0.50	0.012	0.020