74F269

8-bit bidirectional binary counter

Rev. 05 — 25 March 2010 Product data sheet

1. General description

The 74F269 is a fully synchronous 8-stage up/down counter featuring a preset capability for programmable operation, carry look-ahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

2. Features and benefits

- Synchronous counting and loading
- Built-in look-ahead carry capability
- Count frequency 115 MHz (typical)
- Supply current 95 mA (typical)

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
N74F269D	0 °C to 70 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
N74F269DB	0 °C to 70 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

4. Functional diagram

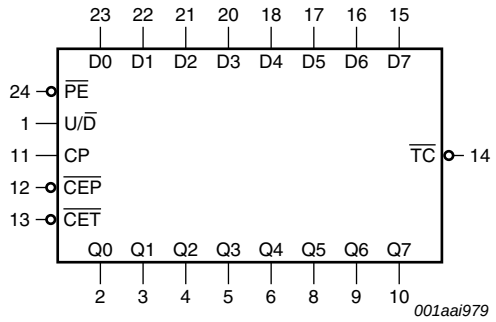


Fig 1. Logic symbol

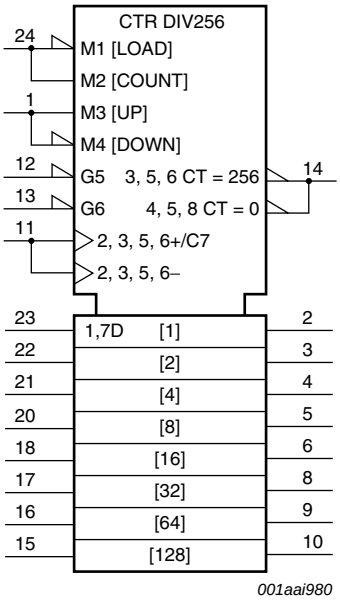


Fig 2. IEC logic symbol

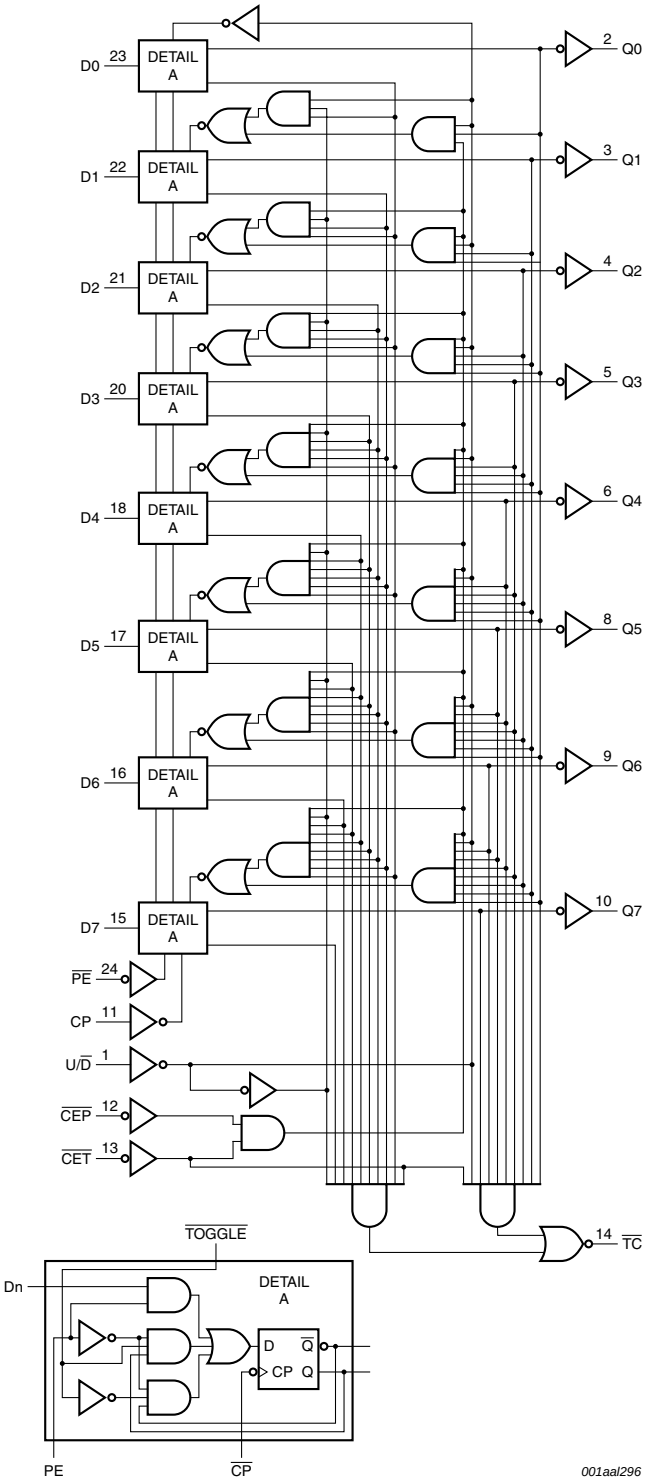


Fig 3. Logic diagram

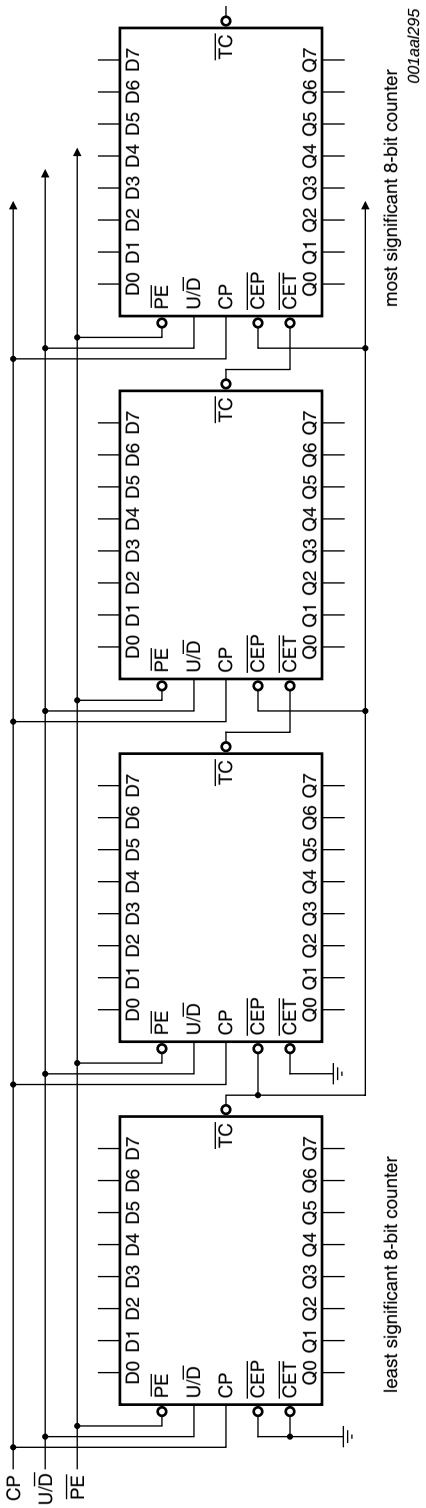


Fig 4. Synchronous multistage counting scheme

5. Pinning information

5.1 Pinning

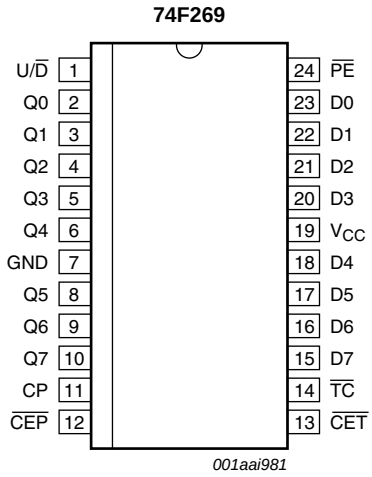


Fig 5. Pin configuration SO24 and SSOP24 package

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description	Unit load HIGH/LOW	Load value[1] HIGH/LOW
U/$\overline{D}$	1	up or down count control input	1.0/1.0	20 μA/0.6 mA
Q0 to Q7	2, 3, 4, 5, 6, 8, 9, 10	data output	50/33	1.0 mA/20 mA
GND	7	ground (0 V)	-	-
CP	11	clock input	1.0/1.0	20 μA/0.6 mA
$\overline{CEP}$	12	count enable parallel input (active LOW)	1.0/1.0	20 μA/0.6 mA
$\overline{CET}$	13	count enable trickle input (active LOW)	1.0/1.0	20 μA/0.6 mA
$\overline{TC}$	14	terminal count output (active LOW)	50/33	1.0 mA/20 mA
D0 to D7	23, 22, 21, 20, 18, 17, 16, 15	data input	1.0/1.0	20 μA/0.6 mA
V_{CC}	19	supply voltage	-	-
$\overline{PE}$	24	parallel enable input (active LOW)	1.0/1.0	20 μA/0.6 mA

[1] One FAST Unit Load (UL) is defined as 20 μA in HIGH state, 0.6 μA in LOW state.

6. Functional description

6.1 Function table

Table 3. Function table[1]

Operating modes	Input						Output	
	CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	Dn	Qn	$\overline{TC}$
Parallel load (Dn to Qn)	↑	X	X	X	l	l	L	*
	↑	X	X	X	l	h	H	*
Count up (increment)	↑	h	l	l	h	X	count up	*
Count down (decrement)	↑	l	l	l	h	X	count down	*
Hold (do nothing)	↑	X	h	l	h	X	qn	*
	↑	X	X	h	h	X	qn	H

[1] H = HIGH voltage level steady state
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level steady state
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
qn = Lower case letters indicate state of referenced output prior to the LOW-to-HIGH clock transition
X = don't care
↑ = LOW-to-HIGH clock transition
* = The $\overline{TC}$ is LOW when $\overline{CET}$ is LOW and the counter is at terminal count
Terminal count up is with all Qn outputs HIGH and terminal count down is with all Qn outputs LOW.

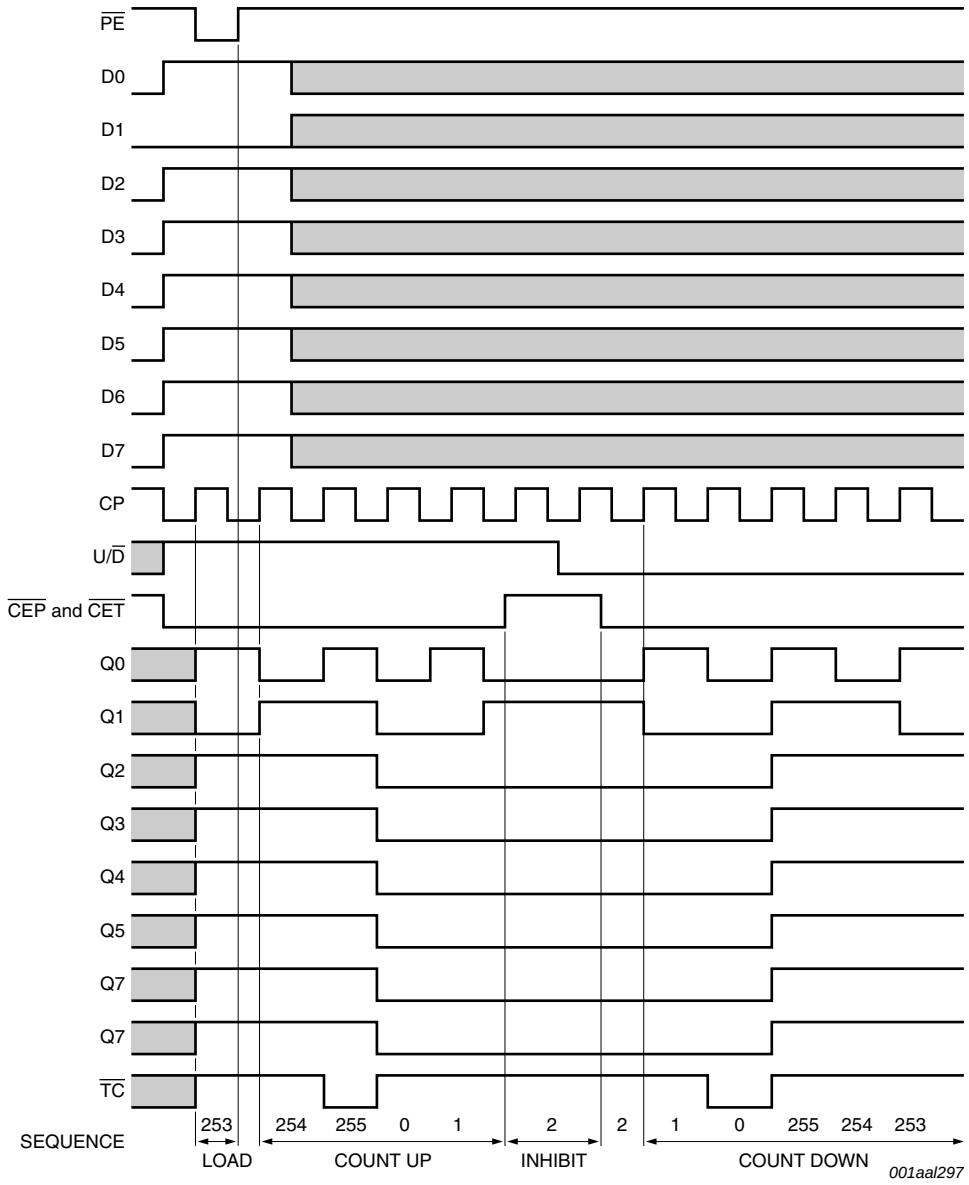


Fig 6. Typical timing sequence

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+7.0	V
V_I	input voltage		[1]	−0.5	+7.0	V
V_O	output voltage	output in HIGH-state	[1]	−0.5	+5.5	V
I_{IK}	input clamping current	$V_I < 0$ V		−30	+5	mA
I_O	output current	output in LOW-state		-	40	mA
T_{amb}	ambient temperature	in free air	[2]	0	70	°C
T_{stg}	storage temperature			−65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{IK}	input clamping current		-	-	−18	mA
I_{OH}	HIGH-level output current		−1	-	-	mA
I_{OL}	LOW-level output current		-	-	20	mA

9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_{IK} = −18 mA	−1.2	−0.73	-	−1.2	-	V
V_{OH}	HIGH-level output voltage	V_{CC} = 4.5 V; V_I = V_{IL} or V_{IH}						
		V_{CC} = ±10 %; I_{OH} = −1 mA	-	-	-	2.5	-	V
		V_{CC} = ±5 %; I_{OH} = −1 mA	-	3.4	-	2.7	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 4.5 V; I_{OL} = 20 mA; V_I = V_{IL} or V_{IH}						
		V_{CC} = ±10 %	-	0.30	-	-	0.50	V
		V_{CC} = ±5 %	-	0.30	-	-	0.50	V
I_I	input leakage current	V_{CC} = 5.5 V; V_I = 7.0 V	-	-	-	-	100	µA
I_{IH}	HIGH-level input current	V_{CC} = 5.5 V; V_I = 2.7 V	-	-	-	-	20	µA
I_{IL}	LOW-level input current	V_{CC} = 5.5 V; V_I = 0.5 V	-	-	-	-	−0.6	mA
I_O	output current	V_{CC} = 5.5 V [2]	-	-	-	−60	−150	mA
I_{CC}	supply current	$\overline{PE}$ = $\overline{CET}$ = $\overline{CEP}$ = U/$\overline{D}$ = GND; V_{CC} = 5.5 V; CP = rising edge						
		Dn: V_I = 4.5 V	-	93	-	-	120	mA
		Dn: V_I = GND	-	98	-	-	125	mA

[1] All typical values are measured at V_{CC} = 5 V.

[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; for test circuit, see Figure 13.

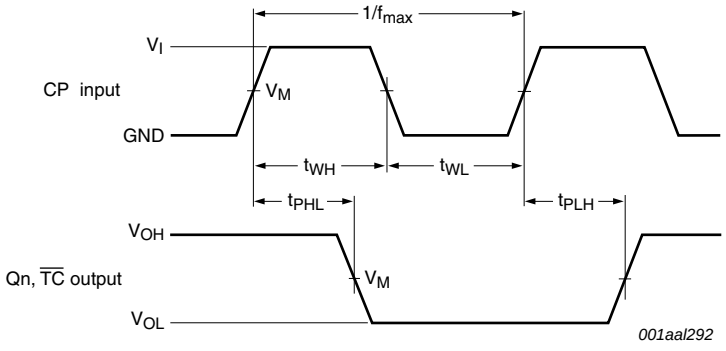
Symbol	Parameter	Conditions	25 °C; V_{CC} = 5.0 V			0 °C to 70 °C; V_{CC} = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	LOW to HIGH propagation delay	CP to Qn; load; $\overline{PE}$ = LOW; see Figure 7	3.0	6.0	8.5	3.0	9.0	ns
		CP to Qn; count; $\overline{PE}$ = HIGH; see Figure 7	3.0	6.0	9.0	3.0	10.0	ns
		CP to $\overline{TC}$; see Figure 7	4.5	6.5	9.5	4.0	10.5	ns
		$\overline{CET}$ to $\overline{TC}$; see Figure 8	3.5	6.0	9.0	3.0	10.0	ns
		U/$\overline{D}$ to $\overline{TC}$; see Figure 9	4.5	7.0	9.0	4.0	10.0	ns
t_{PHL}	HIGH to LOW propagation delay	CP to Qn; load; $\overline{PE}$ = LOW; see Figure 7	4.0	6.5	8.5	4.0	9.0	ns
		CP to Qn; count; $\overline{PE}$ = HIGH; see Figure 7	4.5	7.0	10.0	4.0	10.5	ns
		CP to $\overline{TC}$; see Figure 7	5.0	6.5	9.5	5.0	10.0	ns
		$\overline{CET}$ to $\overline{TC}$; see Figure 8	3.0	6.5	9.0	3.0	10.0	ns
		U/$\overline{D}$ to $\overline{TC}$; see Figure 9	4.5	7.0	9.5	4.0	10.0	ns

Table 7. Dynamic characteristics *...continued*

GND = 0 V; for test circuit, see Figure 13.

Symbol	Parameter	Conditions	25 °C; V_{CC} = 5.0 V			0 °C to 70 °C; V_{CC} = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
$t_{su(H)}$	set-up time HIGH	Dn to CP; see Figure 10	3.5	-	-	2.5	-	ns
		$\overline{PE}$ to CP; see Figure 10	5.5	-	-	5.5	-	ns
		$\overline{CEP}$ or $\overline{CET}$ to CP; see Figure 11	6.0	-	-	5.0	-	ns
		U/$\overline{D}$ to CP; see Figure 12	8.0	-	-	6.5	-	ns
$t_{su(L)}$	set-up time LOW	Dn to CP; see Figure 10	3.5	-	-	2.5	-	ns
		$\overline{PE}$ to CP; see Figure 10	6.5	-	-	6.5	-	ns
		$\overline{CEP}$ or $\overline{CET}$ to CP; see Figure 11	8.0	-	-	6.5	-	ns
		U/$\overline{D}$ to CP; see Figure 12	6.5	-	-	6.5	-	ns
$t_{h(H)}$	hold time HIGH	Dn to CP; see Figure 10	1.0	-	-	0	-	ns
		$\overline{PE}$ to CP; see Figure 10	0	-	-	0	-	ns
		$\overline{CEP}$ or $\overline{CET}$ to CP; see Figure 11	0	-	-	0	-	ns
		U/$\overline{D}$ to CP; see Figure 12	0	-	-	0	-	ns
$t_{h(L)}$	hold time LOW	Dn to CP; see Figure 10	1.0	-	-	1.0	-	ns
		$\overline{PE}$ to CP; see Figure 10	0	-	-	0	-	ns
		$\overline{CEP}$ or $\overline{CET}$ to CP; see Figure 11	0	-	-	0	-	ns
		U/$\overline{D}$ to CP; see Figure 12	0	-	-	0	-	ns
t_{WH}	pulse width HIGH	CP; see Figure 7	4.0	-	-	4.0	-	ns
t_{WL}	pulse width LOW	CP; see Figure 7	4.5	-	-	5.0	-	ns
f_{max}	maximum frequency	see Figure 7	100	115	-	85	-	MHz

11. Waveforms

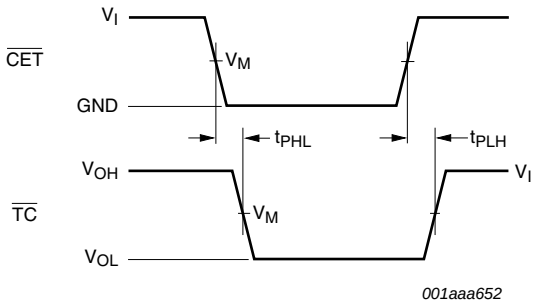


Measurement points are given in Table 8.

V_M = 1.5 V

V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

Fig 7. Clock (CP) to outputs (Qn, $\overline{TC}$) propagation delay, the clock pulse width

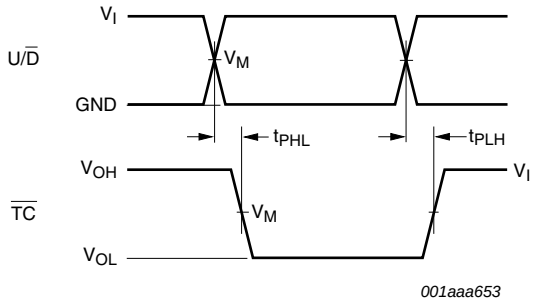


Measurement points are given in Table 8.

V_M = 1.5 V

V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

Fig 8. Input ($\overline{CET}$) to output ($\overline{TC}$) propagation delay

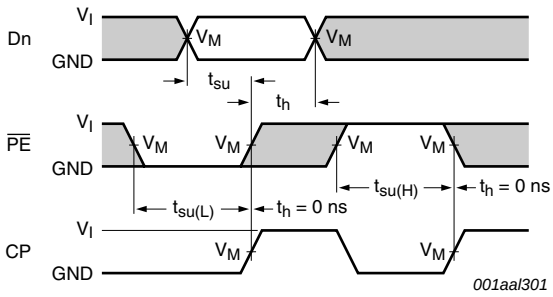


Measurement points are given in Table 8.

V_M = 1.5 V

V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

Fig 9. The up/down control input (U/$\overline{D}$) to output ($\overline{TC}$) propagation delay

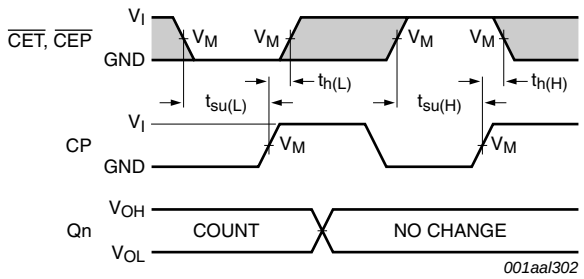


The shaded areas indicate when the input is permitted to change for predictable output performance.

Measurement points are given in Table 8.

V_M = 1.5 V

Fig 10. Data input (Dn), parallel enable input ($\overline{PE}$) and clock input (CP) set-up and hold times



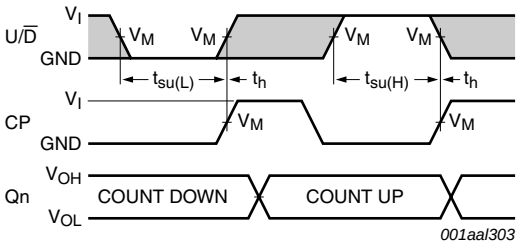
The shaded areas indicate when the input is permitted to change for predictable output performance.

Measurement points are given in Table 8.

V_M = 1.5 V

V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

Fig 11. Count enable inputs ($\overline{CEP}$ and $\overline{CET}$) and clock input (CP) set-up and hold times



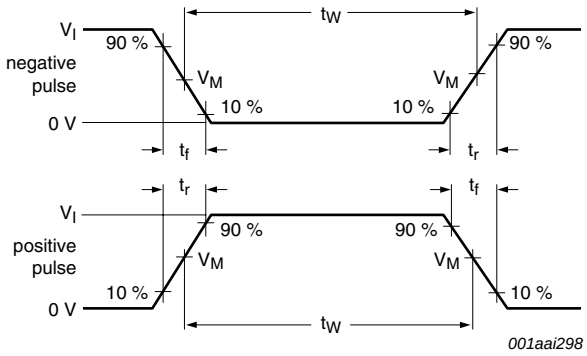
The shaded areas indicate when the input is permitted to change for predictable output performance.

Measurement points are given in Table 8.

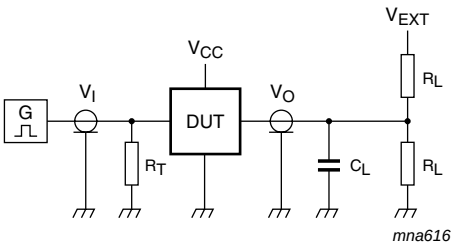
V_M = 1.5 V

V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

Fig 12. Up/down count control input (U/$\overline{D}$) and clock input (CP) set-up and hold times



a. Input pulse definition



b. Test circuit

Test data is given in Table 8.

Definitions for test circuit:

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

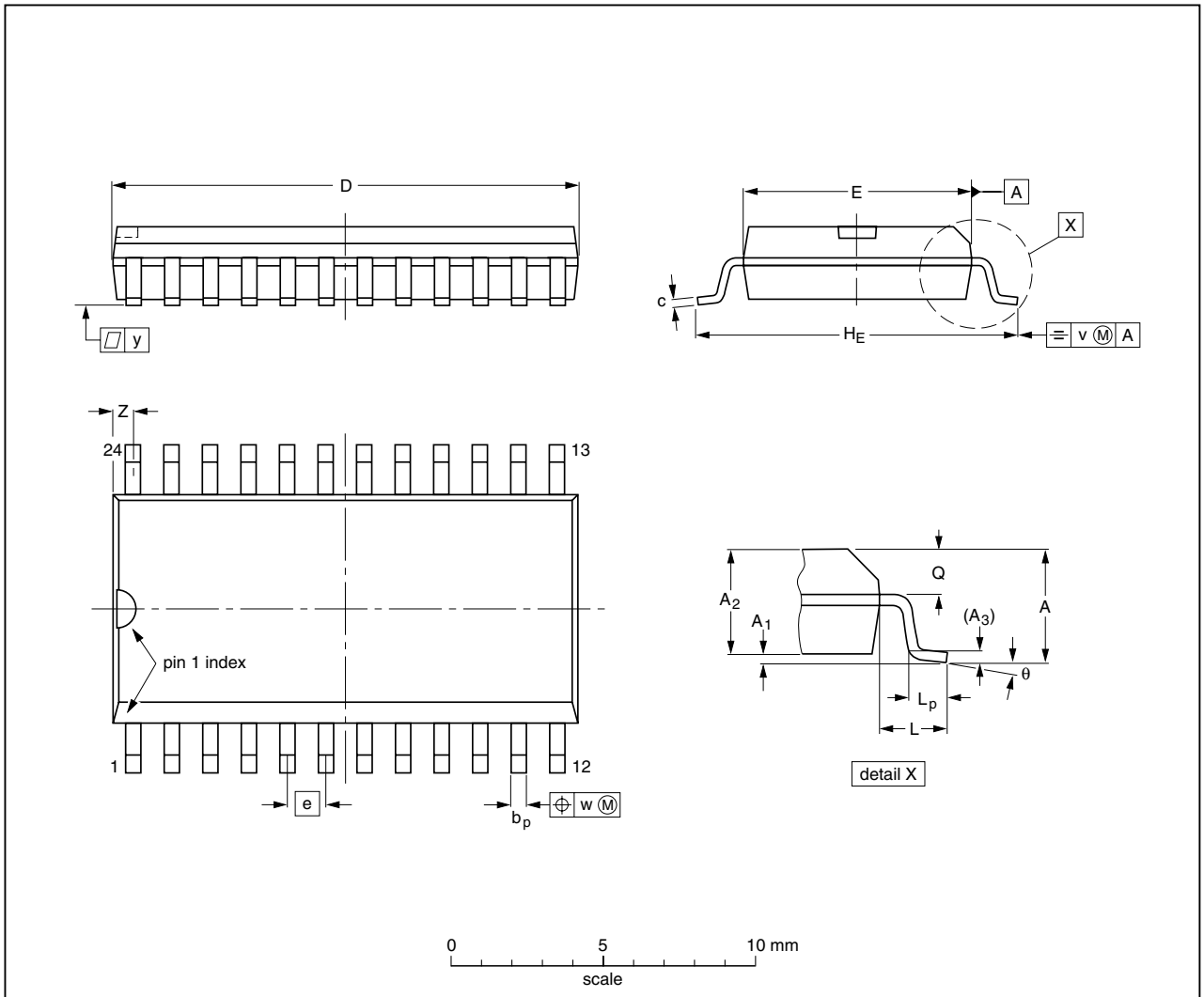
Fig 13. Test circuit for measuring switching times

Table 8. Test data

Input				Load		V_{EXT}		
V_I	f_I	t_W	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
3.0 V	1 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	open	open	7.0 V

12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

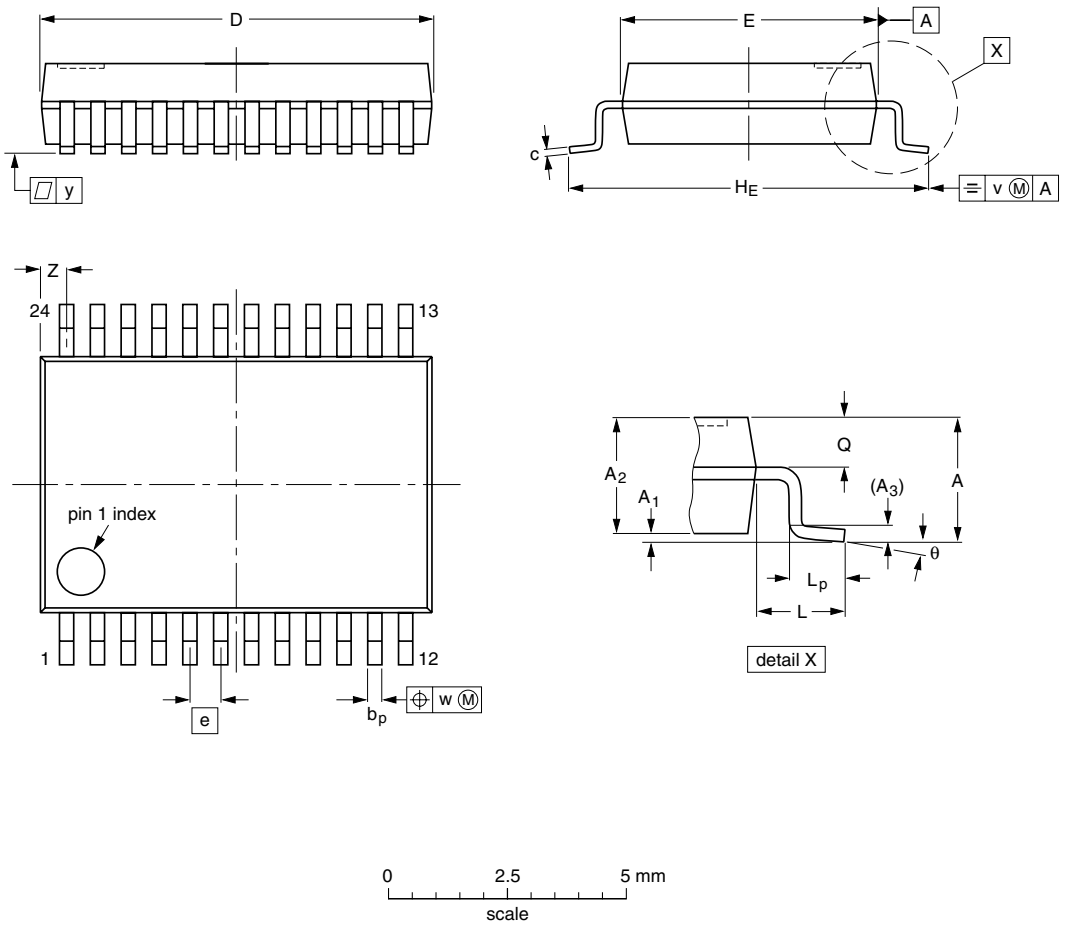
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig 14. Package outline SOT137-1 (SO24)

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				~~99-12-27~~ 03-02-19

Fig 15. Package outline SOT340-1 (SSOP24)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74F269_5	20100325	Product data sheet	-	74F269_4
74F269_4	20100308	Product data sheet	-	74F269_3
Modifications:	• Table 6 “Static characteristics”: Conditions typical values corrected.			
74F269_3	20100126	Product data sheet	-	74F269_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • DIP 24 (SOT222-1) package removed from Section 3 “Ordering information” and Section 12 “Package outline”			
74F269_2	19960105	Product specification	-	74F269_1

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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