ACT8740

Rev PrB, 25-Feb-08
Advanced Product Information—All Information Subject to Change

Six Channel Integrated Power Management IC for Handheld Portable Equipment

FEATURES

- **Multiple Patents Pending**
- **Li+ Battery Charger with Integrated MOSFET**
  - **Programmable Charge Current up to 1A**
  - **ON/OFF Control**
- **Five Integrated Regulators**
  - **350mA PWM Step-Down DC/DC**
  - **Step-Up DC/DC with OVP for WLED Bias**
  - **350mA Low Noise LDO**
  - **250mA Low Noise LDO**
  - **250mA Low Noise LDO**
- **I²C™ Compatible Serial Interface**
  - **Programmable Output Voltages**
  - **Configurable Operating Modes**
- **Minimal External Components**
- **4x4mm, Thin-QFN (TQFN44-24) Package**
  - **Only 0.75mm Height**
  - **RoHS Compliant**

APPLICATIONS

- **Portable Devices and PDAs**
- **Wireless Handhelds**
- **DMB Enabled Devices**
- **GPS Receivers, etc.**

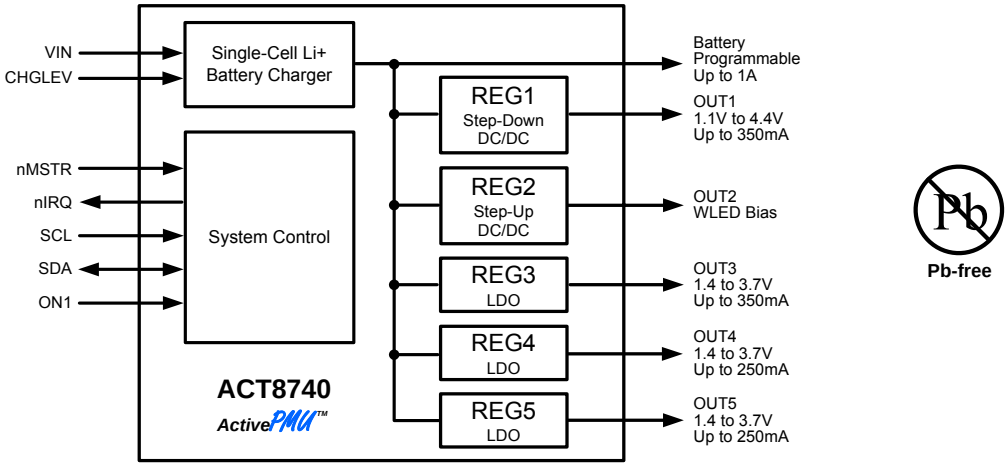
GENERAL DESCRIPTION

The patent-pending ACT8740 is a complete, cost effective, highly-efficient *ActivePMU™* power management solution that is ideal for a wide range of portable handheld equipment. This device integrates one PWM step-down DC/DC converter, one PWM step-up DC/DC converter with over-voltage protection (OVP), three low dropout linear regulators (LDOs) and a full-featured linear-mode Li+ battery charger into a single, thin, space-saving package. An I²C Serial Interface provides programmability for the DC/DC converters, LDOs and battery charger.

REG1 is a fixed-frequency, current-mode PWM step-down DC/DC converter that is optimized for high efficiency and is capable of supplying up to 350mA output current. REG2 is a fixed-frequency, step-up DC/DC converter that safely and efficiently biases a string of up to seven white-LEDs for backlighting. REG3, REG4, and REG5 are low noise, high PSRR linear regulators that are capable of supplying up to 350mA, 250mA, and 250mA, respectively. The battery charger incorporates an internal power MOSFET for constant-current/constant-voltage, thermally regulated charging of a single-cell Li+ battery. All DC/DC converters and LDOs output voltages are programmable and controllable via the I²C interface.

The ACT8740 is available in a tiny 4mm x 4mm 24-pin Thin-QFN package that is just 0.75mm thin.

SYSTEM BLOCK DIAGRAM



Pb-free

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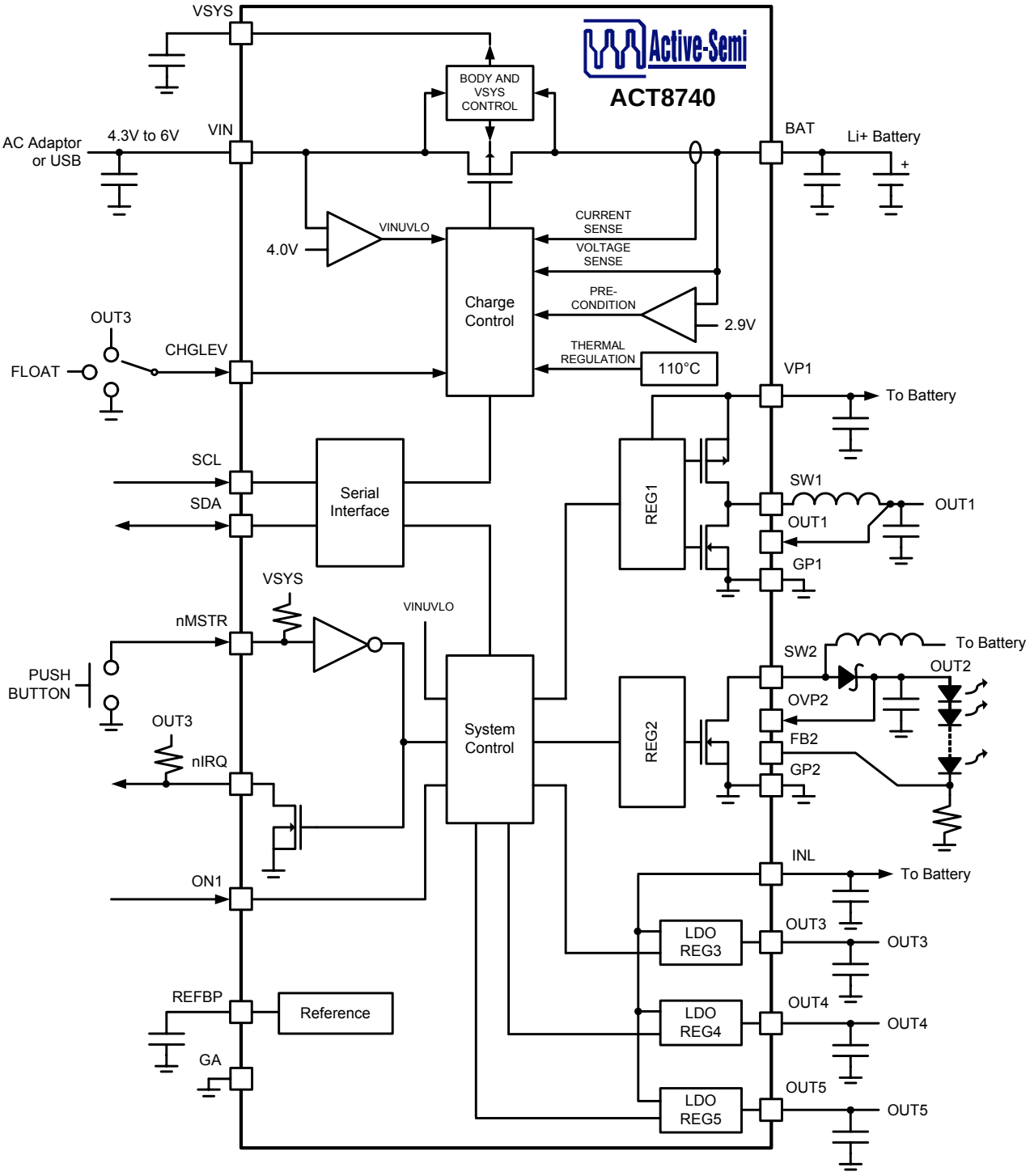
FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION①②

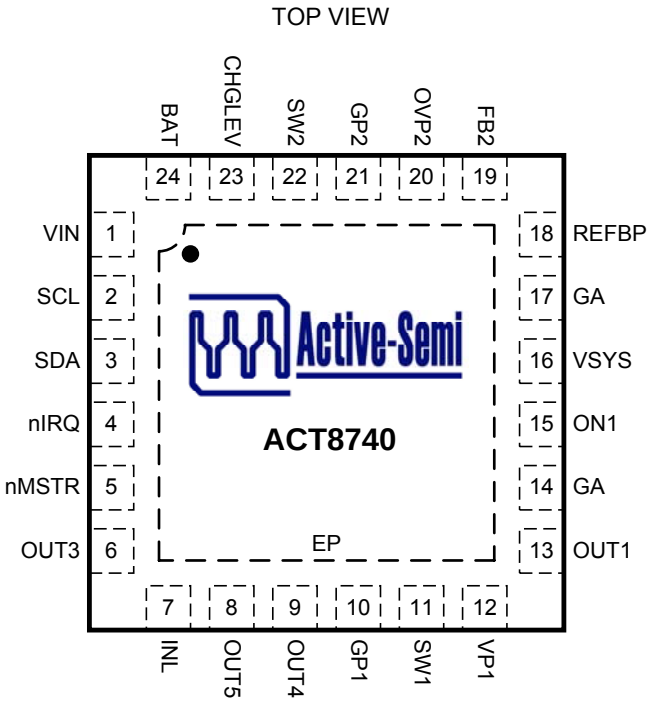
PART NUMBER	V_{OUT1}	V_{OUT3}	V_{OUT4}	V_{OUT5}	PACKAGE	PINS	TEMPERATURE RANGE
ACT8740QLEGA-T	1.8V	3.0V	2.5V	3.0V	TQFN44-24	24	-40°C to +85°C

OUTPUT VOLTAGE CODES					
C	D	E	F	G	H
1.2V	1.5V	1.8V	2.5V	3.0V	3.3V

①: Output voltage options detailed in this table represent standard voltage options, and are available for samples or production orders. Additional output voltage options, as detailed in the *Output Voltage Codes* table, are available for production subject to minimum order quantities. Contact Active-Semi for more information regarding semi-custom output voltage combinations.

②: All Active-Semi components are RoHS Compliant and with Pb-free plating unless specified differently. The term Pb-free means semiconductor products that are in compliance with current RoHS (Restriction of Hazardous Substances) standards.

PIN CONFIGURATION



Thin - QFN (TQFN44-24)

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	VIN	Power Input for the Battery Charger. The Battery Charger, REG1 and REG3 are automatically enabled whenever a valid voltage is present on VIN. Bypass to GA with a high quality ceramic capacitor placed as close as possible to the IC.
2	SCL	Clock Input for I^2C Serial Interface. Data is read on the rising edge of the clock.
3	SDA	Data Input for I^2C Serial Interface. Data is read on the rising edge of the clock.
4	nIRQ	Open-Drain Push-Button Status Output. nIRQ is an open-drain output which sinks current when nMSTR is asserted or when a fault-condition occurs. If interrupts are not masked.
5	nMSTR	Master Enable Input. Drive nMSTR to GA or to a logic low to enable the IC.
6	OUT3	Output voltage for REG3. Capable of delivering up to 350mA of output current. Output has high impedance when disabled.
7	INL	Power input for REG3, REG4 and REG5. Bypass to GA with a high quality ceramic capacitor placed as close as possible to the IC.
8	OUT5	Output voltage for REG5. Capable of delivering up to 250mA of output current. Output has high impedance when disabled.
9	OUT4	Output voltage for REG4. Capable of delivering up to 250mA of output current. Output has high impedance when disabled.
10	GP1	Power Ground for REG1. Connect GA, GP1 and GP2 together at a single point as close to the IC as possible.
11	SW1	Switching Node Output for REG1. Connect this pin to the switching end of the inductor.
12	VP1	Power Input for REG1. Bypass to GP1 with a high quality ceramic capacitor placed as close as possible to the IC.
13	OUT1	Output Feedback Sense for REG1. Connect this pin directly to the output node to connect the internal feedback network to the output voltage.
14,17	GA	Analog Ground. Connect GA directly to a quiet ground node. Connect GA, GP1 and GP2 together at a single point as close to the IC as possible.
15	ON1	Enable Control Input for REG1 and REG3. Drive ON1 to VSYS or to a logic high for normal operation, drive to GA or a logic low to disable REG1 and REG3.
16	VSYS	Power Bypass for System Management Circuitry. Bypass to GA with a high quality ceramic capacitor placed as close as possible to the IC. VSYS is internally connected to the higher voltage of either V_{VIN} or V_{BAT}. Do not load VSYS with more than 100µA.

PIN DESCRIPTIONS CONT'D

PIN	NAME	DESCRIPTION
18	REFBP	Reference Noise Bypass. Connect a 0.01µF ceramic capacitor from REFBP to GA. This pin is discharged to GA in shutdown.
19	FB2	Feedback Sense for REG2. Connect this pin to the LED string current sense resistor to sense the LED current.
20	OVP2	Over-Voltage Protection Input for REG2. Connect this pin directly to the output node to sense and prevent over-voltage conditions.
21	GP2	Power Ground for REG2. Connect GP2 directly to a power ground plane. Connect GA, GP1 and GP2 together at a single point as close to the IC as possible.
22	SW2	Switching Node Output for REG2. Connect this pin to the switching end of the inductor.
23	CHGLEV	Tri-State Charging State Select Input. When ISET1[ ] = [0000], drive CHGLEV to VSYS or to a logic high for high-current charging mode (450mA), and drive to GA or a logic low for low-current charging mode (90mA). Allow CHGLEV to float ($\|I_{CHGLEV}\|$ < 2µA) to disable the charger.
24	BAT	Output Voltage for the Battery Charger. Connect this pin directly to the battery anode (+ terminal) to sense the battery voltage.
EP	EP	Exposed Pad. Must be soldered to ground on PCB.

ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
VP1, SW1 to GP1, VSYS, SCL, SDA, INL, OUT1, OUT2, OUT3, OUT4, OUT5, FB2, BAT, CHGLEV, ON1, nMSTR, nIRQ to GA	-0.3 to +6	V
SW1 to VP1	-6 to +0.3	V
OVP2, SW2 to GP2	-0.3 to +30	V
VIN to GA t <1ms and duty cycle <1% Steady State	 -0.3 to +7 -0.3 to +6	 V V
GP1, GP2 to GA	-0.3 to +0.3	V
RMS Power Dissipation (T_A = 70°C)	1.8	W
Operating Temperature Range	-40 to 85	°C
Junction Temperature	125	°C
Storage Temperature	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

REGISTER DESCRIPTIONS

Table 1:

Global Register Map

OUTPUT	ADDRESS									DATA (DEFAULT VALUE)							
	HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
CHGR	08h	0	0	0	0	1	0	0	0	0	0	0	0	R	R	R	R
CHGR	09h	0	0	0	0	1	0	0	1	0	1	R	R	R	R	R	R
CHGR	0Ah	0	0	0	0	1	0	1	0	0	0	0	0	R	R	R	R
CHGR	0Bh	0	0	0	0	1	0	1	1	R	R	R	R	1	0	R	0
REG1	10h	0	0	0	1	0	0	0	0	R	V	V	V	V	V	V	V
REG1	11h	0	0	0	1	0	0	0	1	R	R	R	R	R	R	R	0
REG1	12h	0	0	0	1	0	0	1	0	R	R	R	R	R	R	R	R
REG1	13h	0	0	0	1	0	0	1	1	R	R	R	R	R	0	R	1
REG2	20h	0	0	1	0	0	0	0	0	R	R	V	V	V	V	V	V
REG2	21h	0	0	1	0	0	0	0	1	R	R	R	R	R	R	R	0
REG2	22h	0	0	1	0	0	0	1	0	R	R	0	0	0	0	0	0
REG2	23h	0	0	1	0	0	0	1	1	0	0	0	0	R	0	R	0
REG3	40h	0	1	0	0	0	0	0	0	R	R	1	V	V	V	V	V
REG4	41h	0	1	0	0	0	0	0	1	R	R	0	V	V	V	V	V
REG5	42h	0	1	0	0	0	0	1	0	R	R	0	V	V	V	V	V
REG345CFG	43h	0	1	0	0	0	0	1	1	R	R	R	0	0	0	0	R

KEY:

R: Read-Only bit. No Default Assigned.

V: Default Values Depend on Voltage Option. Default Values May Vary.

Note: Addresses other than those specified in Table 1 may be used for factory settings. Do not access any registers other than those specified in Table 1.

ELECTRICAL CHARACTERISTICS

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

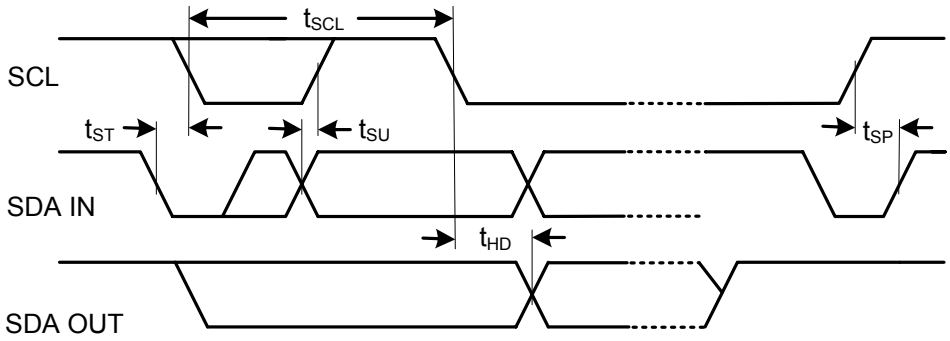
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VSYS Operating Voltage Range		2.6		5.5	V
VSYS UVLO Threshold	VSYS Voltage Rising	2.25	2.4	2.55	V
VSYS UVLO Hysteresis	VSYS Voltage Falling		80		mV
VSYS Output Resistance			10		Ω
Oscillator Frequency		1.35	1.6	1.85	MHz
VSYS Supply Current	ON1 = GA, CHGLEV = floating		1.5		μA
nMSTR Internal Pull-Up Resistance		250	500		kΩ
Logic High Input Voltage	ON1, nMSTR	1.4			V
Logic Low Input Voltage	ON1, nMSTR			0.4	V
Logic Low Output Voltage	nIRQ, I_{SINK} = 5mA			0.3	V
Leakage Current	nIRQ, V_{nIRQ} = 4.2V			1	μA
Thermal Shutdown Temperature	Temperature rising		160		°C
Thermal Shutdown Hysteresis	Temperature falling		20		°C

I²C INTERFACE ELECTRICAL CHARACTERISTICS

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Low Input Voltage				0.4	V
SCL, SDA High Input Voltage		1.4			V
SCL, SDA Leakage Current				1	µA
SDA Low Output Voltage	I_{OL} = 5mA			0.3	V
SCL Clock Period, t_{SCL}	f_{SCL} clock freq = 400kHz	2.5			µs
SDA Data In Setup Time to SCL High, t_{SU}		100			ns
SDA Data Out Hold Time after SCL Low, t_{HD}		300			ns
SDA Data Low Setup Time to SCL Low, t_{ST}	Start Condition	100			ns
SDA Data High Hold Time after Clock High, t_{HP}	Stop Condition	100			ns

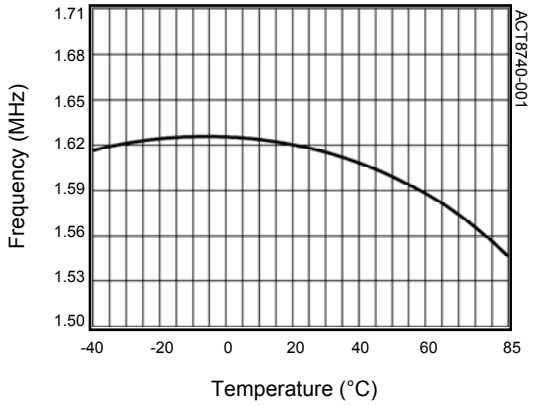
Figure 1:
I²C Serial Bus Timing



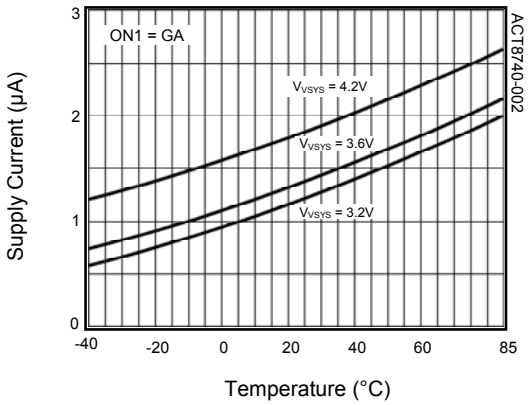
TYPICAL PERFORMANCE CHARACTERISTICS

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

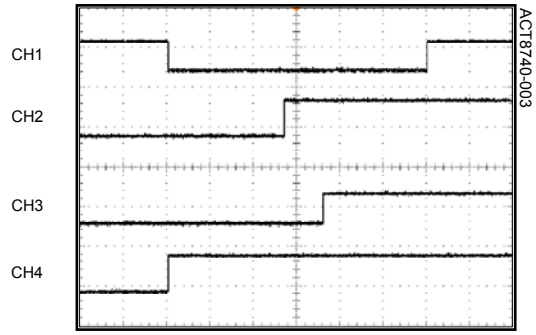
Oscillator Frequency vs. Temperature



VSYS Current vs. Temperature

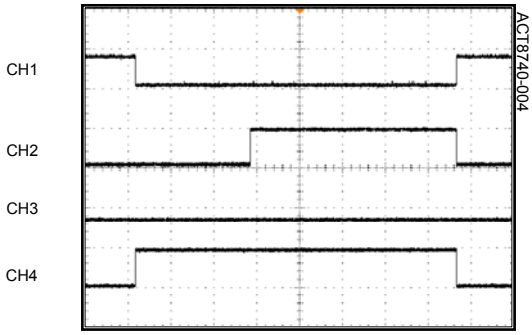


Startup Sequence



CH1: V_{nMSTR}, 5V/div
CH2: Power-On Reset (External Signal), 2V/div
CH3: V_{ON1}, 5V/div
CH4: V_{OUT1}, 2V/div
TIME: 100ms/div

Startup Sequence



CH1: V_{nMSTR}, 5V/div
CH2: Power-On Reset (External Signal), 2V/div
CH3: V_{ON1}, 5V/div
CH4: V_{OUT1}, 2V/div
TIME: 100ms/div

FUNTIONAL DESCRIPTION

General Description

The ACT8740 offers an array of system management functions that allow it to provide optimal performance in a wide range of applications.

I²C Serial Interface

At the core of the ACT8740's flexible architecture is an I²C interface that permits optional programming capability to enhance overall system performance.

To ensure compatibility with a wide range of system processors, the ACT8740 uses standard I²C commands, I²C write-byte commands are used to program the ACT8740 and I²C read-byte commands are used to read the ACT8740's internal registers. The ACT8740 always operates as a slave device, and is addressed using a 7-bit slave address followed by an eighth bit, which indicates whether the transaction is a read-operation or a write-operation, [1011110x].

SDA is a bi-directional data line and SCL is a clock input. The master initiates a transaction by issuing a START condition, defined by SDA transitioning from high to low while SCL is high. Data is transferred in 8-bit packets, beginning with the MSB, and is clocked-in on the rising edge of SCL. Each packet of data is followed by an "Acknowledge" (ACK) bit, used to confirm that the data was transmitted successfully.

For more information regarding the I²C 2-wire serial interface, go to the NXP website: http://www.nxp.com

System Startup and Shutdown

The ACT8740 features a flexible control architecture that supports a variety of software-controlled enable/disable functions that make it a simple yet flexible and highly configurable solution.

The ACT8740 is automatically enabled when any of the following conditions exists:

1) A valid supply voltage is present at VIN,
2) nMSTR is asserted low, or
3) ON1 is asserted high.

If any of these conditions is true, the ACT8740 enables REG1 and REG3, powering up the system processor so that the startup and shutdown sequences may be controlled via software. Each of these startup conditions are described in detail below.

Automatic Enable Due to Valid VIN Supply

The ACT8740 battery charger, REG1, and REG3 are automatically enabled when a valid input supply is applied to VIN. Automatically enabling these functions simplifies system design and eliminates the need for external input supply-detection circuitry.

Manual Enable Due to Asserting nMSTR Low

System startup is initiated when the user presses the push-button, asserting nMSTR low. When this occurs, both REG1 and REG3 are enabled. Once the power-up routine is successfully completed, the microprocessor must assert ON1 so that the ACT8740 remains enabled after the push-button is released by the user. Upon completion of the start-up sequence the processor assumes control of the power system and all further operation is software-controlled.

Manual Enable Due to Asserting ON1 High

The ACT8740 is compatible with applications that do not utilize its push-button control function, and may be enabled by simply driving ON1 to a logic-high. In this case, the signal driving ON1 controls enable/disable timing, although software-controlled enable/disable sequences are still supported if the processor assumes control of the power system once the startup sequence is completed.

Shutdown Sequence

Once a successful power-up routine is completed, the system processor controls the operation of the power system, including the system shutdown timing and sequence. The ACT8740 asserts nIRQ low when nMSTR is asserted low, providing a simple means of alerting the system processor when the user wishes to shut the system down. Asserting nIRQ interrupts the system processor, initiating an interrupt service routine in the processor which will reveal that the user pressed the push-button. The microprocessor may validate the input, such as by ensuring that the push-button is asserted for a minimum amount of time, then initiates a software-controlled power-down routine, the final step of which is to de-assert the ON1 input, disabling REG1 and REG3 and shutting the system down.

nMSTR Enable Input

In most applications, connect nMSTR to an active low, momentary push-button switch to utilize the ACT8740's closed-loop enable/disable functionality. If a momentary-on switch is not used, drive nMSTR to GA or to a logic low to initiate a startup sequence.

nIRQ Output

The ACT8740 provides an active-low, open-drain push-button status output that sinks current when nMSTR is driven to a logic-low. Connect a pull-up resistor from nIRQ to an appropriate voltage supply. nIRQ is typically used to drive the interrupt input of the system processor, and is useful in a variety of software-controlled enable/disable control routines.

Thermal Shutdown

The ACT8740 integrates thermal shutdown protection circuitry to prevent damage resulting from excessive thermal stress, as may be encountered under fault conditions. This circuitry disables all regulators if the ACT8740 die temperature exceeds 160°C, and prevents the regulators from being enabled until the IC temperature drops by 20°C (typ).

ELECTRICAL CHARACTERISTICS

(V_{VP1} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VP1 Operating Voltage Range		3.1		5.5	V
VP1 UVLO Threshold	Input Voltage Rising	2.9	3	3.1	V
VP1 UVLO Hysteresis	Input Voltage Falling		80		mV
Standby Supply Current			130	200	µA
Shutdown Supply Current	ON1 = GA, V_{VP1} = 4.2V		0.1	1	µA
Output Voltage Regulation Accuracy	V_{NOM1} < 1.3V, I_{OUT1} = 10mA	-2.4%	V_{NOM1}①	+1.8%	V
	V_{NOM1} ≥ 1.3V, I_{OUT1} = 10mA	-1.2%	V_{NOM1}	+1.8%	
Line Regulation	V_{VP1} = Max(V_{NOM1} + 1V, 3.2V) to 5.5V		0.15		%/V
Load Regulation	I_{OUT1} = 10mA to 350mA		0.0017		%/mA
Current Limit		0.45	0.6		A
Oscillator Frequency	V_{OUT1} ≥ 20% of V_{NOM1}	1.35	1.6	1.85	MHz
	V_{OUT1} = 0V		530		kHz
PMOS On-Resistance	I_{SW1} = -100mA		0.45	0.75	Ω
NMOS On-Resistance	I_{SW1} = 100mA		0.3	0.5	Ω
SW1 Leakage Current	V_{VP1} = 5.5V, V_{SW1} = 5.5V or 0V			1	µA
Power Good Threshold			94		%V_{NOM1}
Minimum On-Time			70		ns

①: V_{NOM1} refers to the nominal output voltage level for V_{OUT1} as defined by the *Ordering Information* section.

REGISTER DESCRIPTIONS

Note: See Table 1 for default register settings.

Table 2:

REG1 Control Register Map

ADDRESS	DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
10h	R	VRANGE	VSET					
11h	R	R	R	R	R	R	R	MODE
12h	R	R	R	R	R	R	R	R
13h	R	R	R	R	R	W/E	OK	W/E

R: Read-Only bits. Default Values May Vary.

W/E: Write-Exact bits. Read/Write bits which must be written exactly as specified in Table 1 .

Table 3:

REG1 Control Register Bit Descriptions

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION	
10h	VSET	[5:0]	R/W	REG1 Output Voltage Selection	See Table 4	
10h	VRANGE	[6]	R/W	REG1 Voltage Range Selection	0	Min V_{OUT} = 1.1V
					1	Min V_{OUT} = 1.25V
10h		[7]	R		READ ONLY	
11h	MODE	[0]	R/W	Mode Selection	0	PWM/PFM
					1	Forced PWM
11h		[7:1]	R		READ ONLY	
12h		[7:0]	R		READ ONLY	
13h		[0]	W/E		WRITE-EXACT	
13h	OK	[1]	R	REG1 Power-OK	0	Output is not OK
					1	Output is OK
13h		[2]	W/E		WRITE-EXACT	
13h		[7:3]	R		READ ONLY	

REGISTER DESCRIPTIONS CONT'D

Table 4:

REG1/VSET[ ] Output Voltage Setting

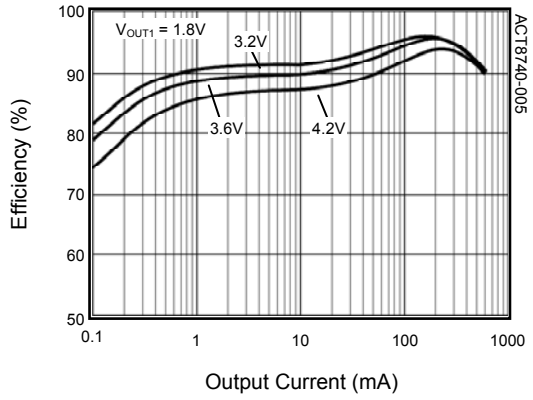
REG1/VSET [3:0]	REG1/VSET[5:4]							
	REG1/VRANGE[ ] = [0]				REG1/VRANGE[ ] = [1]			
	00	01	10	11	00	01	10	11
0000	N/A	N/A	1.455	1.860	1.250	2.050	2.850	3.650
0001	N/A	N/A	1.480	1.890	1.300	2.100	2.900	3.700
0010	N/A	1.100	1.505	1.915	1.350	2.150	2.950	3.750
0011	N/A	1.125	1.530	1.940	1.400	2.200	3.000	3.800
0100	N/A	1.150	1.555	1.965	1.450	2.250	3.050	3.850
0101	N/A	1.175	1.585	1.990	1.500	2.300	3.100	3.900
0110	N/A	1.200	1.610	2.015	1.550	2.350	3.150	3.950
0111	N/A	1.225	1.635	2.040	1.600	2.400	3.200	4.000
1000	N/A	1.255	1.660	2.065	1.650	2.450	3.250	4.050
1001	N/A	1.280	1.685	2.090	1.700	2.500	3.300	4.100
1010	N/A	1.305	1.710	2.115	1.750	2.550	3.350	4.150
1011	N/A	1.330	1.735	2.140	1.800	2.600	3.400	4.200
1100	N/A	1.355	1.760	2.165	1.850	2.650	3.450	4.250
1101	N/A	1.380	1.785	2.190	1.900	2.700	3.500	4.300
1110	N/A	1.405	1.810	2.200	1.950	2.750	3.550	4.350
1111	N/A	1.430	1.835	2.245	2.000	2.800	3.600	4.400

(N/A): Not Available

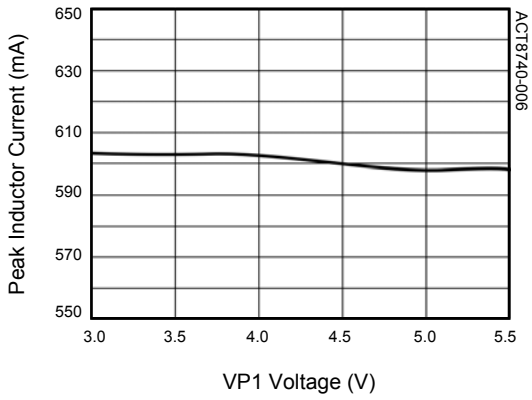
TYPICAL PERFORMANCE CHARACTERISTICS

(ACT8740QLEGA, V_{VP1} = V_{VP2} = 3.6V, L = 3.3µH, C_{VP1} = C_{VP2} = 2.2µF, C_{OUT1} = C_{OUT2} = 10µF, T_A = 25°C, unless otherwise specified.)

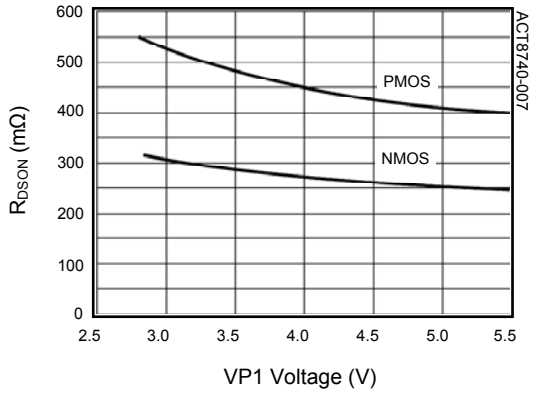
REG1 Efficiency vs. Load Current



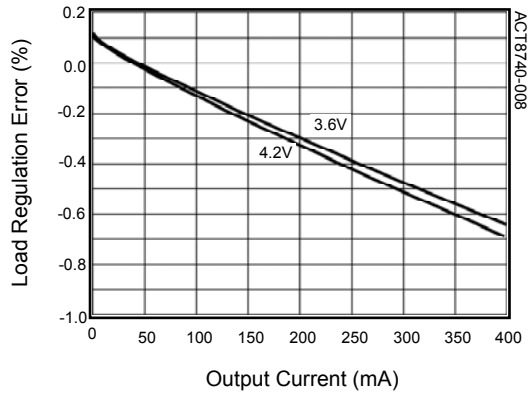
REG1 Transient Peak Inductor Current



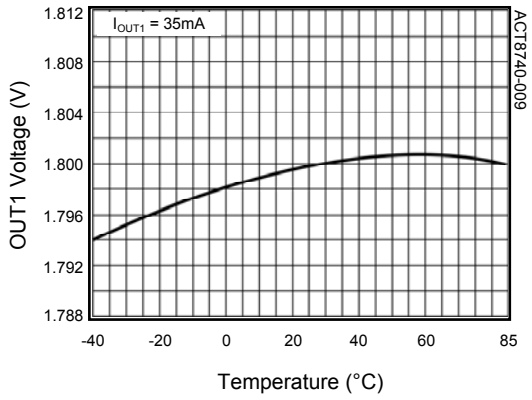
REG1 MOSFET Resistance



REG1 Load Regulation



OUT1 Regulation Voltage



FUNCTIONAL DESCRIPTION

General Description

REG1 is a fixed-frequency, current-mode, synchronous PWM step-down converters that achieves a peak efficiency of up to 97%. REG1 is capable of supplying up to 350mA of output current and operates with a fixed frequency of 1.6MHz, minimizing noise in sensitive applications and allowing the use of small external components. REG1 is available with a variety of standard and custom output voltages, and may be software-controlled via the I^2C interface by systems that require advanced power management functions.

100% Duty Cycle Operation

REG1 is capable of operating at up to 100% duty cycle. During 100% duty-cycle operation, the high-side power MOSFET is held on continuously, providing a direct connection from the input to the output (through the inductor), ensuring the lowest possible dropout voltage in battery-powered applications.

Synchronous Rectification

REG1 features an integrated n-channel synchronous rectifier, which maximizes efficiency and minimizes the total solution size and cost by eliminating the need for an external rectifier.

Enabling and Disabling REG1

Enable/disable functionality is typically implemented as part of a controlled enable/disable scheme utilizing nMSTR and other system control features of the ACT8740. REG1 is automatically enabled whenever either of the following conditions are met:

1) nMSTR is driven low, or

2) ON1 is asserted high.

When none of these conditions are true, REG1 is disabled, and its quiescent supply current drops to less than 1µA.

Programming the Output Voltage

By default, REG1 powers up and regulates to its default output voltage. Once the system is enabled, REG1's output voltage may be programmed to a different value, typically in order to reduce the power consumption of a microprocessor in standby mode. Program the output voltage via the I^2C serial interface by writing to the REG1/VSET1[ ] register.

Programmable Operating Mode

By default, REG1 operates in fixed-frequency PWM mode at medium to heavy loads, then transitions to a proprietary power-saving mode at light loads in order to save power. In applications where low noise is critical, force fixed-frequency PWM operation across the entire load current range, at the expense of light-load efficiency, by setting the REG1/MODE[ ] bit to [1].

Power-OK

REG1 features a power-OK status bit that can be read by the system microprocessor. If the output voltage is lower than the power-OK threshold, typically 6% below the programmed regulation voltage, REG1/OK[ ] will clear to 0.

Soft-Start

REG1 includes internal soft-start circuitry, and enabled its output voltage tracks an internal 80µs soft-start ramp so that it powers up in a monotonic manner that is independent of loading.

Compensation

REG1 utilizes current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over its full operating range. No compensation design is required, simply follow a few simple guidelines described below when choosing external components.

Input Capacitor Selection

The input capacitor reduces peak currents and noise induced upon the voltage source. A 2.2µF ceramic input capacitor is recommended for most applications.

Output Capacitor Selection

For most applications, a 10µF ceramic output capacitor is recommended. Although REG1 was designed to take advantage of the benefits of ceramic capacitors, namely small size and very-low ESR, low-ESR tantalum capacitors can provide acceptable results as well.

Inductor Selection

REG1 utilizes current-mode control and a proprietary internal compensation scheme to simultaneously

simplify external component selection and optimize transient performance over its full operating range. REG1 was optimized for operation with a 3.3µH inductor, although inductors in the 2.2µH to 4.7µH range can be used. Choose an inductor with a low DC-resistance, and avoid inductor saturation by choosing inductors with DC ratings that exceed the maximum output current of the application by at least 30%.

PCB Layout Considerations

High switching frequencies and large peak currents make PC board layout an important part of step-down DC/DC converter design. A good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Step-down DC/DCs exhibit discontinuous input current, so the input capacitors should be placed as close as possible to the IC, and avoiding the use of vias if possible. The inductor, input filter capacitor, and output filter capacitor should be connected as close together as possible, with short, direct, and wide traces. The ground nodes for each regulator's power loop should be connected at a single point in a star-ground configuration, and this point should be connected to the backside ground plane with multiple vias. The output node should be connected to the OUT1 pin through the shortest possible route, while keeping sufficient distance from switching nodes to prevent noise injection. Finally, the exposed pad should be directly connected to the backside ground plane using multiple vias to achieve low electrical and thermal resistance.

ELECTRICAL CHARACTERISTICS

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range①		2		5.5	V
UVLO Voltage Threshold	VSYS Voltage Rising	2.9	3	3.1	V
UVLO Voltage Hysteresis	VSYS Voltage Falling		80		mV
Supply Current	REG2/ON[ ] = [1], V_{FB2} = 0.3V		75	150	μA
	REG2/ON[ ] = [0], I_{LOAD} = 0mA		0.1	1	
FB2 Feedback Voltage		235	255	275	mV
FB2 Input Current			50		nA
Oscillator Frequency		1.35	1.6	1.85	MHz
Minimum On-Time			100		ns
Maximum Duty Cycle		85	90		%
Switch Current Limit	Duty = 83%, L = 22μH, C_{OUT2} = 4.7μF	500	750		mA
Switch On-Resistance	I_{SW2} = 100mA		0.67	1.1	Ω
Switch Leakage Current	V_{SW2} = 30V, Regulator Disabled			10	μA
Over Voltage Threshold	VSET[ ] = [111111]	27.5	28.5	29.5	V

①: As long as VSYS is within the VSYS operating range, this spec refers to the voltage range of the input that the inductor is connected to.

REGISTER DESCRIPTIONS

Note: See Table 1 for default register settings.

Table 5:

REG2 Control Register Map

ADDRESS	DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
20h	R	R	VSET					
21h	R	R	R	R	R	R	R	W/E
22h	R	R	W/E	W/E	W/E	W/E	W/E	W/E
23h	W/E	W/E	W/E	W/E	R	W/E	OK	ON

R: Read-Only bits. Default Values May Vary.

W/E: Write-Exact bits. Read/Write bits which must be written exactly as specified in Table 1.

Table 6:

REG2 Control Register Bit Descriptions

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION	
20h	VSET	[5:0]	R/W	REG2 Over Voltage Threshold Selection	See Table 7	
20h		[7:6]	R		READ ONLY	
21h		[0]	W/E		WRITE-EXACT	
21h		[7:1]	R		READ ONLY	
22h		[5:0]	W/E		WRITE-EXACT	
22h		[7:6]	R		READ ONLY	
23h	ON	[0]	R/W	REG2 Enable	0	REG2 Disable
					1	REG2 Enable
23h	OK	[1]	R	REG2 Power-OK	0	Output is not OK
					1	Output is OK
23h		[2]	W/E		WRITE-EXACT	
23h		[3]	R		READ ONLY	
23h		[7:4]	W/E		WRITE-EXACT	

REGISTER DESCRIPTIONS CONT'D

Table 7:

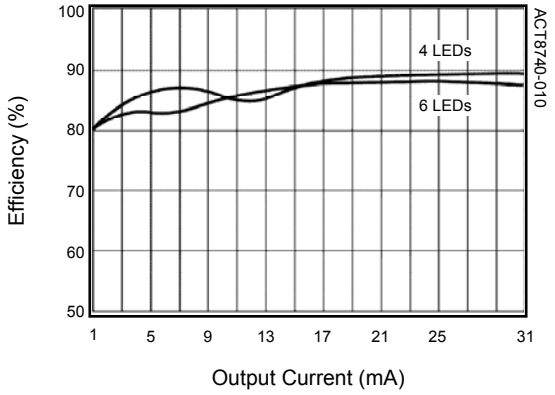
REG2/VSET[ ] Over Voltage Threshold Setting

REG2/VSET [2:0]	REG2/VSET[5:3]							
	000	**001**	**010**	**011**	**100**	**101**	**110**	**111**
000	5.00	7.00	9.000	11.00	13.00	17.00	21.00	25.00
001	5.25	7.25	9.250	11.25	13.50	17.50	21.50	25.50
010	5.50	7.50	9.500	11.50	14.00	18.00	22.00	26.00
011	5.75	7.75	9.750	11.75	14.50	18.50	22.50	26.50
100	6.00	8.00	10.00	12.00	15.00	19.00	23.00	27.00
101	6.25	8.25	10.25	12.25	15.50	19.50	23.50	27.50
110	6.50	8.50	10.50	12.50	16.00	20.00	24.00	28.00
111	6.75	8.75	10.75	12.75	16.50	20.50	24.50	28.50

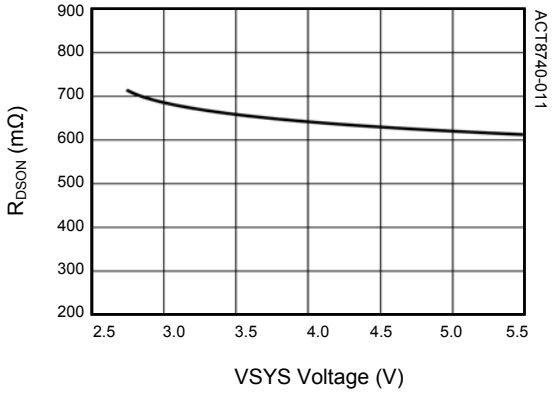
TYPICAL PERFORMANCE CHARACTERISTICS

(ACT8740QLEHA, V_{VSYS} = 3.6V, L = 22µH, C_{OUT} = 2.2µF, T_A = 25°C, unless otherwise specified.)

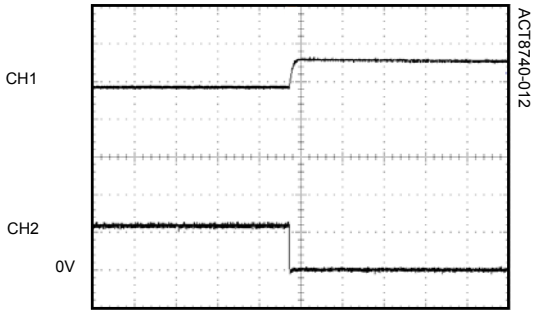
REG2 Efficiency vs. Output Current



REG2 R_{DSON}

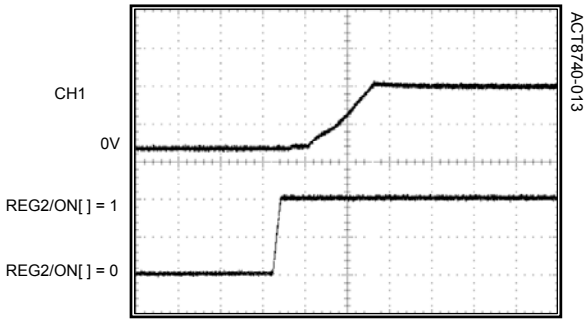


REG2 Over-Voltage Protection



CH1: V_{OUT3}, 10V/div
CH2: V_{FB3}, 200mV/div
TIME: 2ms/div

REG2 Startup Waveform



CH1: V_{OUT2}, 10V/div
TIME: 100µs/div

FUNCTIONAL DESCRIPTION

General Description

REG2 is a highly efficient step-up DC/DC converter that employs a fixed frequency, current-mode, PWM architecture. This regulator is optimized for white-LED bias applications consisting of up to seven white-LEDs.

Enabling and Disabling REG2

Enable/disable control of REG2 is achieved through the ACT8740's I^2C serial interface. Enable REG2 by setting REG2/ON[ ] to [1], disable REG2 by clearing REG2/ON[ ] to [0]. When disabled, REG2's quiescent supply current drops to just 1µA. As with all non-synchronous step-up DC/DC converters, REG2's application circuit produces a DC current path between the input and the output in shutdown mode. Although the forward drop of the WLEDs makes this leakage current very small in most applications, it is important to consider the effect that this may have in your application particularly when using fewer than three WLEDs.

Over-Voltage Protection

REG2 features internal over-voltage protection (OVP) circuitry which protects the system from LED open-circuit fault conditions. If the voltage at OV ever reaches the over-voltage threshold, REG2 will regulate the top of the LED strong to the OVP threshold voltage. By default, the ACT8740's OVP threshold is set at 28.5V, although it may be programmed to a lower value by writing to the REG2/VSET[ ] register.

Power-OK Bit

REG2 features a Power-OK status bit that can be read by the system microprocessor via the I^2C interface. If the voltage at OV is greater than the OVP threshold, REG2/OK[ ] will clear to 0.

Compensation and Stability

REG2 utilizes current-mode control and an internal compensation network to optimize transient performance, ease compensation, and improve stability over a wide range of operating conditions. REG2 is a flexible regulator, and its external components can be chosen to achieve the smallest possible footprint or to achieve the highest possible efficiency.

Inductor Selection

REG2 was designed to provide excellent performance across a wide range of applications, but was optimized for operation with inductors in the 10µH to 22µH range, although larger inductor values of up to 68µH can be used to achieve the highest possible efficiency.

Optimizing for Smallest Footprint

REG2 is capable of operating with very low inductor values in order to achieve the smallest possible footprint. When solution size is of primary concern, best results are achieved when using an inductor that ensures discontinuous conduction mode (DCM) operation over the full load current range.

Optimizing for Highest Efficiency

REG2 achieves excellent efficiency in applications that demand the longest possible battery life. When efficiency is the primary design consideration, best results are achieved when using an inductor that results in continuous conduction mode (CCM) operation and achieves very small inductor ripple current.

Output Capacitor Selection

REG2 was designed to operate with output capacitors ranging from 0.47µF to 10µF, providing design flexibility. A 1µF output capacitor is suitable for most applications, although larger output capacitors may be used to minimize output voltage ripple, if needed. Ceramic capacitors are recommended for most applications.

Rectifier Selection

REG2 requires a Schottky diode to rectify the inductor current. Select a low forward voltage drop Schottky diode with a forward current (I_F) rating that is sufficient to support the maximum switch current and a sufficient peak repetitive reverse voltage (V_{RRM}) to support the output voltage.

Setting the LED Bias Current

The LED bias current is set by a resistor connected from FB2 and ground, and the regulator is satisfied when the LED current is sufficient to generate 250mV across this resistor. Once the bias current is programmed, the LED current can be

adjusted using the ACT8740's Direct-PWM feature. REG2 is also compatible with a variety of well-known LED dimming circuits, such as with a DC control voltage and a filtered PWM signal.

PCB Layout Considerations

High switching frequencies and large peak currents make PC board layout a very important part of the design. Good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Step-up DC/DCs exhibit continuous input current, so there is some amount of flexibility in placing vias in the input capacitor circuit. The inductor, input filter capacitor, rectifier, and output filter capacitor should be connected as close together as possible, with short, direct, and wide traces. Connect the ground nodes together in a star configuration, with a direct connection to the exposed pad. Finally, the exposed pad should be directly connected to the backside ground plane using multiple vias to achieve low electrical and thermal resistance. Note that since the LED string is a low, DC-current path, it does not generally require special layout consideration.

ELECTRICAL CHARACTERISTICS

(V_{INL} = 3.6V, C_{OUT3} = 1μF, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INL Operating Voltage Range		3.1		5.5	V
INL UVLO Threshold	V_{INL} Input Rising	2.9	3	3.1	V
UVLO Hysteresis	V_{INL} Input Falling		0.1		V
Output Voltage Accuracy	T_A = 25°C	-1.2	V_{NOM3}①	+2	%
	T_A = -40°C to 85°C	-2.5	V_{NOM3}	+3	
Line Regulation Error	V_{INL} = Max(V_{OUT3} + 0.5V, 3.6V) to 5.5V		0		mV
Load Regulation Error	I_{OUT3} = 1mA to 350mA		-0.004		%/mA
Power Supply Rejection Ratio	f = 1kHz, I_{OUT3} = 350mA, C_{OUT3} = 1μF		70		dB
	f = 10kHz, I_{OUT3} = 350mA, C_{OUT3} = 1μF		60		
Supply Current per Output	Regulator Enabled		40		μA
	Regulator Disabled		0		
Dropout Voltage②	I_{OUT3} = 160mA, V_{OUT3} > 3.1V		100	200	mV
Output Current				350	mA
Current Limit③	V_{OUT3} = 95% of regulation voltage	400			
Internal Soft-Start			100		μs
Power Good Flag High Threshold	V_{OUT3}, hysteresis = -4%		89		%
Output Noise	C_{OUT3} = 10μF, f = 10Hz to 100kHz		40		μV_{RMS}
Stable C_{OUT3} Range		1		20	μF
Discharge Resistor in Shutdown	LDO Disabled, DIS3[ ] = [1]		650		Ω

①: V_{NOM3} refers to the nominal output voltage level for V_{OUT3} as defined by the *Ordering Information* section.

②: Dropout Voltage is defined as the differential voltage between input and output when the output voltage drops 100mV below the regulation voltage at 1V differential voltage.

③: LDO current limit is defined as the output current at which the output voltage drops to 95% of the respective regulation voltage. Under heavy overload conditions the output current limit folds back by 30% (typ)

ELECTRICAL CHARACTERISTICS

(V_{INL} = 3.6V, C_{OUT4} = 1µF, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INL Operating Voltage Range		3.1		5.5	V
INL UVLO Threshold	V_{INL} Input Rising	2.9	3	3.1	V
UVLO Hysteresis	V_{INL} Input Falling		0.1		V
Output Voltage Accuracy	T_A = 25°C	-1.2	V_{NOM4}①	+2	%
	T_A = -40°C to 85°C	-2.5	V_{NOM4}	+3	
Line Regulation Error	V_{INL} = Max(V_{OUT4} + 0.5V, 3.6V) to 5.5V		0		mV
Load Regulation Error	I_{OUT4} = 1mA to 250mA		-0.004		%/mA
Power Supply Rejection Ratio	f = 1kHz, I_{OUT4} = 250mA, C_{OUT4} = 1µF		70		dB
	f = 10kHz, I_{OUT4} = 250mA, C_{OUT4} = 1µF		60		
Supply Current per Output	Regulator Enabled		40		µA
	Regulator Disabled		0		
Dropout Voltage②	I_{OUT4} = 120mA, V_{OUT4} > 3.1V		100	200	mV
Output Current				250	mA
Current Limit③	V_{OUT4} = 95% of regulation voltage	280			mA
Internal Soft-Start			100		µs
Power Good Flag High Threshold	V_{OUT4}, hysteresis = -4%		89		%
Output Noise	C_{OUT4} = 10µF, f = 10Hz to 100kHz		40		μV_{RMS}
Stable C_{OUT4} Range		1		20	µF
Discharge Resistor in Shutdown	LDO Disabled, DIS4[ ] = [1]		650		Ω

①: V_{NOM4} refers to the nominal output voltage level for V_{OUT4} as defined by the *Ordering Information* section.

②: Dropout Voltage is defined as the differential voltage between input and output when the output voltage drops 100mV below the regulation voltage at 1V differential voltage.

③: LDO current limit is defined as the output current at which the output voltage drops to 95% of the respective regulation voltage. Under heavy overload conditions the output current limit folds back by 30% (typ)

ELECTRICAL CHARACTERISTICS

(V_{INL} = 3.6V, C_{OUT5} = 1µF, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INL Operating Voltage Range		3.1		5.5	V
INL UVLO Threshold	V_{INL} Input Rising	2.9	3	3.1	V
UVLO Hysteresis	V_{INL} Input Falling		0.1		V
Output Voltage Accuracy	T_A = 25°C	-1.2	V_{NOM5}①	+2	%
	T_A = -40°C to 85°C	-2.5	V_{NOM5}	+3	
Line Regulation Error	V_{INL} = Max(V_{OUT5} + 0.5V, 3.6V) to 5.5V		0		mV
Load Regulation Error	I_{OUT5} = 1mA to 250mA		-0.004		%/mA
Power Supply Rejection Ratio	f = 1kHz, I_{OUT5} = 250mA, C_{OUT5} = 1µF		70		dB
	f = 10kHz, I_{OUT5} = 250mA, C_{OUT5} = 1µF		60		
Supply Current per Output	Regulator Enabled		40		µA
	Regulator Disabled		0		
Dropout Voltage②	I_{OUT5} = 120mA, V_{OUT5} > 3.1V		100	200	mV
Output Current				250	mA
Current Limit③	V_{OUT5} = 95% of regulation voltage	280			mA
Internal Soft-Start			100		µs
Power Good Flag High Threshold	V_{OUT5}, hysteresis = -4%		89		%
Output Noise	C_{OUT5} = 10µF, f = 10Hz to 100kHz		40		μV_{RMS}
Stable C_{OUT5} Range		1		20	µF
Discharge Resistor in Shutdown	LDO Disabled, DIS5[ ] = [1]		650		Ω

①: V_{NOM5} refers to the nominal output voltage level for V_{OUT5} as defined by the *Ordering Information* section.

②: Dropout Voltage is defined as the differential voltage between input and output when the output voltage drops 100mV below the regulation voltage at 1V differential voltage.

③: LDO current limit is defined as the output current at which the output voltage drops to 95% of the respective regulation voltage. Under heavy overload conditions the output current limit folds back by 30% (typ)

REGISTER DESCRIPTIONS

Note: See Table 1 for default register settings.

Table 8:

CFG Control Register Map

ADDRESS	DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
40h	R	R	ON3	VSET3				
41h	R	R	ON4	VSET4				
42h	R	R	ON5	VSET5				
43h	OK5	OK4	OK3	DIS5	DIS4	DIS3	W/E	R

R: Read-Only bits. Default Values May Vary.

W/E: Write-Exact bits. Read/Write bits which must be written exactly as specified in Table 1.

Table 9:

REG345 Control Register Bit Descriptions

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION	
40h	VSET3	[4:0]	R/W	REG3 Output Voltage Selection	See Table 10	
40h	ON3	[5]	R/W	REG3 Enable	0	REG3 Disable
					1	REG3 Enable
40h		[7:6]	R		READ ONLY	
41h	VSET4	[4:0]	R/W	REG4 Output Voltage Selection	See Table 10	
41h	ON4	[5]	R/W	REG4 Enable	0	REG4 Disable
					1	REG4 Enable
41h		[7:6]	R		READ ONLY	
42h	VSET5	[4:0]	R/W	REG5 Output Voltage Selection	See Table 10	
42h	ON5	[5]	R/W	REG5 Enable	0	REG5 Disable
					1	REG5 Enable
42h		[7:6]	R		READ ONLY	
43h		[0]	R		READ ONLY	
43h		[1]	W/E		WRITE-EXACT	
43h	DIS3	[2]	R/W	REG3 Discharge Enable	0	Discharge Disable
					1	Discharge Enable
43h	DIS4	[3]	R/W	REG4 Discharge Enable	0	Discharge Disable
					1	Discharge Enable

REGISTER DESCRIPTIONS CONT'D

Table 9:
Control Register Bit Descriptions (Cont'd)

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION	
43h	DIS5	[4]	R/W	REG5 Discharge Enable	0	Discharge Disable
					1	Discharge Enable
43h	OK3	[5]	R	REG3 Power-OK	0	Output is not OK
					1	Output is OK
43h	OK4	[6]	R	REG4 Power-OK	0	Output is not OK
					1	Output is OK
43h	OK5	[7]	R	REG5 Power-OK	0	Output is not OK
					1	Output is OK

Table 10:

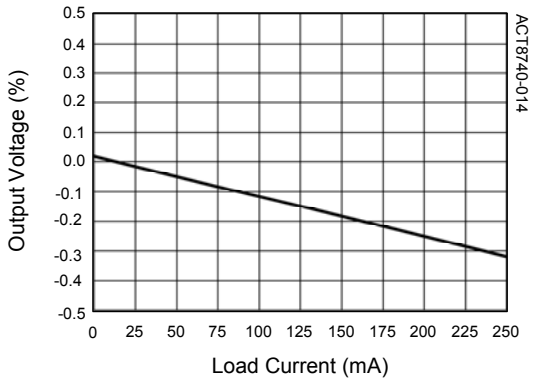
REG345CFG/VSETx[ ] Output Voltage Setting

REG345CFG/VSETx[2:0]	REG345CFG/VSETx[4:3]			
	00	**01**	**10**	**11**
000	1.4	2.15	2.55	3.0
001	1.5	2.20	2.60	3.1
010	1.6	2.25	2.65	3.2
011	1.7	2.30	2.70	3.3
100	1.8	2.35	2.75	3.4
101	1.9	2.40	2.80	3.5
110	2.0	2.45	2.85	3.6
111	2.1	2.50	2.90	3.7

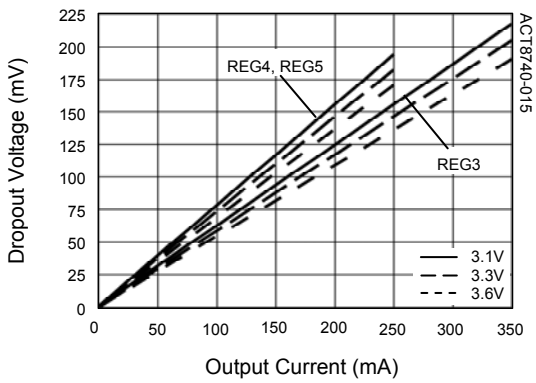
TYPICAL PERFORMANCE CHARACTERISTICS

(ACT8740QLEGA, V_{VIN} = 5V, T_A = 25°C, unless otherwise specified.)

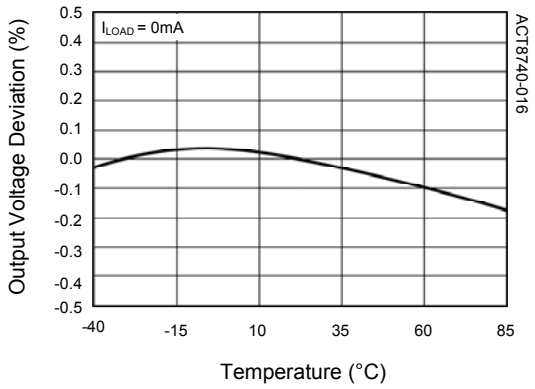
Load Regulation



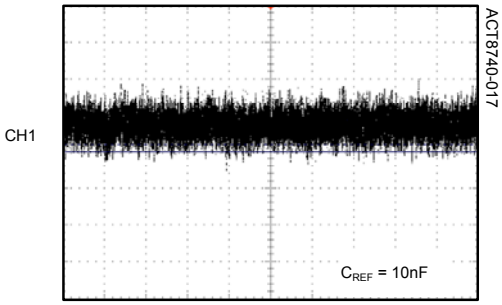
Dropout Voltage vs. Output Current



Output Voltage Deviation vs. Temperature

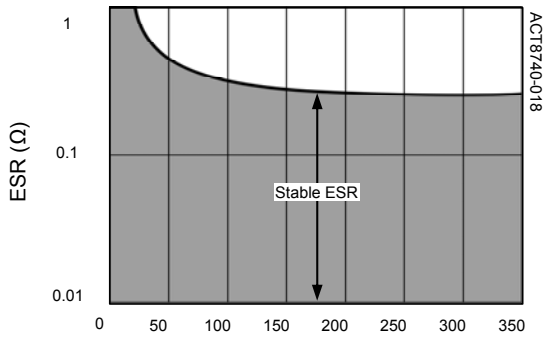


LDO Output Voltage Noise



CH1: V_{OUTx}, 200µV/div (AC COUPLED)
TIME: 200ms/div

Region of Stable C_{OUT} ESR vs. Output Current



FUNCTIONAL DESCRIPTION

General Description

REG3, REG4, and REG5 are low-noise, low-dropout linear regulators (LDOs) that are optimized for low-noise and high-PSRR operation, achieving more than 60dB PSRR at frequencies up to 10kHz.

LDO Output Voltage Programming

All LDOs feature independently-programmable output voltages that are set via the I^{2}C serial interface, increasing the ACT8740's flexibility while reducing total solution size and cost. Set the output voltage by writing to the REG345CFG/VSETx[ ] registers.

Output Current Capability

REG3, REG4, and REG5 each supply 250mA of load current. Excellent performance is achieved over each regulator's entire load current ranges.

Output Current Limit

In order to ensure safe operation under over-load conditions, each LDO features current-limit circuitry with current fold-back. The current-limit circuitry limits the current that can be drawn from the output, providing protection in over-load conditions. For additional protection under extreme over current conditions, current-fold-back protection reduces the current-limit by approximately 30% under extreme overload conditions.

Enabling and Disabling the LDOs

All LDOs feature independent enable/disable control via the I^{2}C serial interface. Independently enable or disable each output by writing to the appropriate REG345CFG/ONx[ ] bit.

Power-OK

Each of the LDOs features Power-OK status bit that can be read by the system microprocessor via the I^{2}C interface. If an output voltage is lower than the power-OK threshold, typically 6% below the programmed regulation voltage, the corresponding REG345CFG/OKx[ ] will clear to 0.

Reference Bypass Pin

The ACT8740 contains a reference bypass pin which filters noise from the reference, providing a low-noise voltage reference to the LDOs. Bypass REF to G with a 0.01µF ceramic capacitor.

Optional LDO Output Discharge

Each of the ACT8740's LDOs features an optional, independent output voltage discharge feature. When this feature is enabled, the LDO output is discharged to ground through a 1kΩ resistance when the LDO is shutdown. This feature may be enabled or disabled via the I^{2}C interface by writing to the REG345CFG/DISx[ ] bits.

Output Capacitor Selection

REG3, REG4, and REG5 each require only a small ceramic capacitor for stability. For best performance, each output capacitor should be connected directly between the OUTx and G pins as possible, with a short and direct connection. To ensure best performance for the device, the output capacitor should have a minimum capacitance of 1µF, and ESR value between 10mΩ and 200mΩ. High quality ceramic capacitors such as X7R and X5R dielectric types are strongly recommended.

PCB Layout Considerations

The ACT8740's LDOs provide good DC, AC, and noise performance over a wide range of operating conditions, and are relatively insensitive to layout considerations. When designing a PCB, however, careful layout is necessary to prevent other circuitry from degrading LDO performance.

A good design places input and output capacitors as close to the LDO inputs and output as possible, and utilizes a star-ground configuration for all regulators to prevent noise-coupling through ground. Output traces should be routed to avoid close proximity to noisy nodes, particularly the SW nodes of the DC/DCs.

REFBP is a filtered reference noise, and internally has a direct connection to the linear regulator controller. Any noise injected onto REFBP will directly affect the outputs of the linear regulators, and therefore special care should be taken to ensure that no noise is injected to the outputs via REFBP. As with the LDO output capacitors, the REFBP bypass capacitor should be placed as close to the IC as possible, with short, direct connections to the star-ground. Avoid the use of vias whenever possible. Noisy nodes, such as from the DC/DCs, should be routed as far away from REFBP as possible.

ELECTRICAL CHARACTERISTICS

(V_{VIN} = 5V, V_{BAT} = 3.6V, ISET1[ ] = [0000], T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN Operating Voltage Range		4.3		6	V
VIN UVLO Threshold	VIN Voltage Rising	3.75	4	4.25	V
VIN UVLO Hysteresis	VIN Voltage Falling		500		mV
On-Resistance			300	500	mΩ
Battery Termination Voltage	T_A = 25°C	4.179	4.200	4.221	V
	V_{VIN} = 4.5V to 5.5V, T_A = 0°C to 85°C	4.158	4.200	4.242	V
Line Regulation	V_{VIN} = 4.5V to 5.5V, I_{BAT} = 10mA		0.2		%/V
Load Regulation	I_{BAT} = 50mA to 500mA		0.001		%/mA
Charge Current	V_{BAT} = 4V, CHGLEV = GA		90	100	mA
	V_{BAT} = 4V, CHGLEV = VSYS	400	450	500	mA
Precondition Charge Current	V_{BAT} = 2.7V, CHGLEV = GA or VSYS	30	45	60	mA
Precondition Threshold Voltage	V_{BAT} Voltage Rising	2.75	2.9	3.05	V
Precondition Threshold Hysteresis	V_{BAT} Voltage Falling		150		mV
End-of-Charge Current Threshold	V_{BAT} = 4.2V, CHGLEV = VSYS	20	38	56	mA
End-of-Charge Delay			4		min
Charge Restart Threshold	VSET[ ] - V_{BAT}, V_{BAT} Falling		200		mV
Thermal Regulation Threshold			110		°C
BAT Reverse Leakage Current	V_{BAT} = 4.2V, VIN = GA or BAT		0.4	2	µA
VIN Supply Current	V_{VIN} < UVLO Voltage		50		µA
	SLEEP, SUSPEND or TIMEOUT-FAULT state		200		µA
	PRECONDITION, FAST-CHARGE, or TOP-OFF state		700		µA
Precondition Timeout Period	TIMOSET[ ] = [10]		90		min
Total Timeout Period	TIMOSET[ ] = [10]		4		hr
CHGLEV Logic High Input Voltage	I_{CHGLEV} ≥ 15µA	1.4			V
CHGLEV Tri-state Current Threshold①		-2		2	µA
CHGLEV Logic Low Input Voltage	I_{CHGLEV} ≤ -15µA			0.4	V

①: Charger is suspended when CHGLEV pin current is within this range

REGISTER DESCRIPTIONS

Note: See Table 1 for default register settings.

Table 11:

Battery Charger (CHGR) Control Register Map

ADDRESS	DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
08h	ISET1				R	R	R	R
09h	TIMOSET		R	BATFLT	TIMOFLT	TEMPFLT	CHGSTAT	VINPOK
0Ah	LDOMODE	ISET2			R	R	R	R
0Bh	R	R	R	R	W/E	ICHGSET	CHGROK	SUSCHG

R: Read-Only bits. Default Values May Vary.

W/E: Write-Exact bits. Read/Write bits which must be written exactly as specified in Table 1.

Table 12:

Battery Charger (CHGR) Control Register Bit Descriptions

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION	
08h		[3:0]	R		READ ONLY	
08h	ISET1	[7:4]	R/W	ISET1 Charge Current Selection	See Table 13	
09h	VINPOK	[0]	R	Input Supply Power-OK	0	Input Power is not OK
					1	Input Power is OK
09h	CHGSTAT	[1]	R	Charging Status	0	Not Charging
					1	Charging
09h	TEMPFLT	[2]	R	Temperature Status	0	No Temperature Fault
					1	Temperature Fault
09h	TIMOFLT	[3]	R	Timeout Fault	0	No Timeout Fault
					1	Timeout Fault
09h	BATFLT	[4]	R	Battery Removed Fault	0	Battery Not Removed
					1	Battery Removed
09h		[5]	R		READ ONLY	
09h	TIMOSET	[7:6]	R/W	Charge Timeout Select	00	60 mins
					01	90 mins
					10	120 mins
					11	No Timeout
0Ah		[3:0]	R		READ ONLY	
0Ah	ISET2	[6:4]	R/W	ISET2 Charger Current Selection	See Table 14	

REGISTER DESCRIPTIONS CONT'D

Table 12:

Battery Charger (CHGR) Control Register Bit Descriptions (Cont'd)

ADDRESS	NAME	BIT	ACCESS	FUNCTION	DESCRIPTION	
0Ah	LDOMODE	[7]	R/W	LDO Mode Enable	0	Charger in Normal Mode
					1	Charger in LDO Mode
0Bh	SUSCHG	[0]	R/W	Suspend Charging	0	Charging Enable
					1	Charging Disable
0Bh	CHGROK	[1]	R	Charge Status	0	Charging Error Occurred
					1	Charging OK
0Bh	ICHGSET	[2]	R/W	USB Charge Current Selection	0	90mA
					1	450mA
0Bh		[3]	W/E		WRITE-EXACT	
0Bh		[7:4]	R		READ ONLY	

Table 13:

ISET1[ ] Charge Current Setting

CHGR/ISET1 [3:0]	FAST CHARGE CURRENT SETTING (mA)	
0000	CHGLEV = 1	450
	CHGLEV = 0	90
0001	300	
0010	350	
0011	400	
0100	450	
0101	500	
0110	550	
0111	600	
1000	650	
1001	700	
1010	750	
1011	800	
1100	850	
1101	900	
1110	950	
1111	1000	

Table 14:

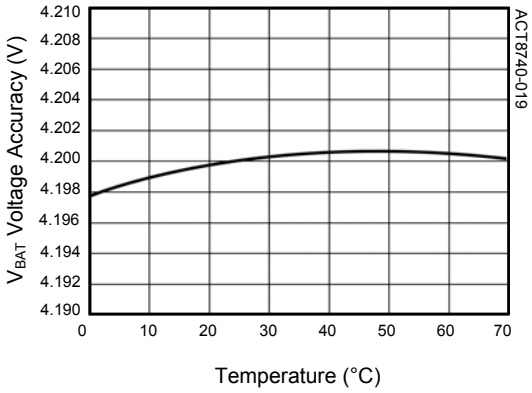
ISET2[ ] Charge Current Setting

CHGR/ISET2[2:0]	ISET2 CURRENT SETTING (mA)
000	300
001	400
010	500
011	600
100	700
101	800
110	900
111	1000

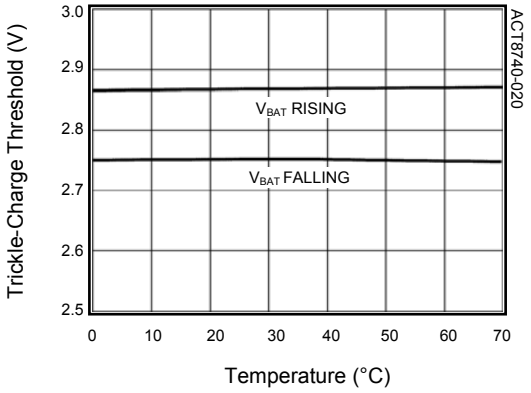
TYPICAL PERFORMANCE CHARACTERISTICS

(ACT8740QLEGA, V_{VIN} = 5V, T_A = 25°C, unless otherwise specified.)

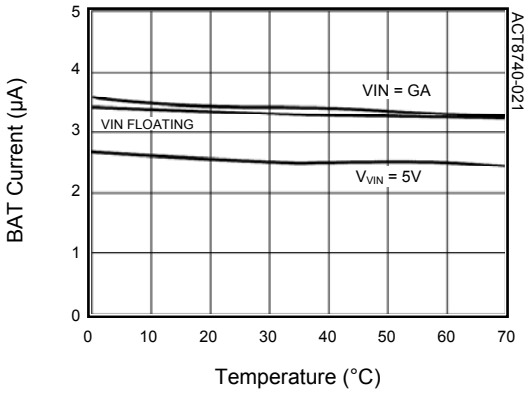
Charge Termination Voltage



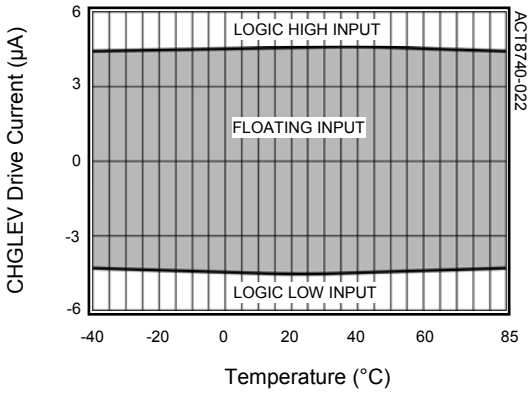
Trickle-Charge Threshold



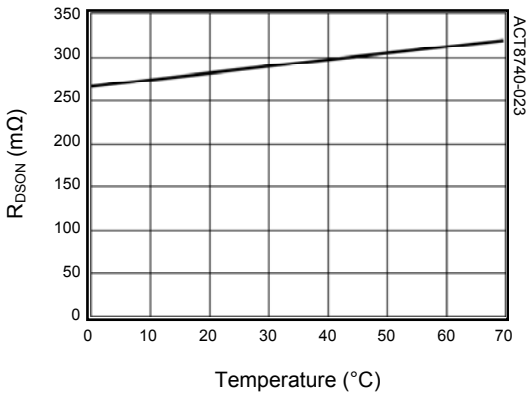
SUSPEND Mode Battery Current



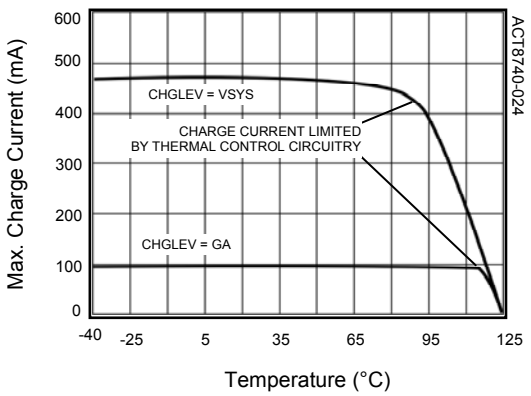
CHGLEV Drive Current Threshold



MOSFET Resistance



Maximum Charge Current



FUNCTIONAL DESCRIPTION

General Description

The ACT8740's internal battery charger is a full-featured, intelligent, linear-mode, single-cell charger for Lithium-based cells. This charger provides a complete selection of advanced functions and requires minimum system design effort.

The core of the charger is a CC/CV (Constant- Current/Constant-Voltage), linear-mode charge controller with a highly-accurate charge termination threshold. This controller incorporates current and voltage sense circuitry, an internal power MOSFET, a full-featured state-machine that implements charge control and safety features, and circuitry that eliminates the reverse-blocking diode required by conventional charger designs. The ACT8740's charger also features thermal-regulation circuitry that protects it against excessive junction temperature, allowing the fastest possible charging times, as well as proprietary input protection circuitry that makes the charger robust against input voltage transients that can damage other chargers.

CC/CV Regulation Loop

At the core of the ACT8740's battery charger is a CC/CV regulation loop, which regulates either current or voltage as necessary to ensure fast and safe charging of the battery. In a normal charge cycle, this loop regulates the charge current to the programmed charge current level and continues charging at this current until the battery cell voltage reaches the charge termination voltage. Once the cell reaches the Charge-Termination Threshold Voltage, the CV loop takes over and charge current is allowed to decrease as necessary to keep the cell voltage at the charge termination voltage.

Charger Enable/Disable

When a valid input voltage is applied to VIN, the battery charger is automatically enabled in order to simplify system design and eliminate the need for external input supply detection circuitry.

Once the charger is enabled, a charge cycle automatically begins unless CHGLEV is floating, CHGR/SUSCHG[ ] is set to [1], or a fault condition has occurred.

Charger Status

During normal operation, the processor can read the status of the input supply by reading CHGR/VINPOK[ ], which is set to [1] when the following conditions are true:

1) The voltage at VIN is greater than the voltage at BAT, and
2) The voltage at VIN is greater than the VIN UVLO threshold.

Alternatively, the processor can read the status of the charger by reading the CHGR/CHGROK[ ] bit, which is set to [1] when the following conditions are true:

1) The voltage at VIN is greater than the voltage at BAT, and
2) The voltage at VIN is greater than the VIN UVLO threshold, and
3) No fault has occurred.

Finally, the status of a charge cycle can be determine by reading the CHGR/CHGSTAT[ ] bit or by evaluating the state of the nSTAT output. nSTAT is an open-drain output that has an internal 8mA current limit, and is capable of directly driving LEDs for a visual charge-status indication without the need of current-limiting resistors or other external circuitry. To drive an LED, simply connect the LED between an appropriate supply, typically VIN, and nSTAT. When a logic-level charge status indicator is desired, simply connect a pull-up resistor of 10kΩ or more from nSTAT to OUT2 or another suitable supply.

CHGR/CHGSTAT[ ] is set to [1] and nSTAT sinks current when any of the following conditions are true:

1) The charger is operating in the PRECONDITION state, or
2) The charger is operating in the FAST-CHARGE state, or
3) The charger is operating in the TOP-OFF state.

When none of these conditions are true, CHGR/CHGSTAT[ ] is cleared to [0] and nSTAT goes into a high-Z state.

FUNCTIONAL DESCRIPTION CONT'D

Input Capacitor Selection

VIN is the power input pin for the ACT8740 battery charger. The battery charger is automatically enabled whenever a valid voltage is present on VIN. In most applications, VIN is connected to either a wall adapter or a USB port. Under normal operation, the input of the charger will often be "hot-plugged" directly to a powered USB or a wall adapter cable, and supply voltage ringing and overshoot may appear at the VIN pin and can potentially be large enough to damage the charger input. In most applications, a capacitor connected from VIN to GA, placed as close as possible to the IC, is sufficient to absorb the energy. The VIN pin is designed for enhanced robustness and has an absolute maximum transient voltage rating of +7V, and attention must be given to bypass techniques to ensure operation within this limit.

Charge Current Programming

The charger was designed for maximum flexibility, and charge current programming is performed using the CHGR/ISET1[ ] and CHGR/ISET2[ ] registers and (optionally) the multifunction CHGLEV input. For applications that desire a combination of pin-control and I^2C control, the CHGLEV input provides charge current selection between the current settings defined by CHGR/ISET1[ ] and CHGR/ISET2[ ]. Alternatively, when complete I^2C control is desired, simply connect CHGLEV to G and utilize the CHGR/ICHGSET[ ] bit. The two methods are functionally equivalent, select the charge current programmed by CHGR/ISET1[ ] by driving CHGLEV to a logic low or by clearing CHGR/ICHGSET[ ] to [0], and select the charge current programmed by CHGR/ISET2[ ] by driving CHGLEV to a logic high or by setting CHGR/ICHGSET[ ] to [1].

The charger's default settings of CHGR/ISET1[ ] =[0000] and CHGR/ISET2[ ]=[0000] ensure compatibility with lower-current input supplies, such as USB ports. In the default configuration, drive CHGLEV to a logic-low for a 90mA charge current, and drive CHGLEV to a logic-high for 450mA charge current. If different charge current settings are desired, the charge current associated with either CHGLEV state is easily modified via the I^2C serial interface. For example, in order to maintain compatibility with USB's high-current mode as well as charge at a higher current if an AC adapter is available, simply reprogram CHGR/ISET1[ ] to select the desired charge current, then select this charge current by driving CHGLEV to a logic low or clear CHGR/ICHGSET[ ] to [0].

Charge Safety Timer

The ACT8740 features a programmable charge safety timer that is utilized during operation in the PRECONDITION state. The safety timer has a default timeout period of 60 minutes, although it may be programmed to either 90 minutes or 120 minutes by writing to the CHGR/TIMOSET[ ] register. This register also provides a timer-disable function, for applications that do not require a charge safety timer function.

Thermal Regulation

The ACT8740 features an internal thermal feedback loop that reduces the charging current as necessary to ensure that the die temperature does not exceed the thermal regulation threshold of 110°C. This feature protects the ACT8740 against excessive junction temperature and makes the ACT8740 more accommodating of aggressive thermal designs without risk of damage. Note, however, that attention to good thermal design is required to achieve the shortest possible charge time.

Reverse Leakage Current

The ACT8740 includes internal circuitry that eliminates the need for series blocking diodes, reducing solution size and cost as well as dropout voltage relative to conventional battery chargers. When the input supply is removed, when V_{VIN} goes below its under-voltage-lockout (UVLO) voltage, or when V_{VIN} drops below V_{BAT}, the ACT8740 automatically goes into SUSPEND mode and reconfigures its power switch to minimize current drain from the battery.

Charger State Machine

PRECONDITION State

A new charging cycle begins in the PRECONDITION state. In this state, the cell is charged at a reduced current of either 45mA or 10% of the selected maximum fast-charge current, whichever is greater. During a normal charge cycle, charging continues at this rate until V_{BAT} reaches the Precondition Threshold Voltage, at which point the state machine jumps to the FAST-CHARGE state. If V_{BAT}

FUNCTIONAL DESCRIPTION CONT'D

does not reach the Precondition Threshold Voltage before the Precondition Charge Timeout period expires, then a damaged cell is detected and the state machine jumps to the TIMEOUT-FAULT state.

FAST-CHARGE State

In the FAST-CHARGE state the charger operates in Constant-Current (CC) mode and charges the cell at the programmed charge current. During a normal charge cycle, constant-current charging continues until V_{BAT} reaches the charge termination voltage, at which point the state machine jumps to the TOP-OFF state.

TOP-OFF State

In the TOP-OFF state the cell is charged in Constant-Voltage (CV) mode with the charge current limited by the internal chemistry of the cell, decreasing as the cell charges. A normal charging cycle continues until the charge current decreases to below the End-Of-Charge (EOC) threshold. In order to improve immunity to conditions that can result in false-EOC detection, the charging continues until the EOC condition persists for 4 consecutive minutes. Once this condition is met, the charge cycle is terminated and the state machine jumps to the SLEEP state.

SLEEP State

In the SLEEP state the ACT8740 presents a high-impedance to the battery, allowing the cell to "relax" and minimizing battery leakage current. The ACT8740 continues to monitor the cell voltage, however, so that it can reinitiate a charging cycle as necessary to ensure that the cell remains fully charged.

Charge Restart

After a charge cycle successfully terminates, the ACT8740 jumps to its SLEEP state to minimize battery drain, but continues to actively monitor the cell voltage. A new charging cycle begins when the cell voltage has dropped by 200mV (typ), keeping the cell fully charged. This charge restart process minimizes cycle-life degradation of the cell by allowing it to "relax" between charges, while ensuring that the cell remains fully-charged while connected to a power source.

SUSPEND State

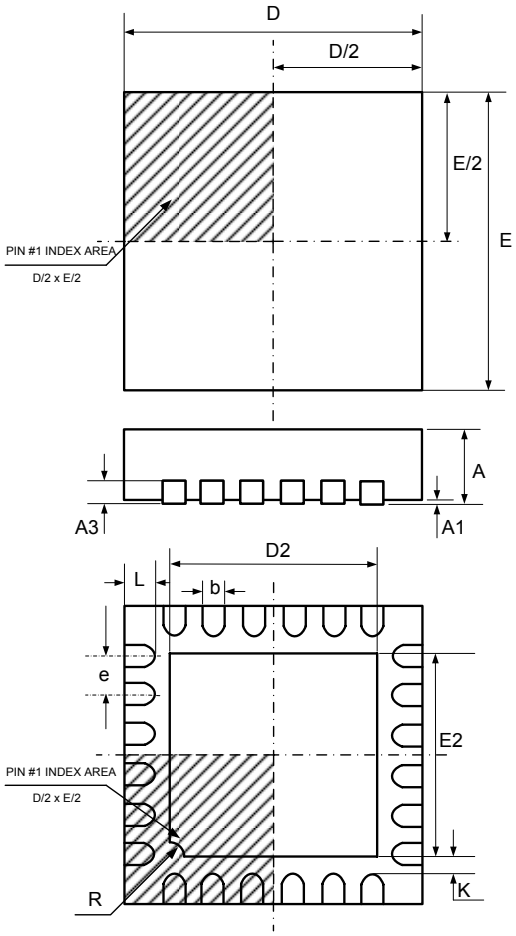
When in the SUSPEND state, the charger is disabled and the charger presents a high-impedance to the battery, but the charge-control circuitry remains functional. When exiting the SUSPEND state, the charge timer is reset and the state machine jumps to the PRECONDITION state.

TIMEOUT-FAULT State

When a TIMEOUT-FAULT occurs, charging is suspended, CHGR/TIMOFLT[ ] is set to [1], and the charger presents a high-impedance to the battery. To maximize safety, there is no direct path to resume charging from the TIMEOUT-FAULT state. A new charging cycle may only be initiated if the state machine first jumps to the SUSPEND state then each of the conditions necessary to enter the PRECONDITION state are satisfied.

PACKAGE OUTLINE

TQFN44-24 PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.200 REF		0.008 REF	
b	0.180	0.300	0.007	0.012
D	3.850	4.150	0.152	0.163
E	3.850	4.150	0.152	0.163
D2	2.500	2.800	0.098	0.110
E2	2.500	2.800	0.098	0.110
e	0.500 BSC		0.020 BSC	
L	0.350	0.450	0.014	0.018
R	0.200 TYP		0.008 TYP	
K	0.200	---	0.008	---

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