Li+ Battery Charger with Thermal Regulation

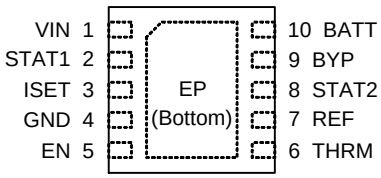
Features

- **Programmable Charge Current Up to 1A**
- **Charge Status Output Pins**
- **Soft-Start Limits Inrush Current**
- **4.2V Charge Voltage with ±1% Accuracy**
- **Fixed 55mA Prequal Charge Current**
- **Thermal Limiting Simplifies Board Design**
- **External Thermistor Monitor**
- **Enable/Disable Control**
- **3mm x 3mm DFN-10 Package (DFN3x3-10)**
- **Disable Charging When V_{IN} > 6.4V**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **PDAs**
- **MP3 Players**
- **Cell Phones**
- **Wireless Appliances**

Pin Configuration



DFN3x3-10
(Top View)

Note : EP should be connected to GND plane for better heat dissipation

General Description

The APL3201 is a constant-current/constant-voltage linear charger for single cell Li+ batteries.

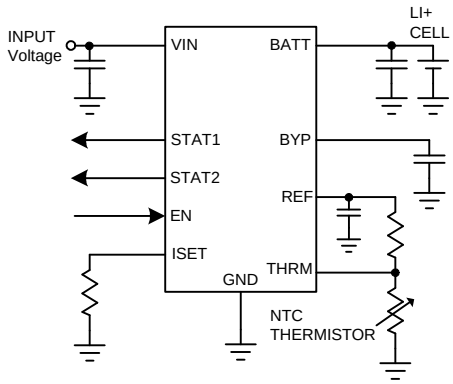
The APL3201 needs no external MOSFET or diodes, and accepts input voltage up to 6.0V. The small packages and low external component count make the APL3201 ideally suited for portable applications.

On-chip thermal limiting simplifies PC board layout and allows optimum charging rate without the thermal limits imposed by worst-case battery and input voltage. When the APL3201 thermal limit is reached, the charger does not shut down but simply reduces charging current. Ambient or battery temperature can be monitored with an external thermistor. When the temperature is out of range, charging pauses.

Other features include the STAT1 and 2 outputs to indicate four charge states, and the EN input, switches the APL3201 on or off.

The APL3201 is available in 3mmx3mm DFN-10 package, and operates over the -40°C to +85°C temperature range.

Simplified Application Circuit



Ordering and Marking Information

APL3201 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QA : DFN3x3-10 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APL3201 QA: APL 3201 XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN to GND	-0.3 to 7	V
V_{EN}, V_{BATT}, V_{THRM}	EN, STAT1, STAT2, BATT, THRM to GND	-0.3 to 7	V
I_{CHG}	Charging Current	1.2	A
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to 150	°C
T_L	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction To Air Thermal Resistance (Note 2) DFN3x3-10	50	°C/W

Note 2 : θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of DFN-10 is soldered directly on the PCB.

Recommended Operating Conditions

Symbol	Parameter	Range	Unit
V_{IN}	VIN To GND	4.35 to 6.0	V
I_{CHG}	Charging Current	0.1 to 1	A
T_J	Junction Temperature	-40 to 125	°C
T_A	Ambient Temperature	-40 to 85	°C

Electrical Characteristics

Refer to the typical application circuit. These specifications apply over V_{IN}=5V, V_{BATT}=4.2V, V_{THRM}=V_{REF}/2, T_J= -40~125°C, T_A= -40~85°C, unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APL3201			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
I_{IN}	VIN Supply Current	V_{EN} = 0V	-	0.6	1.2	mA
		V_{EN} = 5V, I_{CHG}=0A	-	2	4	mA
UNDER-VOLTAGE-LOCKOUT						
	VIN UVLO Threshold	V_{IN} Rising	3.90	4.05	4.2	V
	VIN UVLO Hysteresis		0.15	0.25	0.35	V
BATTERY VOLTAGE AND REFERENCE VOLTAGE						
V_{BATT}	BATT Regulation Voltage		-	4.20	-	V
	BATT Regulation Voltage Accuracy	T_A=25°C, V_{IN}=4.35~6.0V	-0.5	-	0.5	%
		T_A =-40~85°C (T_J=-40~125°C)	-1	-	1	%
	BATT Prequel Voltage Threshold		2.8	3	3.2	V
	Prequel Threshold Hysteresis		-	70	-	mV
V_{REF}	REF Regulation Voltage		-	3	-	V
	REF Voltage Accuracy	I_{REF}=0~500µA, T_J=-40~125°C, V_{IN}=4.35V~6.0V	-2	-	2	%
	REF Maximum Output Current	REF=GND	-	1.5	-	mA
BATTERY CHARGING AND PRECHARGING CURRENT						
I_{CHG}	Charging Current Range	I_{CHG}=K_{SET} x V_{SET} / R_{SET}, Without thermal regulation	100	-	1000	mA
V_{SET}	ISET Regulation Voltage	Without thermal regulation	-	1	-	V
	ISET Regulation Voltage Accuracy	T_J=-40~125°C, V_{IN}=4.35~6.0V	-1	-	1	%
	Maximum ISET Output Current	ISET=GND	-	1.8	-	mA
K_{SET}	Charging Current Set Factor	0.1A≤I_{CHG}≤1A	940	1000	1060	-
	Prequel Charging Current	V_{BATT}<2.8V	35	55	70	mA
	Charge-Done Current Threshold	% of charger current set at ISET	8	12.5	19	%
		Hysteresis	-	12.5	-	%
DROPOUT VOLTAGES						
	VIN to BATT Dropout Voltage	I_{CHG}=1A, V_{IN}=5V	-	250	450	mV
	VIN to BYP Dropout Voltage	I_{BYP}=5mA, V_{IN}=5V	-	300	-	mV
THERMISTER MONITOR AND DIE TEMPERATURE REGULATION						
	THRM Cold Trip Level	V_{THRM} Rising	0.79	0.81	0.82	V_{REF}
	THRM Cold Trip Level Hysteresis		-	0.03	-	V_{REF}
	THRM Hot Trip Level	V_{THRM} Falling	0.28	0.29	0.30	V_{REF}
	THRM Hot Trip Level Hysteresis		-	0.03	-	V_{REF}
	Die Thermal Regulation Limit		-	120	-	°C
	THRM Disable Voltage Threshold		50	100	150	mV

Electrical Characteristics (Cont.)

Refer to the typical application circuit. These specifications apply over V_{IN}=5V, V_{BATT}=4.2V, V_{THRM}=V_{REF}/2, T_J= -40~125 °C, T_A= -40~85°C, unless otherwise specified. Typical values are at T_A=25°C.

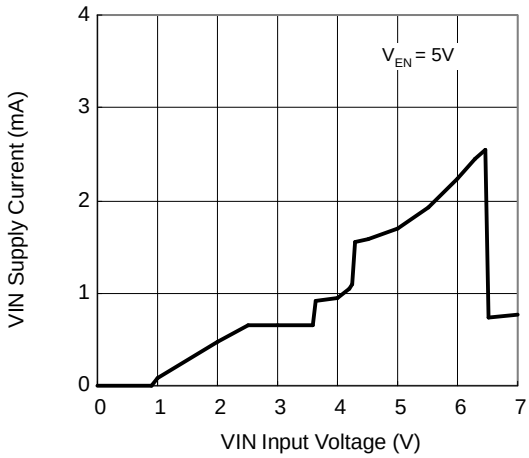
Symbol	Parameter	Test Conditions	APL3201			Unit
			Min.	Typ.	Max.	
SOFT-START AND REVSRSE CURRENT						
T_{SS}	Soft-Start Interval	I_{CHG}=0A to Fast-Charging Current	4	7	12	ms
	BATT Input Current	V_{IN}=0V, V_{BATT}=4.2V	-	-	8	µA
	BATT Shutdown Input Current	V_{EN}=0V, V_{IN}=5V, V_{BATT}=4.2V	-	-	4	µA
LOGIC INPUT/OUTPUTS						
	STAT1, STAT2 Logic-Low Output	Sinking 10mA	-	-	0.4	V
	STAT1, STAT2 Off-Leakage Current	$V_{STAT1, 2}$=5V, V_{IN}=0V	-	-	1	µA
	EN Logic Input-High Level		1.6	-	-	V
	EN Logic Input-Low Level		-	-	0.4	V
	EN Input Bias Current		-	-	1	µA

Pin Description

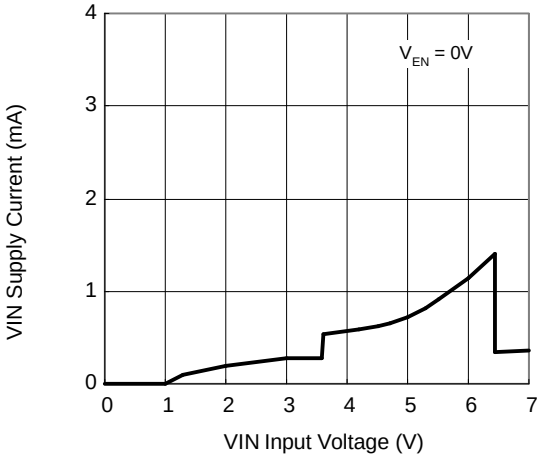
PIN		FUNCTION
NO.	NAME	
1	VIN	Input Supply Pin. Provides power to the charger, V_{IN} can range from 4.35V to 6.0V and should be bypassed with at least a 4.7µF capacitor.
2	STAT1	Charge Status Output Pin 1. This pin is an active-high, open-drain output pin.
3	ISET	Charging Current Setting Pin. Connecting a resistor from this pin to GND set the fast-charge current when the VIN is powering the charger.
4	GND	Ground.
5	EN	Charging Enable/Disable Control Pin. Drive EN high to begin charging, and EN low to stop charging.
6	THRM	External Thermistor Connection Pin. THRM pauses charging when an externally connected thermistor (10kΩ at +25°C) is at less than 0°C or greater than +50°C. Connecting this pin to GND disables this function.
7	REF	3V Reference Voltage Output Pin. Sources up to 500µA to bias the external thermistor. Bypass with 0.1µF to GND. REF loading does not affect BATT regulation accuracy.
8	STAT2	Charge Status Output Pin 2. This pin is an active-high, open-drain output pin.
9	BYP	Bias Supply Pin for Internal Circuitry. Bypass with a 2.2µF capacitor to GND.
10	BATT	Charger Output Pin. Connect this pin to the positive terminal of a Li+ battery.
-	EP	Exposed Pad. Connect a large ground plane for maximum package heat dissipation. Connect directly to GND under the IC.

Typical Operating Characteristics

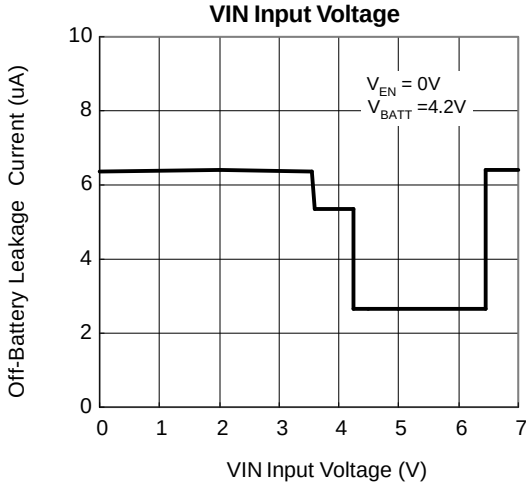
VIN Supply Current vs. VIN Input Voltage



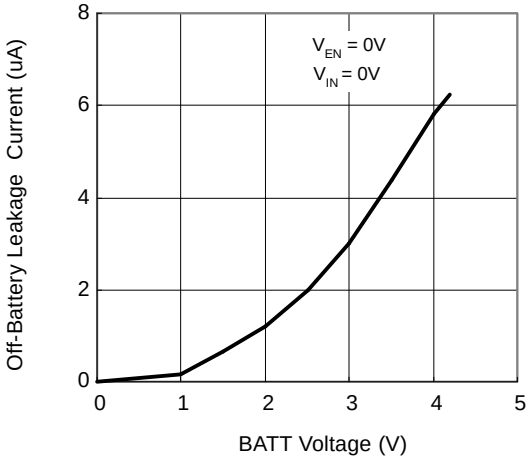
VIN Supply Current vs. VIN Input Voltage



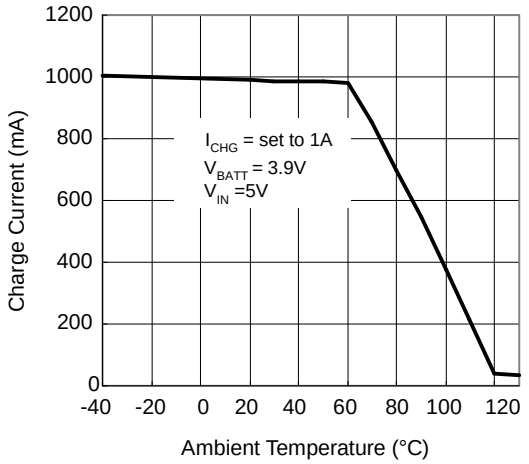
Off-Battery Leakage Current vs. VIN Input Voltage



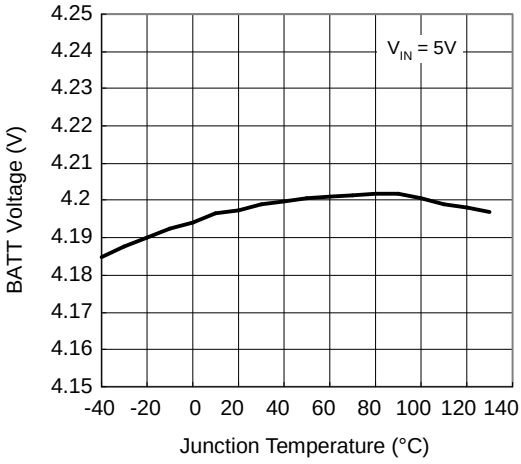
Off-Battery Leakage Current vs. BATT Voltage



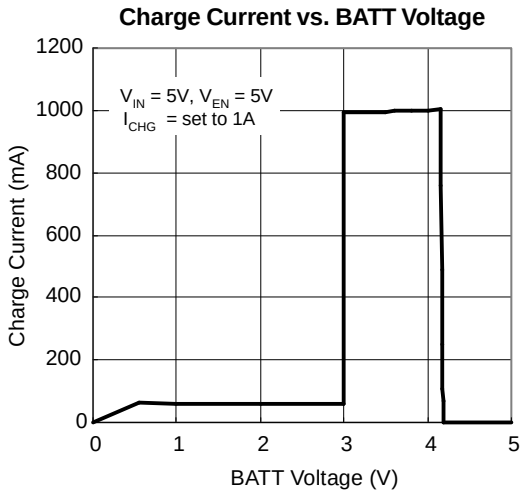
Charge Current vs. Ambient Temperature

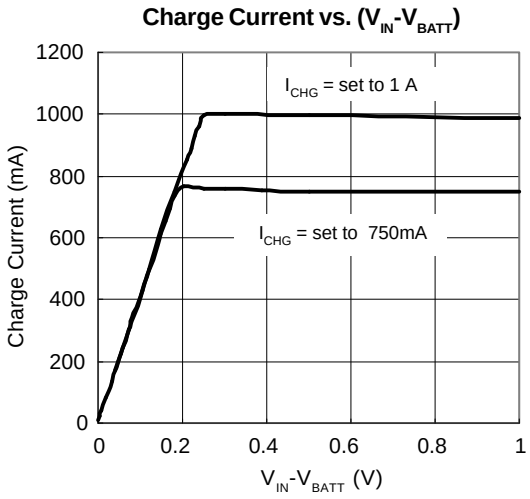


BATT Voltage vs. Junction Temperature



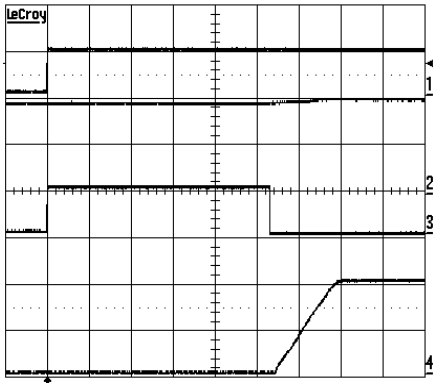
Typical Operating Characteristics (Cont.)





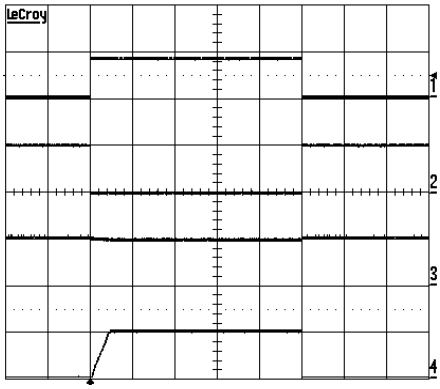
Operating Waveforms

V_{IN} Hot-Plug Power-Up



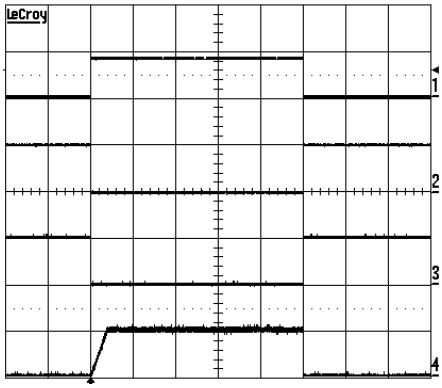
V_{BATT}=3.9V, V_{IN}=5V
CH1: V_{IN} (5V/div)
CH2: V_{BATT} (2V/div)
CH3: V_{STAT1} (5V/div)
CH4: I_{CHG} (0.5A/div)
Time: 5ms/div

Enable in Fast Charge



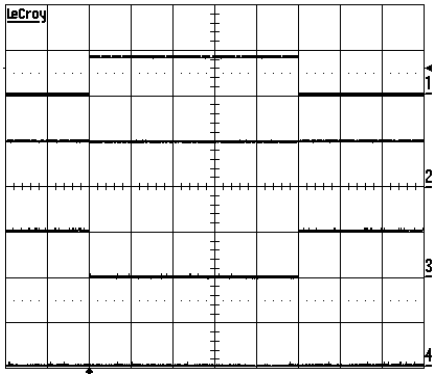
V_{BATT}=3.9V, V_{IN}=5V
CH1: V_{EN} (5V/div)
CH2: V_{STAT1} (5V/div)
CH3: V_{STAT2} (5V/div)
CH4: I_{CHG} (1A/div)
Time: 20ms/div

Enable in Precharge



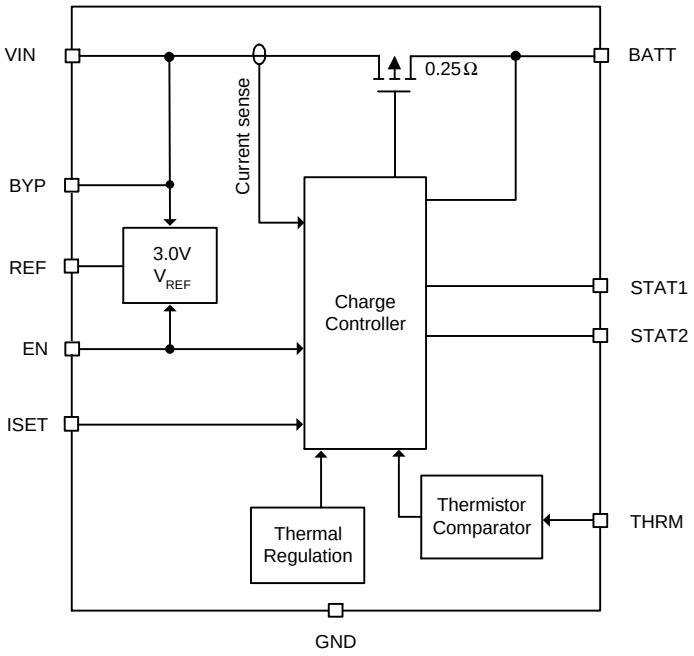
V_{BATT}=2.7V, V_{IN}=5V
CH1: V_{EN} (5V/div)
CH2: V_{STAT1} (5V/div)
CH3: V_{STAT2} (5V/div)
CH4: I_{CHG} (50mA/div)
Time: 20ms/div

Enable in Charge Done

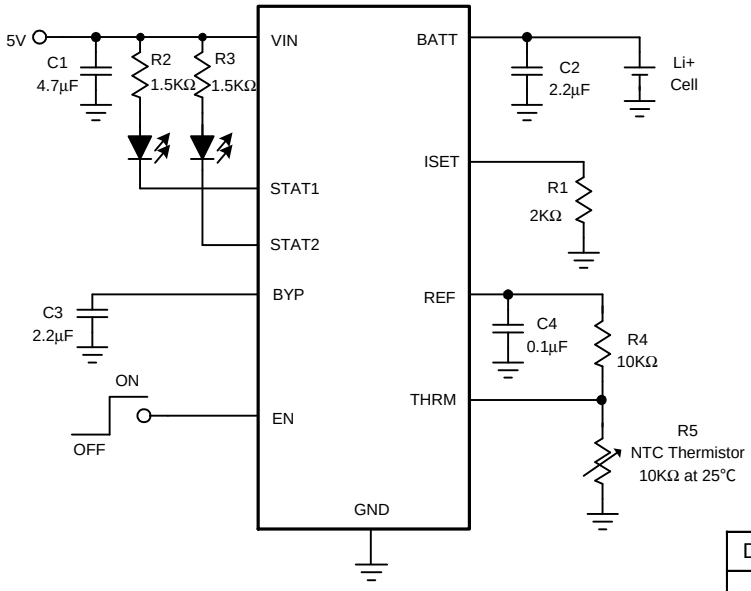


V_{BATT}=4.2V, V_{IN}=5V
CH1: V_{EN} (5V/div)
CH2: V_{STAT1} (5V/div)
CH3: V_{STAT2} (5V/div)
CH4: I_{CHG} (50mA/div)
Time: 20ms/div

Block Diagram



Typical Application Circuit



Designation	Description
C1	4.7µF, 10V, X5R, 0805 Murata GRM188R61A475K
C2	2.2µF, 6.3V, X5R, 0603 Murata GRM188R60J225K
C3	2.2µF, 10V, X5R, 0603 Murata GRM188R61A225K

Murata website: www.murata.com

Function Description

Precharge Current

When the APL3201 is powered with a battery connected, the IC first detects if the cell voltage is ready for full charge current. If the cell voltage is less than the prequal level (3V typ), the battery is precharged with a 55mA current until the cell reaches the proper level. The full charging current, as set by ISET pin, is then applied.

Charging Current Setting

The charge current is programmed by using a resistor from the ISET pin to the ground. The battery charge current is 1000 times the current out of the ISET pin. The battery charge current is calculated by the following equation:

$$I_{CHG} = K_{SET} \times V_{SET} / R_{SET}$$

Where

V_{SET} is ISET regulation voltage (nominal=1V).

K_{SET} is the charging current set factor (nominal=1000).

The charging current set factor and the ISET regulation voltage are shown in the Electrical Characteristics. The ISET regulation voltage is reduced by thermal regulation function.

Enable (EN)

The enable input, EN, switches the charging of APL3201 on or off. With EN high, the APL3201 can begin charging. When EN is low, charging stops, REF is shutdown, and STAT1 and STAT2 outputs are off (high).

Battery Full Indication

Charge-done occurs when I_{CHG} falls to 12.5% of the current set by R_{SET} and the charger is in voltage mode (V_{BATT} near 4.2V). After the APL3201 enunciates the charge-done signal, it keeps operating in voltage mode without turning off the charger. The STAT1 is turned off (high) and STAT2 is turned on (low) when the charger is into charge-done state.

Thermal Regulation

On-chip thermal limiting in the APL3201 simplifies PC board layout and allows charging rates to be automatically optimized without constraints imposed by worst-case minimum battery voltage, maximum input voltage, and maximum ambient temperature. When the APL3201 thermal limit is reached, the charger does not shut down but simply reduces charging current. This allows the board design to be optimized for compact size and typical thermal conditions. The APL3201 reduces charging current to keep its die temperature below +120°C. The APL3201's DFN3x3-10 package includes a bottom metal plate that reduces thermal resistance between the die and the PC board. The external pad should be soldered to a large ground plane. This helps dissipate power and keeps the die temperature below the thermal limit. The APL3201's thermal regulator is set for a +120°C die temperature.

External Thermistor Monitor (THRM)

The APL3201 features an internal window comparator to monitor battery pack temperature or ambient temperature with an external negative temperature coefficient thermistor. In typical systems, temperature is monitored to prevent charging at ambient temperature extremes (below 0°C or above +50°C). When the temperature moves outside these limits, charging is stopped. If the V_{THRM} returns to within its normal window, charging resumes. Connect THRM to GND when not using this feature. Note that the temperature monitor at THRM entirely separates from the on-chip temperature limiting discussed in the Thermal Regulation section. The input thresholds for the THRM input are 0.74 x V_{REF} for the COLD trip point and 0.29 x V_{REF} for the HOT trip point.

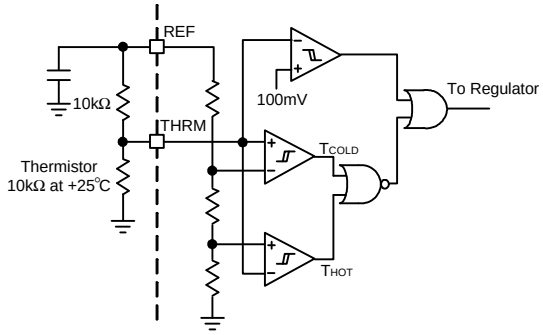


Figure 1. Thermistor Sensing Block Diagram

Function Description (Cont.)

Charge Status Outputs

The open-drain STAT1 and STAT2 outputs indicate four charger operations are shown in Table 1. The two outputs can be used to drive LEDs or communicate to the host processor. Note that OFF indicates the open-drain transistor is turned off.

CHARGE STATE	STAT1	STAT2
Precharge in progress	ON	ON
Fast charge in progress	ON	OFF
Charge done	OFF	ON
Charge suspended	OFF	OFF

Table 1. Status Pin Summary

Soft-Start

The APL3201 includes a soft-start function to control the rise rate of the charging current rising from zero to the fast-charging current level in constant current mode. During charger soft-start, the APL3201 ramps up the voltage on ISET pin with constant well-controlled slew rate. The charging current is proportional to the ISET voltage. The soft-start interval is 7ms (typical), which is independent of the fast-charging current level.

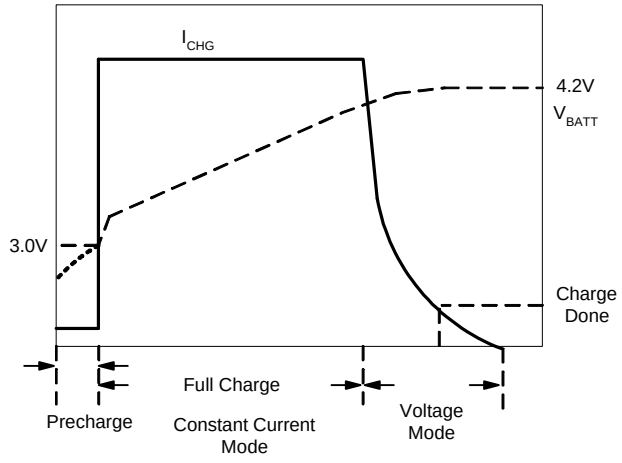


Figure 2. Typical Charging Profile

Disable Charging for V_{IN}>6.4V

When input voltage is over 6.4V overvoltage threshold, the charging of APL3201 will be turned off. The charging will be turned on until the input voltage is below the OVP threshold. The absolute maximum rating of input voltage is 7V. If the input voltage is over 7V the IC may be damaged.

Applicaiton Information

STAT Pins

The STAT1 and STAT2 outputs indicate four charger operations. These two pins can be used to drive LEDs or communicate to the host processor. When status pins are monitored by a processor, there should be a 10kΩ pull-up resistor to connect each status pin and the V_{CC} of the processor; furthermore, when the status is viewed by the LED, the LED with a current rating is less than 10mA and a resistor should be selected to connect the LED in series, so the current will be limited to the desired current value. The resistor is calculated by the following equation:

$$R2,3 = \frac{(V_{IN} - V_{LED\_ON})}{P_D}$$

In other words, the LED and resistor between the input and each status pin shoule be in series.

Capacitor Selection

Typically, a 4.7µF ceramic capacitor is used to connect from VIN to GND. For high charging current, it is recommended to use a larger input bypass capacitance to reduce supply noise. There is a ceramic capacitor connecting from BATT to GND for proper stability. To work well with most application, at least a 2.2µF X5R ceramic capacitor is required.

Thermal Consideration

The APL3201 is available in a thermally enhanced QFN package with an exposed pad. It is recommended to connect the exposed pad to a large copper ground plane on the backside of the circuit board through several thermal vias for heatsinking. The exposed pad transfers heat away from the device, allowing the APL3201 to charge the battery with maximum current while minimizing the increase in die temperature.

The most common measure of package thermal performance is thermal resistance measured from the device junction to the air surrounding the package surface (θ_{JA}). The θ_{JA} can be calculated by the following equation:

$$\theta_{JA} = \frac{T_J - T_A}{P_D}$$

where:

T_J=device junction temperature

T_A= ambient temperature

P_D=device power dissipation

The device power dissipation, P_D, is the function of the charge rate and the voltage drop across the internal FET. It can be calculated by the following equation:

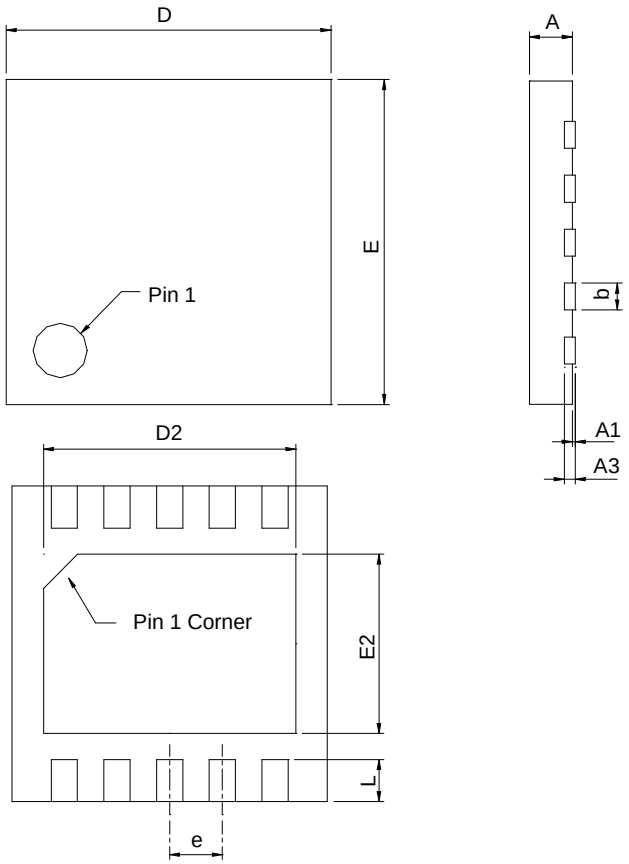
$$P_D = (V_{IN} - V_{BATT}) \times I_{CHG}$$

PCB Layout Consideration

The APL3201 is packaged in a thermally enhanced QFN package. The package includes a thermal pad to provide an effective thermal contact between the device and the printed circuit board. Connecting the exposed pad to a large copper ground plane on the backside of the circuit board through several thermal vias for heatsinking is recommended. Connecting the battery to BATT as close to the device as possible provides accurate battery voltage sensing. All decoupling capacitors and filter capacitors should be placed as close as possible to the device. The high-current charge path into VIN and from the BATT pin must be short and wide to minimize voltage drops.

Package Information

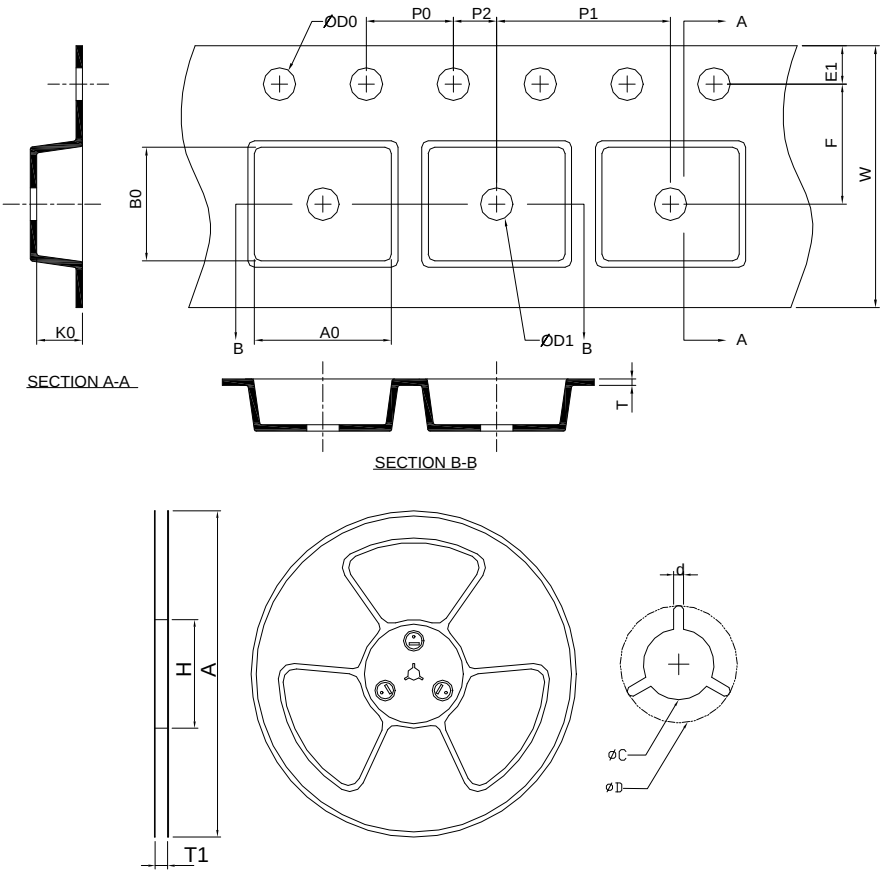
DFN3x3-10



SYMBOL	DFN3x3-10			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	2.20	2.70	0.087	0.106
E	2.90	3.10	0.114	0.122
E2	1.40	1.75	0.055	0.069
e	0.50 BSC		0.020 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	

Note : 1. Followed from JEDEC MO-229 VEED-5.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
DFN3x3-10	178.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.30±0.20

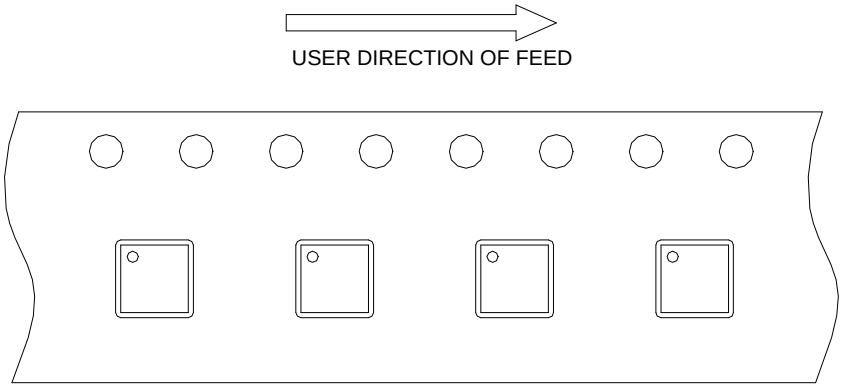
(mm)

Devices Per Unit

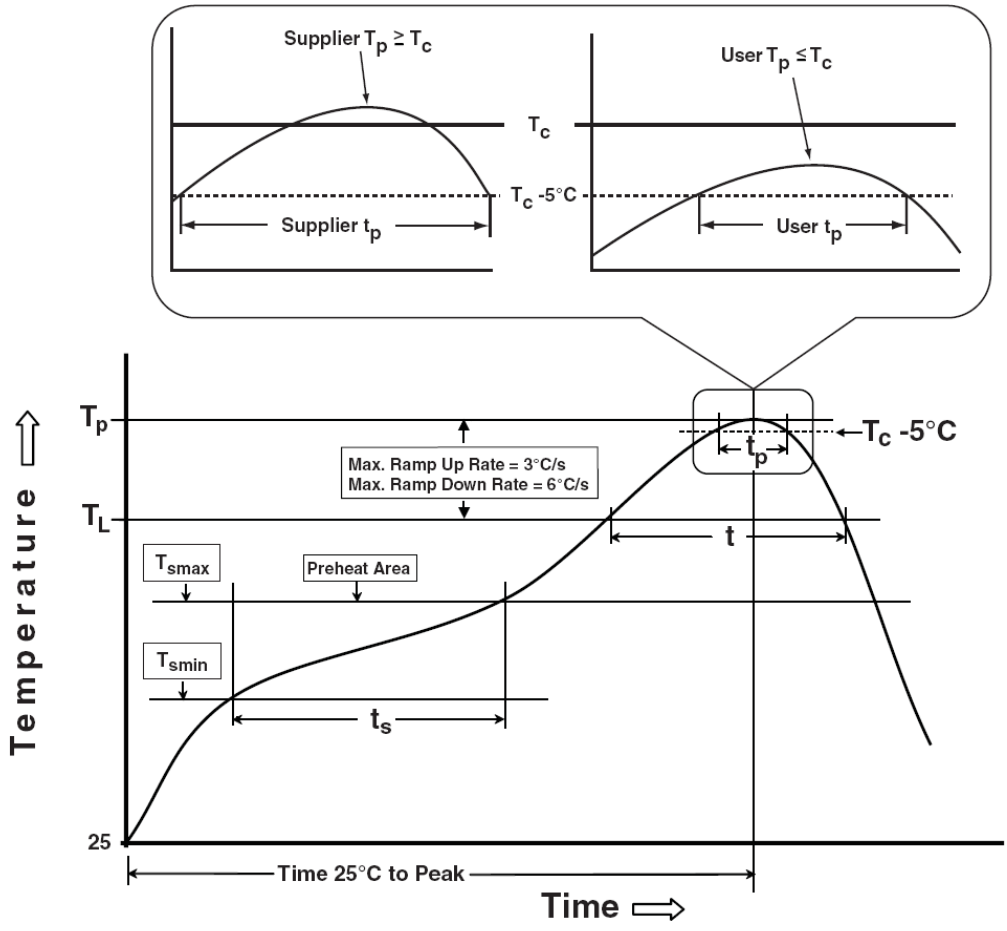
Package Type	Unit	Quantity
DFN3x3-10	Tape & Reel	3000

Taping Direction Information

DFN3x3-10



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ 125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
ESD	MIL-STD-883-3015.7	VHBM≧2KV, VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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