

4V Drive Pch+Pch MOSFET

SH8J66

●Structure

Silicon P-channel MOSFET

●Features

- 1) Low On-resistance.
- 2) Built-in G-S Protection Diode.
- 3) Small Surface Mount Package (SOP8).

●Applications

Switching

●Packaging specifications

Type	Package	Taping
	Code	TB
	Basic ordering unit (pieces)	2500
SH8J66		○

●Absolute maximum ratings (Ta=25°C)

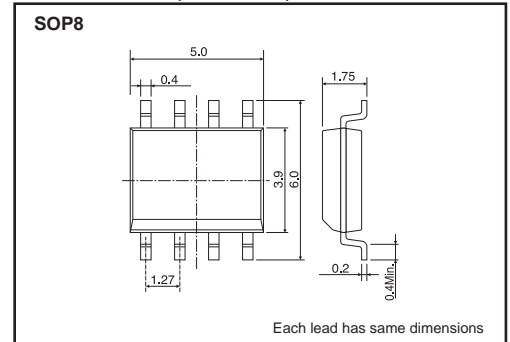
<It is the same ratings for Tr1 and Tr2.>

Parameter	Symbol	Limits	Unit	
Drain-source voltage	V_{DSS}	-30	V	
Gate-source voltage	V_{GSS}	±20	V	
Drain current	Continuous	I_D	±9	A
	Pulsed	I_{DP} *1	±36	A
Source current (Body diode)	Continuous	I_S	-1.6	A
	Pulsed	I_{SP} *1	-36	A
Total power dissipation	P_D *2	2.0	W / TOTAL	
		1.4	W / ELEMENT	
Channel temperature	T_{ch}	150	°C	
Range of Storage temperature	T_{stg}	-55 to +150	°C	

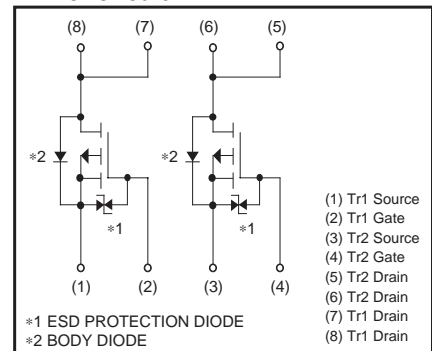
*1 $P_w \leq 10\mu s$, Duty cycle $\leq 1\%$

*2 Mounted on a ceramic board

●Dimensions (Unit : mm)



●Inner circuit



●Electrical characteristics (Ta=25°C)

<It is the same characteristics for Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I _{GSS}	–	–	±10	μA	V _{GS} =±20V, V _{DS} =0V
Drain-source breakdown voltage	V _{(BR)DSS}	–30	–	–	V	I _D = –1mA, V _{GS} =0V
Zero gate voltage drain current	I _{DSS}	–	–	–1	μA	V _{DS} = –30V, V _{GS} =0V
Gate threshold voltage	V _{GS(th)}	–1.0	–	–2.5	V	V _{DS} = –10V, I _D = –1mA
Static drain-source on-state resistance	R _{DS(on)} *	–	13.5	18.5	mΩ	I _D = –9A, V _{GS} = –10V
		–	17.5	23.6	mΩ	I _D = –4.5A, V _{GS} = –4.5V
		–	19.0	24.7	mΩ	I _D = –4.5A, V _{GS} = –4.0V
Forward transfer admittance	Y _{fs} *	11	–	–	S	V _{DS} = –10V, I _D = –9A
Input capacitance	C _{iss}	–	3000	–	pF	V _{DS} = –10V
Output capacitance	C _{oss}	–	400	–	pF	V _{GS} =0V
Reverse transfer capacitance	C _{rss}	–	400	–	pF	f=1MHz
Turn-on delay time	t _{d(on)} *	–	20	–	ns	V _{DD} = –15V
Rise time	t _r *	–	60	–	ns	I _D = –4.5A
Turn-off delay time	t _{d(off)} *	–	170	–	ns	V _{GS} = –10V
Fall time	t _f *	–	100	–	ns	R _L =3.3Ω
Total gate charge	Q _g *	–	35	–	nC	R _G =10Ω
Gate-source charge	Q _{gs} *	–	9	–	nC	V _{DD} = –15V
Gate-drain charge	Q _{gd} *	–	12	–	nC	I _D = –9A
						V _{GS} = –5V
						R _L =1.7Ω / R _G =10Ω

*Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

<It is the same characteristics for Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V _{SD} *	–	–	–1.2	V	I _S = –9A, V _{GS} =0V

* Pulsed

●Electrical characteristic curves

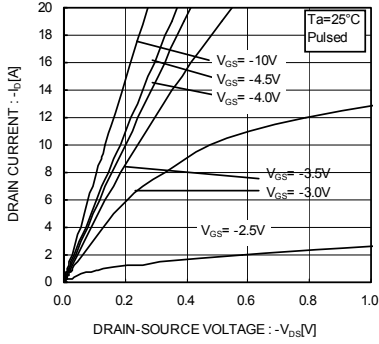


Fig. 1 Typical output characteristics(I)

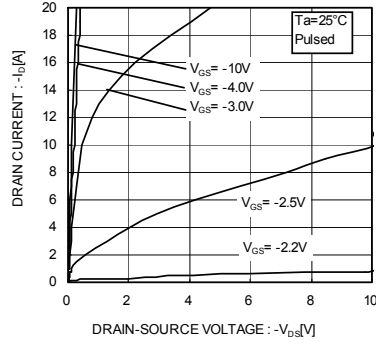


Fig. 2 Typical output characteristics(II)

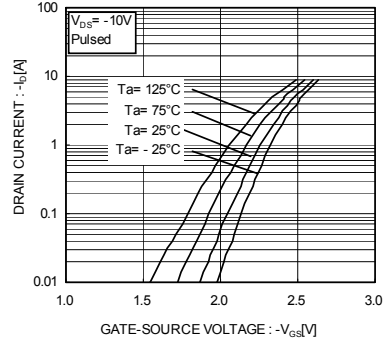


Fig. 3 Typical Transfer Characteristics

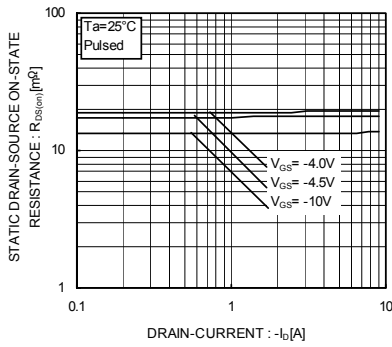


Fig. 4 Static Drain-Source On-State Resistance vs. Drain Current(I)

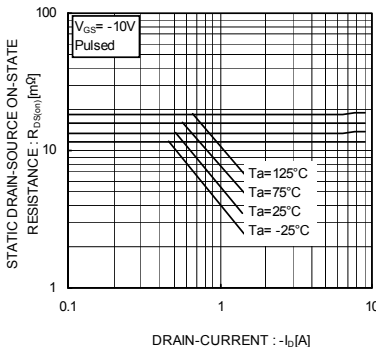


Fig. 5 Static Drain-Source On-State Resistance vs. Drain Current(II)

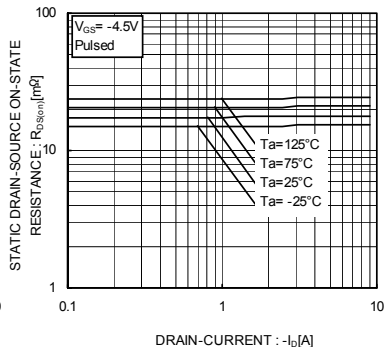


Fig. 6 Static Drain-Source On-State Resistance vs. Drain Current(III)

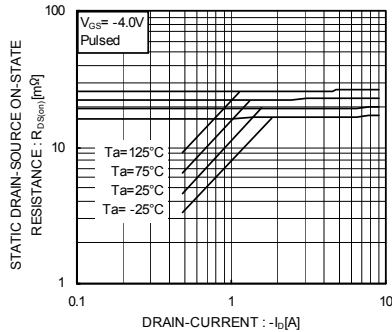


Fig. 7 Static Drain-Source On-State Resistance vs. Drain Current(IV)

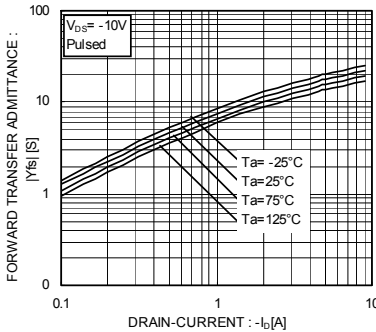


Fig. 8 Forward Transfer Admittance vs. Drain Current

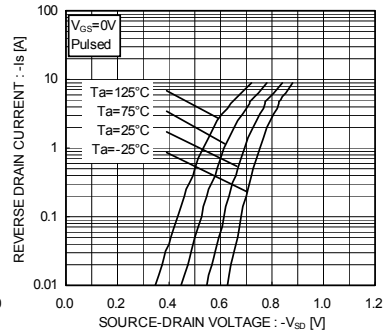


Fig. 9 Reverse Drain Current vs. Source-Drain Voltage

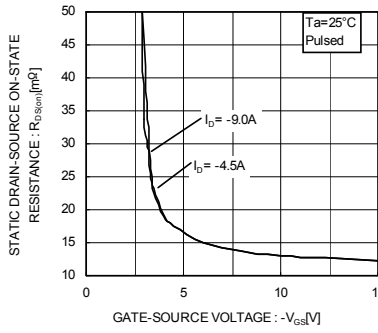


Fig. 10 Static Drain-Source On-State Resistance vs. Gate Source Voltage

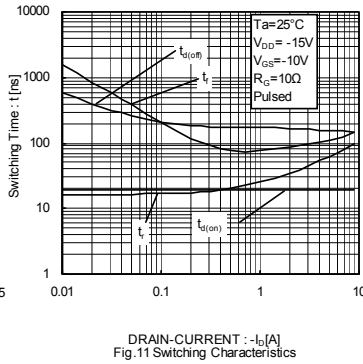


Fig. 11 Switching Characteristics

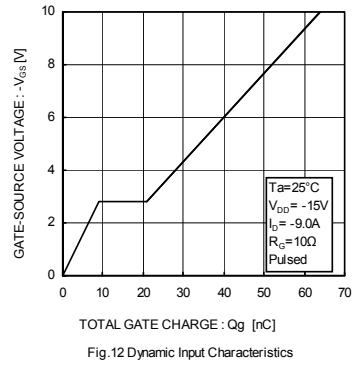


Fig. 12 Dynamic Input Characteristics

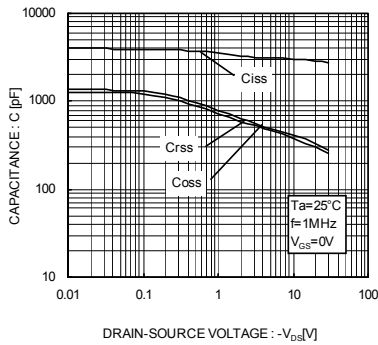


Fig. 13 Typical Capacitance vs. Drain-Source Voltage

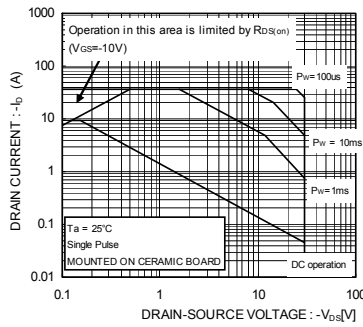


Fig. 14 Maximum Safe Operating Area

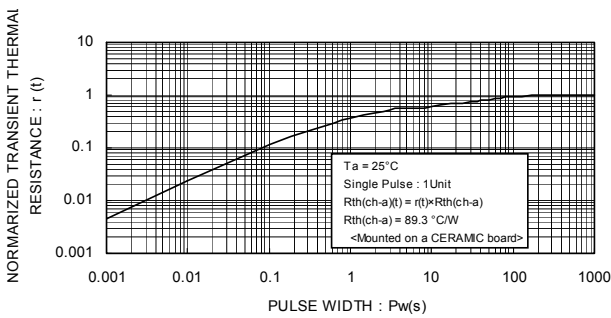


Fig. 15 Normalized Transient Thermal Resistance vs. Pulse Width

●Measurement circuits

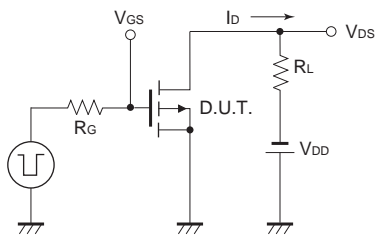


Fig.1-1 Switching Time Test Circuit

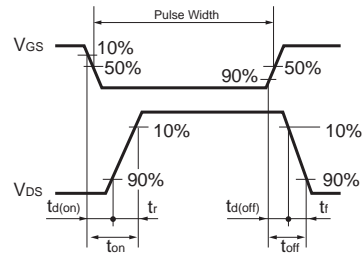


Fig.1-2 Switching Time Waveforms

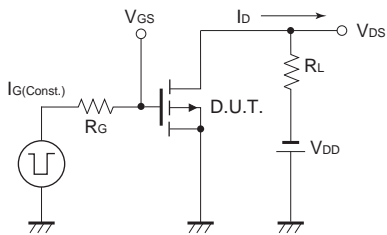


Fig.2-1 Gate Charge Test Circuit

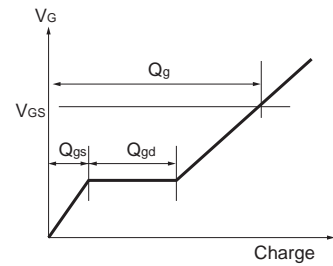


Fig.2-2 Gate Charge Waveform

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