PCF8576D

Universal LCD driver for low multiplex rates

Rev. 7 — 18 December 2008 Product data sheet

1. General description

The PCF8576D is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments. It can be easily cascaded for larger LCD applications. The PCF8576D is compatible with most microprocessors or microcontrollers and communicates via a two-line bidirectional I^2C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

AEC-Q100 compliant (PCF8576DH/2) for automotive applications.

2. Features

- Single chip LCD controller and driver
- Selectable backplane drive configuration: static or 2, 3, 4 backplane multiplexing
- Selectable display bias configuration: static, $\frac{1}{2}$ or $\frac{1}{3}$
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives:
  - Up to twenty 7-segment numeric characters
  - Up to ten 14-segment alphanumeric characters
  - Any graphics of up to 160 elements
- 40×4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- Independent supplies possible for LCD and logic voltages
- Wide power supply range: from 1.8 V to 5.5 V
- Wide logic LCD supply range:
  - From 2.5 V for low-threshold LCDs
  - Up to 6.5 V for guest-host LCDs and high-threshold twisted nematic LCDs
- Low power consumption
- 400 kHz I^2C-bus interface
- May be cascaded for large LCD applications (up to 2560 elements possible)
- No external components
- Compatible with chip-on-glass and chip-on-board technology
- Manufactured in silicon gate CMOS process

founded by Philips

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF8576DH/2	TQFP64	plastic thin quad flat package, 64 leads; body 10 × 10 × 1.0 mm	SOT357-1
PCF8576DT/2	TSSOP56	plastic thin shrink small outline package, 56 leads; body width 6.1 mm	SOT364-1
PCF8576DU/DA/2	PCF8576DU/DA	wire bond die; 59 bonding pads; 2.26 × 2.01 × 0.38 mm[1]	PCF8576DU/DA
PCF8576DU/2DA/2	PCF8576DU/2DA	bare die; 59 bumps; 2.26 × 2.01 × 0.40 mm[1]	PCF8576DU/2DA

[1] Chips in tray.

[1] Chips with bumps in tray.

4. Marking

Table 2. Marking codes

Type number	Marking code
PCF8576DH/2	PCF8576DH
PCF8576DT/2	PCF8576DT
PCF8576DU/DA/2	PC8576D-2
PCF8576DU/2DA/2	PC8576D-2

5. Block diagram

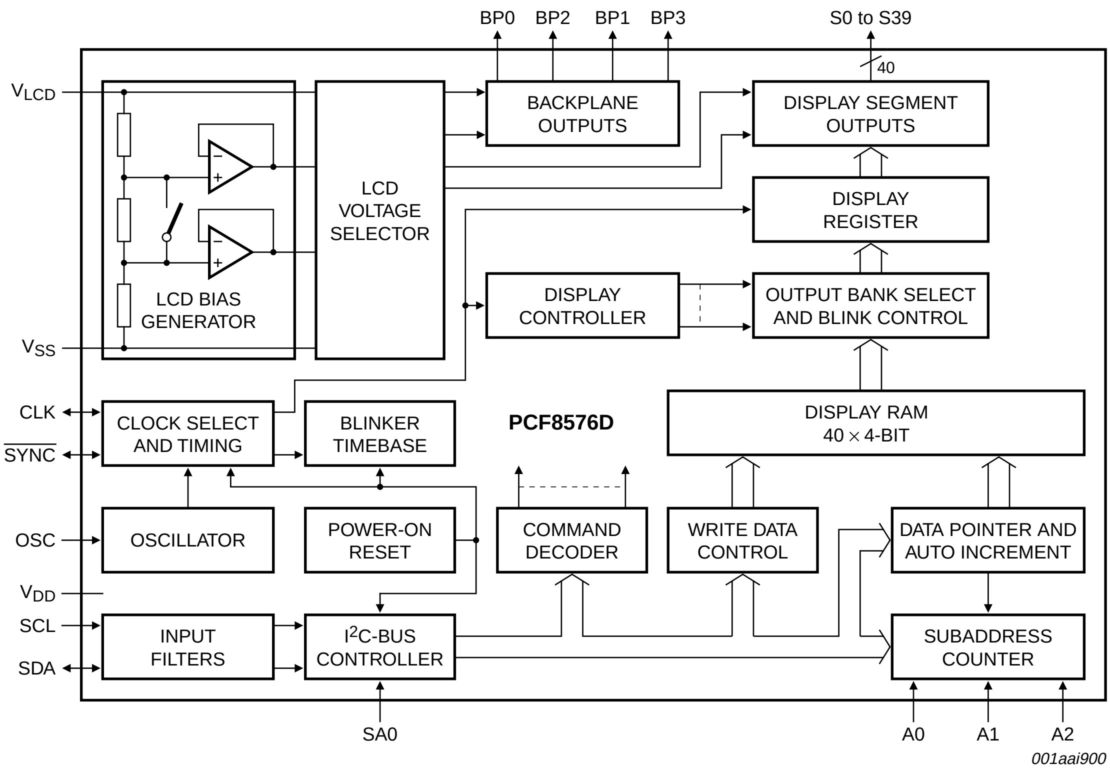
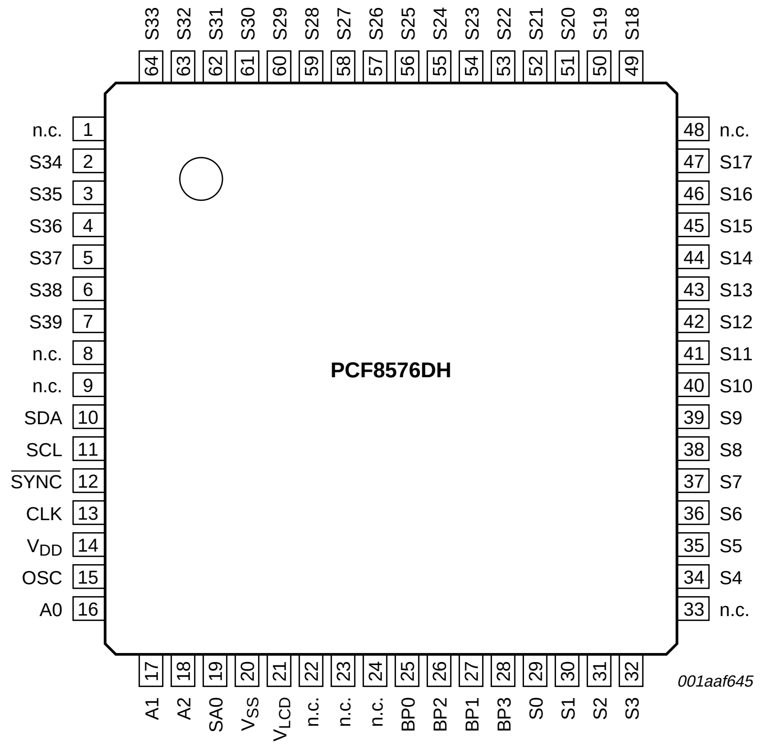


Fig 1. Block diagram of PCF8576D

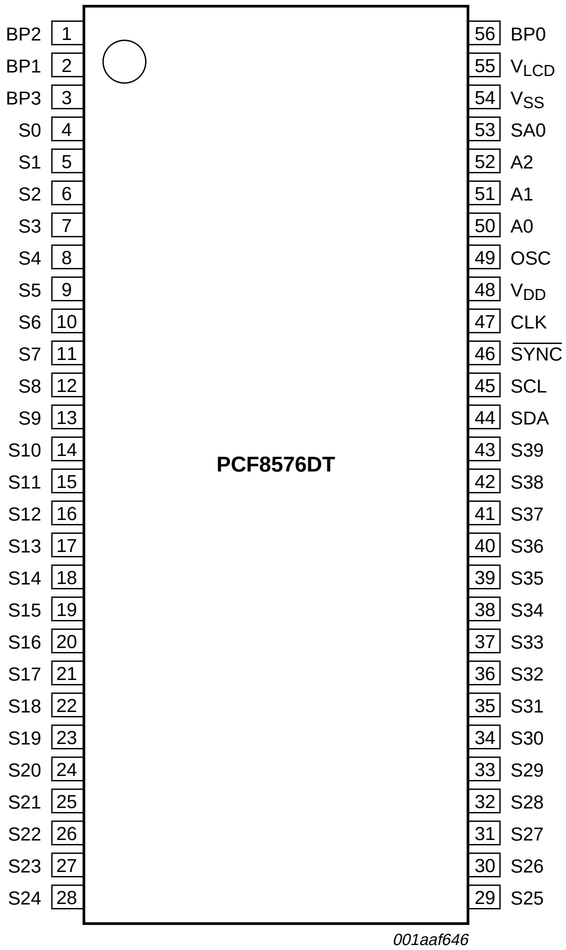
6. Pinning information

6.1 Pinning



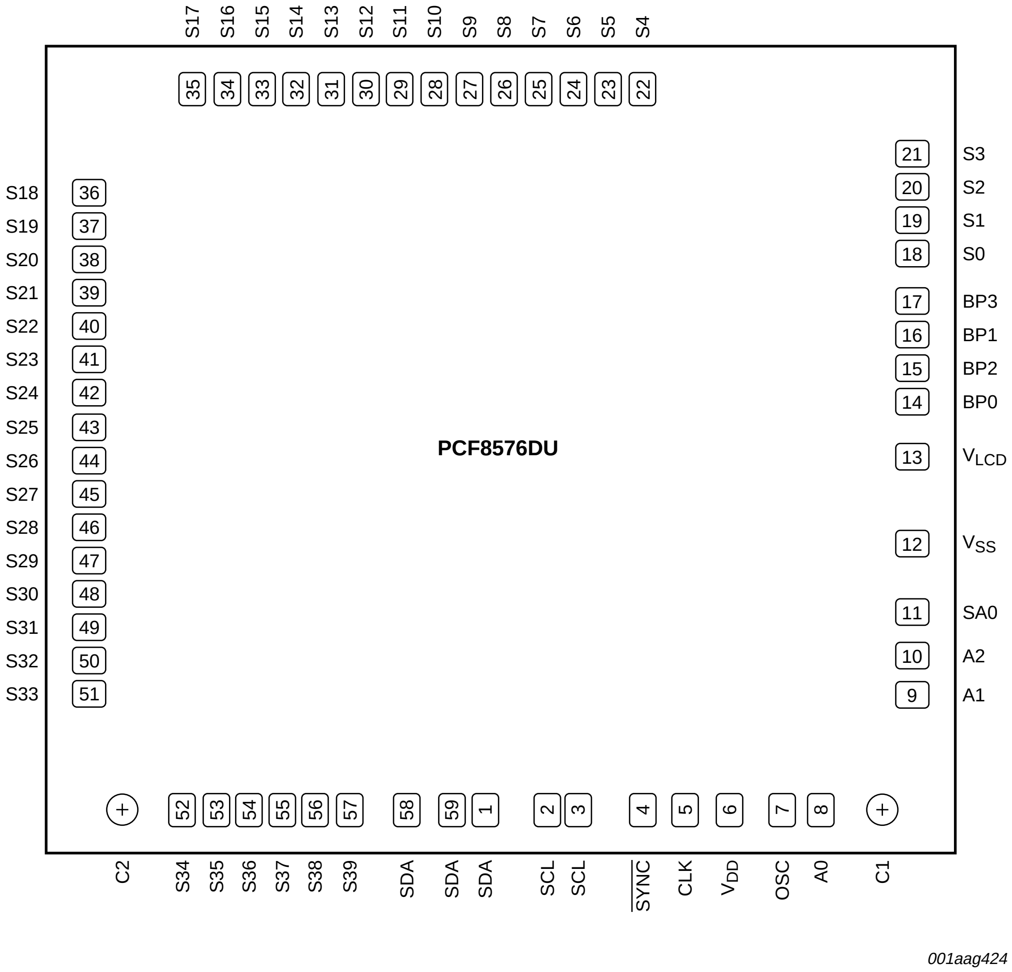
Top view. For mechanical details, see Figure 24.

Fig 2. Pinning diagram for PCF8576DH/2



Top view. For mechanical details, see Figure 25.

Fig 3. Pinning diagram for PCF8576DT/2



Top view. C1 and C2 are alignment marks. For mechanical details, see Figure 26 and Figure 27.

Fig 4. Pinning diagram for PCF8576DUx

6.2 Pin description

Table 3. Pin description

Symbol	Pin			Description
	PCF8576DH/2	PCF8576DT/2	PCF8576DUx	
SDA	10	44	1, 58 and 59	I^2C-bus serial data input and output
SCL	11	45	2 and 3	I^2C-bus serial clock input
CLK	13	47	5	external clock input or output
V_{DD}	14	48	6	supply voltage
$\overline{SYNC}$	12	46	4	cascade synchronization input or output
OSC	15	49	7	internal oscillator enable input
A0 to A2	16 to 18	50 to 52	8 to 10	subaddress inputs
SA0	19	53	11	I^2C-bus address input; bit 0
V_{SS}	20	54	12[1]	ground supply voltage
V_{LCD}	21	55	13	LCD supply voltage
BP0, BP2, BP1, BP3	25 to 28	56, 1, 2, 3	14 to 17	LCD backplane outputs
S0 to S39	29 to 32, 34 to 47, 49 to 64, 2 to 7	4 to 43	18 to 57	LCD segment outputs
n.c.	1, 8, 9, 22 to 24, 33, 48	-	-	not connected

[1] The substrate (rear side of the die) is wired to V_{SS} but should not be electrically connected.

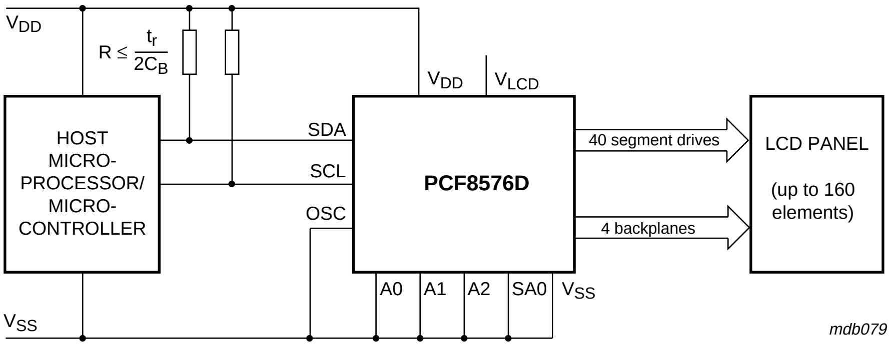
7. Functional description

The PCF8576D is a versatile peripheral device designed to interface any microprocessor or microcontroller with a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments.

The possible display configurations of the PCF8576D depend on the number of active backplane outputs required. A selection of display configurations is shown in Table 4. All of these configurations can be implemented in the typical system shown in Figure 5.

Table 4. Display configurations

Number of:		7-segment numeric		14-segment numeric		Dot matrix
Backplanes	Segments	Digits	Indicator symbols	Characters	Indicator symbols	
4	160	20	20	10	20	160 dots (4 × 40)
3	120	15	15	8	8	120 dots (3 × 40)
2	80	10	10	5	10	80 dots (2 × 40)
1	40	5	5	2	12	40 dots (1 × 40)



The resistance of the power lines must be kept to a minimum.

For chip-on-glass applications, due to the Indium Tin Oxide (ITO) track resistance, each supply line must be routed separately between the chip and the connector.

Fig 5. Typical system configuration

The host microprocessor or microcontroller maintains the 2-line I^{2}C-bus communication channel with the PCF8576D. The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and the LCD panel chosen for the application.

7.1 Power-on reset

At power-on the PCF8576D resets to the following starting conditions:

- All backplane outputs are set to V_{LCD}
- All segment outputs are set to V_{LCD}
- The selected drive mode is: 1:4 multiplex with $\frac{1}{3}$ bias
- Blinking is switched off
- Input and output bank selectors are reset
- The I^{2}C-bus interface is initialized
- The data pointer and the subaddress counter are cleared
- Display is disabled

Data transfers on the I^{2}C-bus must be avoided for 1 ms following power-on to allow the reset action to complete.

7.2 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider consisting of three impedances connected in series between V_{LCD} and V_{SS}. The middle resistor can be bypassed to provide a $\frac{1}{2}$ bias voltage level for the 1:2 multiplex configuration. The LCD voltage can be temperature compensated externally using the supply to pin V_{LCD}.

7.3 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the mode-set command (see Section 7.17) from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D), are given in Table 5.

Table 5. Discrimination ratios

LCD drive mode	Number of:		LCD bias configuration	$\frac{V_{off(RMS)}}{V_{LCD}}$	$\frac{V_{on(RMS)}}{V_{LCD}}$	$D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$
	Backplanes	Levels				
static	1	2	static	0	1	∞
1:2 multiplex	2	3	½	0.354	0.791	2.236
1:2 multiplex	2	4	⅓	0.333	0.745	2.236
1:3 multiplex	3	4	⅓	0.333	0.638	1.915
1:4 multiplex	4	4	⅓	0.333	0.577	1.732

A practical value for V_{LCD} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode a suitable choice is $V_{LCD} > 3V_{th}$.

Multiplex drive modes of 1:3 and 1:4 with ½ bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated by $\frac{1}{1+a}$, where the values for a are

a = 1 for ½ bias

a = 2 for ⅓ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with the equation

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{\frac{1}{n} + \left[(n-1)\times\left(\frac{1}{1+a}\right)\right]^2}{n}} \quad (1)$$

where V_{LCD} is the resultant voltage at the LCD segment and where the values for n are

n = 1 for static mode

n = 2 for 1:2 multiplex

n = 3 for 1:3 multiplex

n = 4 for 1:4 multiplex

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with the equation:

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a^2 - (2a+n)}{n\times(1+a)^2}} \quad (2)$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from the equation:

$$\frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{(a+1)^2 + (n-1)}{(a-1)^2 + (n-1)}} \tag{3}$$

Using Equation 3, the discrimination for an LCD drive mode of 1:3 multiplex with ½ bias is $\sqrt{3} = 1.732$ and the discrimination for an LCD drive mode of 1:4 multiplex with ½ bias is $\frac{\sqrt{21}}{3} = 1.528$.

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage V_{LCD} as follows:

- 1:3 multiplex (½ bias): $V_{LCD} = \sqrt{6} \times V_{off(RMS)} = 2.449V_{off(RMS)}$
- 1:4 multiplex (½ bias): $V_{LCD} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309V_{off(RMS)}$

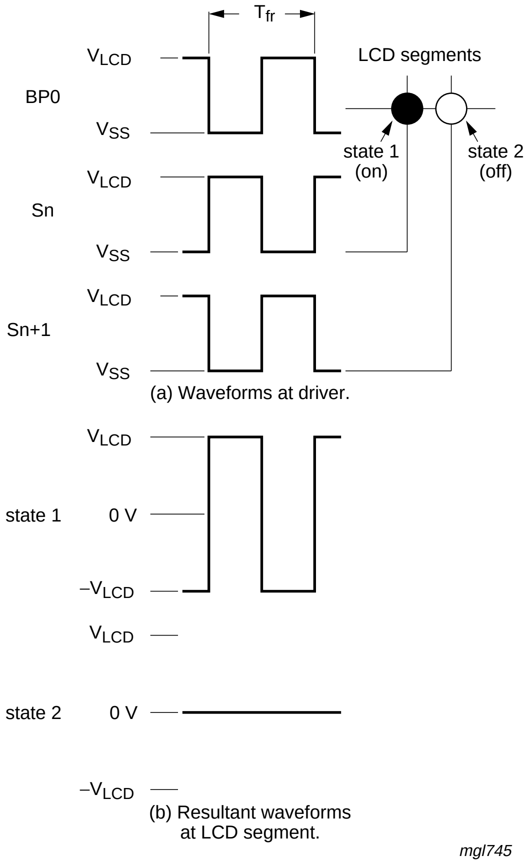
These compare with $V_{LCD} = 3V_{off(RMS)}$ when ⅓ bias is used.

It should be noted that V_{LCD} is sometimes referred as the LCD operating voltage.

7.4 LCD drive mode waveforms

7.4.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. The backplane (BPn) and segment drive (S_n) waveforms for this mode are shown in Figure 6.



(1) $V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

(2) $V_{on(RMS)} = V_{LCD}$.

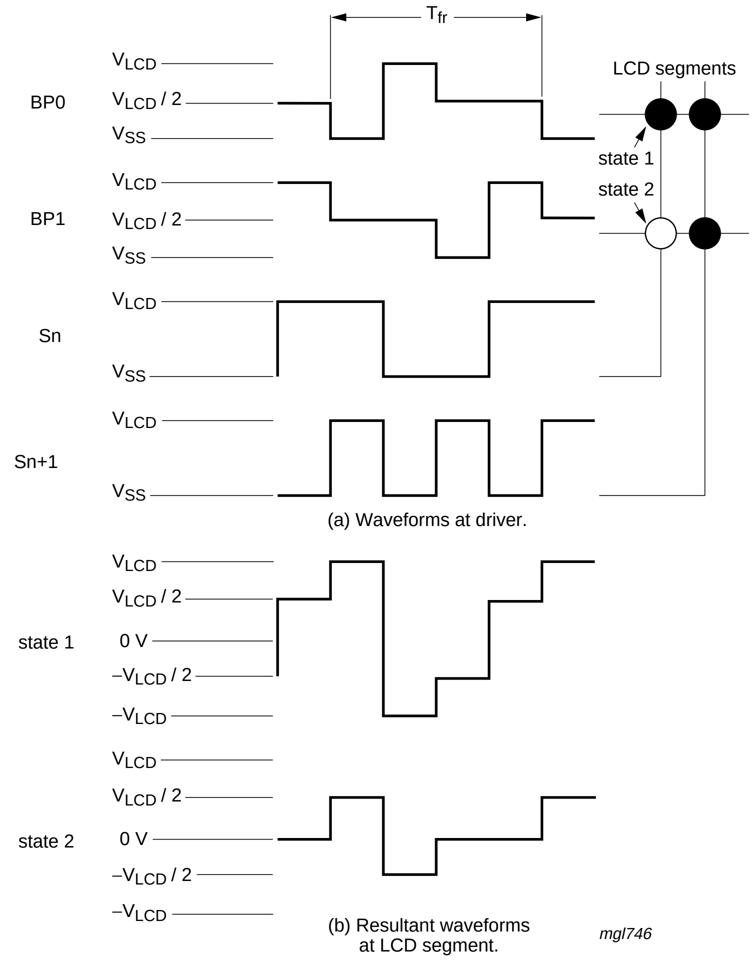
(3) $V_{state2}(t) = V_{Sn+1}(t) - V_{BP0}(t)$.

(4) $V_{off(RMS)} = 0$ V.

Fig 6. Static drive mode waveforms

7.4.2 1:2 Multiplex drive mode

The 1:2 multiplex drive mode is used when two backplanes are provided in the LCD. This mode allows fractional LCD bias voltages of ½ bias or ⅓ bias as shown in Figure 7 and Figure 8.



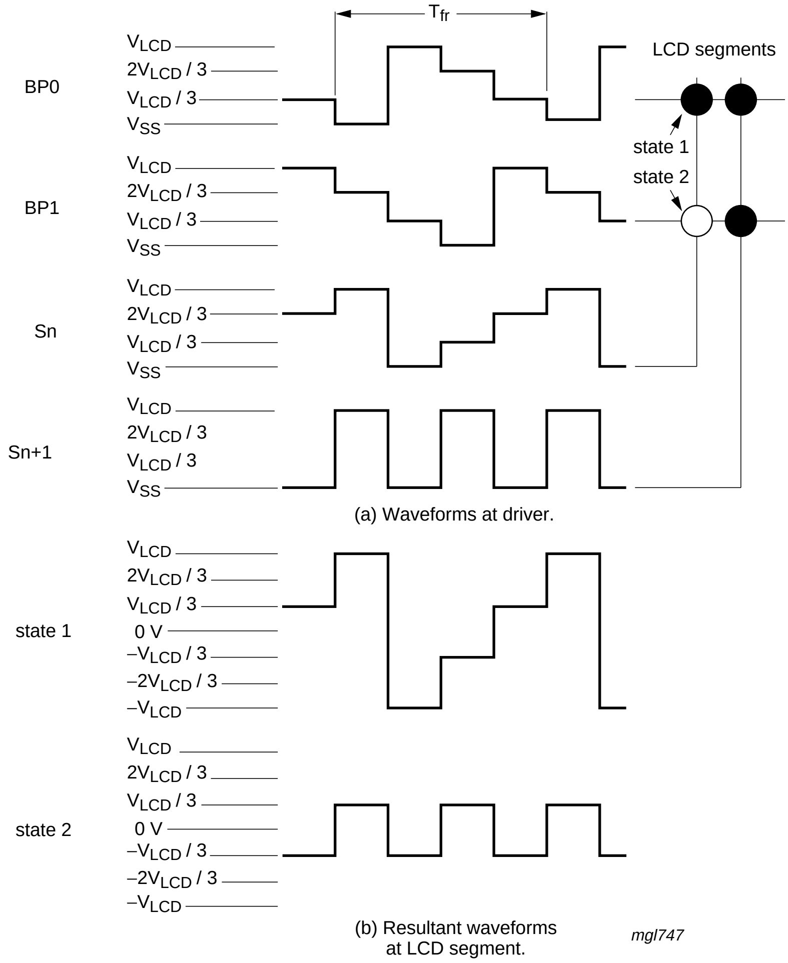
(1) $V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

(2) $V_{on(RMS)} = 0.791 V_{LCD}$.

(3) $V_{state2}(t) = V_{Sn+1}(t) - V_{BP1}(t)$.

(4) $V_{off(RMS)} = 0.354 V_{LCD}$.

Fig 7. Waveforms for the 1:2 multiplex drive mode with ½ bias



(1) $V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

(2) $V_{on(RMS)} = 0.745V_{LCD}$.

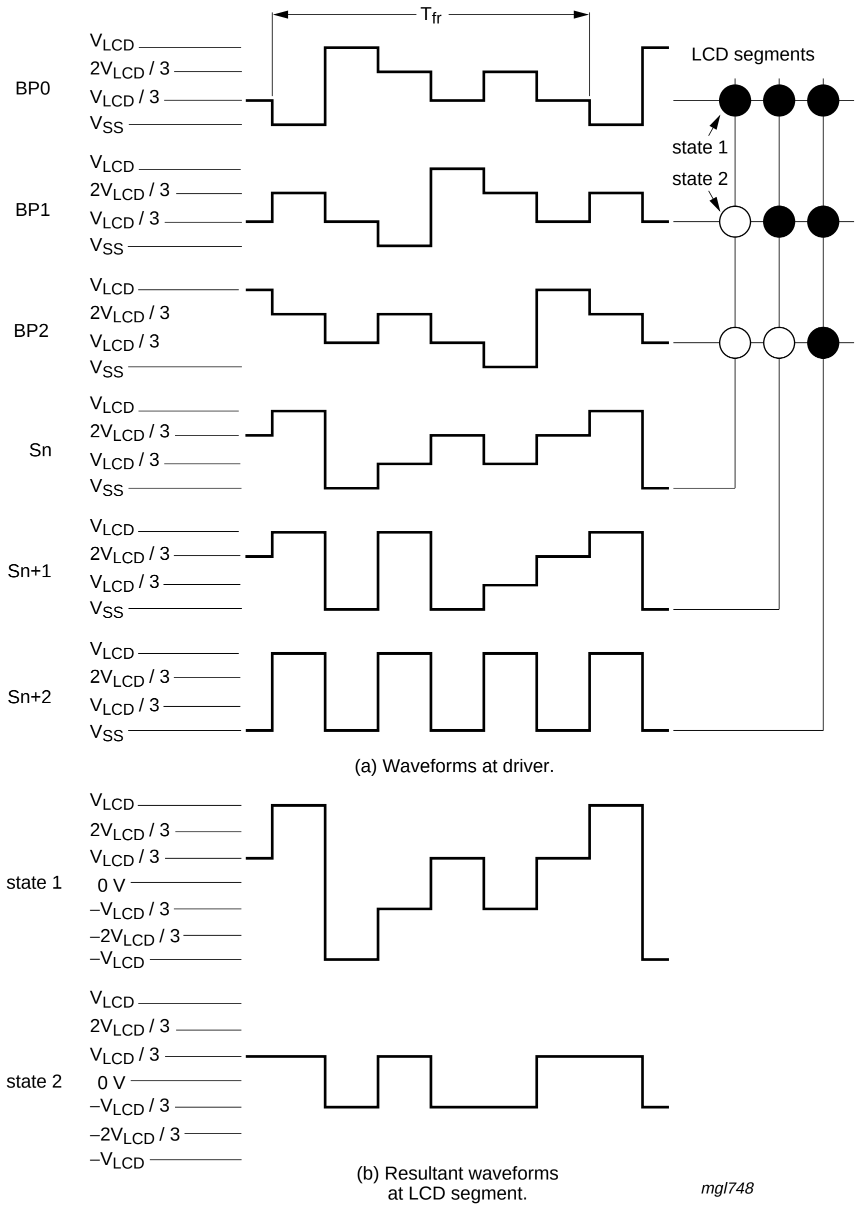
(3) $V_{state2}(t) = V_{Sn+1}(t) - V_{BP1}(t)$.

(4) $V_{off(RMS)} = 0.333V_{LCD}$.

Fig 8. Waveforms for the 1:2 multiplex drive mode with $\frac{1}{3}$ bias

7.4.3 1:3 Multiplex drive mode

When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies (see Figure 9).



(1) $V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

(2) $V_{on(RMS)} = 0.638V_{LCD}$.

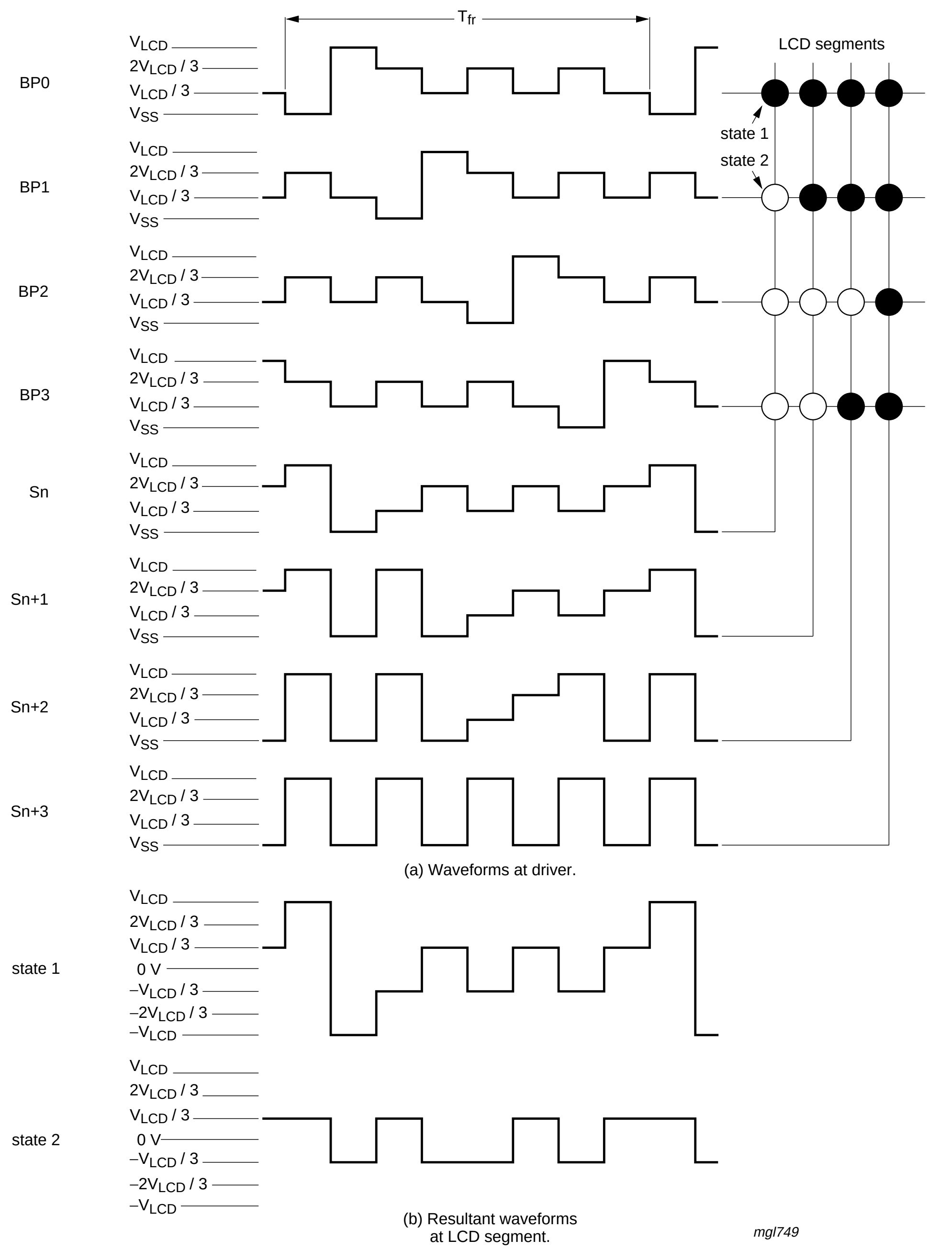
(3) $V_{state2}(t) = V_{Sn+1}(t) - V_{BP1}(t)$.

(4) $V_{off(RMS)} = 0.333V_{LCD}$.

Fig 9. Waveforms for the 1:3 multiplex drive mode with ⅓ bias

7.4.4 1:4 Multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies (see Figure 10).



(1) $V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

(2) $V_{on(RMS)} = 0.577V_{LCD}$.

(3) $V_{state2}(t) = V_{Sn+1}(t) - V_{BP1}(t)$.

(4) $V_{off(RMS)} = 0.333V_{LCD}$.

Fig 10. Waveforms for the 1:4 multiplex drive mode with ⅓ bias

7.5 Oscillator

7.5.1 Internal clock

The internal logic of the PCF8576D and its LCD drive signals are timed either by its internal oscillator or by an external clock. The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. If the internal oscillator is used, the output from pin CLK can be used as the clock signal for several PCF8576Ds in the system that are connected in cascade. After power-on, pin SDA must be HIGH to guarantee that the clock starts.

7.5.2 External clock

Pin CLK is enabled as an external clock input by connecting pin OSC to V_{DD}.

The LCD frame signal frequency is determined by the clock frequency (f_{clk}).

A clock signal must always be supplied to the device; removing the clock freezes the LCD in a DC state.

7.6 Timing

The PCF8576D timing controls the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the correct timing relationship between each PCF8576D in the system is maintained by the synchronization signal at pin $\overline{\text{SYNC}}$. The timing also generates the LCD frame signal whose frequency is derived from the clock frequency. The frame signal frequency is a fixed division of the clock frequency from either the internal or an external clock: $f_{fr} = \frac{f_{clk}}{24}$.

7.7 Display register

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and each column of the display RAM.

7.8 Segment outputs

The LCD drive section includes 40 segment outputs S0 to S39 which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data residing in the display latch. When less than 40 segment outputs are required, the unused segment outputs should be left open-circuit.

7.9 Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which must be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required, the unused outputs can be left open-circuit.

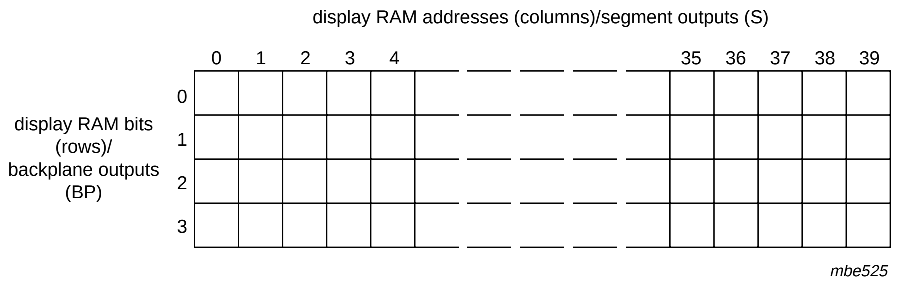
In the 1:3 multiplex drive mode, BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities.

In the 1:2 multiplex drive mode, BP0 and BP2, BP1 and BP3 all carry the same signals and may also be paired to increase the drive capabilities.

In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

7.10 Display RAM

The display RAM is a static 40 × 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the on-state of the corresponding LCD segment; similarly, a logic 0 indicates the off-state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The display RAM bit map Figure 11 shows the rows 0 to 3 which correspond with the backplane outputs BP0 to BP3, and the columns 0 to 39 which correspond with the segment outputs S0 to S39. In multiplexed LCD applications the segment data of the first, second, third and fourth row of the display RAM are time-multiplexed with BP0, BP1, BP2 and BP3 respectively.



Display RAM bit map showing direct relationship between RAM addresses and segment outputs; also between bits in a RAM word and the backplane outputs.

Fig 11. Display RAM bit map

When display data is transmitted to the PCF8576D, the display bytes received are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and does not wait for an acknowledge cycle as with the commands. Depending on the current multiplex drive mode, data is stored singularly, in pairs, triplets or quadruplets. For example, in the 1:2 mode, the RAM data is stored every second bit. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Figure 12; the RAM filling organization depicted applies equally to other LCD types.

With reference to Figure 12, in the static drive mode, the eight transmitted data bits are placed in row 0 of eight successive display RAM addresses.

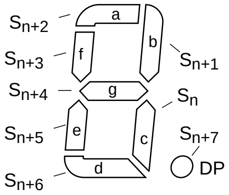
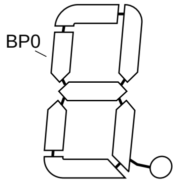
In the 1:2 mode, the eight transmitted data bits are placed in row 0 and 1 of four successive display RAM addresses.

In the 1:3 mode, these bits are placed in row 0, 1 and 2 to three successive addresses, display RAM words, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overwriting adjacent data because always full bytes are transmitted; otherwise this segment should not be connected to the module.

In the 1:4 mode, the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

7.11 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load-data-pointer command (see Section 7.17). Following this, an arriving data byte is stored at the display RAM address indicated by the data pointer in accordance with the filling order shown in Figure 12. After each byte is stored, the contents of the data pointer are automatically incremented by a value dependent on the selected LCD drive mode: eight (static drive mode), four (1:2 mode), three (1:3 mode) or two (1:4 mode). If an I^2C-bus data access is terminated early then the state of the data pointer will be unknown. The data pointer should be re-written prior to further RAM access.

<table>
<tr><th>drive mode</th><th>LCD segments</th><th>LCD backplanes</th><th>display RAM filling order</th><th>transmitted display byte</th></tr>
<tr><td>static</td><td></td><td></td><td>
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<tr><th>bit/ BP</th><th></th><th>n</th><th>n + 1</th><th>n + 2</th><th>n + 3</th><th>n + 4</th><th>n + 5</th><th>n + 6</th><th>n + 7</th></tr>
<tr><td></td><td>0</td><td>c</td><td>b</td><td>a</td><td>f</td><td>g</td><td>e</td><td>d</td><td>DP</td></tr>
<tr><td></td><td>1</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td></tr>
<tr><td></td><td>2</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td></tr>
<tr><td></td><td>3</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td></tr>
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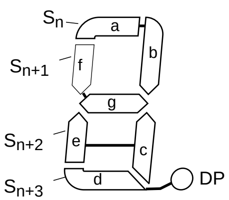
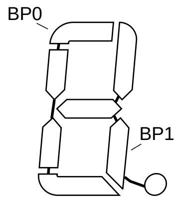
multiplex</td><td></td><td></td><td>
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<tr><td></td><td>2</td><td>x</td><td>x</td><td>x</td><td>x</td></tr>
<tr><td></td><td>3</td><td>x</td><td>x</td><td>x</td><td>x</td></tr>
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a b f g e c d DP</td></tr>
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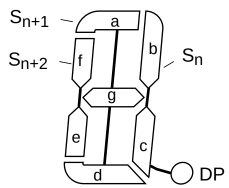
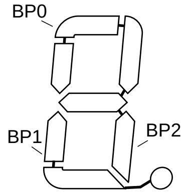
multiplex</td><td></td><td></td><td>
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<tr><td></td><td>2</td><td>c</td><td>g</td><td>x</td></tr>
<tr><td></td><td>3</td><td>x</td><td>x</td><td>x</td></tr>
</table></td><td>MSB LSB
b DP c a d g f e</td></tr>
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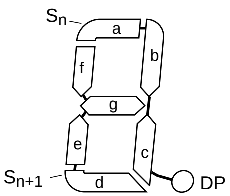
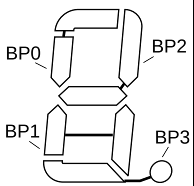
multiplex</td><td></td><td></td><td>
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<tr><td></td><td>2</td><td>b</td><td>g</td></tr>
<tr><td></td><td>3</td><td>DP</td><td>d</td></tr>
</table></td><td>MSB LSB
a c b DP f e g d</td></tr>
</table>

001aag281

x = data bit unchanged.

Fig 12. Relationship between LCD layout, drive mode, display RAM filling order and display data transmitted over the I^{2}C-bus

7.12 Output bank selector

The output bank selector selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the selected LCD drive mode in operation and on the instant in the multiplex sequence.

- In 1:4 mode, all RAM addresses of bit 0 are selected, these are followed by the contents of bit 1, bit 2 and then bit 3.
- In 1:3 mode, bits 0, 1 and 2 are selected sequentially
- In 1:2 mode, bits 0 and 1 are selected
- In static mode, bit 0 is selected

The $\overline{\text{SYNC}}$ signal resets these sequences to the following starting points:

- Bit 3 for 1:4 mode
- Bit 2 for 1:3 mode
- Bit 1 for 1:2 mode
- Bit 0 for static mode

The PCF8576D includes a RAM bank switching feature in the static and 1:2 drive modes. In the static drive mode, the bank-select command (see Section 7.17) may request the contents of bit 2 to be selected for display instead of the contents of bit 0. In 1:2 mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

7.13 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration.

The bank-select command (see Section 7.17) can be used to load display data in bit 2 in static drive mode or in bits 2 and 3 in 1:2 mode. The input bank selector functions are independent of the output bank selector.

7.14 Subaddress counter

The storage of display data is determined by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2. The subaddress counter value is defined by the device-select command (see Section 7.17). If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next PCF8576D occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 14^{th} display data byte transmitted in 1:3 mode).

The hardware subaddress must not be changed while the device is being accessed on the I^2C-bus interface.

7.15 Blinker

The PCF8576D has a very versatile display blinking capability. The whole display can blink at a frequency selected by the blink-select command (see Section 7.17). Each blink frequency is a fraction of the clock frequency; the ratio between the clock frequency and blink frequency depends on the blink mode selected (see Table 6).

An additional feature allows an arbitrary selection of LCD segments to blink in the static and 1:2 drive modes. This is implemented without any communication overheads by the output bank selector which alternates the displayed data between the data in the display RAM bank and the data in an alternative RAM bank at the blink frequency. This mode can also be implemented by the blink-select command (see Section 7.17).

In the 1:3 and 1:4 drive modes, where no alternative RAM bank is available, groups of LCD segments can blink selectively by changing the display RAM data at fixed time intervals.

The entire display can blink at a frequency other than the nominal blink frequency by sequentially resetting and setting the display enable bit E at the required rate using the mode-set command (see Section 7.17).

Table 6. Blinking frequencies[1]

Blink mode	Normal operating mode ratio	Nominal blink frequency
off	-	blinking off
1	$\frac{f_{clk}}{768}$	2 Hz
2	$\frac{f_{clk}}{1536}$	1 Hz
3	$\frac{f_{clk}}{3072}$	0.5 Hz

[1] Blink modes 1, 2 and 3 and the nominal blink frequencies 0.5 Hz, 1 Hz and 2 Hz correspond to an oscillator frequency (f_{clk}) of 1536 Hz (see Section 11).

7.16 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.16.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see Figure 13).

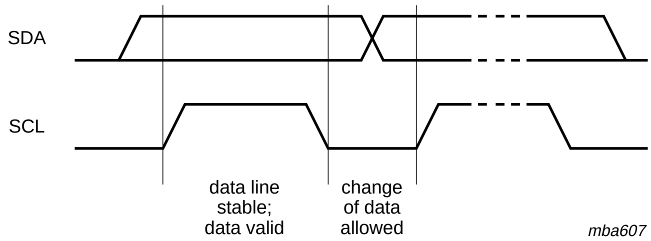


Fig 13. Bit transfer

7.16.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition - S.

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition - P (see Figure 14).

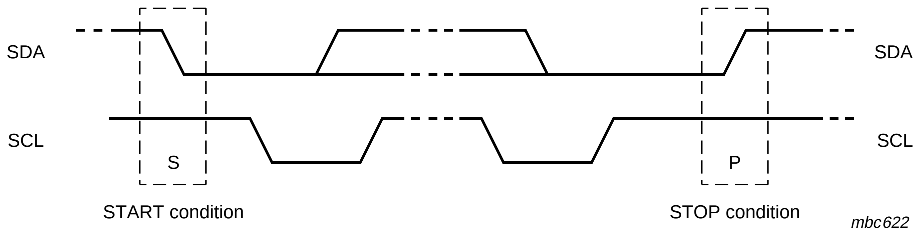


Fig 14. Definition of START and STOP conditions

7.16.3 System configuration

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves (see Figure 15).

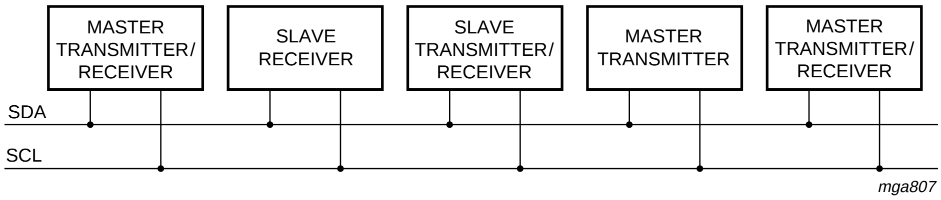


Fig 15. System configuration

7.16.4 Acknowledge

The number of data bytes that can be transferred from transmitter to receiver between the START and STOP conditions is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH-level signal on the bus that is asserted by the transmitter during which time the master generates an extra acknowledge related clock pulse. An addressed slave receiver must generate an acknowledge after receiving each byte. Also a master receiver must generate an acknowledge after receiving each byte that has been clocked out of the slave transmitter. The acknowledging device must pull-down the SDA line during the acknowledge clock pulse so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition (see Figure 16).

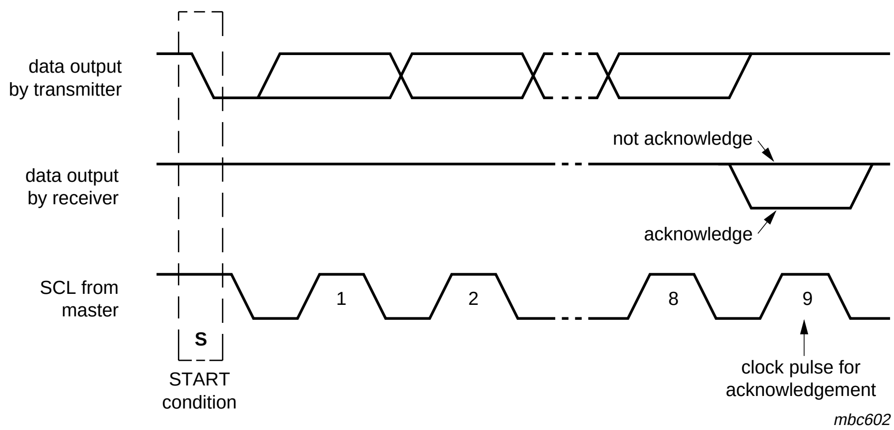


Fig 16. Acknowledgement of the I²C-bus

7.16.5 I²C-bus controller

The PCF8576D acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the PCF8576D are the acknowledge signals of the selected devices. Device selection depends on the I²C-bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are tied to V_{SS} or V_{DD} in accordance with a binary coding scheme such that no two devices with a common I^{2}C-bus slave address have the same hardware subaddress.

7.16.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.16.7 I^{2}C-bus protocol

Two I^{2}C-bus slave addresses (0111 000 and 0111 001) are reserved for the PCF8576D. The least significant bit of the slave address that a PCF8576D will respond to is defined by the level tied to its SA0 input. The PCF8576D is a write-only device and will not respond to a read access. Having two reserved slave addresses allows the following on the same I^{2}C-bus:

- Up to 16 PCF8576Ds for very large LCD applications
- The use of two types of LCD multiplex drive.

The I^{2}C-bus protocol is shown in Figure 17. The sequence is initiated with a START condition (S) from the I^{2}C-bus master which is followed by one of two possible PCF8576D slave addresses available. All PCF8576Ds whose SA0 inputs correspond to bit 0 of the slave address respond by asserting an acknowledge in parallel. This I^{2}C-bus transfer is ignored by all PCF8576Ds whose SA0 inputs are set to the alternative level.

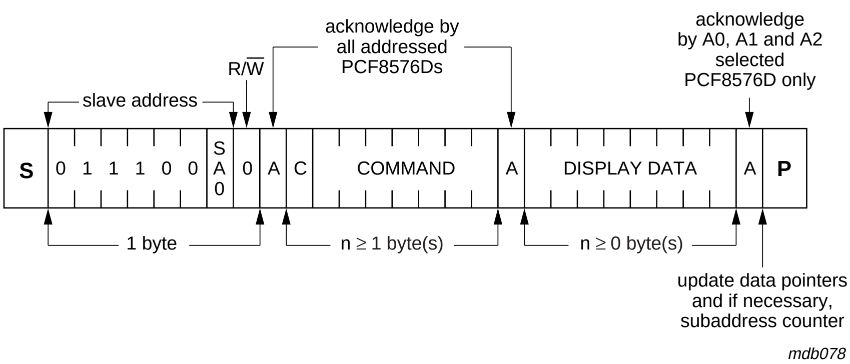


Fig 17. I^{2}C-bus protocol

After an acknowledgement, one or more command bytes follow, that define the status of each addressed PCF8576D.

The last command byte sent is identified by resetting its most significant bit, continuation bit C, (see Figure 18). The command bytes are also acknowledged by all addressed PCF8576Ds on the bus.

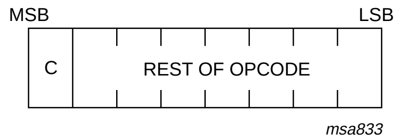


Fig 18. Format of command byte

After the last command byte, one or more display data bytes may follow. Display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data directed to the intended PCF8576D device.

An acknowledgement after each byte is asserted only by the PCF8576Ds that are addressed via address lines A0, A1 and A2. After the last display byte, the I^{2}C-bus master asserts a STOP condition (P). Alternately a START may be asserted to restart an I^{2}C-bus access.

7.17 Command decoder

The command decoder identifies command bytes that arrive on the I^{2}C-bus.

The commands available to the PCF8576D are defined in Table 7.

Table 7. Definition of PCF8576D commands

Command	Operation Code								Reference
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
mode-set	C	1	0	[1]	E	B	M1	M0	Table 9
load-data-pointer	C	0	P5	P4	P3	P2	P1	P0	Table 10
device-select	C	1	1	0	0	A2	A1	A0	Table 11
bank-select	C	1	1	1	1	0	I	O	Table 12
blink-select	C	1	1	1	0	A	BF1	BF0	Table 13

[1] Not used.

All available commands carry a continuation bit C in their most significant bit position as shown in Figure 18. When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If this bit is reset, it indicates that the command byte is the last in the transfer. Further bytes will be regarded as display data (see Table 8).

Table 8. C bit description

Bit	Symbol	Value	Description
7	C		**continue bit**
		0	last control byte in the transfer; next byte will be regarded as display data
		1	control bytes continue; next byte will be a command too

Table 9. Mode-set command bits description

Bit	Symbol	Value	Description
7	C	0, 1	see Table 8
6, 5	-	10	fixed value
4	-	-	unused
3	E		**display status**
		0	disabled (blank)[1]
		1	enabled
2	B		**LCD bias configuration**
		0	$\frac{1}{3}$ bias
		1	$\frac{1}{2}$ bias
1 to 0	M[1:0]		**LCD drive mode selection**
		01	static; BP0
		10	1:2 multiplex; BP0, BP1
		11	1:3 multiplex; BP0, BP1, BP2
		00	1:4 multiplex; BP0, BP1, BP2, BP3

[1] The possibility to disable the display allows implementation of blinking under external control.

Table 10. Load-data-pointer command bits description

Bit	Symbol	Value	Description
7	C	0, 1	see Table 8
6	-	0	fixed value
5 to 0	P[5:0]	000000 to 100111	6 bit binary value, 0 to 39; transferred to the data pointer to define one of forty display RAM addresses

Table 11. Device-select command bits description

Bit	Symbol	Value	Description
7	C	0, 1	see Table 8
6 to 3	-	1100	fixed value
2 to 0	A[2:0]	000 to 111	3 bit binary value, 0 to 7; transferred to the subaddress counter to define one of eight hardware subaddresses

Table 12. Bank-select command bits description

Bit	Symbol	Value	Description	
			Static	1:2 multiplex[1]
7	C	0, 1	see Table 8	
6 to 2	-	11110	fixed value	
1	I		**input bank selection**; storage of arriving display data	
		0	RAM bit 0	RAM bits 0 and 1
		1	RAM bit 2	RAM bits 2 and 3
0	O		**output bank selection**; retrieval of LCD display data	
		0	RAM bit 0	RAM bits 0 and 1
		1	RAM bit 2	RAM bits 2 and 3

[1] The bank-select command has no effect in 1:3 and 1:4 multiplex drive modes.

Table 13. Blink-select command bits description

Bit	Symbol	Value	Description
7	C	0, 1	see Table 8
6 to 3	-	1110	fixed value
2	A		**blink mode selection**
		0	normal blinking[1]
		1	alternate RAM bank blinking[2]
1 to 0	BF[1:0]		**blink frequency selection**
		00	off
		01	1
		10	2
		11	3

[1] Normal blinking is assumed when the LCD multiplex drive modes 1:3 or 1:4 are selected.

[2] Alternating RAM bank blinking does not apply in 1:3 and 1:4 multiplex drive modes.

7.18 Display controller

The display controller executes the commands identified by the command decoder. It contains the device’s status registers and coordinates their effects. The display controller is also responsible for loading display data into the display RAM in the correct filling order.

8. Internal circuitry

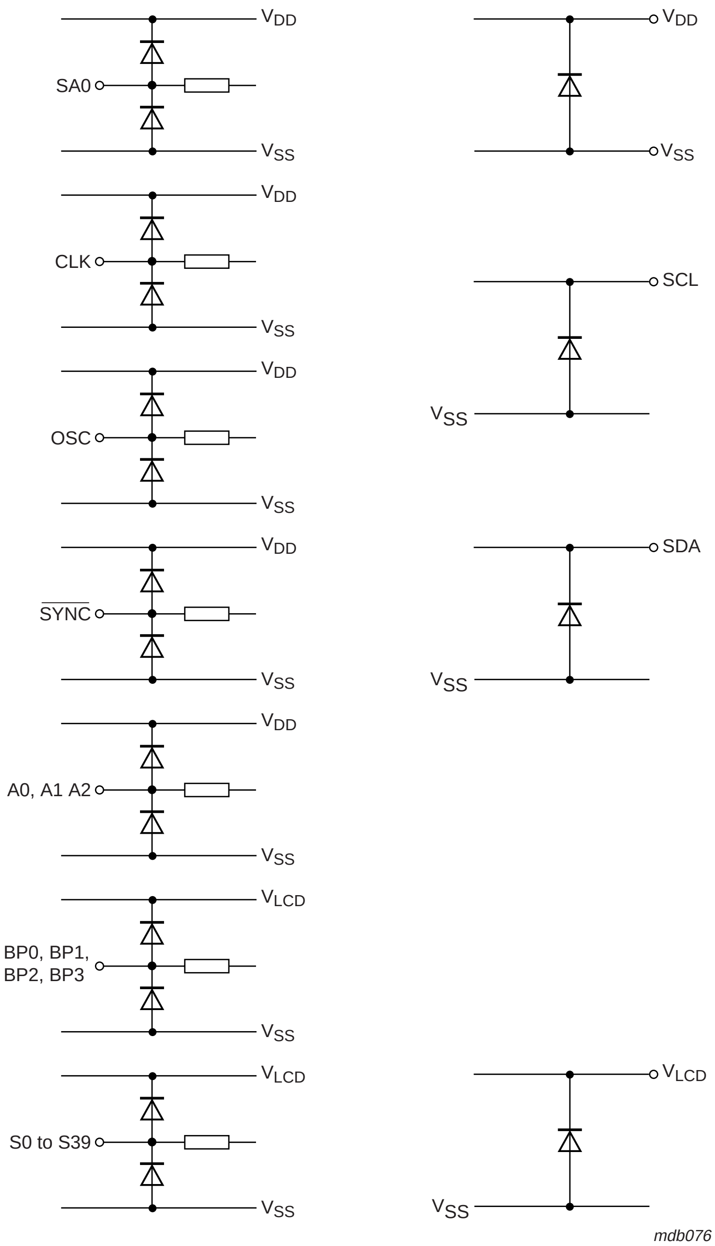


Fig 19. Device protection circuits

9. Limiting values

CAUTION

Static voltages across the liquid crystal display can build up when the LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD}) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

Table 14. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	6.5	V
V_{LCD}	LCD supply voltage			–0.5	+7.5	V
V_I	input voltage	on each of the pins CLK, SDA, SCL, $\overline{\text{SYNC}}$, SA0, OSC, A0 to A2		–0.5	+6.5	V
V_O	output voltage	on each of the pins S0 to S39, BP0 to BP3		–0.5	+7.5	V
I_I	input current			–10	+10	mA
I_O	output current			–10	+10	mA
I_{DD}	supply current			–50	+50	mA
$I_{DD(LCD)}$	LCD supply current			–50	+50	mA
I_{SS}	ground supply current			–50	+50	mA
P_{tot}	total power dissipation			-	400	mW
P_o	output power			-	100	mW
V_{esd}	electrostatic discharge voltage	HBM	[1]	-	±5000	V
		MM	[2]	-	±200	V
		CDM	[3]	-	±1000	V
I_{lu}	latch-up current		[4]	-	100	mA
T_{stg}	storage temperature		[5]	–65	+150	°C

[1] Pass level; Human Body Model (HBM) according to JESD22-A114.

[2] Pass level; Machine Model (MM), according to JESD22-A115.

[3] Pass level; Charged-Device Model (CDM), according to JESD22-C101.

[4] Pass level; latch-up testing, according to JESD78.

[5] According to the NXP store and transport conditions (document *SNW-SQ-623*) the devices have to be stored at a temperature of +5 °C to +45 °C and a humidity of 25 % to 75 %.

10. Static characteristics

Table 15. Static characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 6.5 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage			1.8	-	5.5	V
V_{LCD}	LCD supply voltage		[1]	2.5	-	6.5	V

Table 15. Static characteristics *...continued*

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 6.5 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DD}	supply current	f_{clk} = 1536 Hz	[2]	-	8	20	µA
$I_{DD(LCD)}$	LCD supply current	f_{clk} = 1536 Hz	[2]	-	24	60	µA
Logic							
$V_{P(POR)}$	power-on reset supply voltage			1.0	1.3	1.6	V
V_{IL}	LOW-level input voltage	on pins CLK, $\overline{\text{SYNC}}$, OSC, A0 to A2, SA0, SCL, SDA		V_{SS}	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage	on pins CLK, $\overline{\text{SYNC}}$, OSC, A0 to A2, SA0, SCL, SDA	[3][4]	$0.7V_{DD}$	-	V_{DD}	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 5 V					
		on pins CLK and $\overline{\text{SYNC}}$		1	-	-	mA
		on pin SDA		3	-	-	mA
$I_{OH(CLK)}$	HIGH-level output current on pin CLK	V_{OH} = 4.6 V; V_{DD} = 5 V		–1	-	-	mA
I_L	leakage current	V_I = V_{DD} or V_{SS}; on pins CLK, SCL, SDA, A0 to A2 and SA0		–1	-	+1	µA
$I_{L(OSC)}$	leakage current on pin OSC	V_I = V_{DD}		–1	-	+1	µA
C_I	input capacitance		[5]	-	-	7	pF
LCD outputs							
ΔV_O	output voltage variation	on pins BP0 - BP3 and S0 - S39		–100	-	+100	mV
R_O	output resistance	V_{LCD} = 5 V	[6]				
		on pins BP0 to BP3		-	1.5	-	kΩ
		on pins S0 to S39		-	6.0	-	kΩ

[1] V_{LCD} > 3 V for ⅓ bias.

[2] LCD outputs are open-circuit; inputs at V_{SS} or V_{DD}; external clock with 50 % duty factor; I^2C-bus inactive.

[3] When tested, I^2C pins SCL and SDA have no diode to V_{DD} and may be driven to the V_I limiting values given in Table 14 (see Figure 19 too).

[4] Propagation delay of driver between clock (CLK) and LCD driving signals.

[5] Periodically sampled, not 100 % tested.

[6] Outputs measured one at a time.

11. Dynamic characteristics

Table 16. Dynamic characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 6.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Clock							
$f_{clk(int)}$	internal clock frequency		[1]	1440	1536	2640	Hz
$f_{clk(ext)}$	external clock frequency			960	-	2640	Hz
$t_{clk(H)}$	HIGH-level clock time			60	-	-	µs
$t_{clk(L)}$	LOW-level clock time			60	-	-	µs
Synchronization							
$t_{PD(SYNC\_N)}$	$\overline{\text{SYNC}}$ propagation delay			-	30	-	ns
t_{SYNC_NL}	$\overline{\text{SYNC}}$ LOW time			1	-	-	µs
$t_{PD(drv)}$	driver propagation delay	V_{LCD} = 5 V	[2]	-	-	30	µs
I^2C-bus[3]							
Pin SCL							
f_{SCL}	SCL clock frequency			-	-	400	kHz
t_{LOW}	LOW period of the SCL clock			1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock			0.6	-	-	µs
Pin SDA							
$t_{SU;DAT}$	data set-up time			100	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	-	ns
Pins SCL and SDA							
t_{BUF}	bus free time between a STOP and START condition			1.3	-	-	µs
$t_{SU;STO}$	set-up time for STOP condition			0.6	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition			0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	-	-	µs
t_r	rise time of both SDA and SCL signals	f_{SCL} = 400 kHz		-	-	0.3	µs
		f_{SCL} < 125 kHz		-	-	1.0	µs
t_f	fall time of both SDA and SCL signals			-	-	0.3	µs
C_b	capacitive load for each bus line			-	-	400	pF
$t_{w(spike)}$	spike pulse width	on the I^2C-bus		-	-	50	ns

[1] Typical output duty factor: 50 % measured at the CLK output pin.

[2] Not tested in production.

[3] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

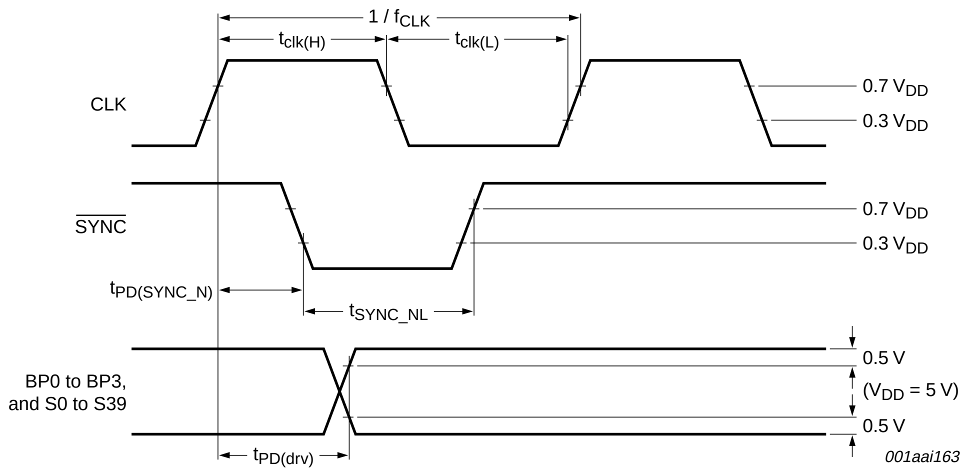


Fig 20. Driver timing waveforms

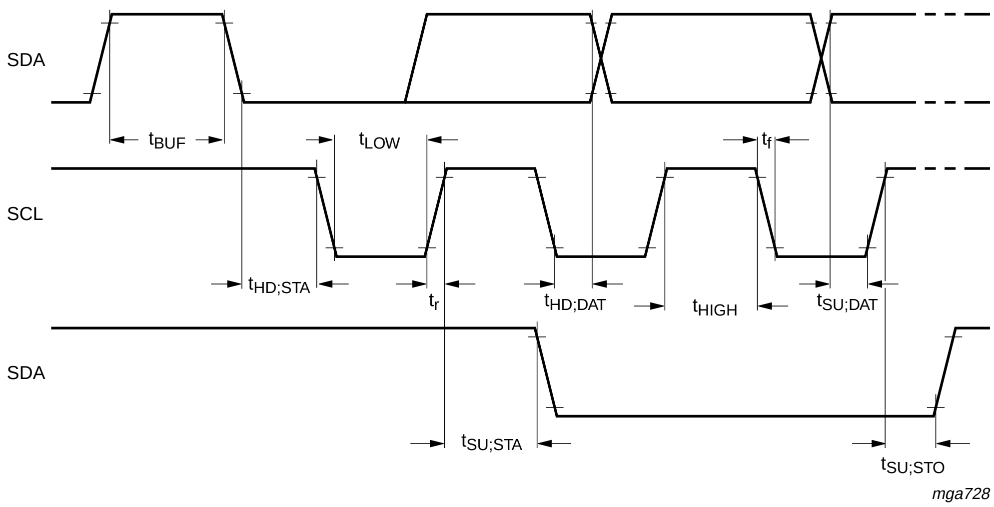


Fig 21. I^{2}C-bus timing waveforms

12. Application information

12.1 Cascaded operation

In large display configurations, up to 16 PCF8576Ds can be differentiated on the same I^2C-bus by using the 3-bit hardware subaddresses (A0, A1 and A2) and the programmable I^2C-bus slave address (SA0).

Table 17. Addressing cascaded PCF8576D

Cluster	Bit SA0	Pin A2	Pin A1	Pin A0	Device
1	0	0	0	0	0
		0	0	1	1
		0	1	0	2
		0	1	1	3
		1	0	0	4
		1	0	1	5
		1	1	0	6
		1	1	1	7
2	1	0	0	0	8
		0	0	1	9
		0	1	0	10
		0	1	1	11
		1	0	0	12
		1	0	1	13
		1	1	0	14
		1	1	1	15

PCF8576Ds connected in cascade are synchronized to allow the backplane signals from only one device in the cascade to be shared. This arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other cascaded PCF8576Ds contribute additional segment outputs but their backplane outputs are left open-circuit (see Figure 22).

All PCF8576Ds connected in cascade are correctly synchronized by the $\overline{\text{SYNC}}$ signal. This synchronization is guaranteed after the power-on reset. The only time that $\overline{\text{SYNC}}$ is likely to be needed is if synchronization is lost accidentally, for example, by noise in adverse electrical environments, or if the LCD multiplex drive mode is changed in an application using several cascaded PCF8576Ds, as the drive mode cannot be changed on all of the cascaded devices simultaneously. $\overline{\text{SYNC}}$ can be either an input or an output signal; a $\overline{\text{SYNC}}$ output is implemented as an open-drain driver with an internal pull-up resistor. The PCF8576D asserts $\overline{\text{SYNC}}$ at the start of its last active backplane signal and monitors the $\overline{\text{SYNC}}$ line at all other times. If cascade synchronization is lost, it is restored by the first PCF8576D to assert $\overline{\text{SYNC}}$. The timing relationship between the backplane waveforms and the $\overline{\text{SYNC}}$ signal for each LCD drive mode is shown in Figure 23.

The contact resistance between the SYNC on each cascaded device must be controlled. If the resistance is too high, the device is not able to synchronize properly; this is particularly applicable to chip-on-glass applications. The maximum SYNC contact resistance allowed for the number of devices in cascade is given in Table 18.

Table 18. SYNC contact resistance

Number of devices	Maximum contact resistance
2	6 kΩ
3 to 5	2.2 kΩ
6 to 10	1.2 kΩ
10 to 16	700 Ω

The PCF8576D can be cascaded with the PCF8562, the PCF8533 or the PCF8534A. This allows optimal drive selection for a given number of pixels to display. Figure 20 and Figure 21 show the timing of the synchronization signals.

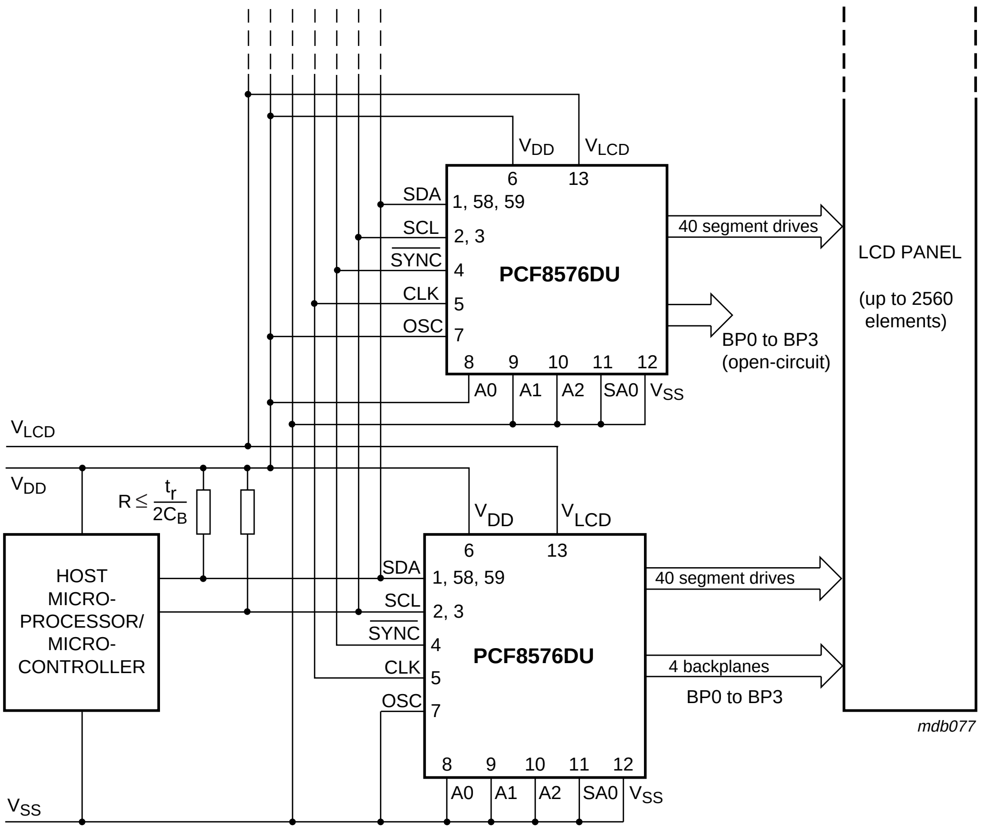


Fig 22. Cascaded PCF8576D configuration

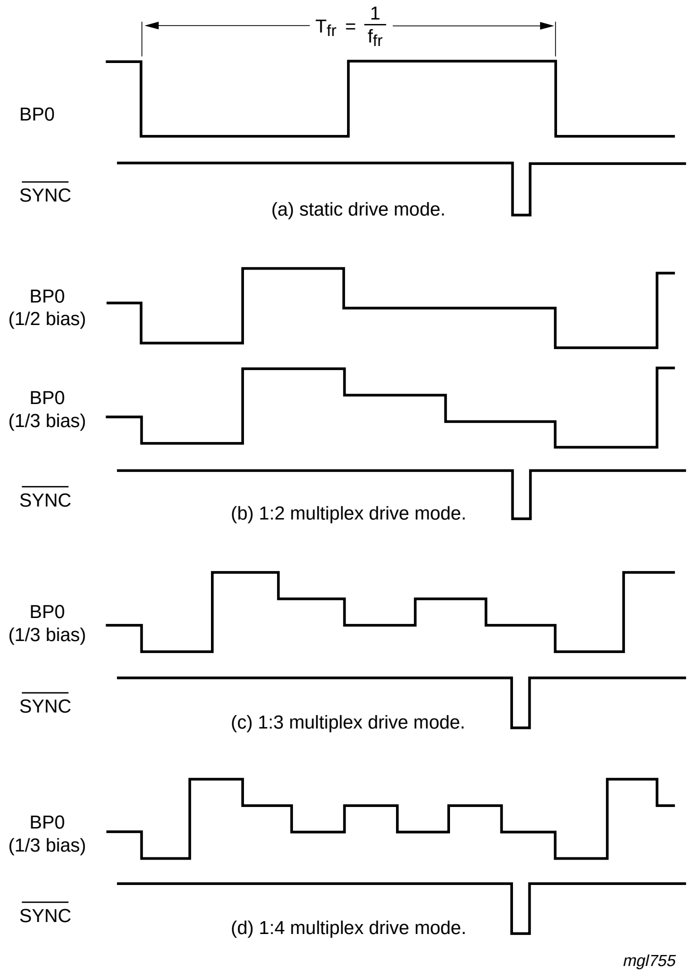
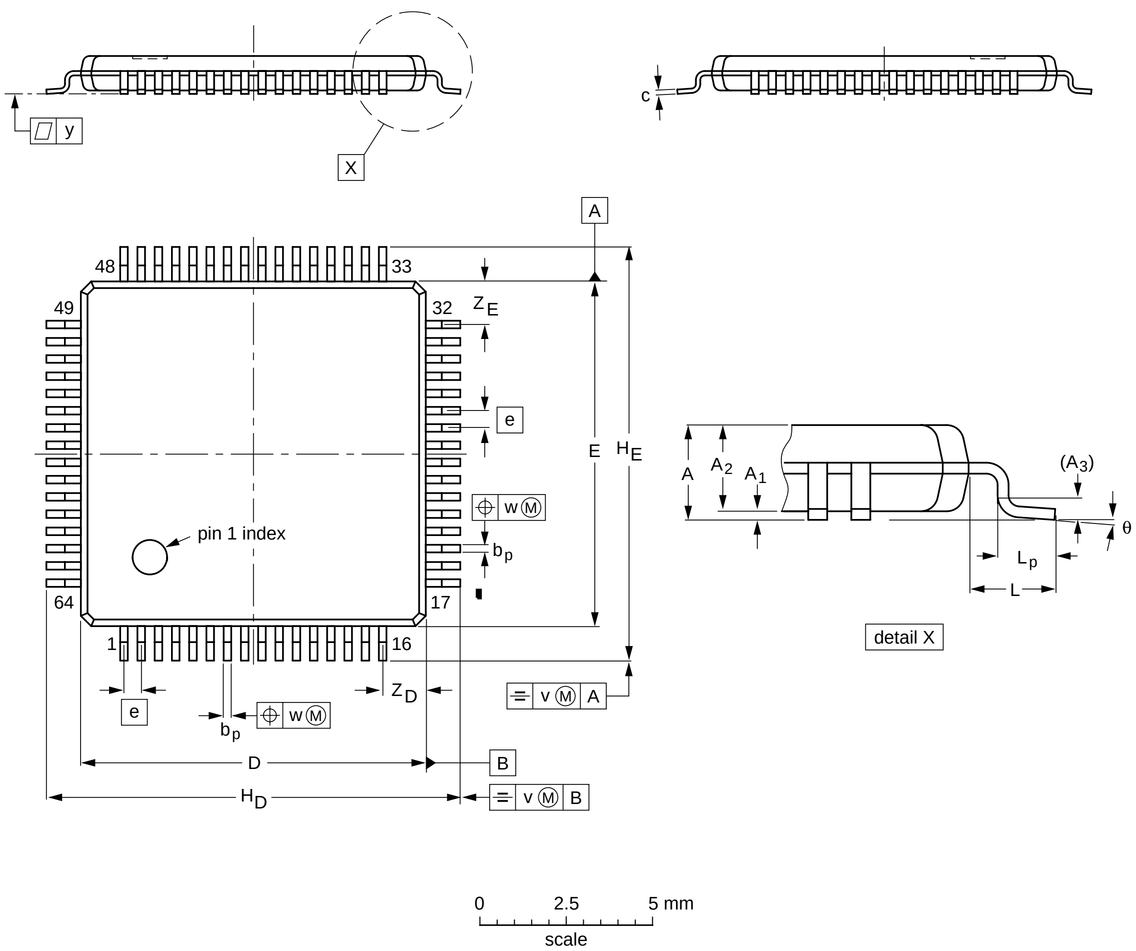


Fig 23. Synchronization of the cascade for the various PCF8576D drive modes

13. Package outline

TQFP64: plastic thin quad flat package; 64 leads; body 10 x 10 x 1.0 mm **SOT357-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_D	H_E	L	L_p	v	w	y	Z_D(1)	Z_E(1)	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.08	0.1	1.45 1.05	1.45 1.05	7° 0°

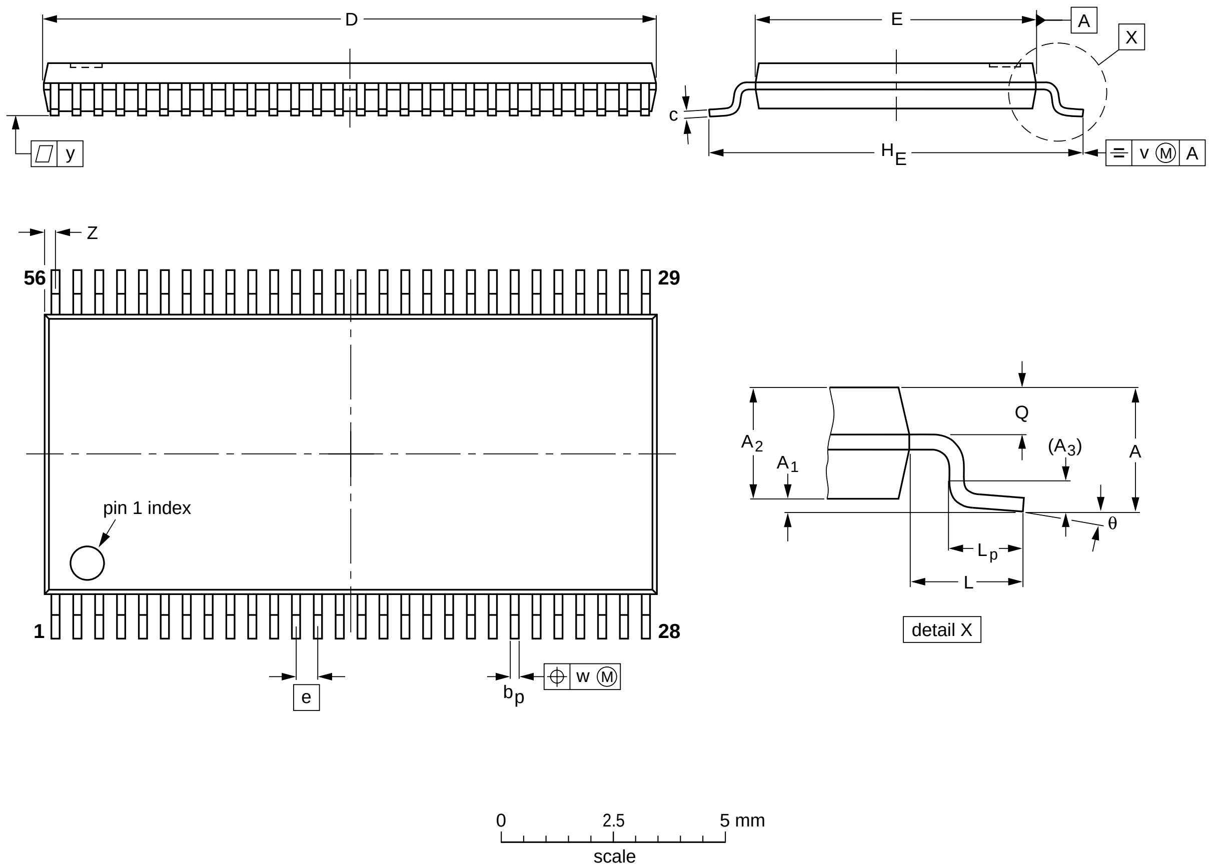
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT357-1	137E10	MS-026				~~00-01-19~~ 02-03-14

Fig 24. Package outline SOT357-1 (TQFP64)

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm **SOT364-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8^o 0^o

Notes

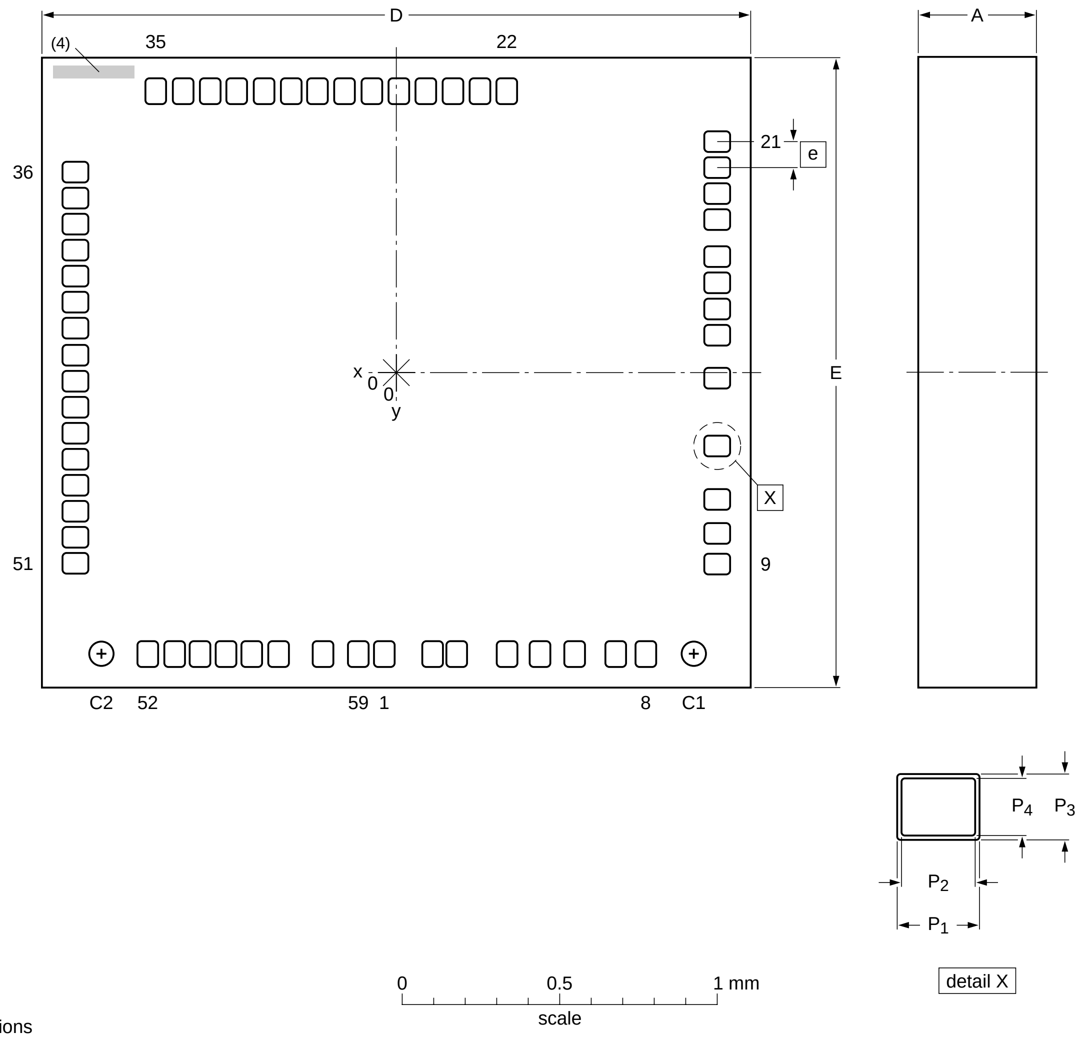
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT364-1		MO-153				~~99-12-27~~ 03-02-19

Fig 25. Package outline SOT364-1 (TSSOP56)

14. Bare die outline

Wire bond die; 59 bonding pads; 2.26 x 2.01 x 0.38 mm **PCF8576DU/DA**



Dimensions

Unit		A	D	E	$e^{(3)}$	$P_1^{(1)}$	$P_2^{(2)}$	$P_3^{(1)}$	$P_4^{(2)}$
mm	max								
	nom	0.38	2.26	2.01		0.09	0.08	0.066	0.056
	min				0.072				

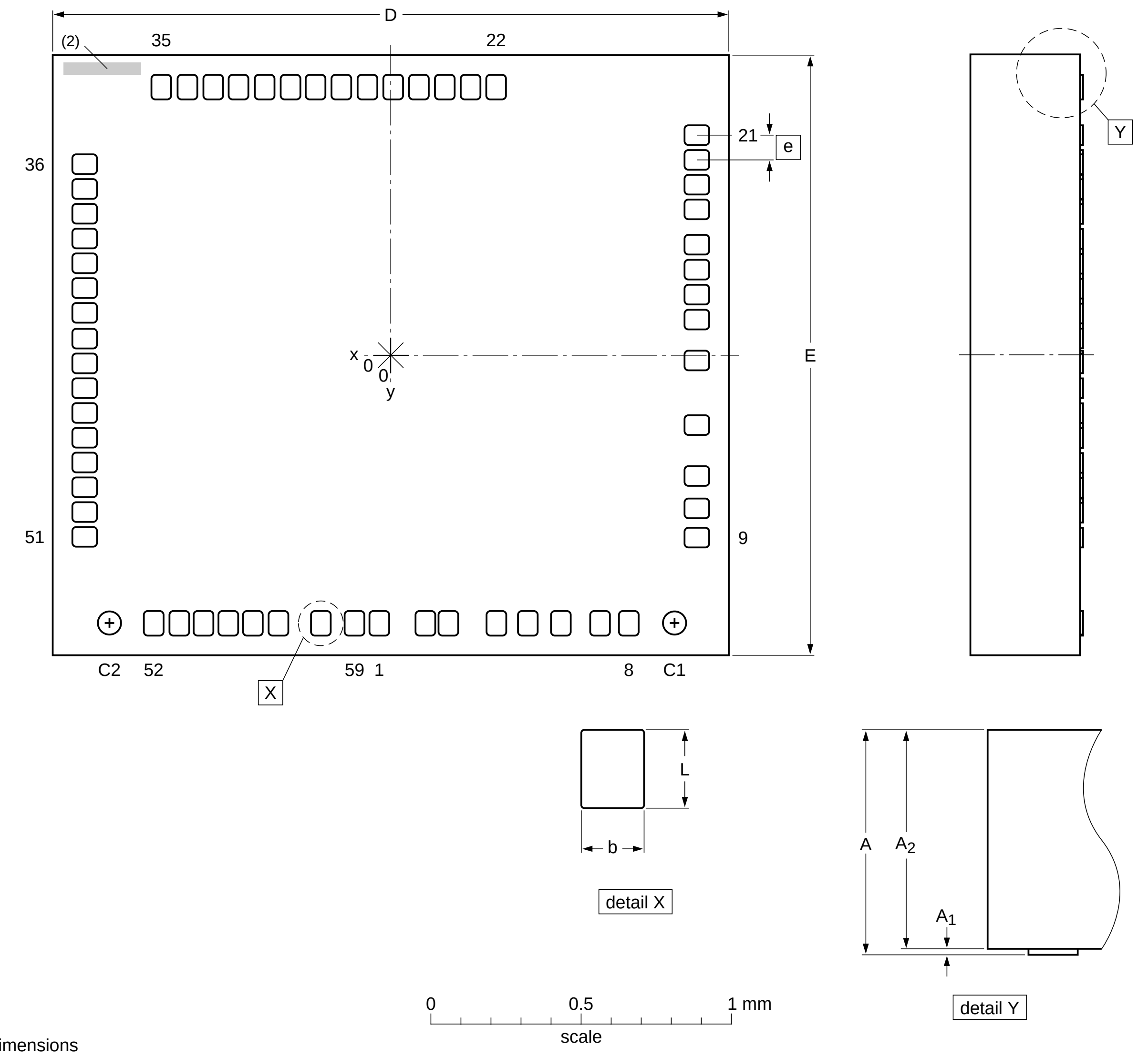
Notes
1. Pad size
2. Passivation opening
3. Dimension not drawn to scale
4. Marking code: PC8576D-2

pcf8576du_da_do

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCF8576DU/DA						~~08-10-20~~ 08-12-10

Fig 26. Bare die outline PCF8576DU/DA/2

Bare die; 59 bumps; 2.26 x 2.01 x 0.40 mm **PCF8576DU/2DA**



Dimensions

Unit		A	A_1	A_2	b	D	E	e(1)	L
mm	max								
	nom	0.40	0.015	0.381	0.052	2.26	2.01		0.077
	min							0.072	

Notes

1. Dimension not drawn to scale
2. Marking code: PC8576D-2

pcf8576du_2da_do

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCF8576DU/2DA						~~08-10-23~~ 08-12-10

Fig 27. Bare die outline PCF8576DU/2DA/2

Table 19. Bonding pad location for PCF8576DUx

All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip (see Figure 4, Figure 26 and Figure 27).

Symbol	Pad	X (μm)	Y (μm)	Description
SDA	1	–34.38	–876.6	I^2C-bus serial data input/output
SCL	2	109.53	–876.6	I^2C-bus serial clock input
SCL	3	181.53	–876.6	
$\overline{SYNC}$	4	365.58	–876.6	cascade synchronization input/output
CLK	5	469.08	–876.6	external clock input/output
V_{DD}	6	577.08	–876.6	supply voltage
OSC	7	740.88	–876.6	internal oscillator enable input
A0	8	835.83	–876.6	subaddress inputs
A1	9	1005.48	–630.9	
A2	10	1005.48	–513.9	
SA0	11	1005.48	–396.9	I^2C-bus address input; bit 0
V_{SS}	12	1005.48	–221.4	ground supply voltage
V_{LCD}	13	1005.48	10.71	LCD supply voltage
BP0	14	1005.48	156.51	LCD backplane outputs
BP2	15	1005.48	232.74	
BP1	16	1005.48	308.97	
BP3	17	1005.48	385.2	
S0	18	1005.48	493.2	LCD segment outputs
S1	19	1005.48	565.2	
S2	20	1005.48	637.2	
S3	21	1005.48	709.2	
S4	22	347.22	876.6	
S5	23	263.97	876.6	
S6	24	180.72	876.6	
S7	25	97.47	876.6	
S8	26	14.22	876.6	
S9	27	–69.03	876.6	
S10	28	–152.28	876.6	
S11	29	–235.53	876.6	
S12	30	–318.78	876.6	
S13	31	–402.03	876.6	
S14	32	–485.28	876.6	
S15	33	–568.53	876.6	
S16	34	–651.78	876.6	
S17	35	–735.03	876.6	
S18	36	–1005.5	625.59	
S19	37	–1005.5	541.62	
S20	38	–1005.5	458.19	
S21	39	–1005.5	374.76	

Table 19. Bonding pad location for PCF8576DUx *…continued*

All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip (see Figure 4, Figure 26 and Figure 27).

Symbol	Pad	X (μm)	Y (μm)	Description
S22	40	–1005.5	291.33	LCD segment outputs
S23	41	–1005.5	207.9	
S24	42	–1005.5	124.47	
S25	43	–1005.5	41.04	
S26	44	–1005.5	–42.39	
S27	45	–1005.5	–125.8	
S28	46	–1005.5	–209.3	
S29	47	–1005.5	–292.7	
S30	48	–1005.5	–376.1	
S31	49	–1005.5	–459.5	
S32	50	–1005.5	–543	
S33	51	–1005.5	–625.6	
S34	52	–735.03	–876.6	
S35	53	–663.03	–876.6	
S36	54	–591.03	–876.6	
S37	55	–519.03	–876.6	
S38	56	–447.03	–876.6	
S39	57	–375.03	–876.6	
SDA	58	–196.38	–876.6	I^2C-bus serial data input/output
SDA	59	–106.38	–876.6	

Table 20. Alignment marks

All x/y coordinates represent the position of the center of each alignment mark with respect to the center (x/y = 0) of the chip (see Figure 4, Figure 26 and Figure 27).

Symbol	X (μm)	Y (μm)
C1	930.42	–870.3
C2	–829.98	–870.3

15. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling MOS devices; see *JESD625-A and/or IEC61340-5*.

16. Packing information

16.1 Tray information

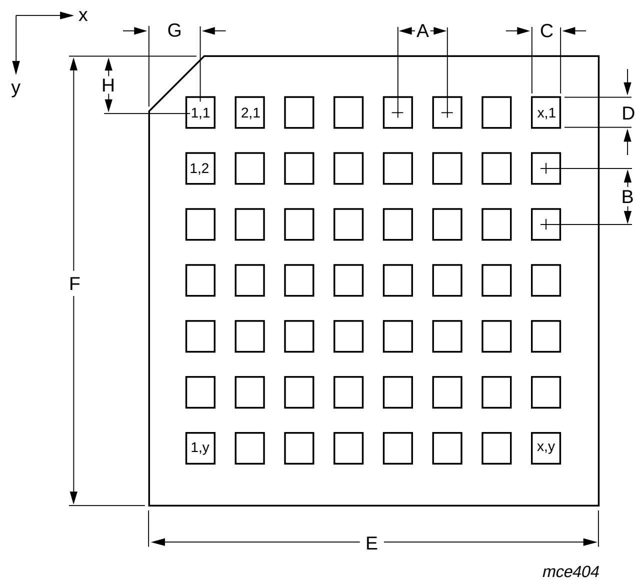


Fig 28. Tray details

Table 21. Tray dimensions (see Figure 28)

Symbol	Description	Value	Unit
A	pocket pitch in x direction	5.59	mm
B	pocket pitch in y direction	6.35	mm
C	pocket width in x direction	3.16	mm
D	pocket width in y direction	3.16	mm
E	tray width in x direction	50.8	mm
F	tray width in y direction	50.8	mm
G	cut corner to pocket 1.1 center	5.83	mm
H	cut corner to pocket 1.1 center	6.35	mm
x	number of pockets, x direction	8	-
y	number of pockets, y direction	7	-

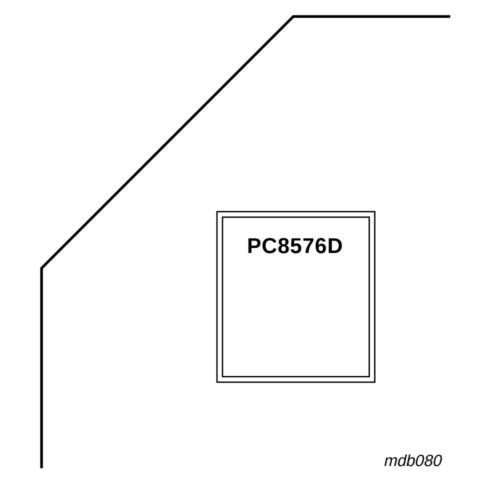


Fig 29. Tray alignment

16.2 Carrier tape information

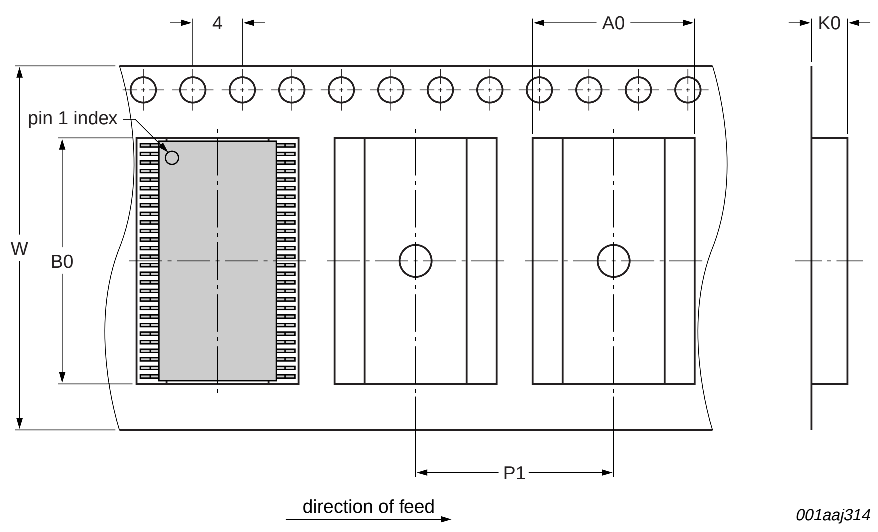


Fig 30. Tape details

Table 22. Carrier tape dimensions

Symbol	Description	Value	Unit
A0	pocket width in x direction	8.6	mm
B0	pocket width in y direction	14.5	mm
K0	pocket height	1.8	mm
P1	sprocket hole pitch	12	mm
W	tape width in y direction	24	mm

17. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 31) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 23 and 24

Table 23. SnPb eutectic process (from J-STD-020C)

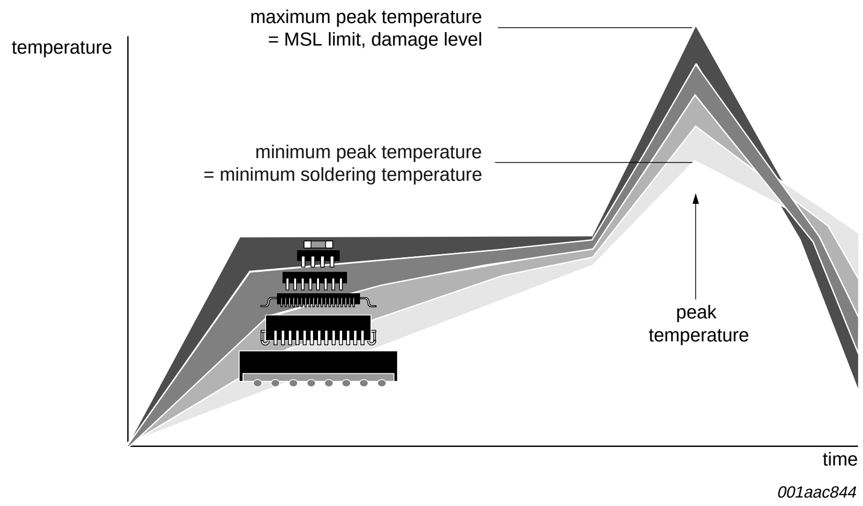
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 24. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 31.



MSL: Moisture Sensitivity Level

Fig 31. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

18. Soldering of WLCSP packages

18.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note *AN10439 “Wafer Level Chip Scale Package”* and in application note *AN10365 “Surface mount reflow soldering description”*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

18.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

18.3 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 32) than a PbSn process, thus reducing the process window

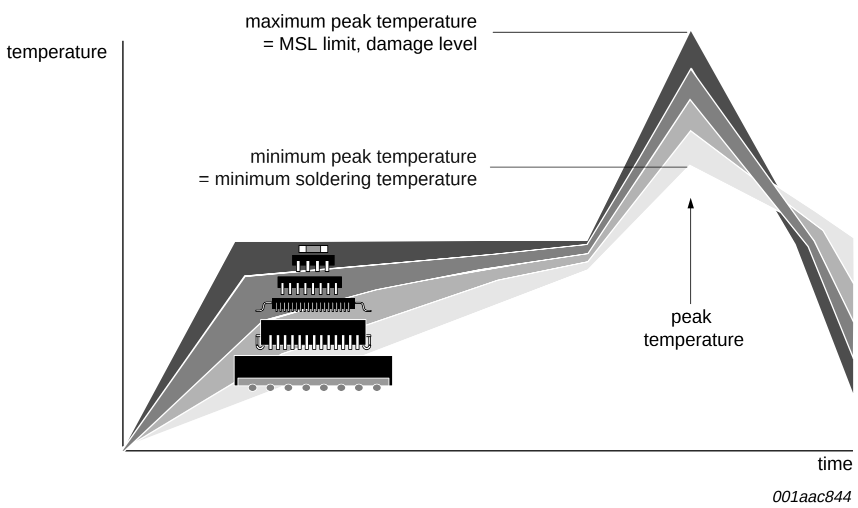
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 24

Table 25. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 32.



MSL: Moisture Sensitivity Level

Fig 32. Temperature profiles for large and small components

For further information on temperature profiles, refer to application note *AN10365 “Surface mount reflow soldering description”*.

18.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate

- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

18.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

18.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 “Surface mount reflow soldering description”*.

18.3.4 Cleaning

Cleaning can be done after reflow soldering.

19. Abbreviations

Table 26. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
CDM	Charged-Device Model
HBM	Human Body Model
ITO	Indium Tin Oxide
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
PCB	Printed Circuit Board

Table 26. Abbreviations *…continued*

Acronym	Description
RAM	Random Access Memory
RMS	Root Mean Square
SMD	Surface Mount Device
WLCSP	Wafer Level Chip-Size Package

20. Revision history

Table 27. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF8576D_7	20081218	Product data sheet	-	PCF8576D_6
Modifications:	• Added tape and reel delivery form			
PCF8576D_6	20081202	Product data sheet	-	PCF8576D_5
PCF8576D_5	20041222	Product specification	-	PCF8576D_4
PCF8576D_4	20041008	Product specification	-	PCF8576D_3
PCF8576D_3	20040617	Product specification	-	PCF8576D_2
PCF8576D_2	20030623	Product specification	-	PCF8576D_1
PCF8576D_1	20030401	Objective specification	-	-

21. Legal information

21.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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For sales office addresses, please send an email to: **salesaddresses@nxp.com**

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