

8 Pin Mini DIP and Mini DIL 5 Tap TTL Compatible Active Delay Lines

EP9458-XX & EP9458-XX-LF

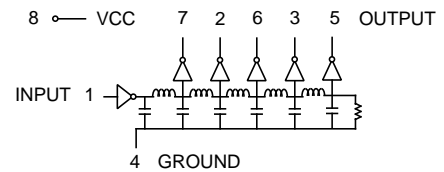
Add "-LF" after part number for Lead-Free

PCA Part Number	Tap Delays ($\pm 5\%$ or $\pm 2nS$)	Total Delay ($\pm 5\%$ or $\pm 2nS$)	PCA Part Number	Tap Delays ($\pm 5\%$ or $\pm 2nS$)	Total Delay ($\pm 5\%$ or $\pm 2nS$)
EP9458-25(-LF)	5, 10, 15, 20	25	EP9458-150(-LF)	30, 60, 90, 120	150
EP9458-30(-LF)	6, 12, 18, 24	30	EP9458-175(-LF)	35, 70, 105, 140	175
EP9458-35(-LF)	7, 14, 21, 28	35	EP9458-200(-LF)	40, 80, 120, 160	200
EP9458-40(-LF)	8, 16, 24, 32	40	EP9458-225(-LF)	45, 90, 135, 180	225
EP9458-45(-LF)	9, 18, 27, 36	45	EP9458-250(-LF)	50, 100, 150, 200	250
EP9458-50(-LF)	10, 20, 30, 40	50	EP9458-300(-LF)	60, 120, 180, 240	300
EP9458-60(-LF)	12, 24, 36, 48	60	EP9458-350(-LF)	70, 140, 210, 280	350
EP9458-75(-LF)	15, 30, 45, 60	75	EP9458-400(-LF)	80, 160, 240, 320	400
EP9458-100(-LF)	20, 40, 60, 80	100	EP9458-450(-LF)	90, 180, 270, 360	450
EP9458-125(-LF)	25, 50, 75, 100	125	EP9458-500(-LF)	100, 200, 300, 400	500

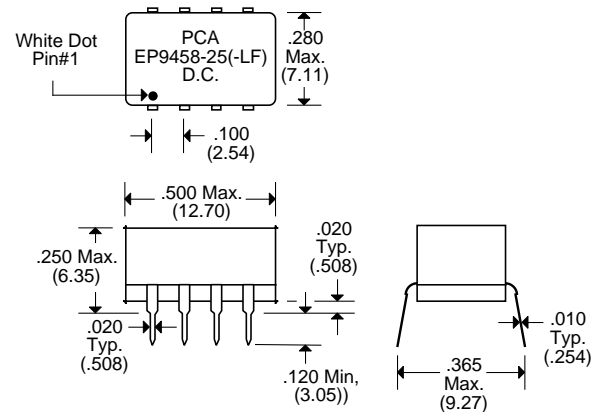
† Whichever is greater. Delay times referenced from input to leading and trailing edges at 25°C, 5.0V, with no load.

DC Electrical Characteristics			Min.	Max.	Unit
Parameter	Test Conditions				
V _{OH}	High-Level Output Voltage	V _{CC} = min. V _{IL} = max. I _{OH} = max	2.7		V
V _{OL}	Low-Level Output Voltage	V _{CC} = min. V _{IH} = min. I _{OL} = max		0.5	V
V _{IK}	Input Clamp Voltage	V _{CC} = min. I _I = I _{IK}		-1.2	V
I _{IH}	High-Level Input Current	V _{CC} = max. V _{IN} = 2.7V		50	µA
		V _{CC} = max. V _{IN} = 5.25V		1.0	mA
I _{IL}	Low-Level Input Current	V _{CC} = max. V _{IN} = 0.5V		-2	mA
I _{OS}	Short Circuit Output Current	V _{CC} = max. V _{OUT} = 0.	-40	-100	mA
		(One output at a time)			
I _{CCH}	High-Level Supply Current	V _{CC} = max. V _{IN} = OPEN		75	mA
I _{CCL}	Low-Level Supply Current	V _{CC} = max. V _{IN} = 0		75	mA
T _{RO}	Output Rise Time	T _d 500 nS (0.75 to 2.4 Volts)		4	nS
N _H	Fanout High-Level Output	V _{CC} = max. V _{OH} = 2.7V		20 TTL Load	
N _L	Fanout Low-Level Output	V _{CC} = max. V _{OL} = 0.5V		10 TTL Load	

Schematic



Package



Recommended Operating Conditions		Min.	Max.	Unit
V _{CC}	Supply Voltage	4.75	5.25	V
V _{IH}	High-Level Input Voltage	2.0		V
V _{IL}	Low-Level Input Voltage		0.8	V
I _{IK}	Input Clamp Current		-18	mA
I _{OH}	High-Level Output Current		-1.0	mA
I _{OL}	Low-Level Output Current		20	mA
PW*	Pulse Width of Total Delay	40		%
d*	Duty Cycle		40	%
T _A	Operating Free-Air Temperature	0	+70	°C

*These two values are inter-dependent.

Input Pulse Test Conditions @ 25° C			Unit
E _{IN}	Pulse Input Voltage	3.2	Volts
PW	Pulse Width % of Total Delay	110	%
T _{RI}	Pulse Rise Time (0.75 - 2.4 Volts)	2.0	nS
PRR	Pulse Repetition Rate @ T _d < 200 nS	1.0	MHz
	Pulse Repetition Rate @ T _d > 200 nS	100	KHz
V _{CC}	Supply Voltage	5.0	Volts

Notes :	EP9458-XX	EP9458-XX-LF
1. Lead Finish	SnPb	Hot Tin Dip (Sn)
2. Peak Solder Rating (Wave Solder Process)	260°C 10 (+2/-0) seconds	260°C 10 (+2/-0) seconds
4. Weight	TBD grams	TBD grams
5. Packaging Information (Tube)	TBD pieces/tube	TBD pieces/tube

Unless Otherwise Specified Dimensions are in Inches /mm ± .010 / .25