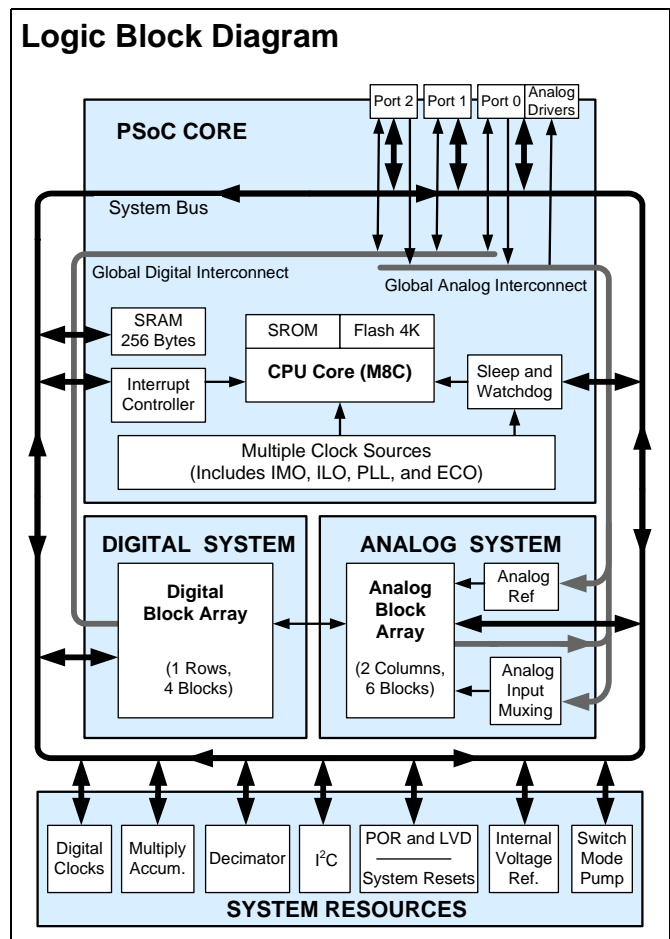


Features

- **Powerful Harvard Architecture Processor**
 - M8C Processor Speeds to 24 MHz
 - 8x8 Multiply, 32-Bit Accumulate
 - Low Power at High Speed
 - 3.0 to 5.25 V Operating Voltage
 - Operating Voltages Down to 1.0V Using On-Chip Switch Mode Pump (SMP)
 - Industrial Temperature Range: -40°C to +85°C
- **Advanced Peripherals (PSoC Blocks)**
 - Six Rail-to-Rail Analog PSoC Blocks Provide:
 - Up to 14-Bit ADCs
 - Up to 8-Bit DACs
 - Programmable Gain Amplifiers
 - Programmable Filters and Comparators
 - Four Digital PSoC Blocks Provide:
 - 8 to 32-Bit Timers, Counters, and PWMs
 - CRC and PRS Modules
 - Full-Duplex UART
 - Multiple SPI[™] Masters or Slaves
 - Connectable to all GPIO Pins
 - Complex Peripherals by Combining Blocks
- **Precision, Programmable Clocking**
 - Internal $\pm 2.5\%$ 24/48 MHz Oscillator
 - High-Accuracy 24 MHz with Optional 32 kHz Crystal and PLL
 - Optional External Oscillator, up to 24 MHz
 - Internal Oscillator for Watchdog and Sleep
- **Flexible On-Chip Memory**
 - 4K Bytes Flash Program Storage 50,000 Erase/Write Cycles
 - 256 Bytes SRAM Data Storage
 - In-System Serial Programming (ISSP[™])
 - Partial Flash Updates
 - Flexible Protection Modes
 - EEPROM Emulation in Flash
- **Programmable Pin Configurations**
 - 25 mA Sink on all GPIO
 - Pull up, Pull down, High Z, Strong, or Open Drain Drive Modes on all GPIO
 - Up to 10 Analog Inputs on GPIO
 - Two 30 mA Analog Outputs on GPIO
 - Configurable Interrupt on all GPIO
- **Additional System Resources**
 - I²C[™] Slave, Master, and Multi-Master to 400 kHz
 - Watchdog and Sleep Timers
 - User-Configurable Low Voltage Detection
 - Integrated Supervisory Circuit
 - On-Chip Precision Voltage Reference
- **Complete Development Tools**
 - Free Development Software (PSoC Designer[™])
 - Full-Featured, In-Circuit Emulator and Programmer
 - Full Speed Emulation
 - Complex Breakpoint Structure
 - 128K Bytes Trace Memory



PSoC[®] Functional Overview

The PSoC[®] family consists of many Mixed Signal Array with On-Chip Controller devices. These devices are designed to replace multiple traditional MCU-based system components with one, low cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, and programmable interconnects. This architecture allows the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable IO are included in a range of convenient pinouts and packages.

The PSoC architecture, as shown in the [Logic Block Diagram](#) on page 1, is comprised of four main areas: PSoC Core, Digital System, Analog System, and System Resources. Configurable global busing allows all the device resources to be combined into a complete custom system. The PSoC CY8C24x23 family can have up to three IO ports that connect to the global digital and analog interconnects, providing access to four digital blocks and 6 analog blocks.

PSoC Core

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIO (General Purpose IO).

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with 11 vectors, to simplify programming of real time embedded events. Program execution is timed and protected using the included Sleep and Watch Dog Timers (WDT).

Memory encompasses 4 KB of Flash for program storage, 256 bytes of SRAM for data storage, and up to 2 KB of EEPROM emulated using the Flash. Program Flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

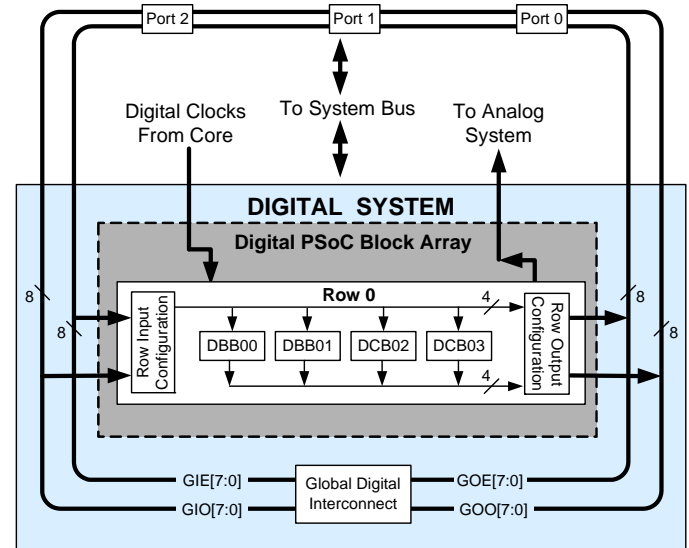
The PSoC device incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator) accurate to 2.5% over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz ILO (internal low speed oscillator) is provided for the Sleep timer and WDT. If crystal accuracy is desired, the ECO (32.768 kHz external crystal oscillator) is available for use as a Real Time Clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

Digital System

The Digital System is composed of four digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.

Figure 1. Digital System Block Diagram



Digital peripheral configurations include:

- PWMs (8 to 32 bit)
- PWMs with Dead band (8 to 32 bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8-bit with selectable parity (up to one)
- SPI master and slave (up to one)
- I2C slave and master (one available as a System Resource)
- Cyclical Redundancy Checker/Generator (8 to 32 bit)
- IrDA (up to one)
- Pseudo Random Sequence Generators (8 to 32 bit)

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows the optimum choice of system resources for your application. Family resources are listed in the table [PSoC Device Characteristics](#) on page 4.

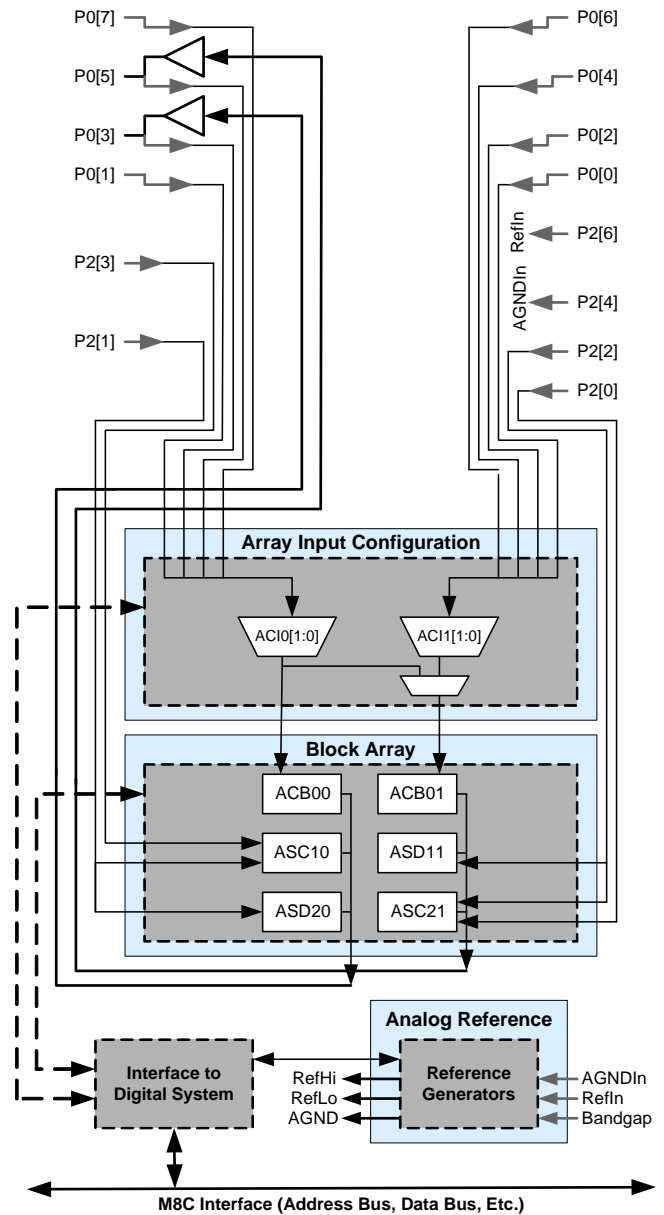
Analog System

The Analog System is composed of six configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- Analog-to-digital converters (up to two, with 6 to 14-bit resolution, selectable as Incremental, Delta Sigma, and SAR)
- Filters (two and four pole band-pass, low-pass, and notch)
- Amplifiers (up to two, with selectable gain to 48x)
- Instrumentation amplifiers (one with selectable gain to 93x)
- Comparators (up to two, with 16 selectable thresholds)
- DACs (up to two, with 6 to 9-bit resolution)
- Multiplying DACs (up to two, with 6- to 9-bit resolution)
- High current output drivers (two with 30 mA drive as a Core Resource)
- 1.3V reference (as a System Resource)
- DTMF dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are provided in columns of three, which includes one CT (Continuous Time) and two SC (Switched Capacitor) blocks. The number of blocks is dependant on the device family which is detailed in the table [PSoC Device Characteristics](#) on page 4.

Figure 2. Analog System Block Diagram



Additional System Resources

System Resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, switch mode pump, low voltage detection, and power on reset. Brief statements describing the merits of each system resource follow:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- A multiply accumulate (MAC) provides a fast 8-bit multiplier with 32-bit accumulate, to assist in both general math and digital filters.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of Delta Sigma ADCs.
- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3V reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch mode pump (SMP) generates normal operating voltages from a single 1.2V battery cell, providing a low cost boost converter.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 3 analog blocks. The following table lists the resources available for specific PSoC device groups.

Table 1. PSoC Device Characteristics

| PSoC Part Number | Digital IO | Digital Rows | Digital Blocks | Analog Inputs | Analog Outputs | Analog Columns | Analog Blocks |
|------------------|-----------------|--------------|----------------|---------------|----------------|----------------|---------------|
| CY8C29x66 | up to 64 | 4 | 16 | 12 | 4 | 4 | 12 |
| CY8C27x66 | up to 44 | 2 | 8 | 12 | 4 | 4 | 12 |
| CY8C27x43 | up to 44 | 2 | 8 | 12 | 4 | 4 | 12 |
| CY8C24x23 | up to 24 | 1 | 4 | 12 | 2 | 2 | 6 |
| CY8C22x13 | up to 16 | 1 | 4 | 8 | 1 | 1 | 3 |

Getting Started

The quickest path to understanding the PSoC silicon is by reading this data sheet and using the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications. For in-depth information, along with detailed programming information, refer the PSoC Programmable System-on-Chip Technical Reference Manual.

For up-to-date Ordering, Packaging, and Electrical Specification information, refer the latest PSoC device data sheets on the web at <http://www.cypress.com/psoc>.

Development Kits

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store contains development kits, C compilers, and all accessories for PSoC development. Go to the Cypress Online Store web site at <http://www.cypress.com>, click the Online Store shopping cart icon at the bottom of the web page, and click *PSoC (Programmable System-on-Chip)* to view a current list of available items.

Technical Training

Free PSoC technical training is available for beginners and is taught by a marketing or application engineer over the phone. PSoC training classes cover designing, debugging, advanced analog, and application-specific classes covering topics, such as PSoC and the LIN bus. Go to <http://www.cypress.com>, click on Design Support located on the left side of the web page, and select Technical Training for more details.

Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to <http://www.cypress.com>, click on Design Support located on the left side of the web page, and select CYPros Consultants.

Technical Support

PSoC application engineers take pride in fast and accurate response. They can be reached with a 4-hour guaranteed response at <http://www.cypress.com/support>.

Application Notes

A long list of application notes can assist you in every aspect of your design effort. To view the PSoC application notes, go to the <http://www.cypress.com> web site and select Application Notes under the Design Resources list located in the center of the web page. Application notes are listed by date as default.

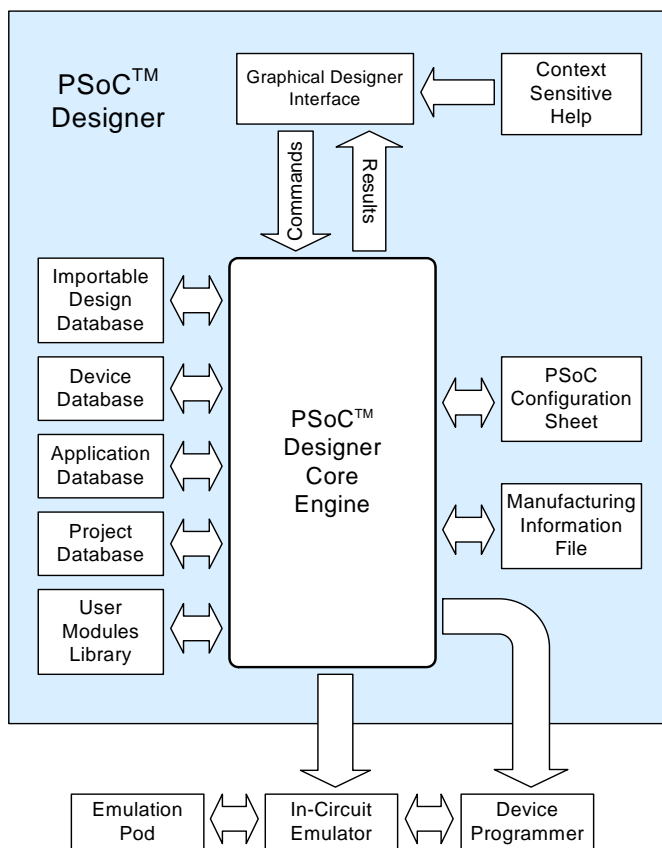
Development Tools

The Cypress MicroSystems PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE and application runs on Windows 98, Windows NT 4.0, Windows 2000, Windows Millennium (Me), or Windows XP (refer Figure 3).

PSoC Designer helps the customer to select an operating configuration for the PSoC, write application code that uses the PSoC, and debug the application. This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and the CYASM macro assembler for the CPUs.

PSoC Designer also supports a high-level C language compiler developed specifically for the devices in the family.

Figure 3. PSoC Designer Subsystems



PSoC Designer Software Subsystems

Device Editor

The Device Editor subsystem allows the user to select different onboard analog and digital components called user modules using the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

PSoC Designer sets up power on initialization tables for selected PSoC block configurations and creates source code for an application framework. The framework contains software to operate the selected components and, if the project uses more than one operating configuration, contains routines to switch between different sets of PSoC block configurations at run time. PSoC Designer can print out a configuration sheet for a given project configuration for use during application programming in conjunction with the Device Data Sheet. After the framework is generated, the user can add application-specific code to flesh out the framework. It is also possible to change the selected components and regenerate the framework.

Design Browser

The Design Browser allows users to select and import preconfigured designs into the user's project. Users can easily browse a catalog of preconfigured designs to facilitate time-to-design. Examples provided in the tools include a 300-baud modem, LIN Bus master and slave, fan controller, and magnetic card reader.

Application Editor

In the Application Editor you can edit your C language and Assembly language source code. You can also assemble, compile, link, and build.

Assembler. The macro assembler allows the assembly code to be merged seamlessly with C code. The link libraries automatically use absolute addressing or can be compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compiler. A C language compiler is available that supports Cypress MicroSystems' PSoC family devices. Even if you have never worked in the C language before, the product quickly allows you to create complete C programs for the PSoC family devices.

The embedded, optimizing C compiler provides all the features of C tailored to the PSoC architecture. It comes complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing the designer to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write IO registers, read and write CPU registers, set and clear break-points, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

Hardware Tools

In-Circuit Emulator

A low cost, high functionality ICE (In-Circuit Emulator) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of the parallel or USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

Figure 4. PSoC Development Tool Kit



User Modules and the PSoC Development Process

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. Each block has several registers that determine its function and connectivity to other blocks, multiplexers, buses and to the IO pins. Iterative development cycles permit you to adapt the hardware as well as the software. This substantially lowers the risk of having to select a different part to meet the final design requirements.

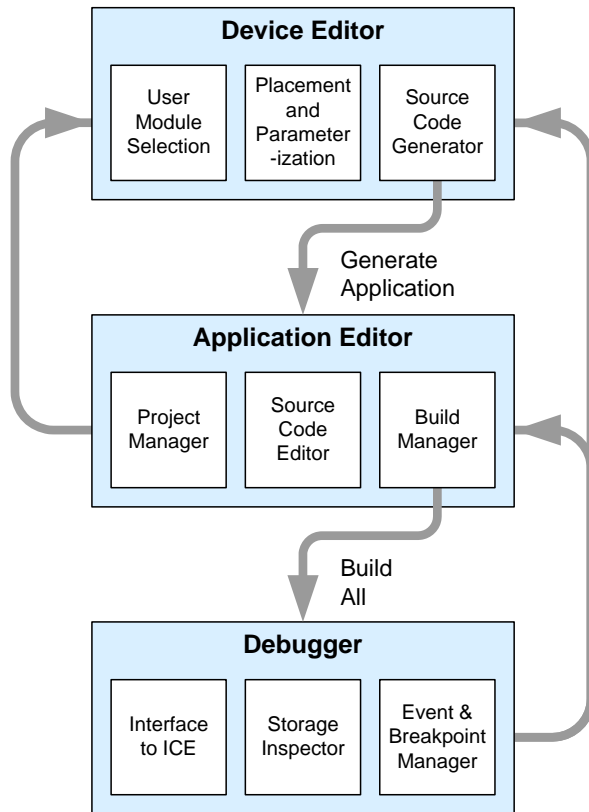
To speed the development process, the PSoC Designer Integrated Development Environment (IDE) provides a library of pre-built, pre-tested hardware peripheral functions, called "User Modules." User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and mixed signal varieties. The standard User Module library contains over 50 common peripherals such as ADCs, DACs Timers, Counters, UARTs, and other not-so common peripherals such as DTMF Generators and Bi-Quad analog filter sections.

Each user module establishes the basic register settings that implement the selected function. It also provides parameters that allow you to tailor its precise configuration to your particular application. For example, a Pulse Width Modulator User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. User modules also provide tested software to cut your development time. The user module application programming interface (API) provides high-level functions to control and respond to hardware events at run-time. The API also provides optional interrupt service routines that you can adapt as needed.

The API functions are documented in user module data sheets that are viewed directly in the PSoC Designer IDE. These data sheets explain the internal operation of the user module and provide performance specifications. Each data sheet describes the use of each user module parameter and documents the setting of each register controlled by the user module.

The development process starts when you open a new project and bring up the Device Editor, a pictorial environment (GUI) for configuring the hardware. You pick the user modules you need for your project and map them onto the PSoC blocks with point-and-click simplicity. Next, you build signal chains by inter-connecting user modules to each other and the IO pins. At this stage, you also configure the clock source connections and enter parameter values directly or by selecting values from drop-down menus. When you are ready to test the hardware configuration or move on to developing code for the project, you perform the "Generate Application" step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the high-level user module API functions.

Figure 5. User Module and Source Code Development Flows



The next step is to write your main program, and any sub-routines using PSoC Designer's Application Editor subsystem. The Application Editor includes a Project Manager that allows you to open the project source code files (including all generated code files) from a hierarchal view. The source code editor provides syntax coloring and advanced edit features for both C and assembly language. File search capabilities include simple string searches and recursive "grep-style" patterns. A single mouse click invokes the Build Manager. It employs a professional-strength "makefile" system to automatically analyze all file dependencies and run the compiler and assembler as necessary. Project-level options control optimization strategies used by the compiler and linker. Syntax errors are displayed in a console window. Double clicking the error message takes you directly to the offending line of source code. When all is correct, the linker builds a ROM file image suitable for programming.

The last step in the development process takes place inside the PSoC Designer's Debugger subsystem. The Debugger downloads the ROM image to the In-Circuit Emulator (ICE) where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Document Conventions

Acronyms Used

The following table lists the acronyms that are used in this document.

Table 2. Acronyms

| Acronym | Description |
|---------|-----------------------------------------------------|
| AC | alternating current |
| ADC | analog-to-digital converter |
| API | application programming interface |
| CPU | central processing unit |
| CT | continuous time |
| DAC | digital-to-analog converter |
| DC | direct current |
| EEPROM | electrically erasable programmable read-only memory |
| FSR | full scale range |
| GPIO | general purpose IO |
| IO | input/output |
| IPOR | imprecise power on reset |
| LSb | least-significant bit |
| LVD | low voltage detect |
| MSb | most-significant bit |
| PC | program counter |
| POR | power on reset |
| PPOR | precision power on reset |
| PSoC® | Programmable System-on-Chip |
| PWM | pulse width modulator |
| RAM | random access memory |
| ROM | read only memory |
| SC | switched capacitor |
| SMP | switch mode pump |

Units of Measure

A units of measure table is located in the Electrical Specifications section. Table 7 on page 11 lists all the abbreviations used to measure the PSoC devices.

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h' or 'b' are decimal.

Pinouts

The CY8C24x23 PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital IO. However, Vss, Vdd, SMP, and XRES are not capable of Digital IO.

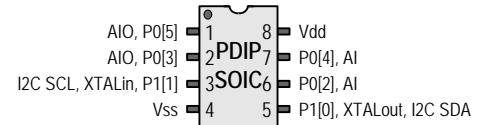
8-Pin Part Pinout

Table 3. 8-Pin Part Pinout (PDIP, SOIC)

| Pin No. | Type | | Pin Name | Description |
|---------|---------|--------|----------|-------------------------------------------------|
| | Digital | Analog | | |
| 1 | IO | IO | P0[5] | Analog column mux input and column output |
| 2 | IO | IO | P0[3] | Analog column mux input and column output |
| 3 | IO | | P1[1] | Crystal Input (XTALin), I2C Serial Clock (SCL) |
| 4 | Power | | Vss | Ground connection |
| 5 | IO | | P1[0] | Crystal Output (XTALout), I2C Serial Data (SDA) |
| 6 | IO | I | P0[2] | Analog column mux input |
| 7 | IO | I | P0[4] | Analog column mux input |
| 8 | Power | | Vdd | Supply voltage |

LEGEND: A = Analog, I = Input, and O = Output.

Figure 6. CY8C24123 8-Pin PSoC Device



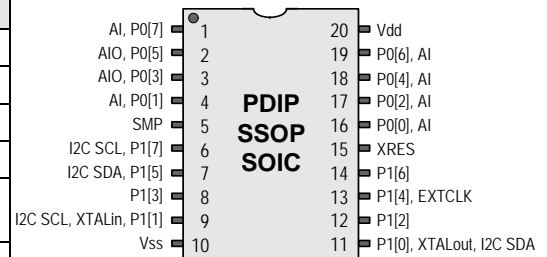
20-Pin Part Pinout

Table 4. 20-Pin Part Pinout (PDIP, SSOP, SOIC)

| Pin No. | Type | | Pin Name | Description |
|---------|---------|--------|----------|-------------------------------------------------------------------|
| | Digital | Analog | | |
| 1 | IO | I | P0[7] | Analog column mux input |
| 2 | IO | IO | P0[5] | Analog column mux input and column output |
| 3 | IO | IO | P0[3] | Analog column mux input and column output |
| 4 | IO | I | P0[1] | Analog column mux input |
| 5 | Power | | SMP | Switch Mode Pump (SMP) connection to external components required |
| 6 | IO | | P1[7] | I2C Serial Clock (SCL) |
| 7 | IO | | P1[5] | I2C Serial Data (SDA) |
| 8 | IO | | P1[3] | |
| 9 | IO | | P1[1] | Crystal Input (XTALin), I2C Serial Clock (SCL) |
| 10 | Power | | Vss | Ground connection |
| 11 | IO | | P1[0] | Crystal Output (XTALout), I2C Serial Data (SDA) |
| 12 | IO | | P1[2] | |
| 13 | IO | | P1[4] | Optional External Clock Input (EXTCLK) |
| 14 | IO | | P1[6] | |
| 15 | Input | | XRES | Active high external reset with internal pull down |
| 16 | IO | I | P0[0] | Analog column mux input |
| 17 | IO | I | P0[2] | Analog column mux input |
| 18 | IO | I | P0[4] | Analog column mux input |
| 19 | IO | I | P0[6] | Analog column mux input |
| 20 | Power | | Vdd | Supply voltage |

LEGEND: A = Analog, I = Input, and O = Output.

Figure 7. CY8C24223 20-Pin PSoC Device



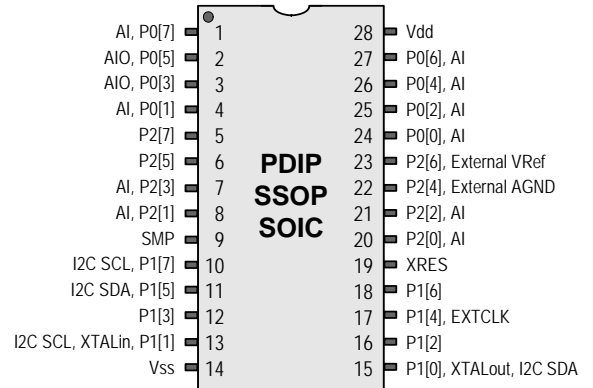
28-Pin Part Pinout

Table 5. 28-Pin Part Pinout (PDIP, SSOP, SOIC)

| Pin No. | Type | | Pin Name | Description |
|---------|---------|--------|----------|-------------------------------------------------------------------|
| | Digital | Analog | | |
| 1 | IO | I | P0[7] | Analog column mux input |
| 2 | IO | IO | P0[5] | Analog column mux input and column output |
| 3 | IO | IO | P0[3] | Analog column mux input and column output |
| 4 | IO | I | P0[1] | Analog column mux input. |
| 5 | IO | | P2[7] | |
| 6 | IO | | P2[5] | |
| 7 | IO | I | P2[3] | Direct switched capacitor block input |
| 8 | IO | I | P2[1] | Direct switched capacitor block input |
| 9 | Power | | SMP | Switch Mode Pump (SMP) connection to external components required |
| 10 | IO | | P1[7] | I2C Serial Clock (SCL) |
| 11 | IO | | P1[5] | I2C Serial Data (SDA) |
| 12 | IO | | P1[3] | |
| 13 | IO | | P1[1] | Crystal Input (XTALin), I2C Serial Clock (SCL) |
| 14 | Power | | Vss | Ground connection |
| 15 | IO | | P1[0] | Crystal Output (XTALout), I2C Serial Data (SDA) |
| 16 | IO | | P1[2] | |
| 17 | IO | | P1[4] | Optional External Clock Input (EXTCLK) |
| 18 | IO | | P1[6] | |
| 19 | Input | | XRES | Active high external reset with internal pull down |
| 20 | IO | I | P2[0] | Direct switched capacitor block input |
| 21 | IO | I | P2[2] | Direct switched capacitor block input |
| 22 | IO | | P2[4] | External Analog Ground (AGND) |
| 23 | IO | | P2[6] | External Voltage Reference (VRef) |
| 24 | IO | I | P0[0] | Analog column mux input |
| 25 | IO | I | P0[2] | Analog column mux input |
| 26 | IO | I | P0[4] | Analog column mux input |
| 27 | IO | I | P0[6] | Analog column mux input |
| 28 | Power | | Vdd | Supply voltage |

LEGEND: A = Analog, I = Input, and O = Output.

Figure 8. CY8C24423 28-Pin PSOC Device



32-Pin Part Pinout

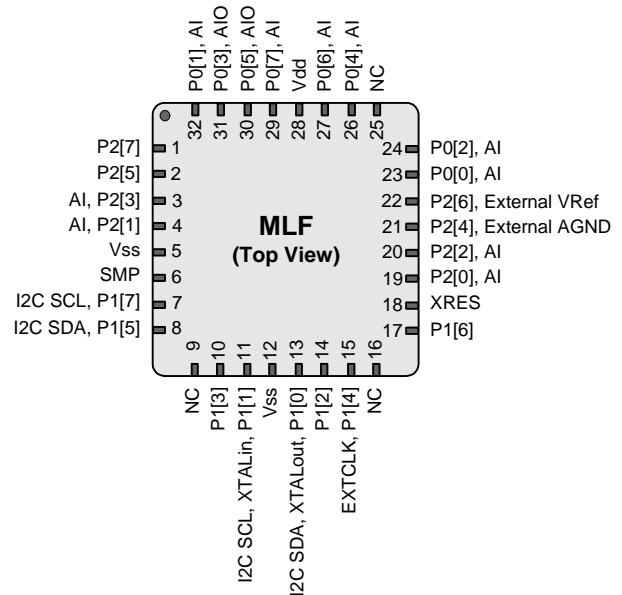
Table 6. 32-Pin Part Pinout (MLF*)

| Pin No. | Type | | Pin Name | Description |
|---------|---------|--------|----------|-------------------------------------------------------------------|
| | Digital | Analog | | |
| 1 | IO | | P2[7] | |
| 2 | IO | | P2[5] | |
| 3 | IO | I | P2[3] | Direct switched capacitor block input |
| 4 | IO | I | P2[1] | Direct switched capacitor block input |
| 5 | Power | | Vss | Ground connection |
| 6 | Power | | SMP | Switch Mode Pump (SMP) connection to external components required |
| 7 | IO | | P1[7] | I2C Serial Clock (SCL) |
| 8 | IO | | P1[5] | I2C Serial Data (SDA) |
| 9 | | | NC | No connection. Do not use. |
| 10 | IO | | P1[3] | |
| 11 | IO | | P1[1] | Crystal Input (XTALin), I2C Serial Clock (SCL) |
| 12 | Power | | Vss | Ground connection |
| 13 | IO | | P1[0] | Crystal Output (XTALout), I2C Serial Data (SDA) |
| 14 | IO | | P1[2] | |
| 15 | IO | | P1[4] | Optional External Clock Input (EXTCLK) |
| 16 | | | NC | No connection. Do not use. |
| 17 | IO | | P1[6] | |
| 18 | Input | | XRES | Active high external reset with internal pull down |
| 19 | IO | I | P2[0] | Direct switched capacitor block input |
| 20 | IO | I | P2[2] | Direct switched capacitor block input |
| 21 | IO | | P2[4] | External Analog Ground (AGND) |
| 22 | IO | | P2[6] | External Voltage Reference (VRef) |
| 23 | IO | I | P0[0] | Analog column mux input |
| 24 | IO | I | P0[2] | Analog column mux input |
| 25 | | | NC | No connection. Do not use. |
| 26 | IO | I | P0[4] | Analog column mux input |
| 27 | IO | I | P0[6] | Analog column mux input |
| 28 | Power | | Vdd | Supply voltage |
| 29 | IO | I | P0[7] | Analog column mux input |
| 30 | IO | IO | P0[5] | Analog column mux input and column output |
| 31 | IO | IO | P0[3] | Analog column mux input and column output |
| 32 | IO | I | P0[1] | Analog column mux input |

LEGEND: A = Analog, I = Input, and O = Output.

* The MLF package has a center pad that must be connected to the same ground as the Vss pin.

Figure 9. CY8C24423 32-Pin PSoC Device



Register Reference

This section lists the registers of the CY8C27xxx PSoC device by way of mapping tables, in offset order. For detailed register information, reference the *PSoC Programmable System-on-Chip Technical Reference Manual*.

Register Conventions

Abbreviations Used

The register conventions specific to this section are listed in the following table.

Table 7. Abbreviations

| Convention | Description |
|------------|-----------------------------------|
| RW | Read and write register or bit(s) |
| R | Read register or bit(s) |
| W | Write register or bit(s) |
| L | Logical register or bit(s) |
| C | Clearable register or bit(s) |
| # | Access is bit specific |

Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is also referred to as IO space and is broken into two parts. The XOI bit in the Flag register determines which bank the user is currently in. When the XOI bit is set, the user is said to be in the “extended” address space or the “configuration” registers.

Note In the following register mapping tables, blank fields are Reserved and must not be accessed.

Table 8. Register Map Bank 0 Table: User Space

| Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access |
|----------|--------------|--------|---------|--------------|--------|----------|--------------|--------|----------|--------------|--------|
| PRT0DR | 00 | RW | | 40 | | ASC10CR0 | 80 | RW | | C0 | |
| PRT0IE | 01 | RW | | 41 | | ASC10CR1 | 81 | RW | | C1 | |
| PRT0GS | 02 | RW | | 42 | | ASC10CR2 | 82 | RW | | C2 | |
| PRT0DM2 | 03 | RW | | 43 | | ASC10CR3 | 83 | RW | | C3 | |
| PRT1DR | 04 | RW | | 44 | | ASD11CR0 | 84 | RW | | C4 | |
| PRT1IE | 05 | RW | | 45 | | ASD11CR1 | 85 | RW | | C5 | |
| PRT1GS | 06 | RW | | 46 | | ASD11CR2 | 86 | RW | | C6 | |
| PRT1DM2 | 07 | RW | | 47 | | ASD11CR3 | 87 | RW | | C7 | |
| PRT2DR | 08 | RW | | 48 | | | 88 | | | C8 | |
| PRT2IE | 09 | RW | | 49 | | | 89 | | | C9 | |
| PRT2GS | 0A | RW | | 4A | | | 8A | | | CA | |
| PRT2DM2 | 0B | RW | | 4B | | | 8B | | | CB | |
| | 0C | | | 4C | | | 8C | | | CC | |
| | 0D | | | 4D | | | 8D | | | CD | |
| | 0E | | | 4E | | | 8E | | | CE | |
| | 0F | | | 4F | | | 8F | | | CF | |
| | 10 | | | 50 | | ASD20CR0 | 90 | RW | | D0 | |
| | 11 | | | 51 | | ASD20CR1 | 91 | RW | | D1 | |
| | 12 | | | 52 | | ASD20CR2 | 92 | RW | | D2 | |
| | 13 | | | 53 | | ASD20CR3 | 93 | RW | | D3 | |
| | 14 | | | 54 | | ASC21CR0 | 94 | RW | | D4 | |
| | 15 | | | 55 | | ASC21CR1 | 95 | RW | | D5 | |
| | 16 | | | 56 | | ASC21CR2 | 96 | RW | I2C_CFG | D6 | RW |
| | 17 | | | 57 | | ASC21CR3 | 97 | RW | I2C_SCR | D7 | # |
| | 18 | | | 58 | | | 98 | | I2C_DR | D8 | RW |
| | 19 | | | 59 | | | 99 | | I2C_MSCR | D9 | # |
| | 1A | | | 5A | | | 9A | | INT_CLR0 | DA | RW |
| | 1B | | | 5B | | | 9B | | INT_CLR1 | DB | RW |
| | 1C | | | 5C | | | 9C | | | DC | |
| | 1D | | | 5D | | | 9D | | INT_CLR3 | DD | RW |
| | 1E | | | 5E | | | 9E | | INT_MSK3 | DE | RW |
| | 1F | | | 5F | | | 9F | | | DF | |
| DBB00DR0 | 20 | # | AMX_IN | 60 | RW | | A0 | | INT_MSK0 | E0 | RW |
| DBB00DR1 | 21 | W | | 61 | | | A1 | | INT_MSK1 | E1 | RW |
| DBB00DR2 | 22 | RW | | 62 | | | A2 | | INT_VC | E2 | RC |
| DBB00CR0 | 23 | # | ARF_CR | 63 | RW | | A3 | | RES_WDT | E3 | W |
| DBB01DR0 | 24 | # | CMP_CR0 | 64 | # | | A4 | | DEC_DH | E4 | RC |
| DBB01DR1 | 25 | W | ASY_CR | 65 | # | | A5 | | DEC_DL | E5 | RC |
| DBB01DR2 | 26 | RW | CMP_CR1 | 66 | RW | | A6 | | DEC_CR0 | E6 | RW |
| DBB01CR0 | 27 | # | | 67 | | | A7 | | DEC_CR1 | E7 | RW |
| DCB02DR0 | 28 | # | | 68 | | | A8 | | MUL_X | E8 | W |
| DCB02DR1 | 29 | W | | 69 | | | A9 | | MUL_Y | E9 | W |
| DCB02DR2 | 2A | RW | | 6A | | | AA | | MUL_DH | EA | R |
| DCB02CR0 | 2B | # | | 6B | | | AB | | MUL_DL | EB | R |
| DCB03DR0 | 2C | # | | 6C | | | AC | | ACC_DR1 | EC | RW |
| DCB03DR1 | 2D | W | | 6D | | | AD | | ACC_DR0 | ED | RW |

Blank fields are Reserved and must not be accessed.

Access is bit specific.

Table 8. Register Map Bank 0 Table: User Space (continued)

| Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access |
|----------|--------------|--------|----------|--------------|--------|---------|--------------|--------|----------|--------------|--------|
| DCB03DR2 | 2E | RW | | 6E | | | AE | | ACC_DR3 | EE | RW |
| DCB03CR0 | 2F | # | | 6F | | | AF | | ACC_DR2 | EF | RW |
| | 30 | | ACB00CR3 | 70 | RW | RDI0RI | B0 | RW | | F0 | |
| | 31 | | ACB00CR0 | 71 | RW | RDI0SYN | B1 | RW | | F1 | |
| | 32 | | ACB00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| | 33 | | ACB00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| | 34 | | ACB01CR3 | 74 | RW | RDI0LT1 | B4 | RW | | F4 | |
| | 35 | | ACB01CR0 | 75 | RW | RDI0RO0 | B5 | RW | | F5 | |
| | 36 | | ACB01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| | 37 | | ACB01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| | 38 | | | 78 | | | B8 | | | F8 | |
| | 39 | | | 79 | | | B9 | | | F9 | |
| | 3A | | | 7A | | | BA | | | FA | |
| | 3B | | | 7B | | | BB | | | FB | |
| | 3C | | | 7C | | | BC | | | FC | |
| | 3D | | | 7D | | | BD | | | FD | |
| | 3E | | | 7E | | | BE | | CPU_SCR1 | FE | # |
| | 3F | | | 7F | | | BF | | CPU_SCR0 | FF | # |

Blank fields are Reserved and must not be accessed.

Access is bit specific.

Table 9. Register Map Bank 1 Table: Configuration Space

| Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access |
|---------|--------------|--------|------|--------------|--------|----------|--------------|--------|----------|--------------|--------|
| PRT0DM0 | 00 | RW | | 40 | | ASC10CR0 | 80 | RW | | C0 | |
| PRT0DM1 | 01 | RW | | 41 | | ASC10CR1 | 81 | RW | | C1 | |
| PRT0IC0 | 02 | RW | | 42 | | ASC10CR2 | 82 | RW | | C2 | |
| PRT0IC1 | 03 | RW | | 43 | | ASC10CR3 | 83 | RW | | C3 | |
| PRT1DM0 | 04 | RW | | 44 | | ASD11CR0 | 84 | RW | | C4 | |
| PRT1DM1 | 05 | RW | | 45 | | ASD11CR1 | 85 | RW | | C5 | |
| PRT1IC0 | 06 | RW | | 46 | | ASD11CR2 | 86 | RW | | C6 | |
| PRT1IC1 | 07 | RW | | 47 | | ASD11CR3 | 87 | RW | | C7 | |
| PRT2DM0 | 08 | RW | | 48 | | | 88 | | | C8 | |
| PRT2DM1 | 09 | RW | | 49 | | | 89 | | | C9 | |
| PRT2IC0 | 0A | RW | | 4A | | | 8A | | | CA | |
| PRT2IC1 | 0B | RW | | 4B | | | 8B | | | CB | |
| | 0C | | | 4C | | | 8C | | | CC | |
| | 0D | | | 4D | | | 8D | | | CD | |
| | 0E | | | 4E | | | 8E | | | CE | |
| | 0F | | | 4F | | | 8F | | | CF | |
| | 10 | | | 50 | | ASD20CR0 | 90 | RW | GDI_O_IN | D0 | RW |
| | 11 | | | 51 | | ASD20CR1 | 91 | RW | GDI_E_IN | D1 | RW |
| | 12 | | | 52 | | ASD20CR2 | 92 | RW | GDI_O_OU | D2 | RW |
| | 13 | | | 53 | | ASD20CR3 | 93 | RW | GDI_E_OU | D3 | RW |
| | 14 | | | 54 | | ASC21CR0 | 94 | RW | | D4 | |
| | 15 | | | 55 | | ASC21CR1 | 95 | RW | | D5 | |
| | 16 | | | 56 | | ASC21CR2 | 96 | RW | | D6 | |

Blank fields are Reserved and must not be accessed.

Access is bit specific.

Table 9. Register Map Bank 1 Table: Configuration Space (continued)

| Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access |
|---------|--------------|--------|----------|--------------|--------|----------|--------------|--------|-----------|--------------|--------|
| | 17 | | | 57 | | ASC21CR3 | 97 | RW | | D7 | |
| | 18 | | | 58 | | | 98 | | | D8 | |
| | 19 | | | 59 | | | 99 | | | D9 | |
| | 1A | | | 5A | | | 9A | | | DA | |
| | 1B | | | 5B | | | 9B | | | DB | |
| | 1C | | | 5C | | | 9C | | | DC | |
| | 1D | | | 5D | | | 9D | | OSC_GO_EN | DD | RW |
| | 1E | | | 5E | | | 9E | | OSC_CR4 | DE | RW |
| | 1F | | | 5F | | | 9F | | OSC_CR3 | DF | RW |
| DBB00FN | 20 | RW | CLK_CR0 | 60 | RW | | A0 | | OSC_CR0 | E0 | RW |
| DBB00IN | 21 | RW | CLK_CR1 | 61 | RW | | A1 | | OSC_CR1 | E1 | RW |
| DBB00OU | 22 | RW | ABF_CR0 | 62 | RW | | A2 | | OSC_CR2 | E2 | RW |
| | 23 | | AMD_CR0 | 63 | RW | | A3 | | VLT_CR | E3 | RW |
| DBB01FN | 24 | RW | | 64 | | | A4 | | VLT_CMP | E4 | R |
| DBB01IN | 25 | RW | | 65 | | | A5 | | | E5 | |
| DBB01OU | 26 | RW | AMD_CR1 | 66 | RW | | A6 | | | E6 | |
| | 27 | | ALT_CR0 | 67 | RW | | A7 | | | E7 | |
| DCB02FN | 28 | RW | | 68 | | | A8 | | IMO_TR | E8 | W |
| DCB02IN | 29 | RW | | 69 | | | A9 | | ILO_TR | E9 | W |
| DCB02OU | 2A | RW | | 6A | | | AA | | BDG_TR | EA | RW |
| | 2B | | | 6B | | | AB | | ECO_TR | EB | W |
| DCB03FN | 2C | RW | | 6C | | | AC | | | EC | |
| DCB03IN | 2D | RW | | 6D | | | AD | | | ED | |
| DCB03OU | 2E | RW | | 6E | | | AE | | | EE | |
| | 2F | | | 6F | | | AF | | | EF | |
| | 30 | | ACB00CR3 | 70 | RW | RDI0RI | B0 | RW | | F0 | |
| | 31 | | ACB00CR0 | 71 | RW | RDI0SYN | B1 | RW | | F1 | |
| | 32 | | ACB00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| | 33 | | ACB00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| | 34 | | ACB01CR3 | 74 | RW | RDI0LT1 | B4 | RW | | F4 | |
| | 35 | | ACB01CR0 | 75 | RW | RDI0RO0 | B5 | RW | | F5 | |
| | 36 | | ACB01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| | 37 | | ACB01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| | 38 | | | 78 | | | B8 | | | F8 | |
| | 39 | | | 79 | | | B9 | | | F9 | |
| | 3A | | | 7A | | | BA | | | FA | |
| | 3B | | | 7B | | | BB | | | FB | |
| | 3C | | | 7C | | | BC | | | FC | |
| | 3D | | | 7D | | | BD | | | FD | |
| | 3E | | | 7E | | | BE | | CPU_SCR1 | FE | # |
| | 3F | | | 7F | | | BF | | CPU_SCR0 | FF | # |

Blank fields are Reserved and must not be accessed.

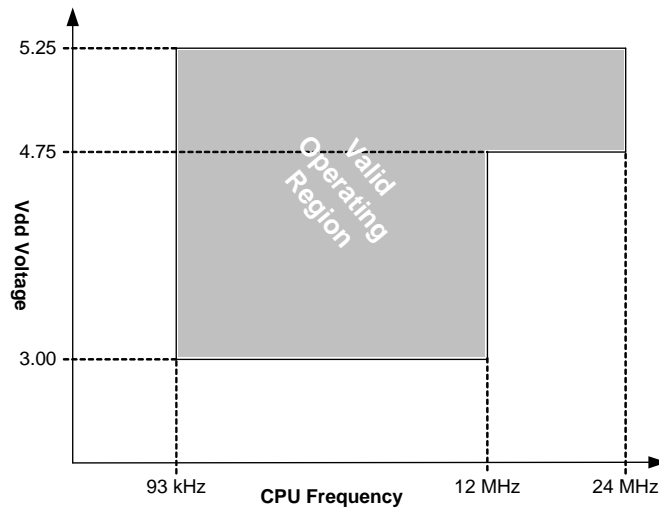
Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C24x23 PSoC device. For latest electrical specifications, <http://www.cypress.com>.

Specifications are valid for $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ and $T_J \leq 100^{\circ}\text{C}$, except where noted. Specifications for devices running at greater than 12 MHz are valid for $-40^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ and $T_J \leq 82^{\circ}\text{C}$.

Figure 10. Voltage versus Operating Frequency



The following table lists the units of measure that are used in this section.

Table 10. Units of Measure

| Symbol | Unit of Measure | Symbol | Unit of Measure |
|--------|------------------------------|--------|-------------------------------|
| °C | degree Celsius | μW | micro watts |
| dB | decibels | mA | milli-ampere |
| fF | femto farad | ms | milli-second |
| Hz | hertz | mV | milli-volts |
| KB | 1024 bytes | nA | nano ampere |
| Kbit | 1024 bits | ns | nanosecond |
| kHz | kilohertz | nV | nanovolts |
| kΩ | kilohm | W | ohm |
| MHz | megahertz | pA | pico ampere |
| MΩ | megaohm | pF | pico farad |
| μA | micro ampere | pp | peak-to-peak |
| μF | micro farad | ppm | parts per million |
| μH | micro henry | ps | picosecond |
| μs | microsecond | sps | samples per second |
| μV | micro volts | s | sigma: one standard deviation |
| μVrms | micro volts root-mean-square | V | volts |

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 11. Absolute Maximum Ratings

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-------------------|---------------------------------------------------------------|-----------------------|-----|-----------------------|-------|---------------------------------------------------------|
| T _{STG} | Storage Temperature | -55 | – | +100 | °C | Higher storage temperatures reduce data retention time. |
| T _A | Ambient Temperature with Power Applied | -40 | – | +85 | °C | |
| V _{dd} | Supply Voltage on V _{dd} Relative to V _{ss} | -0.5 | – | +6.0 | V | |
| V _{IO} | DC Input Voltage | V _{ss} - 0.5 | – | V _{dd} + 0.5 | V | |
| – | DC Voltage Applied to Tri-state | V _{ss} - 0.5 | – | V _{dd} + 0.5 | V | |
| I _{MIO} | Maximum Current into any Port Pin | -25 | – | +50 | mA | |
| I _{MAIO} | Maximum Current into any Port Pin Configured as Analog Driver | -50 | – | +50 | mA | |
| – | Static Discharge Voltage | 2000 | – | – | V | |
| – | Latch-up Current | – | – | 200 | mA | |

Operating Temperature

Table 12. Operating Temperature

| Symbol | Description | Min | Typ | Max | Units | Notes |
|----------------|----------------------|-----|-----|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| T _A | Ambient Temperature | -40 | – | +85 | °C | |
| T _J | Junction Temperature | -40 | – | +100 | °C | The temperature rise from ambient to junction is package specific. See Thermal Impedances per Package on page 41. The user must limit the power consumption to comply with this requirement. |

DC Electrical Characteristics

DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 13. DC Chip-Level Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------------|--------------------------------------------------------------------------------------------------------------|-------|-----|-------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| V _{DD} | Supply Voltage | 3.00 | – | 5.25 | V | |
| I _{DD} | Supply Current | – | 5 | 8 | mA | Conditions are V _{DD} = 5.0V, 25 °C, CPU = 3 MHz, 48 MHz disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz. |
| I _{DD3} | Supply Current | – | 3.3 | 6.0 | mA | Conditions are V _{DD} = 3.3V, T _A = 25 °C, CPU = 3 MHz, 48 MHz = Disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz. |
| I _{SB} | Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT. ^a | – | 3 | 6.5 | μA | Conditions are with internal slow speed oscillator, V _{DD} = 3.3V, $-40^{\circ}\text{C} \leq T_A \leq 55^{\circ}\text{C}$. |
| I _{SBH} | Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT at high temperature. ^a | – | 4 | 25 | μA | Conditions are with internal slow speed oscillator, V _{DD} = 3.3V, $55^{\circ}\text{C} < T_A \leq 85^{\circ}\text{C}$. |
| I _{SBXTL} | Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal. ^a | – | 4 | 7.5 | μA | Conditions are with properly loaded, 1 μW max, 32.768 kHz crystal. V _{DD} = 3.3V, $-40^{\circ}\text{C} \leq T_A \leq 55^{\circ}\text{C}$. |
| I _{SBXTLH} | Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal at high temperature. ^a | – | 5 | 26 | μA | Conditions are with properly loaded, 1 μW max, 32.768 kHz crystal. V _{DD} = 3.3 V, $55^{\circ}\text{C} < T_A \leq 85^{\circ}\text{C}$. |
| V _{REF} | Reference Voltage (Bandgap) | 1.275 | 1.3 | 1.325 | V | Trimmed for appropriate V _{DD} . |

a. Standby current includes all functions (POR, LVD, WDT, Sleep Time) needed for reliable system operation. This must be compared with devices that have similar functions enabled.

DC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 14. DC GPIO Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|------------------|-----------------------------------|-----------------------|-----|------|-------|-----------------------------------------------------------------------------------------------------------|
| R _{PU} | Pull up Resistor | 4 | 5.6 | 8 | kΩ | |
| R _{PD} | Pull down Resistor | 4 | 5.6 | 8 | kΩ | |
| V _{OH} | High Output Level | V _{DD} - 1.0 | – | – | V | I _{OH} = 10 mA, V _{DD} = 4.75 to 5.25V (80 mA maximum combined I _{OH} budget) |
| V _{OL} | Low Output Level | – | – | 0.75 | V | I _{OL} = 25 mA, V _{DD} = 4.75 to 5.25V (150 mA maximum combined I _{OL} budget) |
| V _{IL} | Input Low Level | – | – | 0.8 | V | V _{DD} = 3.0 to 5.25 |
| V _{IH} | Input High Level | 2.1 | – | – | V | V _{DD} = 3.0 to 5.25 |
| V _H | Input Hysteresis | – | 60 | – | mV | |
| I _{IL} | Input Leakage (Absolute Value) | – | 1 | – | nA | Gross tested to 1 μA |
| C _{IN} | Capacitive Load on Pins as Input | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25°C |
| C _{OUT} | Capacitive Load on Pins as Output | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25°C |

DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Cap PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 15. 5V DC Operational Amplifier Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------------|-----------------------------------------------------------|-----|-----|-----------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| V _{OSOA} | Input Offset Voltage (absolute value) Low Power | – | 1.6 | 10 | mV | |
| | Input Offset Voltage (absolute value) Mid Power | – | 1.3 | 8 | mV | |
| | Input Offset Voltage (absolute value) High Power | – | 1.2 | 7.5 | mV | |
| TCV _{OSOA} | Average Input Offset Voltage Drift | – | 7.0 | 35.0 | μV/°C | |
| I _{EBOA} | Input Leakage Current (Port 0 Analog Pins) | – | 20 | – | pA | Gross tested to 1 μA. |
| C _{INOA} | Input Capacitance (Port 0 Analog Pins) | – | 4.5 | 9.5 | pF | Package and pin dependent. Temp = 25°C. |
| V _{CMOA} | Common Mode Voltage Range | 0.0 | – | V _{DD} | V | The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer. |
| | Common Mode Voltage Range (high power or high opamp bias) | 0.5 | – | V _{DD} - 0.5 | | |

Table 15. 5V DC Operational Amplifier Specifications (continued)

| Symbol | Description | Min | Typ | Max | Units | Notes |
|----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------|-------------------------------------------|-------------------------------------------|----------------------------------|-----------------------------------------------------------------------------------------------------------------------------|
| G _{OLOA} | Open Loop Gain Power = Low Power = Medium Power = High | 60 60 80 | – | – | dB | Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB. |
| V _{OHIGHOA} | High Output Voltage Swing (worst case internal load) Power = Low Power = Medium Power = High | V _{dd} - 0.2 – V _{dd} - 0.5 | – – – | – – – | V V V | |
| V _{OLOWOA} | Low Output Voltage Swing (worst case internal load) Power = Low Power = Medium Power = High | – – – | – – – | 0.2 0.2 0.5 | V V V | |
| I _{SOA} | Supply Current (including associated AGND buffer) Power = Low Power = Low, Opamp Bias = High Power = Medium Power = Medium, Opamp Bias = High Power = High Power = High, Opamp Bias = High | – – – – – – | 150 300 600 1200 2400 4600 | 200 400 800 1600 3200 6400 | μA μA μA μA μA μA | |
| PSRR _{OA} | Supply Voltage Rejection Ratio | 60 | – | – | dB | |

Table 16. 3.3V DC Operational Amplifier Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------------------------|------------------------------------------------------|-----------------------|------|-----------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| V _{OSOA} | Input Offset Voltage (absolute value) Low Power | – | 1.65 | 10 | mV | |
| | Input Offset Voltage (absolute value) Mid Power | – | 1.32 | 8 | mV | |
| | High Power is 5 Volt Only | | | | | |
| TCV _{OSOA} | Average Input Offset Voltage Drift | – | 7.0 | 35.0 | μV/°C | |
| I _{EBOA} | Input Leakage Current (Port 0 Analog Pins) | – | 20 | – | pA | Gross tested to 1 μA. |
| C _{I_{NOA}} | Input Capacitance (Port 0 Analog Pins) | – | 4.5 | 9.5 | pF | Package and pin dependent. Temp = 25°C. |
| V _{CMOA} | Common Mode Voltage Range | 0.2 | – | V _{dd} - 0.2 | V | The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer. |
| G _{O_{LOA}} | Open Loop Gain | | – | – | dB | Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB. |
| | Power = Low | 60 | | | | |
| | Power = Medium | 60 | | | | |
| | Power = High | 80 | | | | |
| V _{O_{HIGH}OA} | High Output Voltage Swing (worst case internal load) | | | | | |
| | Power = Low | V _{dd} - 0.2 | – | – | V | |
| | Power = Medium | V _{dd} - 0.2 | – | – | V | |
| | Power = High is 5V only | V _{dd} - 0.2 | – | – | V | |
| V _{O_{LOW}OA} | Low Output Voltage Swing (worst case internal load) | | | | | |
| | Power = Low | – | – | 0.2 | V | |
| | Power = Medium | – | – | 0.2 | V | |
| | Power = High | – | – | 0.2 | V | |
| I _{SOA} | Supply Current (including associated AGND buffer) | | | | | |
| | Power = Low | – | 150 | 200 | μA | |
| | Power = Low, Opamp Bias = High | – | 300 | 400 | μA | |
| | Power = Medium | – | 600 | 800 | μA | |
| | Power = Medium, Opamp Bias = High | – | 1200 | 1600 | μA | |
| | Power = High | – | 2400 | 3200 | μA | |
| | Power = High, Opamp Bias = High | – | 4600 | 6400 | μA | |
| PSRR _{OA} | Supply Voltage Rejection Ratio | 50 | – | – | dB | |

DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 17. 5V DC Analog Output Buffer Specifications

| Symbol | Description | Min | Typ | Max | Units |
|----------------------|------------------------------------------------------------------|------------------------------------------------------------|------------|------------------------------------------------------------|----------|
| V _{OSOB} | Input Offset Voltage (Absolute Value) | – | 3 | 12 | mV |
| TCV _{OSOB} | Average Input Offset Voltage Drift | – | +6 | – | μV/°C |
| V _{CMOB} | Common-Mode Input Voltage Range | 0.5 | – | V _{dd} - 1.0 | V |
| R _{OUTOB} | Output Resistance | | | | |
| | Power = Low Power = High | – – | 1 1 | – – | W W |
| V _{OHIGHOB} | High Output Voltage Swing (Load = 32 ohms to V _{dd} /2) | | | | |
| | Power = Low Power = High | 0.5 x V _{dd} + 1.1 0.5 x V _{dd} + 1.1 | – – | – – | V V |
| V _{LOWOB} | Low Output Voltage Swing (Load = 32 ohms to V _{dd} /2) | | | | |
| | Power = Low Power = High | – – | – – | 0.5 x V _{dd} - 1.3 0.5 x V _{dd} - 1.3 | V V |
| I _{SOB} | Supply Current Including Bias Cell (No Load) | | | | |
| | Power = Low Power = High | – – | 1.1 2.6 | 5.1 8.8 | mA mA |
| PSRR _{OB} | Supply Voltage Rejection Ratio | 60 | – | – | dB |

Table 18. 3.3V DC Analog Output Buffer Specifications

| Symbol | Description | Min | Typ | Max | Units |
|----------------------|------------------------------------------------------------------|------------------------------------------------------------|------------|------------------------------------------------------------|----------|
| V _{OSOB} | Input Offset Voltage (Absolute Value) | – | 3 | 12 | mV |
| TCV _{OSOB} | Average Input Offset Voltage Drift | – | +6 | – | μV/°C |
| V _{CMOB} | Common-Mode Input Voltage Range | 0.5 | – | V _{dd} - 1.0 | V |
| R _{OUTOB} | Output Resistance | | | | |
| | Power = Low Power = High | – – | 1 1 | – – | W W |
| V _{OHIGHOB} | High Output Voltage Swing (Load = 1K ohms to V _{dd} /2) | | | | |
| | Power = Low Power = High | 0.5 x V _{dd} + 1.0 0.5 x V _{dd} + 1.0 | – – | – – | V V |
| V _{LOWOB} | Low Output Voltage Swing (Load = 1K ohms to V _{dd} /2) | | | | |
| | Power = Low Power = High | – – | – – | 0.5 x V _{dd} - 1.0 0.5 x V _{dd} - 1.0 | V V |
| I _{SOB} | Supply Current Including Bias Cell (No Load) | | | | |
| | Power = Low Power = High | – – | 0.8 2.0 | 2.0 4.3 | mA mA |
| PSRR _{OB} | Supply Voltage Rejection Ratio | 50 | – | – | dB |

DC Switch Mode Pump Specifications

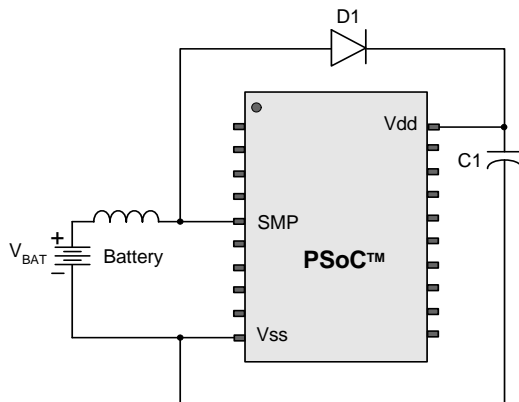
The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 19. DC Switch Mode Pump (SMP) Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------------------|-------------------------------------------------------------------------------------------------------------------------------------|--------|--------|--------|------------------------------|--------------------------------------------------------------------------------|
| V _{PUMP 5V} | 5V Output voltage | 4.75 | 5.0 | 5.25 | V | Average, neglecting ripple |
| V _{PUMP 3V} | 3V Output voltage | 3.00 | 3.25 | 3.60 | V | Average, neglecting ripple |
| I _{PUMP} | Available Output Current V _{BAT} = 1.5V, V _{PUMP} = 3.25V V _{BAT} = 1.8V, V _{PUMP} = 5.0V | 8 5 | – – | – – | mA mA | For implementation, which includes 2 uH inductor, 1 uF cap, and Schottky diode |
| V _{BAT5V} | Input Voltage Range from Battery | 1.8 | – | 5.0 | V | |
| V _{BAT3V} | Input Voltage Range from Battery | 1.0 | – | 3.3 | V | |
| V _{BATSTART} | Minimum Input Voltage from Battery to Start Pump | 1.1 | – | – | V | |
| ΔV _{PUMP_Line} | Line Regulation (over V _{BAT} range) | – | 5 | – | %V _O ^a | |
| ΔV _{PUMP_Load} | Load Regulation | – | 5 | – | %V _O ^a | |
| ΔV _{PUMP_Ripple} | Output Voltage Ripple (depends on cap/load) | – | 25 | – | mVpp | Configuration of note 2, load is 5mA |
| – | Efficiency | 35 | 50 | – | % | Configuration of note 2, load is 5mA, Vout is 3.25V. |
| F _{PUMP} | Switching Frequency | – | 1.3 | – | MHz | |
| DC _{PUMP} | Switching Duty Cycle | – | 50 | – | % | |

a. V_O is the “Vdd Value for PUMP Trip” specified by the VM[2:0] setting in the DC POR and LVD Specification, [Table 23](#) on page 25.

Figure 11. Basic Switch Mode Pump Circuit



DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block.

Note Avoid using P2[4] for digital signaling when using an analog resource that depends on the Analog Reference. Some coupling of the digital signal may appear on the AGND.

Table 20. 5V DC Analog Reference Specifications

| Symbol | Description | Min | Typ | Max | Units |
|--------|----------------------------------------------------------------------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|-------|
| BG | Bandgap Voltage Reference | 1.274 | 1.30 | 1.326 | V |
| – | AGND = $V_{dd}/2^a$ CT Block Power = High | $V_{dd}/2 - 0.043$ | $V_{dd}/2 - 0.025$ | $V_{dd}/2 + 0.003$ | V |
| – | AGND = $2 \times \text{BandGap}^a$ CT Block Power = High | $2 \times \text{BG} - 0.048$ | $2 \times \text{BG} - 0.030$ | $2 \times \text{BG} + 0.024$ | V |
| – | AGND = P2[4] ($P2[4] = V_{dd}/2^a$) CT Block Power = High | $P2[4] - 0.013$ | P2[4] | $P2[4] + 0.014$ | V |
| – | AGND = BandGap^a CT Block Power = High | $\text{BG} - 0.009$ | $\text{BG} + 0.008$ | $\text{BG} + 0.016$ | V |
| – | AGND = $1.6 \times \text{BandGap}^a$ CT Block Power = High | $1.6 \times \text{BG} - 0.022$ | $1.6 \times \text{BG} - 0.010$ | $1.6 \times \text{BG} + 0.018$ | V |
| – | AGND Column to Column Variation (AGND = $V_{dd}/2^a$) CT Block Power = High | -0.034 | 0.000 | 0.034 | V |
| – | RefHi = $V_{dd}/2 + \text{BandGap}$ Ref Control Power = High | $V_{dd}/2 + \text{BG} - 0.140$ | $V_{dd}/2 + \text{BG} - 0.018$ | $V_{dd}/2 + \text{BG} + 0.103$ | V |
| – | RefHi = $3 \times \text{BandGap}$ Ref Control Power = High | $3 \times \text{BG} - 0.112$ | $3 \times \text{BG} - 0.018$ | $3 \times \text{BG} + 0.076$ | V |
| – | RefHi = $2 \times \text{BandGap} + P2[6]$ ($P2[6] = 1.3\text{V}$) Ref Control Power = High | $2 \times \text{BG} + P2[6] - 0.113$ | $2 \times \text{BG} + P2[6] - 0.018$ | $2 \times \text{BG} + P2[6] + 0.077$ | V |
| – | RefHi = $P2[4] + \text{BandGap}$ ($P2[4] = V_{dd}/2$) Ref Control Power = High | $P2[4] + \text{BG} - 0.130$ | $P2[4] + \text{BG} - 0.016$ | $P2[4] + \text{BG} + 0.098$ | V |
| – | RefHi = $P2[4] + P2[6]$ ($P2[4] = V_{dd}/2$, $P2[6] = 1.3\text{V}$) Ref Control Power = High | $P2[4] + P2[6] - 0.133$ | $P2[4] + P2[6] - 0.016$ | $P2[4] + P2[6] + 0.100$ | V |
| – | RefHi = $3.2 \times \text{BandGap}$ Ref Control Power = High | $3.2 \times \text{BG} - 0.112$ | $3.2 \times \text{BG}$ | $3.2 \times \text{BG} + 0.076$ | V |
| – | RefLo = $V_{dd}/2 - \text{BandGap}$ Ref Control Power = High | $V_{dd}/2 - \text{BG} - 0.051$ | $V_{dd}/2 - \text{BG} + 0.024$ | $V_{dd}/2 - \text{BG} + 0.098$ | V |
| – | RefLo = BandGap Ref Control Power = High | $\text{BG} - 0.082$ | $\text{BG} + 0.023$ | $\text{BG} + 0.129$ | V |
| – | RefLo = $2 \times \text{BandGap} - P2[6]$ ($P2[6] = 1.3\text{V}$) Ref Control Power = High | $2 \times \text{BG} - P2[6] - 0.084$ | $2 \times \text{BG} - P2[6] + 0.025$ | $2 \times \text{BG} - P2[6] + 0.134$ | V |
| – | RefLo = $P2[4] - \text{BandGap}$ ($P2[4] = V_{dd}/2$) Ref Control Power = High | $P2[4] - \text{BG} - 0.056$ | $P2[4] - \text{BG} + 0.026$ | $P2[4] - \text{BG} + 0.107$ | V |
| – | RefLo = $P2[4] - P2[6]$ ($P2[4] = V_{dd}/2$, $P2[6] = 1.3\text{V}$) Ref Control Power = High | $P2[4] - P2[6] - 0.057$ | $P2[4] - P2[6] + 0.026$ | $P2[4] - P2[6] + 0.110$ | V |

a. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is $1.3\text{V} \pm 2\%$.

Table 21. 3.3V DC Analog Reference Specifications

| Symbol | Description | Min | Typ | Max | Units |
|--------|---------------------------------------------------------------------------------------------|--------------------------------|--------------------------------|--------------------------------|-------|
| BG | Bandgap Voltage Reference | 1.274 | 1.30 | 1.326 | V |
| – | AGND = $V_{dd}/2^a$ CT Block Power = High | $V_{dd}/2 - 0.037$ | $V_{dd}/2 - 0.020$ | $V_{dd}/2 + 0.002$ | V |
| – | AGND = $2 \times \text{BandGap}^a$ CT Block Power = High | Not Allowed | | | |
| – | AGND = P2[4] (P2[4] = $V_{dd}/2$) CT Block Power = High | P2[4] - 0.008 | P2[4] + 0.001 | P2[4] + 0.009 | V |
| – | AGND = BandGap^a CT Block Power = High | BG - 0.009 | BG + 0.005 | BG + 0.015 | V |
| – | AGND = $1.6 \times \text{BandGap}^a$ CT Block Power = High | $1.6 \times \text{BG} - 0.027$ | $1.6 \times \text{BG} - 0.010$ | $1.6 \times \text{BG} + 0.018$ | V |
| – | AGND Column to Column Variation (AGND = $V_{dd}/2^a$) CT Block Power = High | -0.034 | 0.000 | 0.034 | mV |
| – | RefHi = $V_{dd}/2 + \text{BandGap}$ Ref Control Power = High | Not Allowed | | | |
| – | RefHi = $3 \times \text{BandGap}$ Ref Control Power = High | Not Allowed | | | |
| – | RefHi = $2 \times \text{BandGap} + \text{P2}[6]$ (P2[6] = 0.5V) Ref Control Power = High | Not Allowed | | | |
| – | RefHi = P2[4] + BandGap (P2[4] = $V_{dd}/2$) Ref Control Power = High | Not Allowed | | | |
| – | RefHi = P2[4] + P2[6] (P2[4] = $V_{dd}/2$, P2[6] = 0.5V) Ref Control Power = High | P2[4] + P2[6] - 0.075 | P2[4] + P2[6] - 0.009 | P2[4] + P2[6] + 0.057 | V |
| – | RefHi = $3.2 \times \text{BandGap}$ Ref Control Power = High | Not Allowed | | | |
| – | RefLo = $V_{dd}/2 - \text{BandGap}$ Ref Control Power = High | Not Allowed | | | |
| – | RefLo = BandGap Ref Control Power = High | Not Allowed | | | |
| – | RefLo = $2 \times \text{BandGap} - \text{P2}[6]$ (P2[6] = 0.5V) Ref Control Power = High | Not Allowed | | | |
| – | RefLo = P2[4] - BandGap (P2[4] = $V_{dd}/2$) Ref Control Power = High | Not Allowed | | | |
| – | RefLo = P2[4] - P2[6] (P2[4] = $V_{dd}/2$, P2[6] = 0.5V) Ref Control Power = High | P2[4] - P2[6] - 0.048 | P2[4] - P2[6] + 0.022 | P2[4] - P2[6] + 0.092 | V |

a. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is $1.3V \pm 2\%$

DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 22. DC Analog PSoC Block Specifications

| Symbol | Description | Min | Typ | Max | Units |
|-----------------|---------------------------------------|-----|-------|-----|-------|
| R _{CT} | Resistor Unit Value (Continuous Time) | – | 12.24 | – | kΩ |
| C _{SC} | Capacitor Unit Value (Switch Cap) | – | 80 | – | fF |

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Note The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the *PSoC Programmable System-on-Chip Technical Reference Manual* for more information on the VLT_CR register.

Table 23. DC POR and LVD Specifications

| Symbol | Description | Min | Typ | Max | Units |
|---------------------|--------------------------------------------------------------------------|-------|-------|--------------------|-------|
| V _{PPOR0R} | V _{dd} Value for PPOR Trip (positive ramp) PORLEV[1:0] = 00b | | 2.908 | | V |
| V _{PPOR1R} | PORLEV[1:0] = 01b | – | 4.394 | – | V |
| V _{PPOR2R} | PORLEV[1:0] = 10b | | 4.548 | | V |
| V _{PPOR0} | V _{dd} Value for PPOR Trip (negative ramp) PORLEV[1:0] = 00b | | 2.816 | | V |
| V _{PPOR1} | PORLEV[1:0] = 01b | – | 4.394 | – | V |
| V _{PPOR2} | PORLEV[1:0] = 10b | | 4.548 | | V |
| V _{PH0} | PPOR Hysteresis PORLEV[1:0] = 00b | – | 92 | – | mV |
| V _{PH1} | PORLEV[1:0] = 01b | – | 0 | – | mV |
| V _{PH2} | PORLEV[1:0] = 10b | – | 0 | – | mV |
| V _{LVD0} | V _{dd} Value for LVD Trip VM[2:0] = 000b | 2.863 | 2.921 | 2.979 ^a | V |
| V _{LVD1} | VM[2:0] = 001b | 2.963 | 3.023 | 3.083 | V |
| V _{LVD2} | VM[2:0] = 010b | 3.070 | 3.133 | 3.196 | V |
| V _{LVD3} | VM[2:0] = 011b | 3.920 | 4.00 | 4.080 | V |
| V _{LVD4} | VM[2:0] = 100b | 4.393 | 4.483 | 4.573 | V |
| V _{LVD5} | VM[2:0] = 101b | 4.550 | 4.643 | 4.736 ^b | V |
| V _{LVD6} | VM[2:0] = 110b | 4.632 | 4.727 | 4.822 | V |
| V _{LVD7} | VM[2:0] = 111b | 4.718 | 4.814 | 4.910 | V |
| V _{PUMP0} | V _{dd} Value for PUMP Trip VM[2:0] = 000b | 2.963 | 3.023 | 3.083 | V |
| V _{PUMP1} | VM[2:0] = 001b | 3.033 | 3.095 | 3.157 | V |
| V _{PUMP2} | VM[2:0] = 010b | 3.185 | 3.250 | 3.315 | V |
| V _{PUMP3} | VM[2:0] = 011b | 4.110 | 4.194 | 4.278 | V |
| V _{PUMP4} | VM[2:0] = 100b | 4.550 | 4.643 | 4.736 | V |
| V _{PUMP5} | VM[2:0] = 101b | 4.632 | 4.727 | 4.822 | V |
| V _{PUMP6} | VM[2:0] = 110b | 4.719 | 4.815 | 4.911 | V |
| V _{PUMP7} | VM[2:0] = 111b | 4.900 | 5.000 | 5.100 | V |

a. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
b. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 24. DC Programming Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-----------------------|--------------------------------------------------------------------------------------|----------------|-----|-----------------|-------|--------------------------------------|
| I_{DDP} | Supply Current During Programming or Verify | – | 5 | 25 | mA | |
| V_{ILP} | Input Low Voltage During Programming or Verify | – | – | 0.8 | V | |
| V_{IHP} | Input High Voltage During Programming or Verify | 2.2 | – | – | V | |
| I_{ILP} | Input Current when Applying V_{ilp} to P1[0] or P1[1] During Programming or Verify | – | – | 0.2 | mA | Driving internal pull down resistor. |
| I_{IHP} | Input Current when Applying V_{ihp} to P1[0] or P1[1] During Programming or Verify | – | – | 1.5 | mA | Driving internal pull down resistor. |
| V_{OLV} | Output Low Voltage During Programming or Verify | – | – | $V_{ss} + 0.75$ | V | |
| V_{OHV} | Output High Voltage During Programming or Verify | $V_{dd} - 1.0$ | – | V_{dd} | V | |
| Flash _{ENPB} | Flash Endurance (per block) | 50,000 | – | – | – | Erase/write cycles per block. |
| Flash _{ENT} | Flash Endurance (total) ^a | 1,800,000 | – | – | – | Erase/write cycles. |
| Flash _{DR} | Flash Data Retention | 10 | – | – | Years | |

a. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (and so forth to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at <http://www.cypress.com> under Application Notes for more information.

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 25. AC Chip-Level Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------------------------|---------------------------------------------------------|------|--------|-----------------------|-------|--------------------------------------------------------------|
| F _{IMO} | Internal Main Oscillator Frequency | 23.4 | 24 | 24.6 ^a | MHz | Trimmed. Using factory trim values. |
| F _{CPU1} | CPU Frequency (5V Nominal) | 0.93 | 24 | 24.6 ^{a,b} | MHz | |
| F _{CPU2} | CPU Frequency (3.3V Nominal) | 0.93 | 12 | 12.3 ^{b,c} | MHz | |
| F _{48M} | Digital PSoC Block Frequency | 0 | 48 | 49.2 ^{a,b,d} | MHz | Refer to the AC Digital Block Specifications. |
| F _{24M} | Digital PSoC Block Frequency | 0 | 24 | 24.6 ^{b,e,d} | MHz | |
| F _{32K1} | Internal Low Speed Oscillator Frequency | 15 | 32 | 64 | kHz | |
| F _{32K2} | External Crystal Oscillator | – | 32.768 | – | kHz | Accuracy is capacitor and crystal dependent. 50% duty cycle. |
| F _{PLL} | PLL Frequency | – | 23.986 | – | MHz | Is a multiple (x732) of crystal frequency. |
| Jitter24M2 | 24 MHz Period Jitter (PLL) | – | – | 600 | ps | |
| T _{PLLSLEW} | PLL Lock Time | 0.5 | – | 10 | ms | |
| T _{PLLSLEWSLOW} | PLL Lock Time for Low Gain Setting | 0.5 | – | 50 | ms | |
| T _{OS} | External Crystal Oscillator Startup to 1% | – | 1700 | 2620 | ms | |
| T _{OSACC} | External Crystal Oscillator Startup to 100 ppm | – | 2800 | 3800 ^f | ms | |
| Jitter32k | 32 kHz Period Jitter | – | 100 | – | ns | |
| T _{XRST} | External Reset Pulse Width | 10 | – | – | μs | |
| DC24M | 24 MHz Duty Cycle | 40 | 50 | 60 | % | |
| Step24M | 24 MHz Trim Step Size | – | 50 | – | kHz | |
| F _{out48M} | 48 MHz Output Frequency | 46.8 | 48.0 | 49.2 ^{a,c} | MHz | Trimmed. Using factory trim values. |
| Jitter24M1 | 24 MHz Period Jitter (IMO) | – | 600 | – | ps | |
| F _{MAX} | Maximum frequency of signal on row input or row output. | – | – | 12.3 | MHz | |
| T _{RAMP} | Supply Ramp Time | 0 | – | – | μs | |

a. 4.75V < V_{dd} < 5.25V.

b. Accuracy derived from Internal Main Oscillator with appropriate trim for V_{dd} range.

c. 3.0V < V_{dd} < 3.6V. See Application Note [AN2012](#) "Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation" for information on trimming for operation at 3.3V.

d. See the individual user module data sheets for information on maximum frequencies for user modules.

e. 3.0V < 5.25V.

f. The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{osacc} period. Correct operation assumes a properly loaded 1 uW maximum drive level 32.768 kHz crystal. 3.0V ≤ V_{dd} ≤ 5.5V, -40 °C ≤ T_A ≤ 85 °C.

Figure 12. PLL Lock Timing Diagram

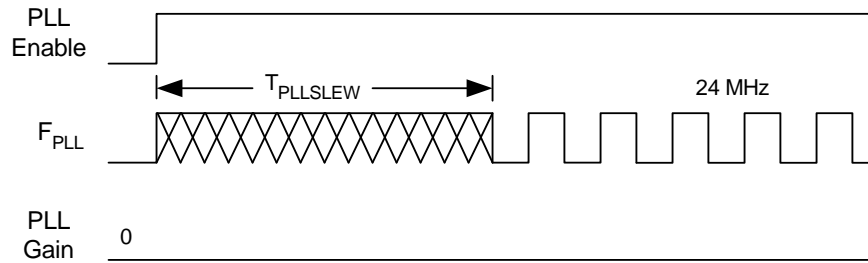


Figure 13. PLL Lock for Low Gain Setting Timing Diagram

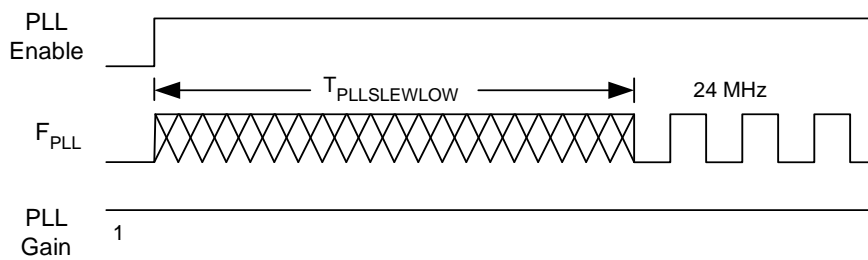


Figure 14. External Crystal Oscillator Startup Timing Diagram

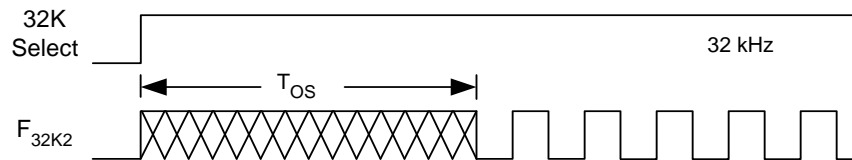


Figure 15. 24 MHz Period Jitter (IMO) Timing Diagram



Figure 16. 32 kHz Period Jitter (ECO) Timing Diagram



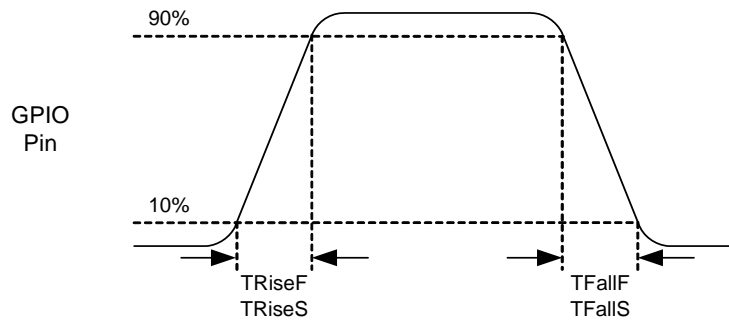
AC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 26. AC GPIO Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------------------|----------------------------------------------|-----|-----|-----|-------|-------------------------------|
| F_{GPIO} | GPIO Operating Frequency | 0 | – | 12 | MHz | |
| T_{RiseF} | Rise Time, Normal Strong Mode, Cloud = 50 pF | 3 | – | 18 | ns | Vdd = 4.5 to 5.25V, 10% - 90% |
| T_{FallF} | Fall Time, Normal Strong Mode, Cloud = 50 pF | 2 | – | 18 | ns | Vdd = 4.5 to 5.25V, 10% - 90% |
| T_{RiseS} | Rise Time, Slow Strong Mode, Cloud = 50 pF | 10 | 27 | – | ns | Vdd = 3 to 5.25V, 10% - 90% |
| T_{FallS} | Fall Time, Slow Strong Mode, Cloud = 50 pF | 10 | 22 | – | ns | Vdd = 3 to 5.25V, 10% - 90% |

Figure 17. GPIO Timing Diagram



AC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Note Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Table 27. 5V AC Operational Amplifier Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------------------------|---------------------------------------------------------------------------------------------|------|------|------------------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| T _{ROA} | Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) | | | | | Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels. |
| | Power = Low | – | – | 3.9 | μs | |
| | Power = Low, Opamp Bias = High | – | – | | μs | |
| | Power = Medium | – | – | | μs | |
| | Power = Medium, Opamp Bias = High | – | – | 0.72 | μs | |
| | Power = High | – | – | | μs | |
| Power = High, Opamp Bias = High | – | – | 0.62 | μs | | |
| T _{SOA} | Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) | | | | | Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels. |
| | Power = Low | – | – | 5.9 | μs | |
| | Power = Low, Opamp Bias = High | – | – | | μs | |
| | Power = Medium | – | – | | μs | |
| | Power = Medium, Opamp Bias = High | – | – | 0.92 | μs | |
| | Power = High | – | – | | μs | |
| Power = High, Opamp Bias = High | – | – | 0.72 | μs | | |
| SR _{ROA} | Rising Slew Rate (20% to 80%) (10 pF load, Unity Gain) | | | | | Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels. |
| | Power = Low | 0.15 | – | | V/ μs | |
| | Power = Low, Opamp Bias = High | | – | | V/ μs | |
| | Power = Medium | | – | | V/ μs | |
| | Power = Medium, Opamp Bias = High | 1.7 | – | | V/ μs | |
| | Power = High | | – | | V/ μs | |
| Power = High, Opamp Bias = High | 6.5 | – | | V/ μs | | |
| SR _{FOA} | Falling Slew Rate(20% to 80%) (10 pF load, Unity Gain) | | | | | Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels. |
| | Power = Low | 0.01 | – | | V/ μs | |
| | Power = Low, Opamp Bias = High | | – | | V/ μs | |
| | Power = Medium | | – | | V/ μs | |
| | Power = Medium, Opamp Bias = High | 0.5 | – | | V/ μs | |
| | Power = High | | – | | V/ μs | |
| Power = High, Opamp Bias = High | 4.0 | – | | V/ μs | | |
| BW _{OA} | Gain Bandwidth Product | | | | | Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels. |
| | Power = Low | 0.75 | – | | MHz | |
| | Power = Low, Opamp Bias = High | | – | | MHz | |
| | Power = Medium | | – | | MHz | |
| | Power = Medium, Opamp Bias = High | 3.1 | – | | MHz | |
| | Power = High | | – | | MHz | |
| Power = High, Opamp Bias = High | 5.4 | – | | MHz | | |
| E _{NOA} | Noise at 1 kHz (Power = Medium, Opamp Bias = High) | – | 200 | – | nV/rt-Hz | |

Table 28. 3.3V AC Operational Amplifier Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-------------------|-----------------------------------------------------------------------------|------|-----|------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| T _{ROA} | Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) | | | | | Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels. |
| | Power = Low | – | – | 3.92 | μs | |
| | Power = Low, Opamp Bias = High | – | – | | μs | |
| | Power = Medium | – | – | | μs | |
| | Power = Medium, Opamp Bias = High | – | – | 0.72 | μs | |
| | Power = High (3.3 Volt High Bias Operation not supported) | – | – | – | μs | |
| T _{SOA} | Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) | | | | | Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels. |
| | Power = Low | – | – | 5.41 | μs | |
| | Power = Low, Opamp Bias = High | – | – | | μs | |
| | Power = Medium | – | – | | μs | |
| | Power = Medium, Opamp Bias = High | – | – | 0.72 | μs | |
| | Power = High (3.3 Volt High Bias Operation not supported) | – | – | – | μs | |
| SR _{ROA} | Rising Slew Rate (20% to 80%) (10 pF load, Unity Gain) | | | | | Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels. |
| | Power = Low | 0.31 | – | | V/μs | |
| | Power = Low, Opamp Bias = High | | – | | V/μs | |
| | Power = Medium | | – | | V/μs | |
| | Power = Medium, Opamp Bias = High | 2.7 | – | | V/μs | |
| | Power = High (3.3 Volt High Bias Operation not supported) | – | – | – | V/μs | |
| SR _{FOA} | Falling Slew Rate(20% to 80%) (10 pF load, Unity Gain) | | | | | Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels. |
| | Power = Low | 0.24 | – | | V/μs | |
| | Power = Low, Opamp Bias = High | | – | | V/μs | |
| | Power = Medium | | – | | V/μs | |
| | Power = Medium, Opamp Bias = High | 1.8 | – | | V/μs | |
| | Power = High (3.3 Volt High Bias Operation not supported) | – | – | – | V/μs | |
| BW _{OA} | Gain Bandwidth Product | | | | | Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels. |
| | Power = Low | 0.67 | – | | MHz | |
| | Power = Low, Opamp Bias = High | | – | | MHz | |
| | Power = Medium | | – | | MHz | |
| | Power = Medium, Opamp Bias = High | 2.8 | – | | MHz | |
| | Power = High (3.3 Volt High Bias Operation not supported) | – | – | – | MHz | |
| E _{NOA} | Noise at 1 kHz (Power = Medium, Opamp Bias = High) | – | 200 | – | nV/rt-Hz | |

AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 29. AC Digital Block Specifications

| Function | Description | Min | Typ | Max | Units | Notes |
|-------------------|--------------------------------------------|-----------------|-----|------|-------|---------------------|
| Timer | Capture Pulse Width | 50 ^a | – | – | ns | |
| | Maximum Frequency, No Capture | – | – | 49.2 | MHz | 4.75V < Vdd < 5.25V |
| | Maximum Frequency, With Capture | – | – | 24.6 | MHz | |
| Counter | Enable Pulse Width | 50 ^a | – | – | ns | |
| | Maximum Frequency, No Enable Input | – | – | 49.2 | MHz | 4.75V < Vdd < 5.25V |
| | Maximum Frequency, Enable Input | – | – | 24.6 | MHz | |
| Dead Band | Kill Pulse Width: | | | | | |
| | Asynchronous Restart Mode | 20 | – | – | ns | |
| | Synchronous Restart Mode | 50 ^a | – | – | ns | |
| | Disable Mode | 50 ^a | – | – | ns | |
| | Maximum Frequency | – | – | 49.2 | MHz | 4.75V < Vdd < 5.25V |
| CRCPRS (PRS Mode) | Maximum Input Clock Frequency | – | – | 49.2 | MHz | 4.75V < Vdd < 5.25V |
| CRCPRS (CRC Mode) | Maximum Input Clock Frequency | – | – | 24.6 | MHz | |
| SPIM | Maximum Input Clock Frequency | – | – | 8.2 | MHz | |
| SPIS | Maximum Input Clock Frequency | – | – | 4.1 | ns | |
| | Width of SS_ Negated Between Transmissions | 50 ^a | – | – | ns | |
| Transmitter | Maximum Input Clock Frequency | – | – | 16.4 | MHz | |
| Receiver | Maximum Input Clock Frequency | – | 16 | 49.2 | MHz | 4.75V < Vdd < 5.25V |

a. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 30. 5V AC Analog Output Buffer Specifications

| Symbol | Description | Min | Typ | Max | Units |
|-------------------|------------------------------------------------------------------|------|-----|-----|-------|
| T _{ROB} | Rising Settling Time to 0.1%, 1V Step, 100 pF Load | – | – | 2.5 | μs |
| | Power = Low | – | – | 2.5 | μs |
| T _{SOB} | Falling Settling Time to 0.1%, 1V Step, 100 pF Load | – | – | 2.2 | μs |
| | Power = High | – | – | 2.2 | μs |
| SR _{ROB} | Rising Slew Rate (20% to 80%), 1V Step, 100 pF Load | 0.65 | – | – | V/μs |
| | Power = High | 0.65 | – | – | V/μs |
| SR _{FOB} | Falling Slew Rate (80% to 20%), 1V Step, 100 pF Load | 0.65 | – | – | V/μs |
| | Power = High | 0.65 | – | – | V/μs |
| BW _{OB} | Small Signal Bandwidth, 20mV _{pp} , 3dB BW, 100 pF Load | 0.8 | – | – | MHz |
| | Power = High | 0.8 | – | – | MHz |
| BW _{OB} | Large Signal Bandwidth, 1V _{pp} , 3dB BW, 100 pF Load | 300 | – | – | kHz |
| | Power = High | 300 | – | – | kHz |

Table 31. 3.3V AC Analog Output Buffer Specifications

| Symbol | Description | Min | Typ | Max | Units |
|-------------------|------------------------------------------------------------------|-----|-----|-----|-------|
| T _{ROB} | Rising Settling Time to 0.1%, 1V Step, 100 pF Load | – | – | 3.8 | μs |
| | Power = High | – | – | 3.8 | μs |
| T _{SOB} | Falling Settling Time to 0.1%, 1V Step, 100 pF Load | – | – | 2.6 | μs |
| | Power = High | – | – | 2.6 | μs |
| SR _{ROB} | Rising Slew Rate (20% to 80%), 1V Step, 100 pF Load | 0.5 | – | – | V/μs |
| | Power = High | 0.5 | – | – | V/μs |
| SR _{FOB} | Falling Slew Rate (80% to 20%), 1V Step, 100 pF Load | 0.5 | – | – | V/μs |
| | Power = High | 0.5 | – | – | V/μs |
| BW _{OB} | Small Signal Bandwidth, 20mV _{pp} , 3dB BW, 100 pF Load | 0.7 | – | – | MHz |
| | Power = High | 0.7 | – | – | MHz |
| BW _{OB} | Large Signal Bandwidth, 1V _{pp} , 3dB BW, 100 pF Load | 200 | – | – | kHz |
| | Power = High | 200 | – | – | kHz |

AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 32. 5V AC External Clock Specifications

| Symbol | Description | Min | Typ | Max | Units |
|---------------------|------------------------|------|-----|-------|-------|
| F _{OSCEXT} | Frequency | 0 | – | 24.24 | MHz |
| – | High Period | 20.6 | – | – | ns |
| – | Low Period | 20.6 | – | – | ns |
| – | Power Up IMO to Switch | 150 | – | – | μs |

Table 33. 3.3V AC External Clock Specifications

| Symbol | Description | Min | Typ | Max | Units |
|---------------------|--------------------------------------------------------------|------|-----|-------|-------|
| F _{OSCEXT} | Frequency with CPU Clock divide by 1 ^a | 0 | – | 12.12 | MHz |
| F _{OSCEXT} | Frequency with CPU Clock divide by 2 or greater ^b | 0 | – | 24.24 | MHz |
| – | High Period with CPU Clock divide by 1 | 41.7 | – | – | ns |
| – | Low Period with CPU Clock divide by 1 | 41.7 | – | – | ns |
| – | Power Up IMO to Switch | 150 | – | – | μs |

- a. Maximum CPU frequency is 12 MHz at 3.3V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
- b. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.

AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 34. AC Programming Specifications

| Symbol | Description | Min | Typ | Max | Units |
|---------------------|------------------------------------------|-----|-----|-----|-------|
| T _{RSCLK} | Rise Time of SCLK | 1 | – | 20 | ns |
| T _{FSCLK} | Fall Time of SCLK | 1 | – | 20 | ns |
| T _{SSCLK} | Data Set up Time to Falling Edge of SCLK | 40 | – | – | ns |
| T _{HSCLK} | Data Hold Time from Falling Edge of SCLK | 40 | – | – | ns |
| F _{SCLK} | Frequency of SCLK | 0 | – | 8 | MHz |
| T _{ERASEB} | Flash Erase Time (Block) | – | 15 | – | ms |
| T _{WRITE} | Flash Block Write Time | – | 30 | – | ms |
| T _{DSCLK} | Data Out Delay from Falling Edge of SCLK | – | – | 45 | ns |

AC I²C Specifications

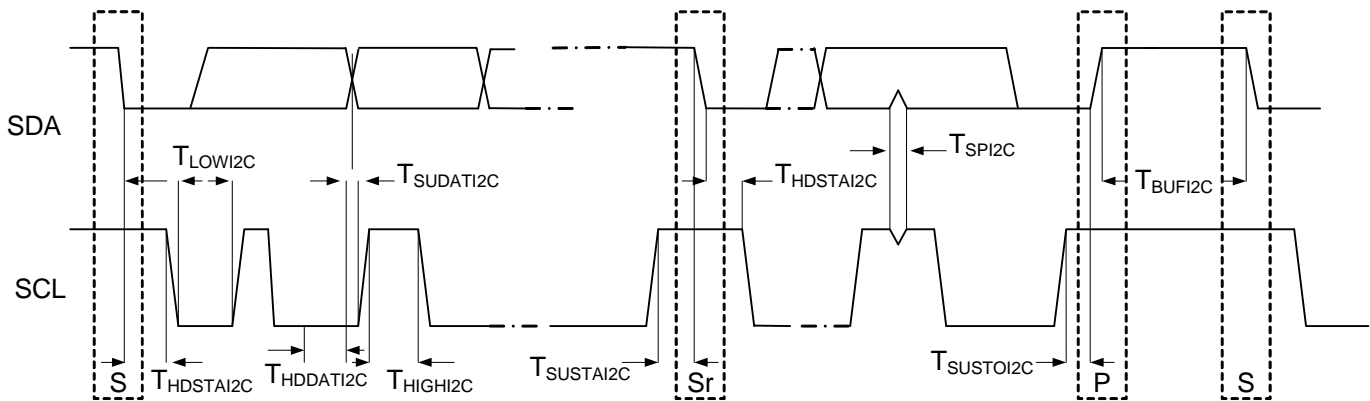
The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

Table 35. AC Characteristics of the I²C SDA and SCL Pins

| Symbol | Description | Standard Mode | | Fast Mode | | Units |
|------------------------|----------------------------------------------------------------------------------------------|---------------|-----|------------------|-----|-------|
| | | Min | Max | Min | Max | |
| F _{SCL I2C} | SCL Clock Frequency | 0 | 100 | 0 | 400 | kHz |
| T _{HDSTAI2C} | Hold Time (repeated) START Condition. After this period, the first clock pulse is generated. | 4.0 | – | 0.6 | – | μs |
| T _{LOWI2C} | LOW Period of the SCL Clock | 4.7 | – | 1.3 | – | μs |
| T _{HIGHI2C} | HIGH Period of the SCL Clock | 4.0 | – | 0.6 | – | μs |
| T _{SUSTA I2C} | Setup Time for a Repeated START Condition | 4.7 | – | 0.6 | – | μs |
| T _{HDDATI2C} | Data Hold Time | 0 | – | 0 | – | μs |
| T _{SUDATI2C} | Data Setup Time | 250 | – | 100 ^a | – | ns |
| T _{SUSTOI2C} | Setup Time for STOP Condition | 4.0 | – | 0.6 | – | μs |
| T _{BUFI2C} | Bus Free Time Between a STOP and START Condition | 4.7 | – | 1.3 | – | μs |
| T _{SPI2C} | Pulse Width of spikes are suppressed by the input filter. | – | – | 0 | 50 | ns |

a. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $t_{\text{SU, DAT}} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{\text{max}} + t_{\text{SU, DAT}} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

Figure 18. Definition for Timing for Fast/Standard Mode on the I2C Bus



Packaging Information

This section presents the packaging specifications for the CY8C24x23 PSoC device, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

Figure 19. 8-Pin (300-Mil) PDIP

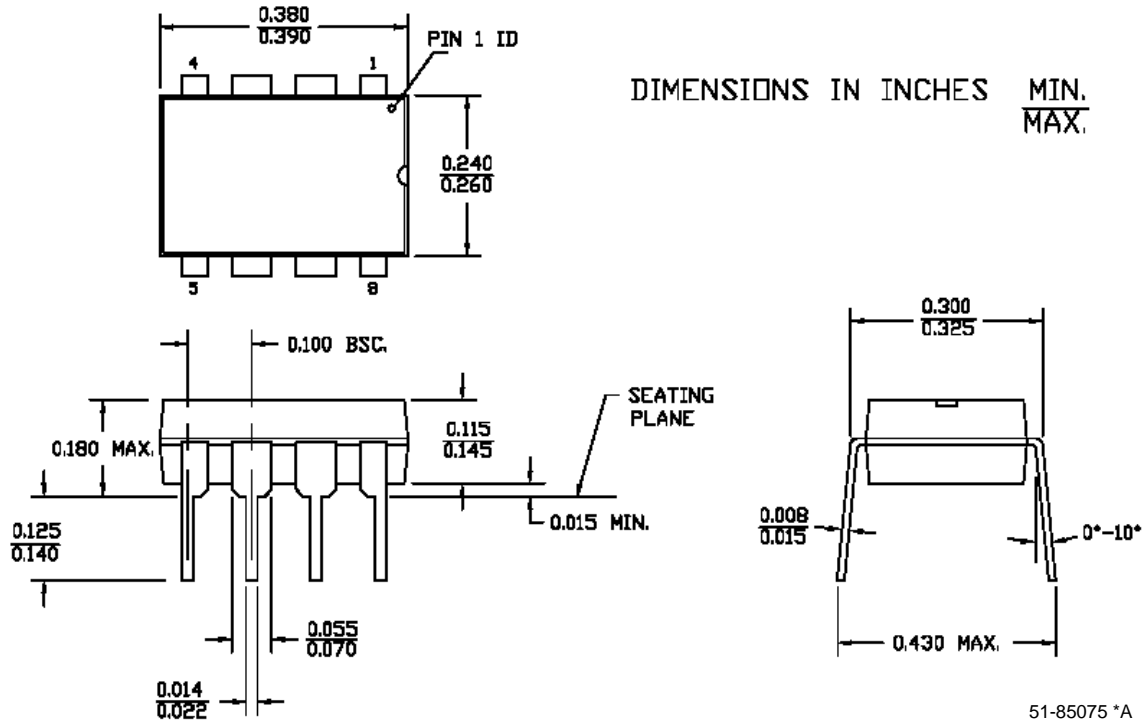


Figure 20. 8-Pin (150-Mil) SOIC

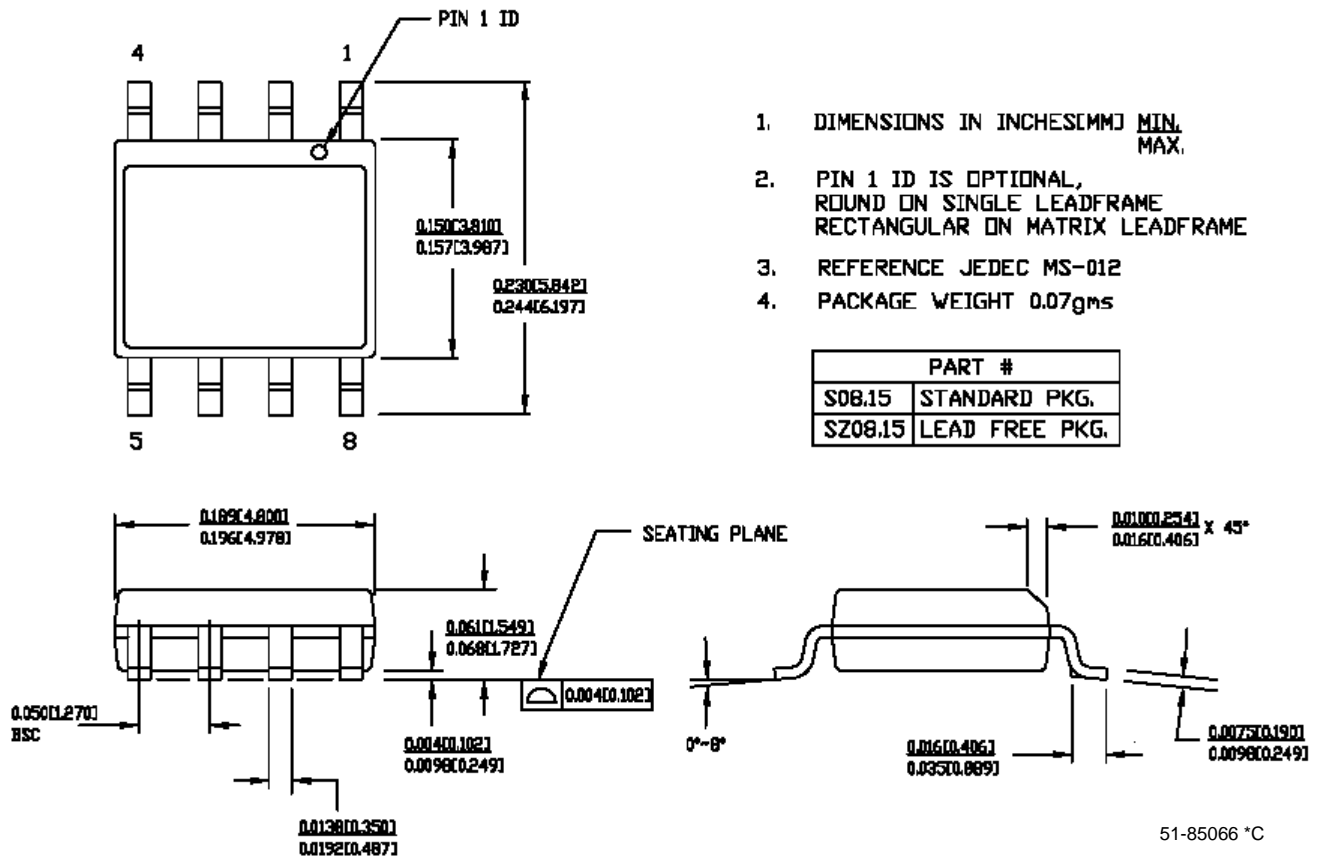


Figure 21. 20-Pin (300-Mil) Molded DIP

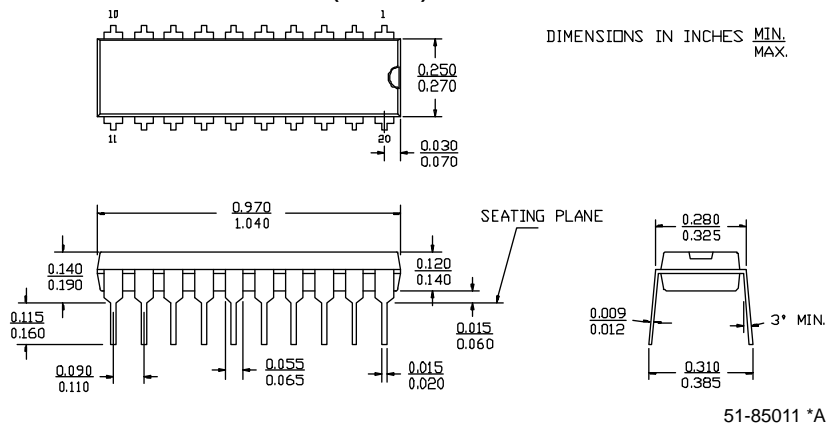


Figure 22. 20-Pin (210-Mil) SSOP

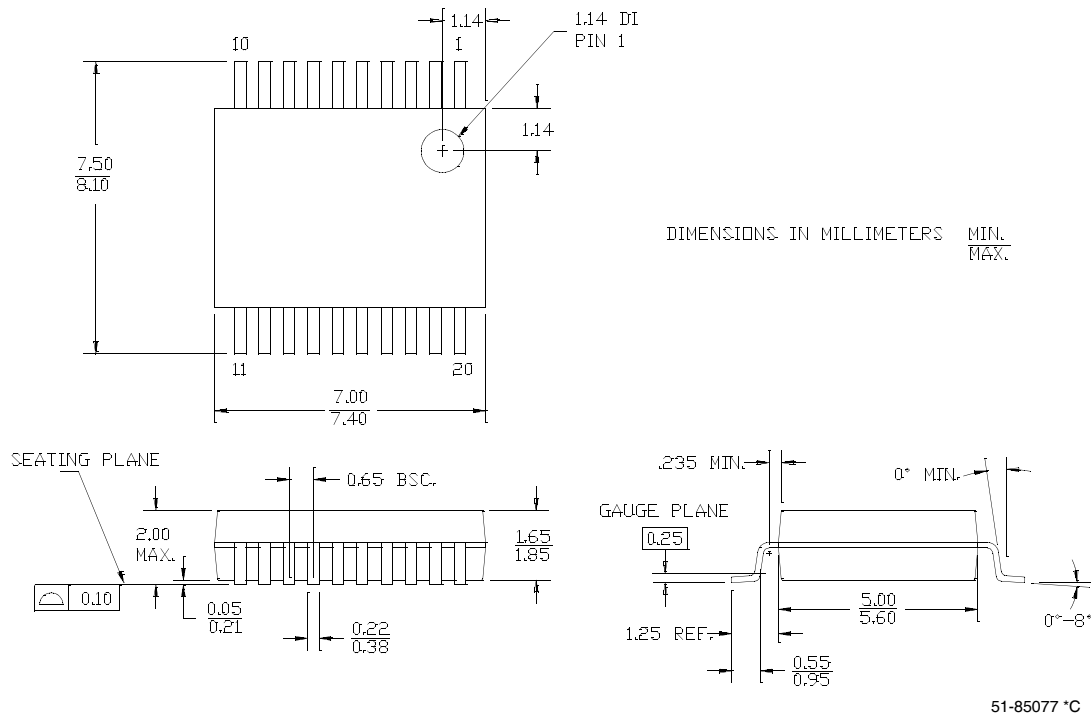


Figure 23. 20-Pin (300-Mil) Molded SOIC

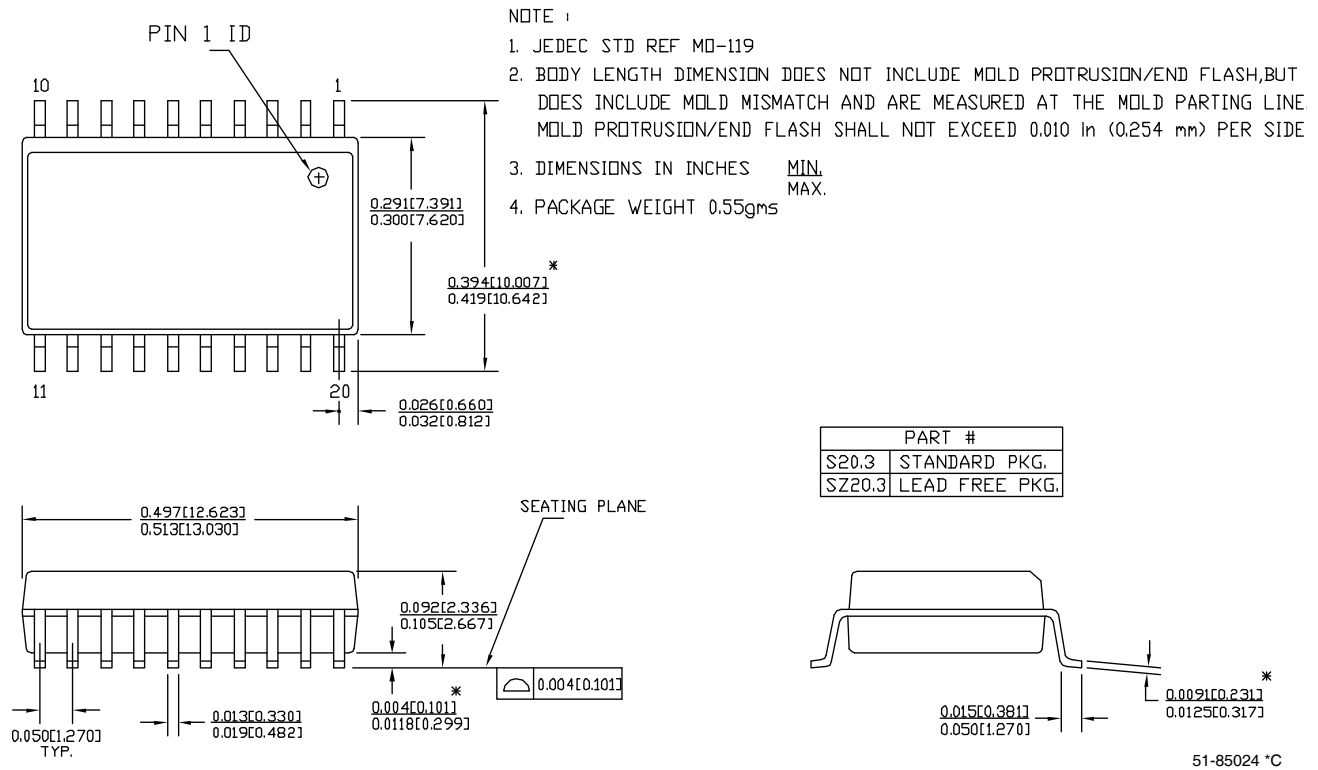
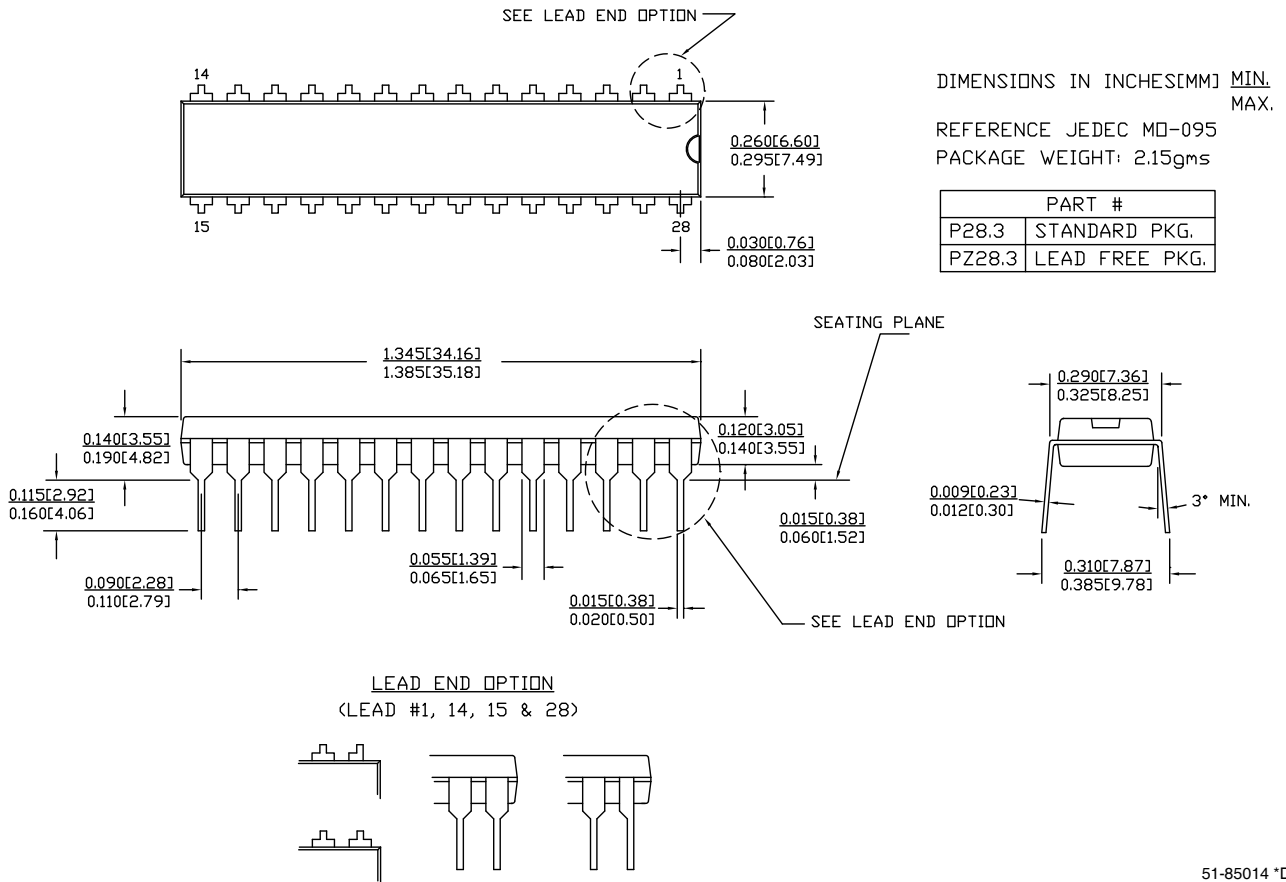


Figure 24. 28-Pin (300-Mil) Molded DIP



51-85014 *D

Figure 25. 28-Pin (210-Mil) SSOP

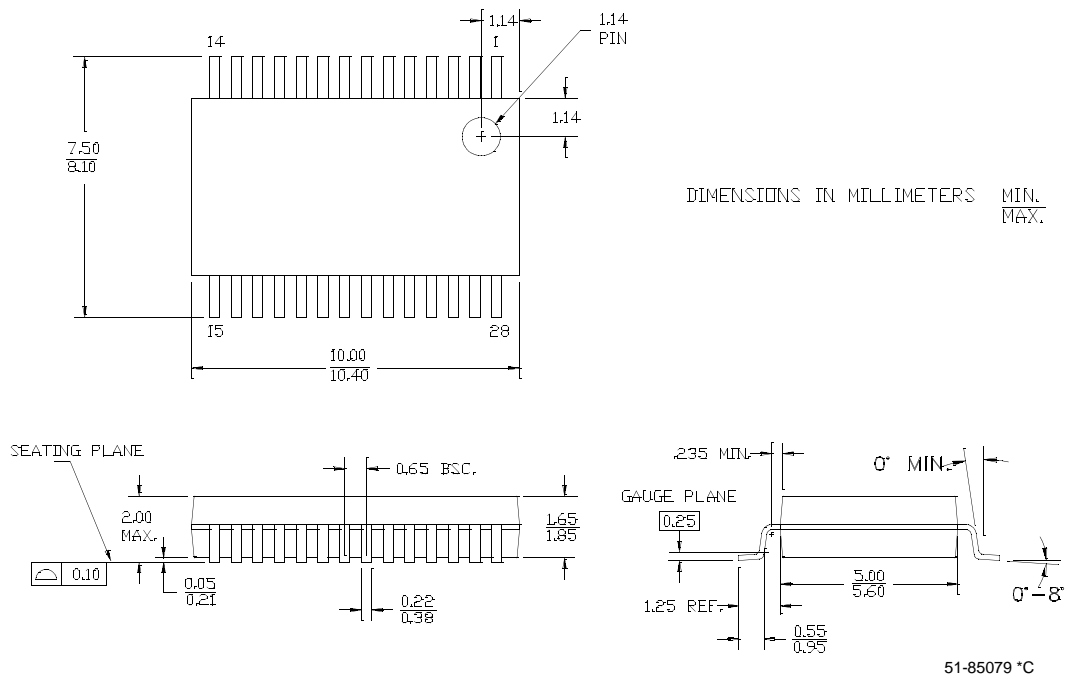


Figure 26. 28-Pin (300-Mil) Molded SOIC

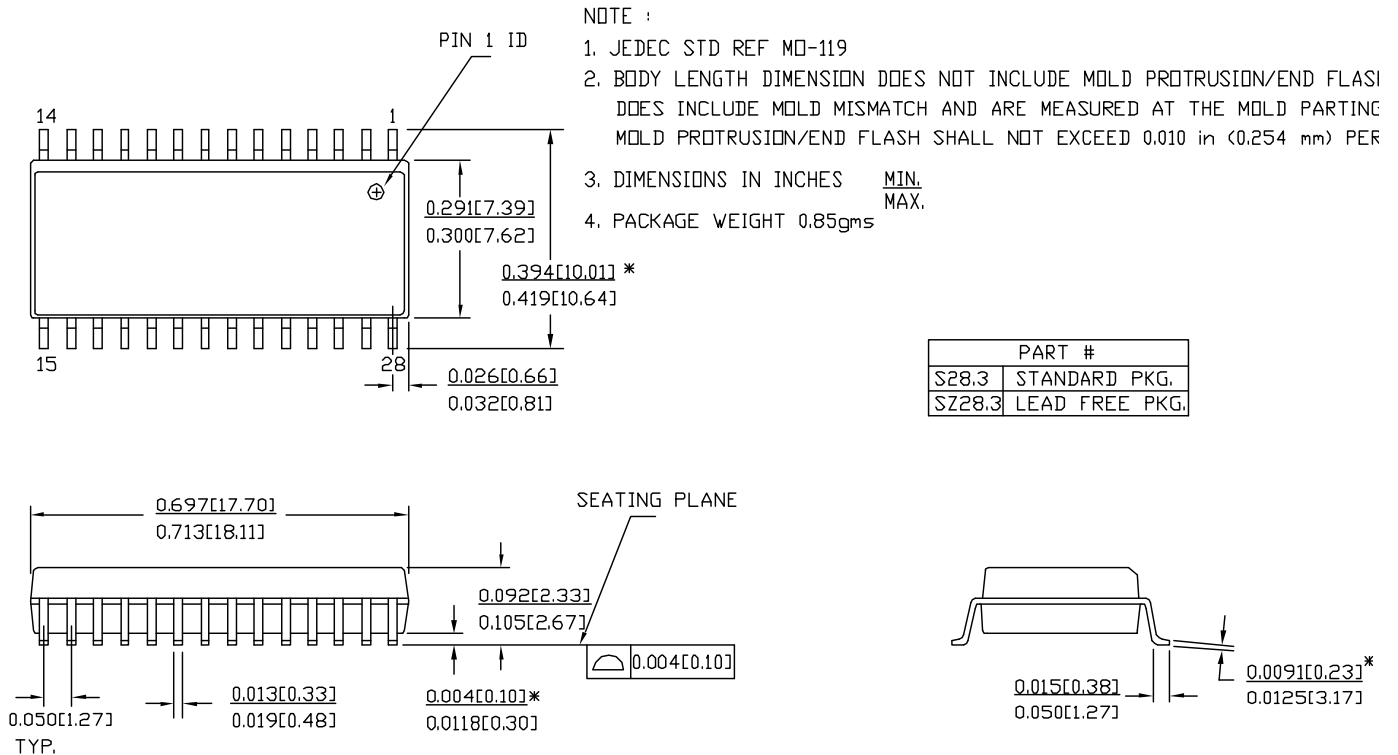
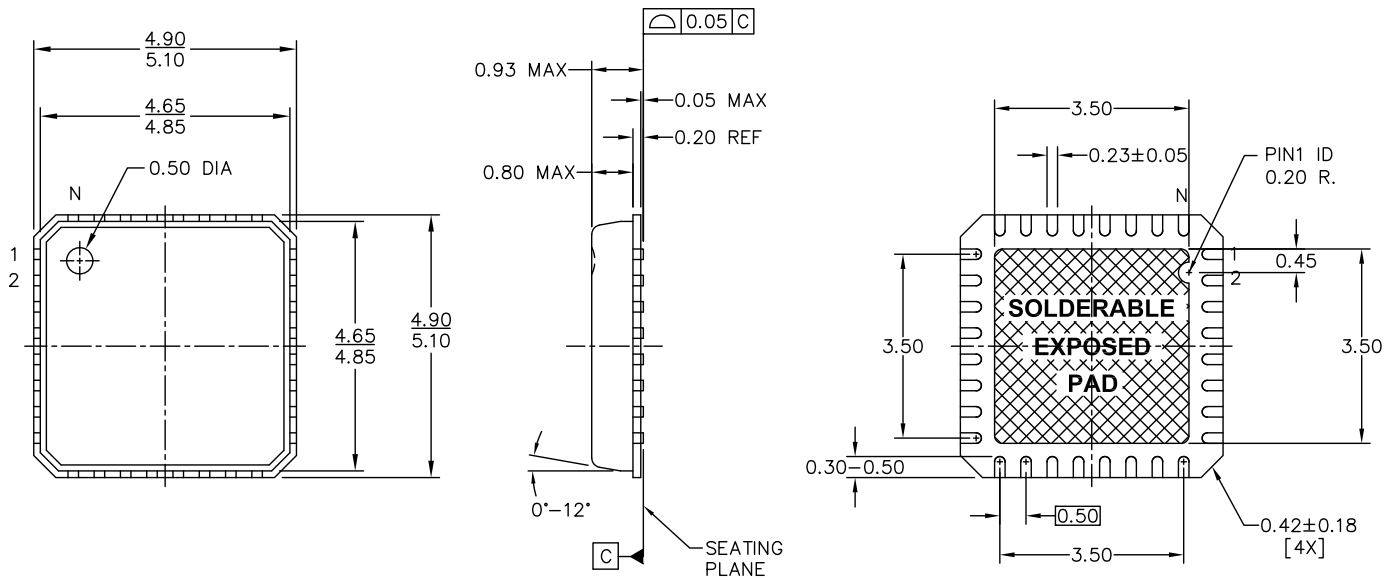



Figure 27. 32-Pin (5x5 mm) MLF



NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED PAD.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.054g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

| PART # | DESCRIPTION |
|--------|-------------|
| LF32 | STANDARD |
| LY32 | PB-FREE |

51-85188 *B

Thermal Impedances

Table 36. Thermal Impedances per Package

| Package | Typical θ_{JA} * |
|---------|-------------------------|
| 8 PDIP | 123 °C/W |
| 8 SOIC | 185 °C/W |
| 20 PDIP | 109 °C/W |
| 20 SSOP | 117 °C/W |
| 20 SOIC | 81 °C/W |
| 28 PDIP | 69 °C/W |
| 28 SSOP | 101 °C/W |
| 28 SOIC | 74 °C/W |
| 32 MLF | 22 °C/W |

* $T_J = T_A + \text{POWER} \times \theta_{JA}$

Capacitance on Crystal Pins

Table 37. Typical Package Capacitance on Crystal Pins

| Package | Package Capacitance |
|---------|---------------------|
| 8 PDIP | 2.8 pF |
| 8 SOIC | 2.0 pF |
| 20 PDIP | 3.0 pF |
| 20 SSOP | 2.6 pF |
| 20 SOIC | 2.5 pF |
| 28 PDIP | 3.5 pF |
| 28 SSOP | 2.8 pF |
| 28 SOIC | 2.7 pF |
| 32 MLF | 2.0 pF |

Ordering Information

The following table lists the CY8C24x23 PSoC Device family's key package features and ordering codes.

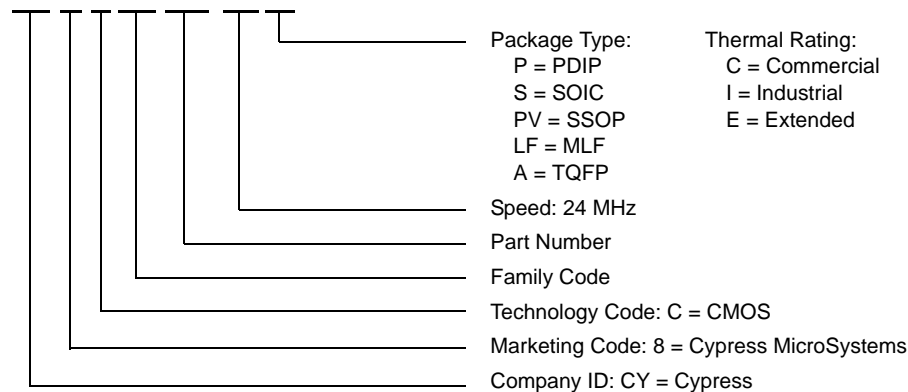
Table 38. CY8C24x23 PSoC Device Family Key Features and Ordering Information

| Package | Ordering Code | Flash (Kbytes) | RAM (Bytes) | Switch Mode Pump | Temperature Range | Digital Blocks (Rows of 4) | Analog Blocks (Columns of 3) | Digital IO Pins | Analog Inputs | Analog Outputs | XRES Pin |
|---------------------------------------|------------------|----------------|-------------|------------------|-------------------|----------------------------|------------------------------|-----------------|---------------|----------------|----------|
| 8 Pin (300 Mil) DIP | CY8C24123-24PI | 4 | 256 | No | -40°C to +85°C | 4 | 6 | 6 | 4 | 2 | No |
| 8 Pin (150 Mil) SOIC | CY8C24123-24SI | 4 | 256 | Yes | -40°C to +85°C | 4 | 6 | 6 | 4 | 2 | No |
| 8 Pin (150 Mil) SOIC (Tape and Reel) | CY8C24123-24SIT | 4 | 256 | Yes | -40°C to +85°C | 4 | 6 | 6 | 4 | 2 | No |
| 20 Pin (300 Mil) DIP | CY8C24223-24PI | 4 | 256 | Yes | -40°C to +85°C | 4 | 6 | 16 | 8 | 2 | Yes |
| 20 Pin (210 Mil) SSOP | CY8C24223-24PVI | 4 | 256 | Yes | -40°C to +85°C | 4 | 6 | 16 | 8 | 2 | Yes |
| 20 Pin (210 Mil) SSOP (Tape and Reel) | CY8C24223-24PVIT | 4 | 256 | Yes | -40°C to +85°C | 4 | 6 | 16 | 8 | 2 | Yes |
| 20 Pin (300 Mil) SOIC | CY8C24223-24SI | 4 | 256 | Yes | -40°C to +85°C | 4 | 6 | 16 | 8 | 2 | Yes |
| 20 Pin (300 Mil) SOIC (Tape and Reel) | CY8C24223-24SIT | 4 | 256 | Yes | -40°C to +85°C | 4 | 6 | 16 | 8 | 2 | Yes |
| 28 Pin (300 Mil) DIP | CY8C24423-24PI | 4 | 256 | Yes | -40°C to +85°C | 4 | 6 | 24 | 10 | 2 | Yes |
| 28 Pin (210 Mil) SSOP | CY8C24423-24PVI | 4 | 256 | Yes | -40°C to +85°C | 4 | 6 | 24 | 10 | 2 | Yes |
| 28 Pin (210 Mil) SSOP (Tape and Reel) | CY8C24423-24PVIT | 4 | 256 | Yes | -40°C to +85°C | 4 | 6 | 24 | 10 | 2 | Yes |
| 28 Pin (300 Mil) SOIC | CY8C24423-24SI | 4 | 256 | Yes | -40°C to +85°C | 4 | 6 | 24 | 10 | 2 | Yes |
| 28 Pin (300 Mil) SOIC (Tape and Reel) | CY8C24423-24SIT | 4 | 256 | Yes | -40°C to +85°C | 4 | 6 | 24 | 10 | 2 | Yes |
| 32 Pin (5x5 mm) MLF | CY8C24423-24LFI | 4 | 256 | Yes | -40°C to +85°C | 4 | 6 | 24 | 10 | 2 | Yes |

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

Ordering Code Definitions

CY 8 C 24 xxx-SPxx



Document History Page

| Document Title: CY8C24123, CY8C24223, CY8C24423 PSoC® Programmable System-on-Chip™ Document Number: 38-12011 | | | | |
|-----------------------------------------------------------------------------------------------------------------|---------|---------------------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | 127043 | New Silicon and NWJ | 05/15/2003 | New document – Advanced Data Sheet (two page product brief). |
| *A | 128779 | NWJ | 08/13/2003 | New document – Preliminary Data Sheet (300 page product detail). |
| *B | 129775 | MWR/NWJ | 09/26/2003 | Changes to Electrical Specifications section, Register Details chapter, and chapter changes in the Analog System section. |
| *C | 130128 | NWJ | 10/14/2003 | Revised document for Silicon Revision A. |
| *D | 131678 | NWJ | 12/04/2003 | Changes to Electrical Specifications section, Miscellaneous changes to I2C, GDI, RDI, Registers, and Digital Block chapters. |
| *E | 131802 | NWJ | 12/22/2003 | Changes to Electrical Specifications and miscellaneous small changes throughout the data sheet. |
| *F | 229418 | SFV | 06/04/2004 | New data sheet format and organization. Reference the <i>PSoC Programmable System-on-Chip Technical Reference Manual</i> for additional information. Title change. |
| *G | 2619935 | ONGE/AESA | 12/11/2008 | Changed title to “CY8C24123, CY8C24223, CY8C24423 PSoC® Programmable System-on-Chip™” Updated package diagrams 51-85188, 51-85024, 51-85014, and 51-85026. Added note on digital signaling in Table on page 23. Added Die Sales information note to Ordering Information on page 42. Updated data sheet template. |

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