Data Sheet | September 25, 2007 | FN6461.1

Ultra Low ON-Resistance, Low Voltage, Single Supply, Single SPST/1:2 Distribution Analog Switch

The Intersil ISL54054 and ISL54055 devices consist of low ON-resistance, low voltage, bi-directional SPST analog switches designed to operate from a single +1.8V to +5.5V supply. These devices have an unique architecture. They have two signal pins (pin 1 and pin 3) that are simultaneously connected or disconnected to a common pin (pin 4) under the control of a single logic control pin (pin 6). The ISL54054 switches are OFF when the logic is low and ON when the logic is high. The ISL54055 switches are ON when the logic is low and OFF when the logic is high. This architecture allows these devices to be used as a single SPST switch or as a distribution switch to distribute a single source to two different loads.

SPST operation is achieved by using one of the signal pins while floating the other signal pin or by externally connecting the two signal pins together. When both signal pins are tied together, the r_{ON} of the SPST is reduced by half, from 1Ω to 0.5Ω (when operated with a 5V supply).

Targeted applications include battery powered equipment that benefit from low r_{ON} resistance, excellent r_{ON} flatness, and fast switching speeds (t_{ON} = 12ns, t_{OFF} = 12ns). The digital logic input is 1.8V logic compatible when using a single 2.7V to +3.6V supply and TTL compatible when the supply is > +3.6V.

The ISL54054 and the ISL54055 are offered in a 6 Ld 1.2mmx1.0mmx0.5mm μTDFN package, alleviating board space limitations.

The ISL54054 has two normally open (NO) switches and the ISL54055 has two normally closed (NC) switches.

TABLE 1. FEATURES AT A GLANCE

	ISL54054	ISL54055
Number of Switches	1	1
SW	NO	NC
1.8V r_{ON}	1.1Ω	1.1Ω
1.8V t_{ON}/t_{OFF}	115ns/90ns	115ns/90ns
3V r_{ON}	0.51Ω	0.51Ω
3V t_{ON}/t_{OFF}	22ns/17ns	22ns/17ns
5V r_{ON}	0.34Ω	0.34Ω
5V t_{ON}/t_{OFF}	12ns/12ns	12ns/12ns
Packages	6 Ld μTDFN	

Features

- ON-resistance (r_{ON}) (Signal Pins Connected)
  - V_{CC} = +5.0V 0.34Ω
  - V_{CC} = +3.0V 0.51Ω
  - V_{CC} = +1.8V 1.1Ω
- r_{ON} flatness (+4.5V supply) 0.13Ω
- Single supply operation . . . . . +1.8V to +5.5V
- Fast switching action (+4.5V supply)
  - t_{ON} 12ns
  - t_{OFF} 12ns
- ESD HBM rating . . . . . >6kV
- 1.8V logic compatible (+3V supply)
- Available in 6 lead μTDFN Package
- Pb-free (RoHS compliant)

Applications

- Battery powered, handheld and portable equipment
  - Cellular/mobile phones
  - Pagers
  - Laptops, notebooks, palmtops
- Portable test and measurement
- Medical equipment
- Audio and video switching

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”

Ordering Information

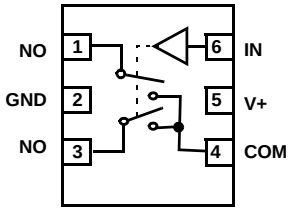
PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL54054IRUZ-T*	D	-40 to +85	6 Ld μTDFN Tape and Reel	L6.1.2x1.0A
ISL54055IRUZ-T*	E	-40 to +85	6 Ld μTDFN Tape and Reel	L6.1.2x1.0A

*Please refer to TB347 for details on reel specifications.

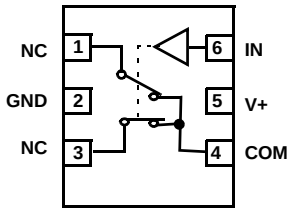
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinouts (Note 1)

ISL54054
(6 LD μTDFN)
TOP VIEW



ISL54055
(6 LD μTDFN)
TOP VIEW



NOTE:

1. Switches Shown for Logic “0” Input.

Truth Table

LOGIC	ISL54054 Both NO Switches	ISL54055 Both NC Switches
0	Off	On
1	On	Off

NOTE: Logic “0” ≤0.5V. Logic “1” ≥1.4V with a 3V supply.

Pin Descriptions

PIN	FUNCTION
V+	System Power Supply Input (+1.8V to +5.5V)
GND	Ground Connection
IN	Digital Control Input
COM	Analog Switch Common Pin
NO	Analog Switch Normally Open Pin
NC	Analog Switch Normally Closed Pin

Absolute Maximum Ratings

V+ to GND . . . . . -0.5V to 6.5V
Input Voltages
NO, NC, IN (Note 2). . . . . -0.5 to ((V+) + 0.5V)
Output Voltages
COM (Note 2). . . . . -0.5 to ((V+) + 0.5V)
Continuous Current NO, NC, or COM . . . . . ±300mA
Peak Current NO, NC, or COM
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . .±600mA
ESD Rating
Human Body Model . . . . . .>6kV
Machine Model. . . . . .>200V
Charged Device Model. . . . . .>1000V

Operating Conditions

V+ (Positive DC Supply Voltage) . . . . . 1.8V to 5.5V
Analog Signal Range . . . . . 0V to V+
V_{IN} (Digital Logic Input Voltage (IN). . . . . 0V to V+
Temperature Range . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
6 Ld μTDFN Package	175

Maximum Junction Temperature (Plastic Package). . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

2. Signals on NC, NO, IN, or COM exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum current ratings.
3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications - 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 4), Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 6)	TYP	MAX (Notes 5, 6)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON-Resistance, r_{ON} (Nx Inputs Connected)	V+ = 4.5V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+, (See Figure 4)	25	-	0.36	-	Ω
		Full	-	0.49	-	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$ (Nx Inputs Connected)	V+ = 4.5V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+, (Note 7)	25	-	0.12	-	Ω
		Full	-	0.13	-	Ω
ON-Resistance, r_{ON} (Single Nx Input)	V+ = 4.5V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+, (See Figure 4)	25	-	0.85	-	Ω
		Full	-	1.1	-	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$ (Single Nx Input)	V+ = 4.5V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+, (Note 7)	25	-	0.25	-	Ω
		Full	-	0.25	-	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 5.5V, V_{COM} = 0.3V, 5V, V_{NO} or V_{NC} = 5V, 0.3V	25	-10	5	10	nA
		Full	-150	-	150	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 5.5V, V_{COM} = 0.3V, 5V, or V_{NO} or V_{NC} = 0.3V, 5V, or floating	25	-20	9	20	nA
		Full	-300	-	300	nA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 4.5V, V_{NO} or V_{NC} = 3.0V, R_L = 50Ω, C_L = 35pF (See Figure 1)	25	-	12	-	ns
		Full	-	15	-	ns
Turn-OFF Time, t_{OFF}	V+ = 4.5V, V_{NO} or V_{NC} = 3.0V, R_L = 50Ω, C_L = 35pF (See Figure 1)	25	-	12	-	ns
		Full	-	15	-	ns
Charge Injection, Q	V_G = 0V, R_G = 0Ω, C_L = 1.0nF (See Figure 2)	25	-	71	-	pC
OFF Isolation (Nx Inputs Connected)	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$ (See Figure 3)	25	-	74	-	dB
OFF Isolation (Single Nx Input)	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$ (See Figure 3)	25	-	83	-	dB

Electrical Specifications - 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 4), Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 6)	TYP	MAX (Notes 5, 6)	UNITS
-3dB Bandwidth (Nx Inputs Connected)	R_L = 50Ω	25	-	72	-	MHz
-3dB Bandwidth (Single Nx Input)	R_L = 50Ω	25	-	138	-	MHz
NO or NC OFF Capacitance, C_{OFF} (Nx Inputs Connected)	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 5)	25	-	30	-	pF
COM ON Capacitance, $C_{COM(ON)}$ (Nx Inputs Connected)	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 5)	25	-	62	-	pF
NO or NC OFF Capacitance, C_{OFF} (Single Nx Input)	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 5)	25	-	16	-	pF
COM ON Capacitance, $C_{COM(ON)}$ (Single Nx Input)	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 5)	25	-	89	-	pF
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	1.8	-	5.5	V
Positive Supply Current, I+	V+ = 5.5V, V_{IN} = 0V or V+	25	-	-	0.5	µA
		Full	-	-	1.0	µA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	0.8	V
Input Voltage High, V_{INH}		Full	2.4	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 5.5V, V_{IN} = 0V or V+	Full	-1	-	1	µA

Electrical Specifications - 3V Supply

Test Conditions: V+ = +2.7V to +3.6V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V (Note 4), Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 6)	TYP	MAX (Notes 5, 6)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON-Resistance, r_{ON} (Nx Inputs Connected)	V+ = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+, (See Figure 4)	25	-	0.57	0.65	Ω
		Full	-	0.73	1.0	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$ (Nx Inputs Connected)	V+ = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+, (Note 7)	25	-	0.2	0.4	Ω
		Full	-	0.2	0.5	Ω
ON-Resistance, r_{ON} (Single Nx Input)	V+ = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+, (See Figure 4)	25	-	1.3	1.7	Ω
		Full	-	1.6	2.0	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$ (Single Nx Input)	V+ = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+, (Note 7)	25	-	0.4	0.6	Ω
		Full	-	0.4	0.7	Ω
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (See Figure 1)	25	-	22	-	ns
		Full	-	25	-	ns
Turn-OFF Time, t_{OFF}	V+ = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (See Figure 1)	25	-	17	-	ns
		Full	-	20	-	ns
Charge Injection, Q	V_G = 0V, R_G = 0Ω, C_L = 1.0nF (See Figure 2)	25	-	42	-	pC
OFF Isolation (Nx Inputs Connected)	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$ (See Figure 3)	25	-	74	-	dB
OFF Isolation (Single Nx Input)	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$ (See Figure 3)	25	-	83	-	dB
NO or NC OFF Capacitance, C_{OFF} (Nx Inputs Connected)	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 5)	25	-	30	-	pF

Electrical Specifications - 3V Supply

Test Conditions: V+ = +2.7V to +3.6V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V (Note 4), Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 6)	TYP	MAX (Notes 5, 6)	UNITS
COM ON Capacitance, $C_{COM(ON)}$ (Nx Inputs Connected)	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 5)	25	-	62	-	pF
NO or NC OFF Capacitance, C_{OFF} (Single Nx Input)	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 5)	25	-	16	-	pF
COM ON Capacitance, $C_{COM(ON)}$ (Single Nx Input)	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 5)	25	-	89	-	pF
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	0.5	V
Input Voltage High, V_{INH}		Full	1.4	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 3.6V, V_{IN} = 0V or V+	Full	-1	-	1	µA

Electrical Specifications - 1.8V Supply

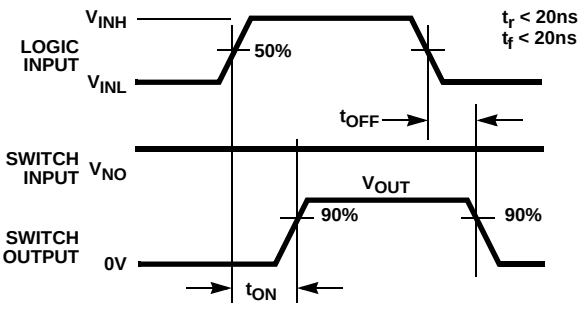
Test Conditions: V+ = +1.8V, GND = 0V, V_{INH} = 1.8V, V_{INL} = 0V (Note 4), Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 6)	TYP	MAX (Notes 5, 6)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON-Resistance, r_{ON} (Nx Inputs Connected)	V+ = 1.8V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+, Pins 1 and 3 connected, (See Figure 4)	25	-	1.1	-	Ω
		Full	-	1.3	-	Ω
ON-Resistance, r_{ON} (Single Nx Input)	V+ = 1.8V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+ (See Figure 4)	25	-	2.3	-	Ω
		Full	-	2.53	-	Ω
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 1.8V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (See Figure 1)	25	-	115	-	ns
		Full	-	246	-	ns
Turn-OFF Time, t_{OFF}	V+ = 1.8V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (See Figure 1)	25	-	90	-	ns
		Full	-	192	-	ns
Charge Injection, Q	V_G = 0V, R_G = 0Ω,C_L = 1.0nF (See Figure 2)	25	-	22	-	pC

NOTES:

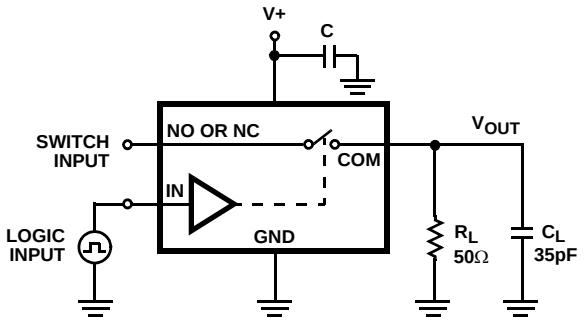
4. V_{IN} = input voltage to perform proper function.
5. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. Parts are 100% tested at +25°C. Over-temperature limits established by characterization and are not production tested.
7. Flatness is defined as the difference between maximum and minimum value of on-resistance over the specified analog signal range.

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + r_{(ON)}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

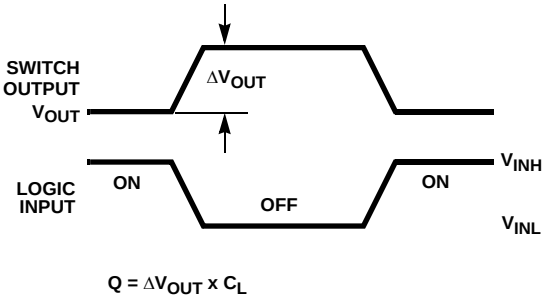


FIGURE 2A. MEASUREMENT POINTS

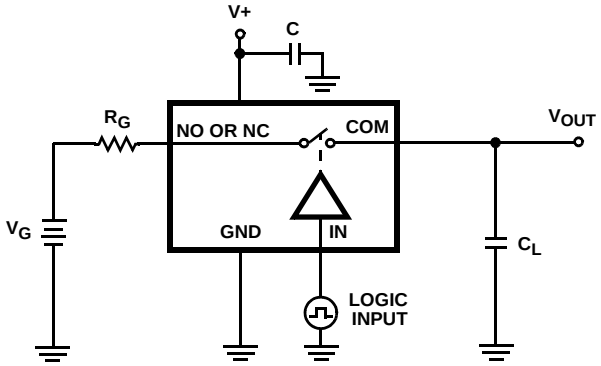


FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

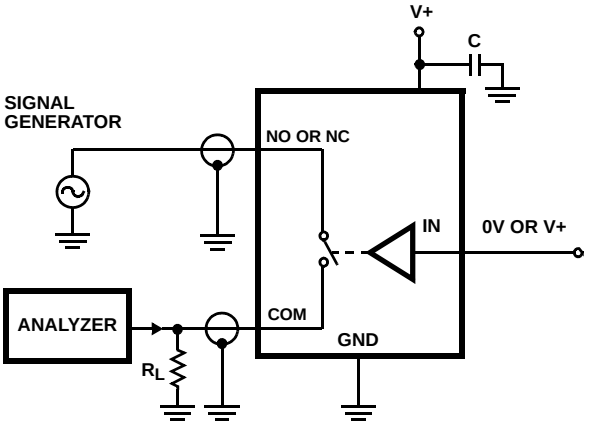


FIGURE 3. OFF ISOLATION TEST CIRCUIT

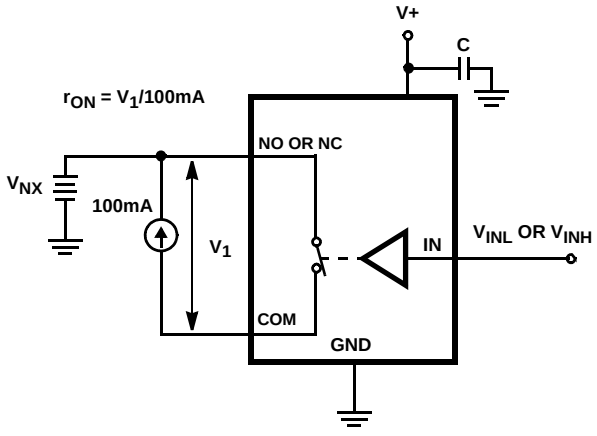


FIGURE 4. r_{ON} TEST CIRCUIT

Test Circuits and Waveforms (Continued)

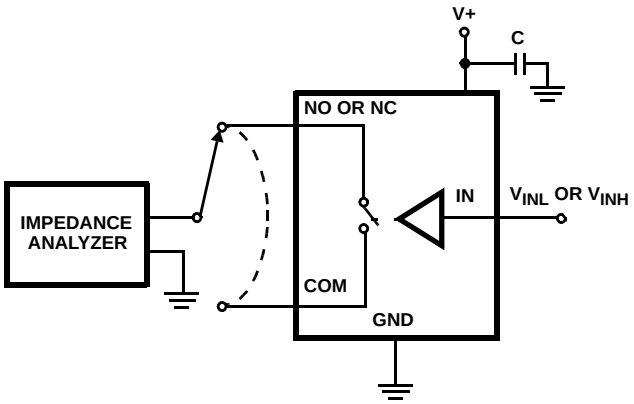


FIGURE 5. CAPACITANCE TEST CIRCUIT

Detailed Description

The Intersil ISL54054 and ISL54055 devices consist of low ON-resistance, low voltage, bi-directional analog switches designed to operate from a single +1.8V to +5.5V supply. With a single supply of 5V the typical ON-resistance is only 0.34Ω, with a typical turn-on and turn-off time of: t_{ON} = 12ns, t_{OFF} = 12ns. The devices are especially well suited for portable battery powered equipment due to its low operating supply voltage (1.8V), low power consumption (5.5µW), low leakage currents (300nA max) and the tiny µTDFN package.

These devices have an unique architecture. They have two signal pins (pin 1 and pin 3) that are simultaneously connected or disconnected to a single common pin (pin 4) under the control of a single logic control pin (pin 6). The ISL54054 switches are OFF when the logic is low and ON when the logic is high. The ISL54055 are ON when the logic is low and OFF when the logic is high. This architecture allows these devices to be used as a single SPST switch or as a distribution switch to distribute a single source to two different loads.

SPST operation is achieved by using one of the Nx signal pins while floating the other Nx signal pin or by externally connecting the two Nx signal pins together. When both signal pins are tied together, the r_{ON} of the SPST is reduced by half, from 1Ω to 0.5Ω (when operated with a 5V supply).

The ISL54054 is a normally open (NO) SPST analog switch. The ISL54055 is a normally closed (NC) SPST analog switch.

Supply Sequencing and Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents, which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to GND (see Figure 6). To prevent forward biasing these diodes, V+ must be applied before any input signals, and the input signal voltages must remain between V+ and GND. If these conditions cannot be guaranteed, then one of the following two protection methods should be employed.

Logic inputs can easily be protected by adding a 1kΩ resistor in series with the input (see Figure 6). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

This method is not acceptable for the signal path inputs. Adding a series resistor to the switch input defeats the purpose of using a low r_{ON} switch. Connecting schottky diodes to the signal pins (as shown in Figure 6) will shunt the fault current to the supply or to ground, thereby protecting the switch. These schottky diodes must be sized to handle the expected fault current.

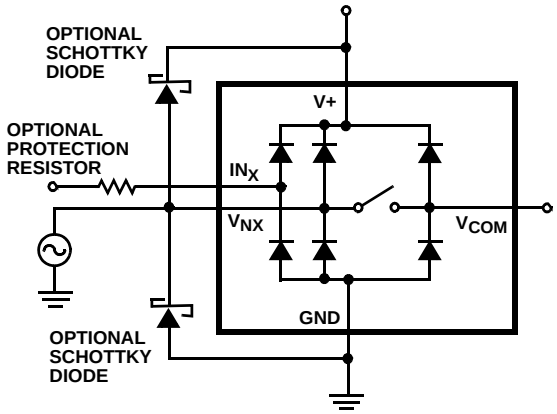


FIGURE 6. OVERVOLTAGE PROTECTION

Power-Supply Considerations

The construction of the ISL54054 and the ISL54055 is typical of most single supply CMOS analog switches in that they have two supply pins: V+ and GND. V+ and GND drive the internal CMOS switches and set their analog voltage limits. Unlike switches with a 4.5V maximum supply voltage, the ISL54054 and the ISL54055's 5.5V maximum supply voltage provides plenty of room for the 10% tolerance of 4.5V supplies, as well as room for overshoot and noise spikes.

The minimum recommended supply voltage is 1.8V. It is important to note that the input signal range, switching times, and on-resistance degrade at lower supply voltages. Refer to the "Electrical Specifications" tables starting on page 3 and "Typical Performance Curves" on page 8 for details.

V+ and GND also power the internal logic and level shiftier. The level shiftier converts the input logic levels to switched V+ and GND signals to drive the analog switch gate terminals.

This family of switches cannot be operated with bipolar supplies, because the input switching point becomes negative in this configuration.

Logic-Level Thresholds

This switch family is 1.8V logic compatible (0.5V and 1.4V) over a supply range of 2.5V to 5V (see Figure 19). At 5V the V_{IH} level is about 1.38V. This is still below the 1.8V CMOS guaranteed high output minimum level of 1.4V, but noise margin is reduced. At 1.8V operation the V_{IL} level is around 0.1V and can only be used in 1.8V applications with minimal ground bounce.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation.

High-Frequency Performance

In 50Ω systems, the ISL54054 and the ISL54055 have a -3dB bandwidth of 72MHz with Nx pins connected and 138MHz for a single Nx input (see Figure 20). The frequency response is very consistent over a wide V+ range, and for varying analog signal levels.

An OFF switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feedthrough from a switch's input to its output. Off isolation is the resistance to this feedthrough. Figure 21 details the high off isolation rejection provided by this family. At 100kHz, off isolation in 50Ω systems is about 74dB with Nx pins connected and 83dB with a single Nx input, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease off isolation rejection due to the voltage divider action of the switch OFF impedance and the load impedance.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND.

Virtually all the analog leakage current comes from the ESD diodes to V+ or GND. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and V+ or GND.

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified

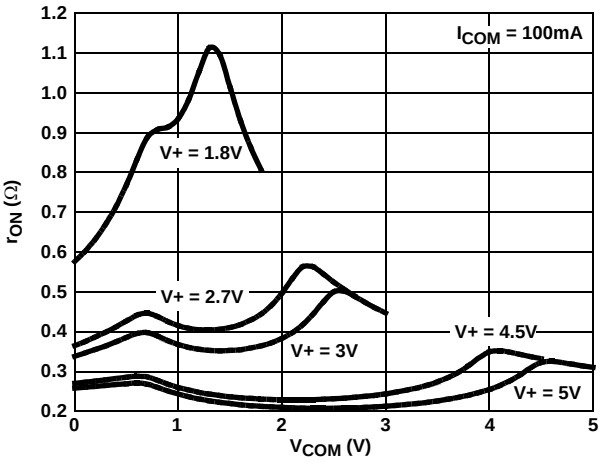


FIGURE 7. ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE (NX PINS CONNECTED)

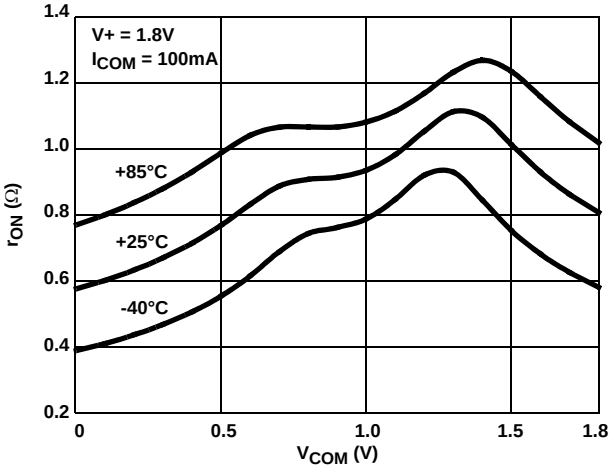


FIGURE 8. ON-RESISTANCE vs SWITCH VOLTAGE (NX PINS CONNECTED)

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

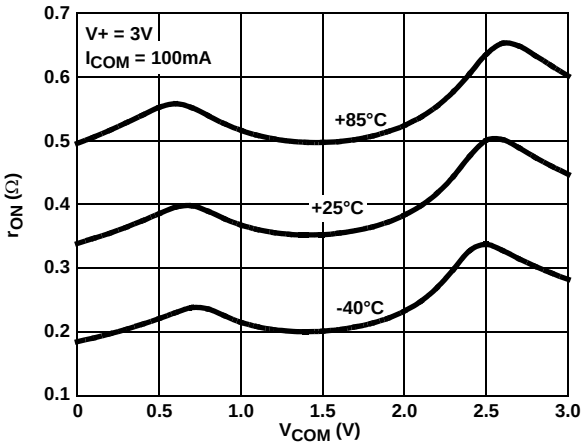


FIGURE 9. ON-RESISTANCE VS SWITCH VOLTAGE (NX PINS CONNECTED)

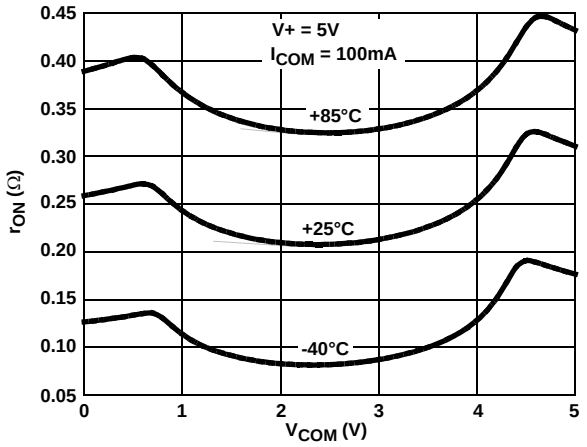


FIGURE 10. ON-RESISTANCE vs SWITCH VOLTAGE (NX PINS CONNECTED)

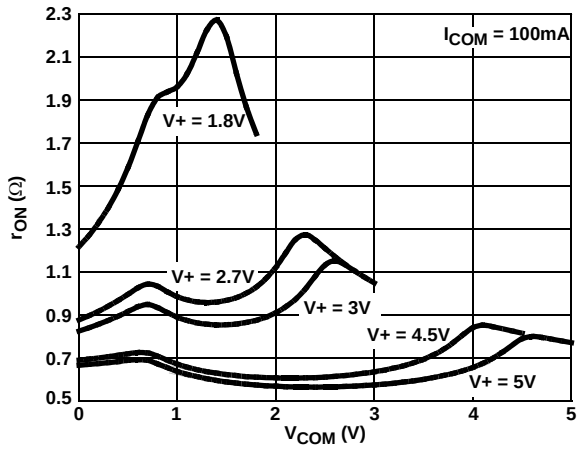


FIGURE 11. ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE (SINGLE NX INPUT)

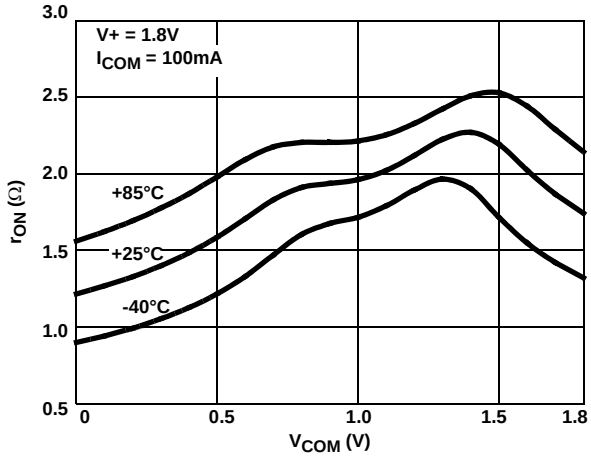


FIGURE 12. ON-RESISTANCE vs SWITCH VOLTAGE (SINGLE NX INPUT)

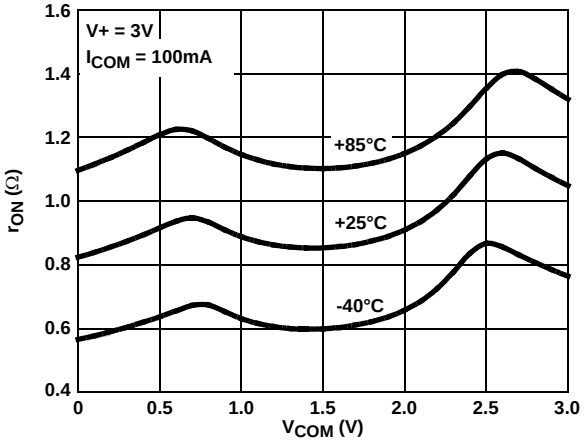


FIGURE 13. ON-RESISTANCE vs SWITCH VOLTAGE (SINGLE NX INPUT)

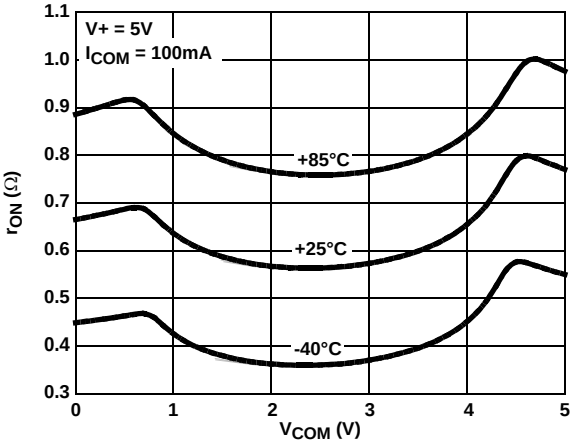


FIGURE 14. ON-RESISTANCE vs SWITCH VOLTAGE (SINGLE NX INPUT)

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

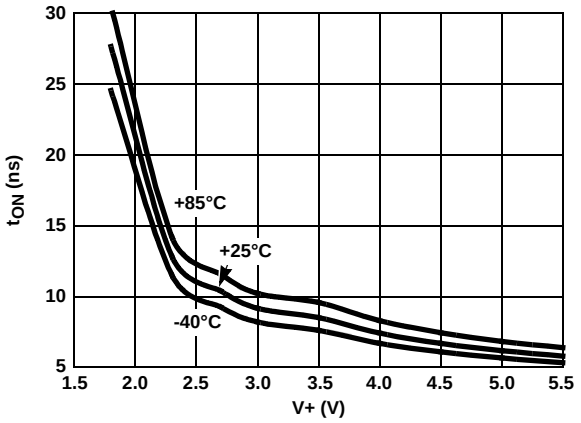


FIGURE 15. TURN ON TIME vs SUPPLY VOLTAGE (ISL54054)

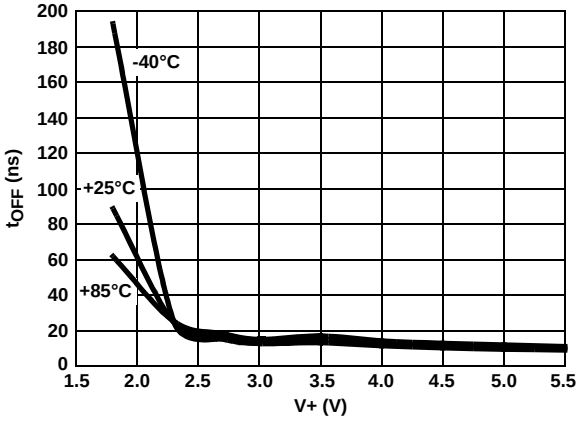


FIGURE 16. TURN OFF TIME vs SUPPLY VOLTAGE (ISL54054)

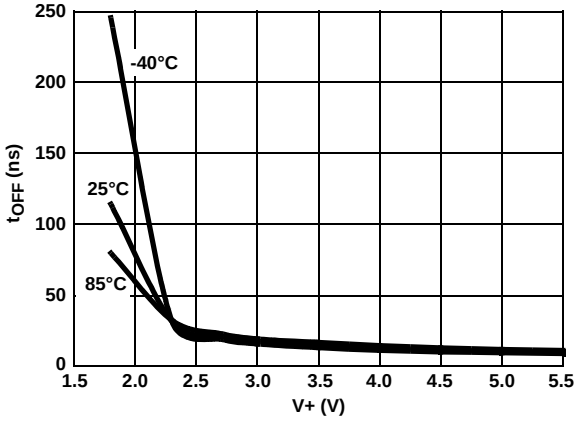


FIGURE 17. TURN ON TIME vs SUPPLY VOLTAGE (ISL54055)

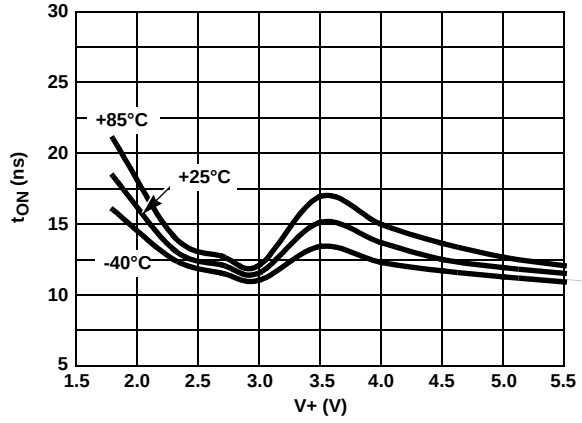


FIGURE 18. TURN OFF TIME vs SUPPLY VOLTAGE (ISL54055)

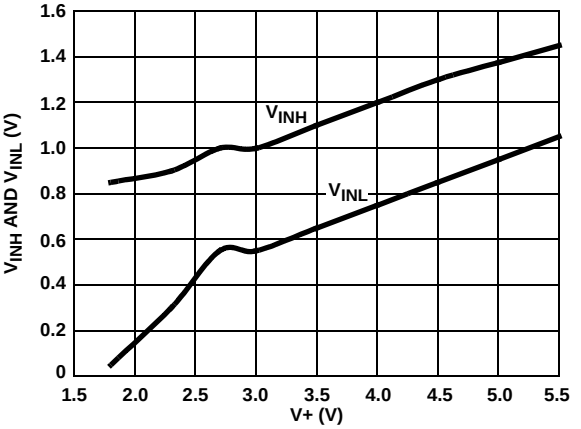


FIGURE 19. DIGITAL SWITCHING POINT vs SUPPLY VOLTAGE

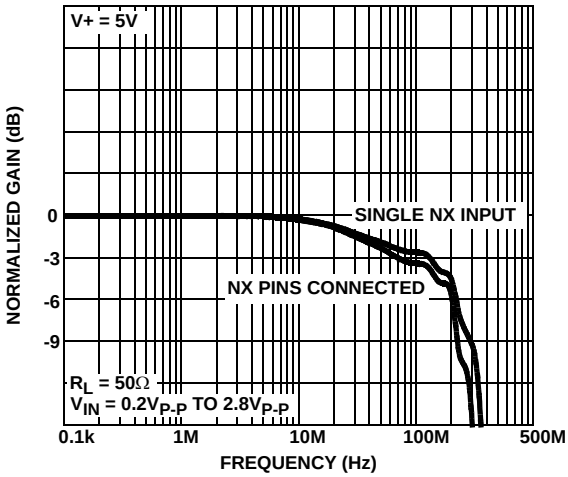


FIGURE 20. FREQUENCY RESPONSE

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

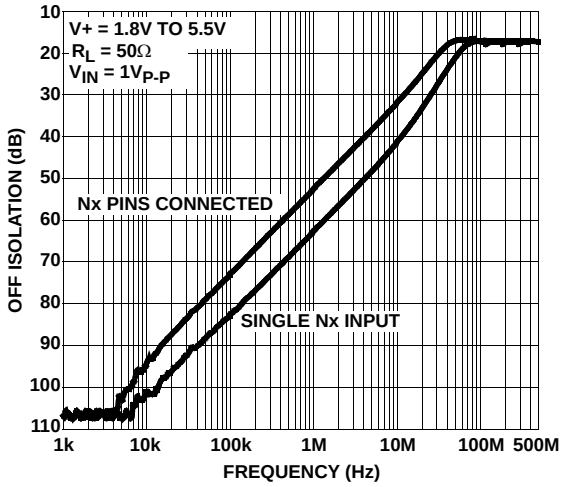


FIGURE 21. OFF ISOLATION

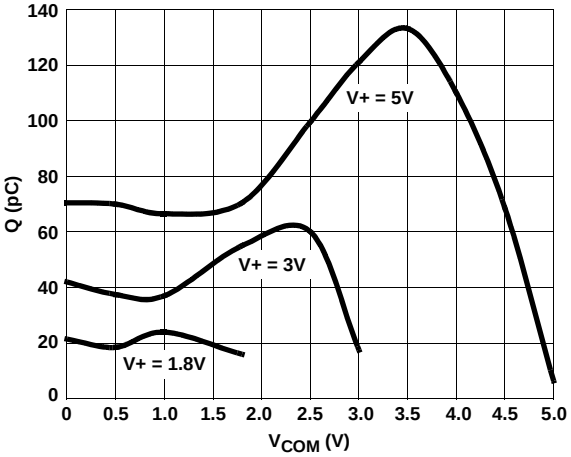


FIGURE 22. CHARGE INJECTION vs SWITCH VOLTAGE

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

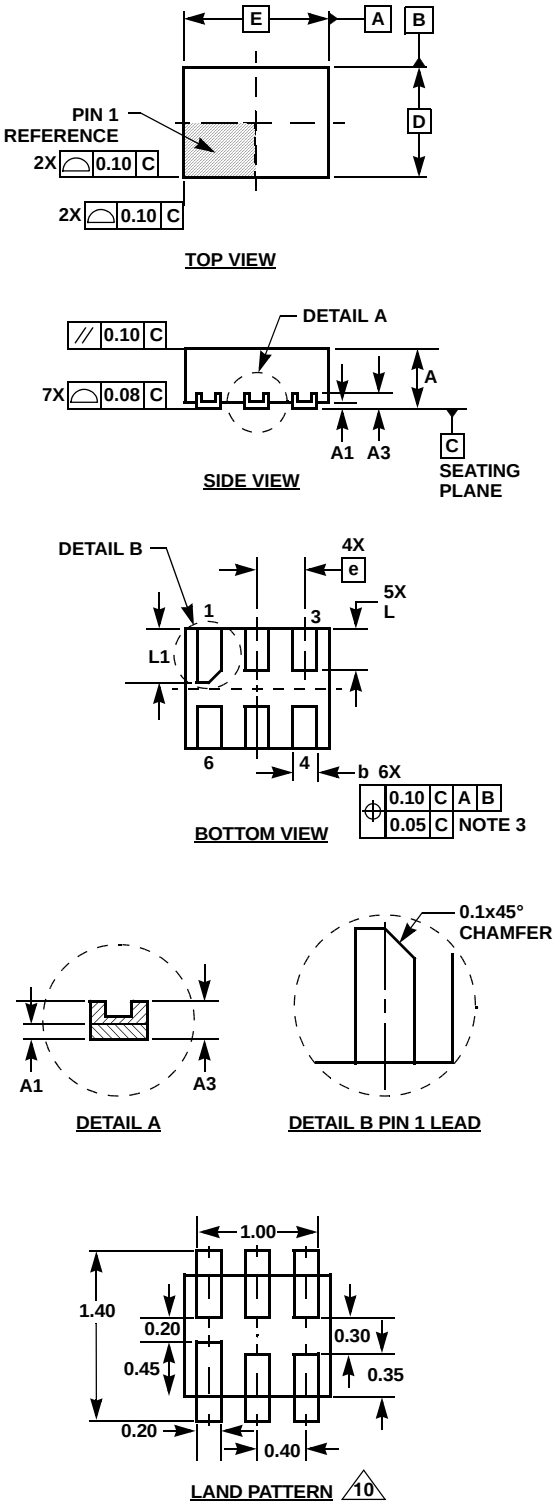
TRANSISTOR COUNT:

57

PROCESS:

Submicron CMOS

Ultra Thin Dual Flat No-Lead Plastic Package (UTDFN)



L6.1.2x1.0A

6 LEAD ULTRA THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3		0.127 REF		-
b	0.15	0.20	0.25	5
D	0.95	1.00	1.05	-
E	1.15	1.20	1.25	-
e		0.40 BSC		-
L	0.30	0.35	0.40	-
L1	0.40	0.45	0.50	-
N		6		2
Ne		3		3
θ	0	-	12	4

Rev. 2 8/06

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Ne refers to the number of terminals on E side.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05mm.
8. Maximum allowable burrs is 0.076mm in all directions.
9. JEDEC Reference MO-255.
10. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.