19-5017; Rev 0; 10/09

High-ESD Profibus RS-485 Transceiver

General Description

The MAX14770E is a half-duplex, ±35kV high ESD-protected transceiver for Profibus-DP® and RS-485 applications. In addition, it can be used for RS-422/V.11 communications. The MAX14770E is designed to meet IEC 61158-2, TIA/EIA-422-B, TIA/EIA-485-A, V.11, and X.27 standards.

The MAX14770E operates from a +5V supply and has true fail-safe circuitry that guarantees a logic-high receiver output when the receiver inputs are open or shorted.

The MAX14770E features a 1/4 standard-unit load receiver input impedance, allowing up to 128 1/4 unit load transceivers on the bus. Drivers are short-circuit current limited and are protected against excessive power dissipation by thermal-shutdown circuitry.

The MAX14770E is available in 8-pin SO and tiny TDFN (3mm x 3mm) packages, and is specified over the extended (-40°C to +85°C) and automotive (-40°C to +125°C) temperature ranges.

Applications

Profibus-DP Networks

Industrial Fieldbusses

Motion Controllers

RS-485 Networks

Machine Encoders

Typical Profibus-DP Operating Circuit appears at end of data sheet.

Features

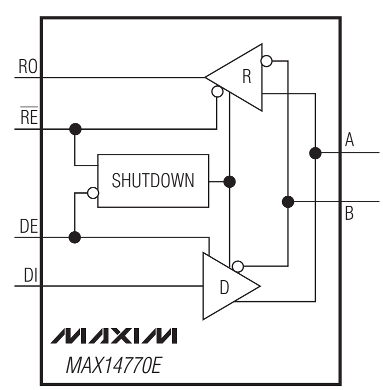
- ♦ **Meets EIA 61158-2 Type 3 Profibus-DP**
- ♦ **+4.5V to +5.5V Supply Voltage**
- ♦ **20Mbps Data Rate**
- ♦ **Short-Circuit Protected**
- ♦ **True Fail-Safe Receiver**
- ♦ **Thermal-Shutdown Protected**
- ♦ **Hot Swappable**
- ♦ **High ESD Protection**
  - **±35kV Human Body Model (HBM)**
  - **±20kV IEC 61000-4-2 Air Gap**
  - **±10kV IEC 61000-4-2 Contact**
- ♦ **-40°C to +125°C Automotive Temperature Range in Tiny 8-Pin (3mm x 3mm) TDFN**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX14770EESA+T	-40°C to +85°C	8 SO	—
MAX14770EATA+T	-40°C to +125°C	8 TDFN-EP*	BMG

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed pad.*

Functional Diagram



High-ESD Profibus RS-485 Transceiver

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)
V_{CC} ....-0.3V to +6.0V
$\overline{RE}$, RO...-0.3V to (V_{CC} + 0.3V)
DE, DI ....-0.3V to +6.0V
A, B...-8.0V to +13.0V
Short-Circuit Duration (RO, A, B) to GND ....Continuous
Continuous Power Dissipation (T_A = +70°C)
8-Pin SOIC (derate 7.6mW/°C above +70°C) 606mW
8-Pin TDFN (derate 24.4mW/°C above +70°C)........1951mW
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 1)
8-Pin SO...132°C/W
8-Pin TDFN...41°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) (Note 1)
8-Pin SO...38°C/W
8-Pin TDFN...8°C/W
Operating Temperature Range
8-Pin SO..-40°C to +85°C
8-Pin TDFN..-40°C to +125°C
Storage Temperature Range............................ -65°C to +150°C
Junction Temperature Range........................... -40°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic/thermal-tutorial.**

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Range	V_{CC}		4.5		5.5	V
Supply Current	I_{CC}	DE = 1, $\overline{RE}$ = 0 or DE = 0, $\overline{RE}$ = 0 or DE = 1, $\overline{RE}$ = 1; no load		2.5	4	mA
Shutdown Supply Current	I_{SH}	DE = 0, $\overline{RE}$ = 1			15	µA
DRIVER						
Differential Driver Output	$\|V_{OD}\|$	R_L = 54Ω, V_{DI} = V_{CC} or GND; Figure 1	2.1			V
Differential Driver Peak-to-Peak Output	V_{ODPP}	Figure 2 (Note 3)	4.0		6.8	V
Change in Magnitude of Differential Output Voltage	ΔV_{OD}	R_L = 54Ω; Figure 1 (Note 4)	-0.2	0	+0.2	V
Driver Common-Mode Output Voltage	V_{OC}	R_L = 54Ω; Figure 1		1.8	3	V
Change in Common-Mode Voltage	ΔV_{OC}	R_L = 54Ω; Figure 1 (Note 4)	-0.2		+0.2	V
Driver Short-Circuit Output Current (Note 5)	I_{OSD}	0V ≤ V_{OUT} ≤ +12V; output low			+250	mA
		-7V ≤ V_{OUT} ≤ V_{CC}; output high	-250			
Driver Short-Circuit Foldback Output Current (Note 5)	I_{OSDF}	(V_{CC} - 1V) ≤ V_{OUT} ≤ +12V; output low	-15			mA
		-7V ≤ V_{OUT} ≤ +1V; output high			+15	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS						
Driver Input High Voltage	V_{IH}	DE, DI, $\overline{RE}$	2.0			V
Driver Input Low Voltage	V_{IL}	DE, DI, $\overline{RE}$			0.8	V
Driver Input Hysteresis	V_{HYS}	DE, DI, $\overline{RE}$		50		mV
Driver Input Current	I_{IN}	DE, DI, $\overline{RE}$	-1		+1	µA
Input Impedance in Hot Swap	R_{DE}	Figure 11 until the first low-to-high transition of DE occurs	1	5.6	10	kΩ
	$R_{\overline{RE}}$	Figure 11 until the first high-to-low transition of $\overline{RE}$ occurs				
RECEIVER						
Input Current (A, B)	I_A, I_B	DE = GND, V_{CC} = GND or +5.5V; V_{IN} = 12V			+250	µA
		DE = GND, V_{CC} = GND or +5.5V; V_{IN} = -7V	-200			
Differential Input Capacitance	C_{AB}	Between A and B, DE = $\overline{RE}$ = GND at 6MHz		8		pF
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ 12V	-200	-125	-50	mV
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V		15		mV
LOGIC OUTPUT						
Output High Voltage	V_{OH}	I_{OUT} = -1mA, V_A - V_B = V_{TH}	V_{CC} - 1.5			V
Output Low Voltage	V_{OL}	I_{OUT} = 1mA, V_A - V_B = -V_{TH}			0.4	V
Three-State Receiver Output Current	I_{OZR}	0V ≤ V_{OUT} ≤ V_{CC}	-1		+1	µA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V	48			kΩ
Receiver Output Short-Circuit Current	I_{OSR}	0V ≤ V_{RO} ≤ V_{CC}	-110		+110	mA
PROTECTION SPECIFICATIONS						
Thermal-Shutdown Threshold	V_{TS}			+160		°C
Thermal-Shutdown Hysteresis	V_{TSH}			15		°C
ESD Protection, A and B Pins		HBM		±35		kV
		IEC 61000-4-2 Air-Gap Discharge to GND		±20		
		IEC 61000-4-2 Contact Discharge to GND		±10		
ESD Protection, All Other Pins		HBM		±2		kV

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER SWITCHING CHARACTERISTICS						
Driver Propagation Delay	t_{DPLH} t_{DPHL}	R_L = 54Ω, C_L = 50pF; Figures 3 and 4			28	ns
Differential Driver Output Skew $\|t_{DPLH} - t_{DPHL}\|$	t_{DSKEW}	R_L = 54Ω, C_L = 50pF; Figures 3 and 4		1.2		ns
Driver Output Transition Skew $\|t_{t(MLH)}\|$, $\|t_{t(MHL)}\|$	t_{TSKEW}	R_L = 54Ω, C_L = 50pF; Figures 3 and 5		2		ns
Driver Differential Output Rise or Fall Time	t_{LH}, t_{HL}	R_L = 54Ω, C_L = 50pF; Figures 3 and 4			15	ns
Maximum Data Rate			20			Mbps
Driver Enable to Output High	t_{DZH}	R_L = 500Ω, C_L = 50pF; Figure 6			50	ns
Driver Enable to Output Low	t_{DZL}	R_L = 500Ω, C_L = 50pF; Figure 7			50	ns
Driver Disable Time from Low	t_{DLZ}	R_L = 500Ω, C_L = 50pF; Figure 7			40	ns
Driver Disable Time from High	t_{DHZ}	R_L = 500Ω, C_L = 50pF, Figure 6			40	ns
Driver Enable Skew Time	$\|t_{ZL} - t_{ZH}\|$	R_L = 500Ω, C_L = 50pF; Figures 6 and 7			8	ns
Driver Disable Skew Time	$\|t_{LZ} - t_{HZ}\|$	R_L = 500Ω, C_L = 50pF; Figures 6 and 7			8	ns
Driver Enable from Shutdown to Output High	$t_{DZL(SHDN)}$	R_L = 500Ω, C_L = 50pF; Figure 7 (Note 6)			100	µs
Driver Enable from Shutdown to Output Low	$t_{DZH(SHDN)}$	R_L = 500Ω, C_L = 50pF; Figure 6 (Note 6)			100	µs
Time to Shutdown	t_{SHDN}	(Note 6)	50		800	ns
RECEIVER SWITCHING CHARACTERISTICS						
Receiver Propagation Delay	t_{RPLH} t_{RPHL}	C_L = 15pF; Figures 8 and 9 (Note 7)			28	ns
Receiver Output Skew	t_{RSKEW}	C_L = 15pF; Figures 8 and 9 (Notes 7, 8)			2	ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Data Rate			20			Mbps
Receiver Enable to Output High	t_{RZH}	S2 closed; R_L = 1kΩ, C_L = 15pF; Figure 10			30	ns
Receiver Enable to Output Low	t_{RZL}	S1 closed; R_L = 1kΩ, C_L = 15pF; Figure 10			30	ns
Receiver Disable Time from Low	t_{RLZ}	S1 closed; R_L = 1kΩ, C_L = 15pF; Figure 10			30	ns
Receiver Disable Time from High	t_{RHZ}	S2 closed; R_L = 1kΩ, C_L = 15pF; Figure 10			30	ns
Receiver Enable from Shutdown to Output High	$t_{RZL(SHDN)}$	S1 closed; R_L = 1kΩ, C_L = 15pF; Figure 10 (Notes 6, 7)			100	µs
Receiver Enable from Shutdown to Output Low	$t_{RZH(SHDN)}$	S2 closed; R_L = 1kΩ, C_L = 15pF; Figure 10 (Notes 6, 7)			100	µs
Time to Shutdown	t_{SHDN}	(Note 6)	50		800	ns

Note 2: Devices are production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.
Note 3: V_{ODPP} is the difference in V_{OD}, with the DI at high and DI at low.
Note 4: ΔV_{OD} and ΔV_{OC} are the changes in $|V_{OD}|$ and $|V_{OC}|$, respectively, with the DI at high and DI at low.
Note 5: The short-circuit output current applies to peak current just prior to foldback current limiting; the short-circuit foldback output current applies during current limiting to allow a recovery from bus contention.
Note 6: Shutdown is enabled by bringing $\overline{RE}$ high and DE low. If the enable inputs are in this state for less than 50ns, the device is guaranteed not to enter shutdown. If the enable inputs are in this state for at least 800ns, the device is guaranteed to have entered shutdown.
Note 7: Capacitive load includes test probe and fixture capacitance.
Note 8: Guaranteed by characterization, not production tested.

High-ESD Profibus RS-485 Transceiver

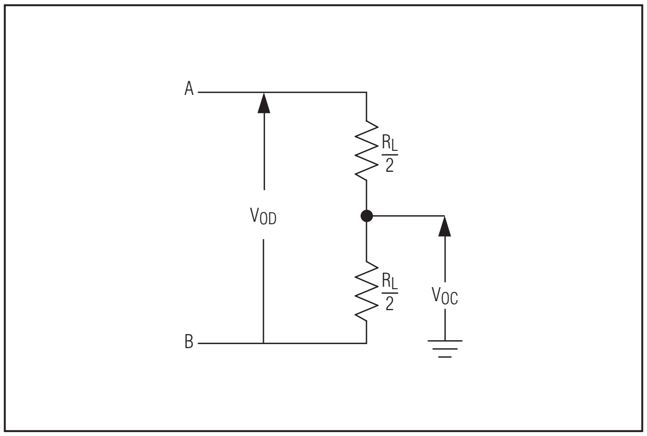


Figure 1. Driver DC Test Load

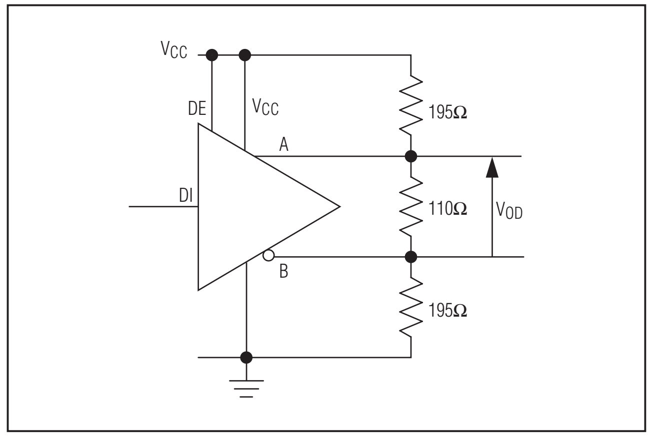


Figure 2. V_{ODPP} Swing Under Profibus Equivalent Load Test

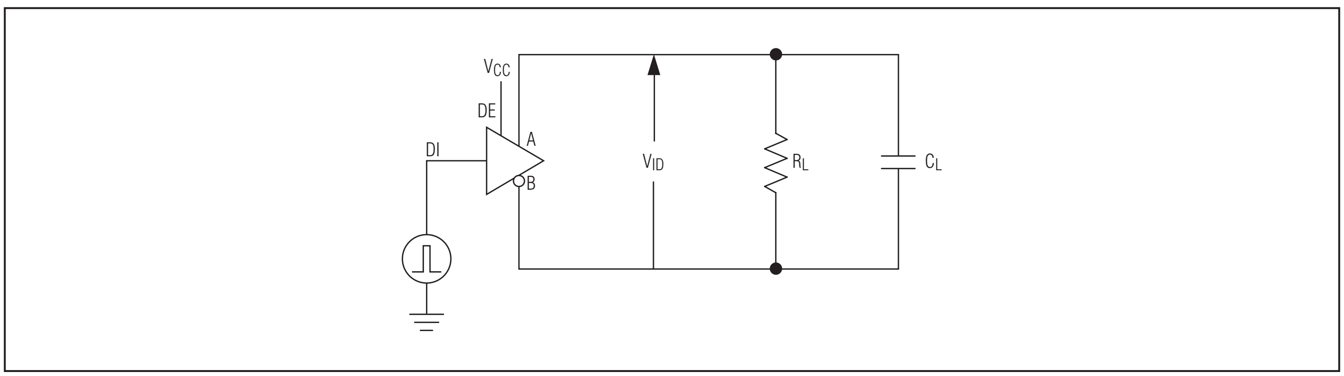


Figure 3. Driver Timing Test Circuit

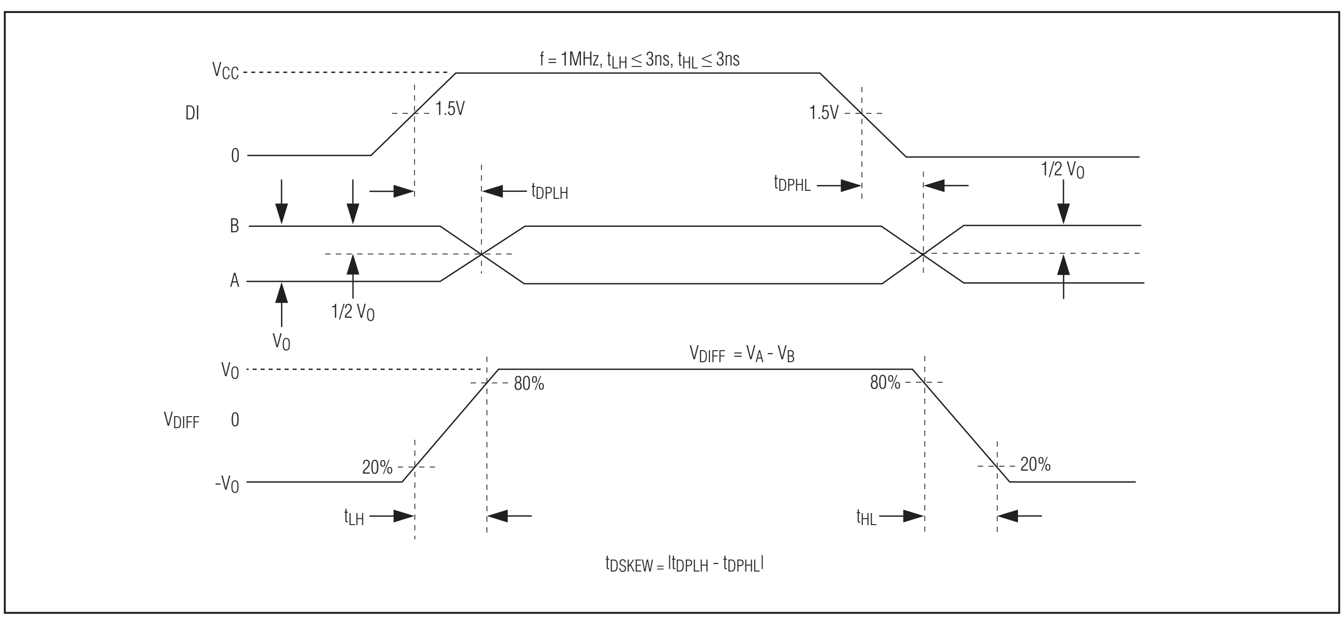


Figure 4. Driver Propagation Delays

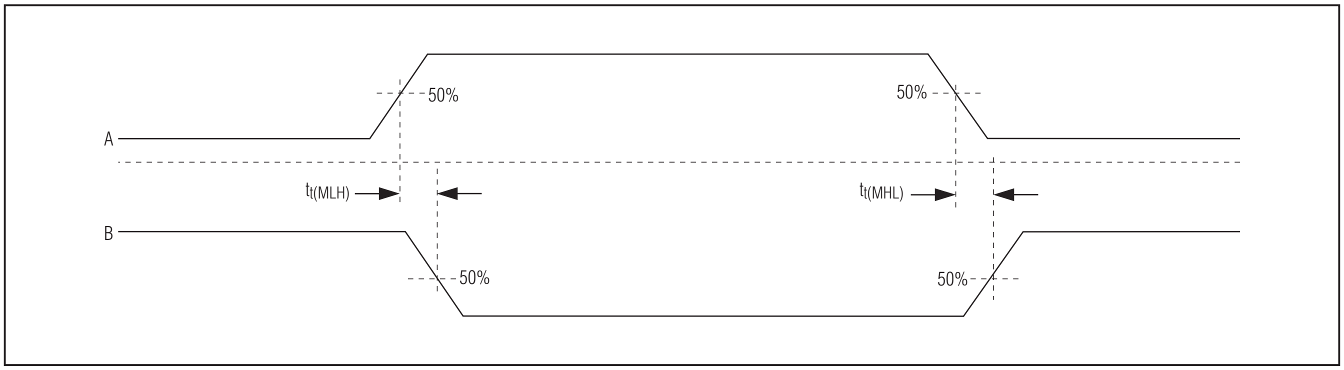


Figure 5. Driver Transition Skew

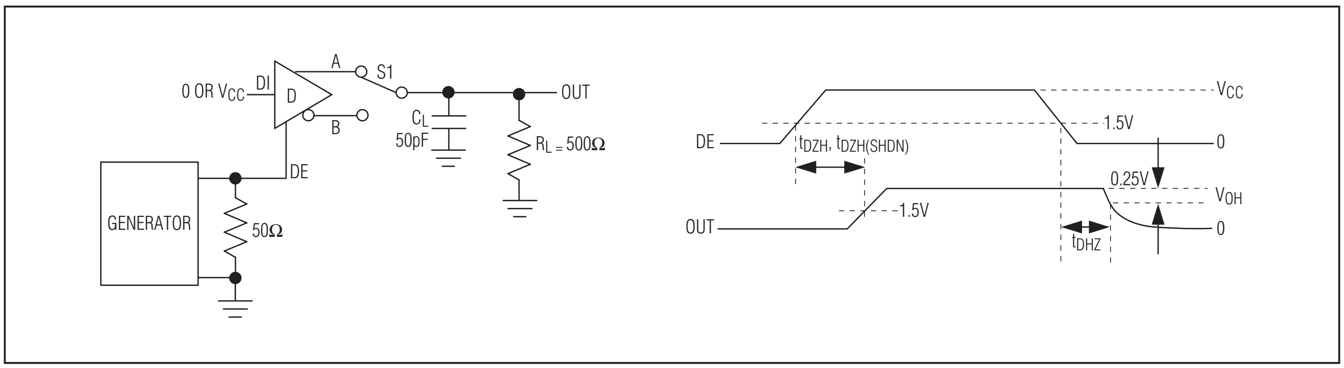


Figure 6. Driver Enable and Disable Times

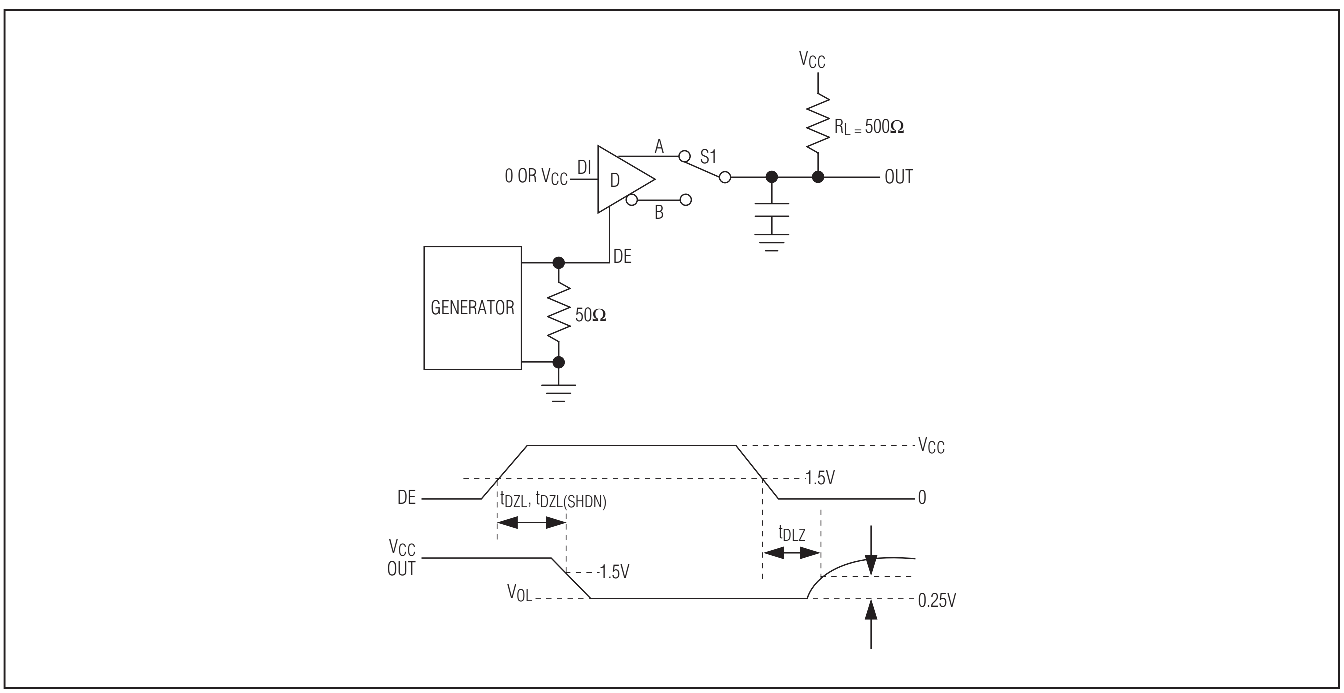


Figure 7. Driver Enable and Disable Times

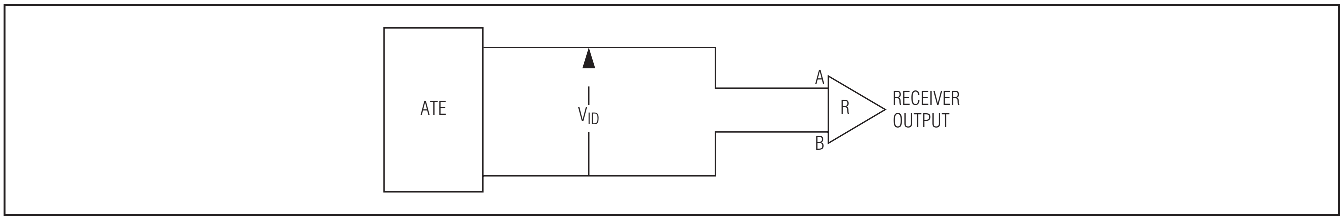


Figure 8. Receiver Propagation Delay Test Circuit

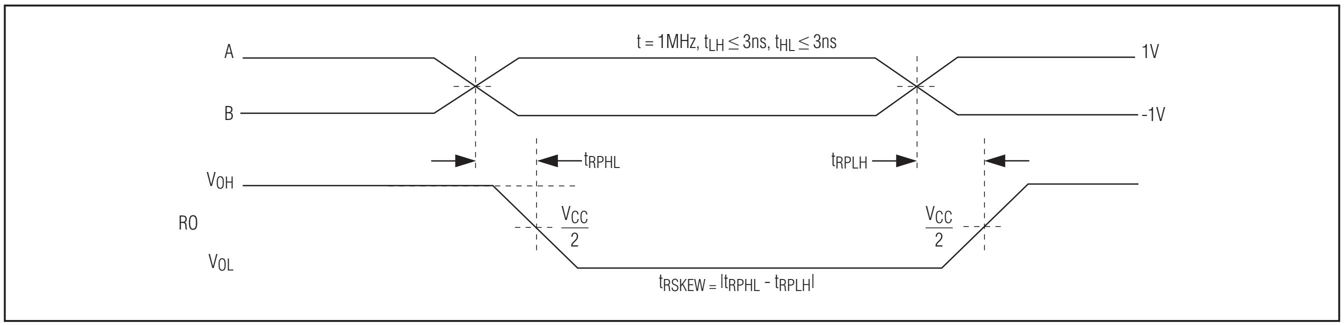


Figure 9. Receiver Propagation Delays

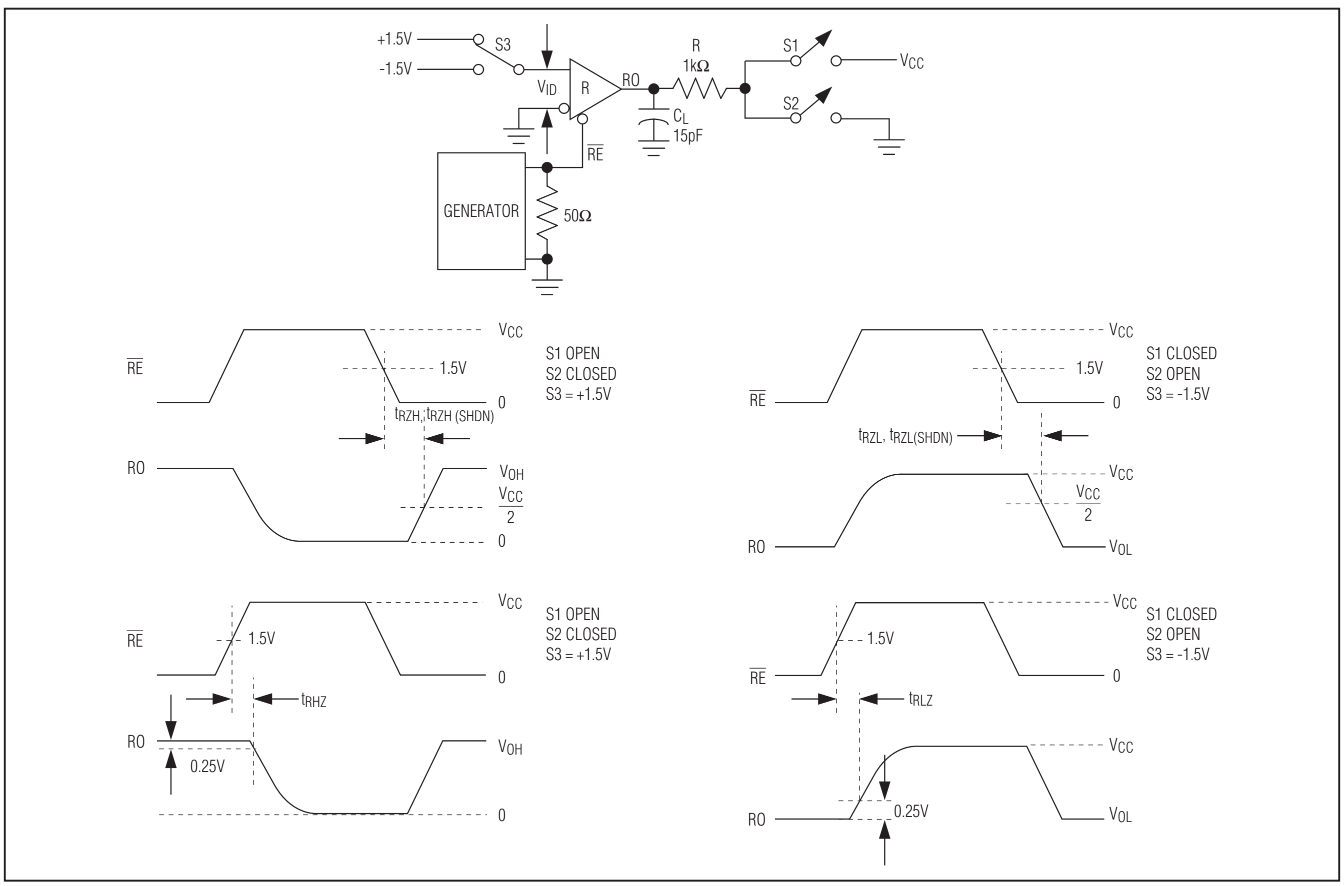
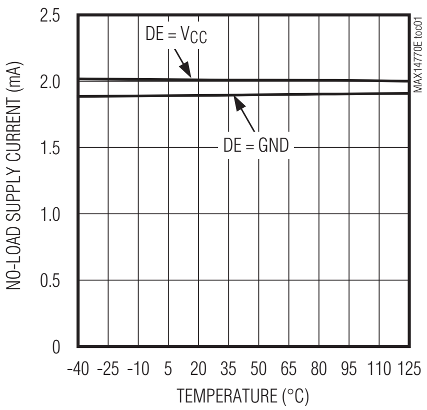


Figure 10. Receiver Enable and Disable Times

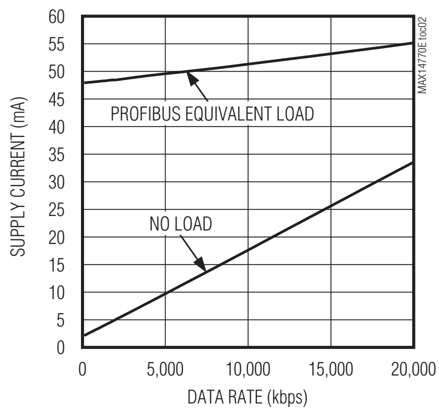
Typical Operating Characteristics

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

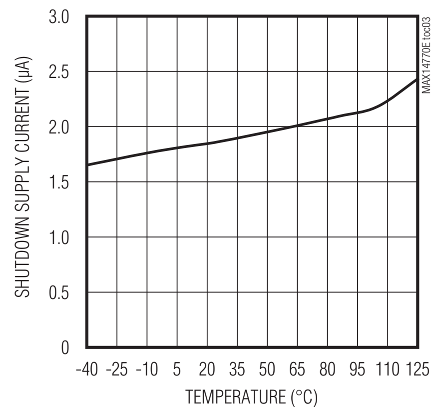
NO-LOAD DC SUPPLY CURRENT vs. TEMPERATURE



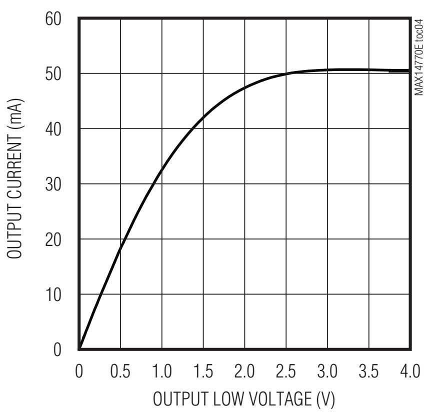
SUPPLY CURRENT vs. DATA RATE



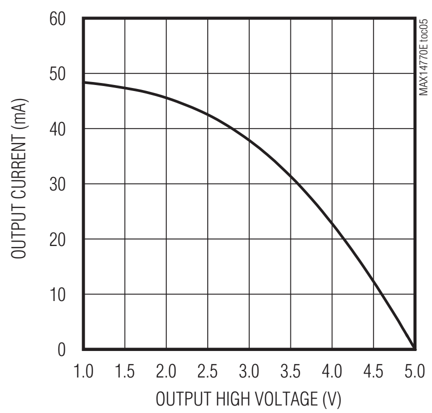
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



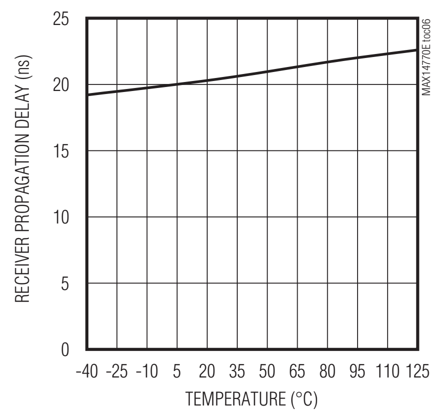
RECEIVER OUTPUT RO CURRENT vs. OUTPUT LOW VOLTAGE



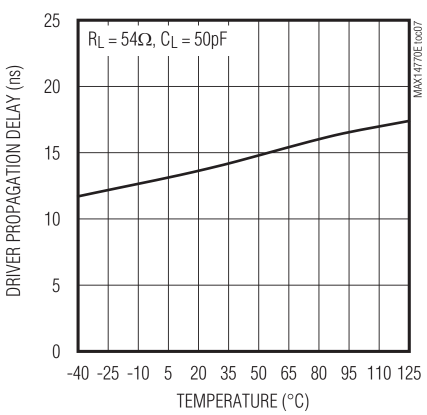
RECEIVER OUTPUT RO CURRENT vs. OUTPUT HIGH VOLTAGE



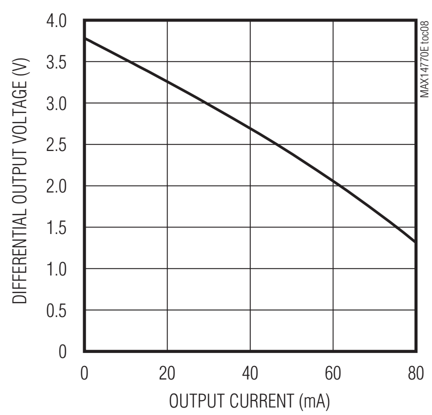
RECEIVER PROPAGATION DELAY vs. TEMPERATURE



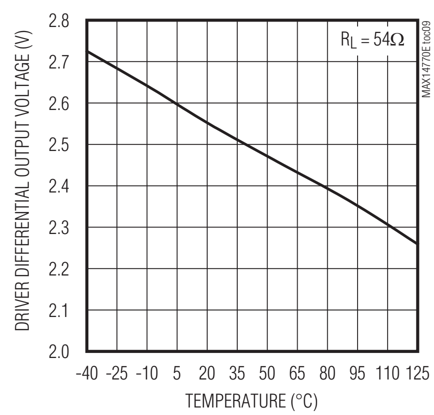
DRIVER PROPAGATION DELAY vs. TEMPERATURE



DIFFERENTIAL OUTPUT VOLTAGE V_{OD} vs. OUTPUT CURRENT



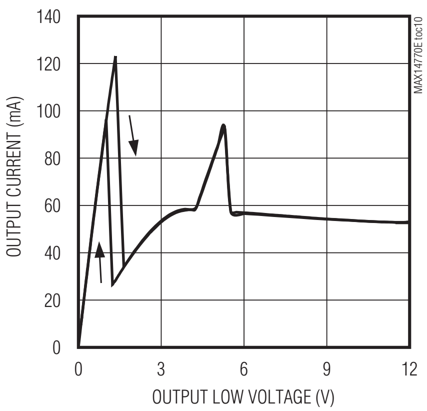
DIFFERENTIAL OUTPUT VOLTAGE V_{OD} vs. TEMPERATURE



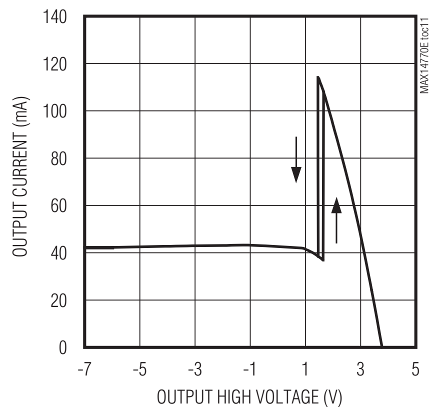
Typical Operating Characteristics (continued)

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

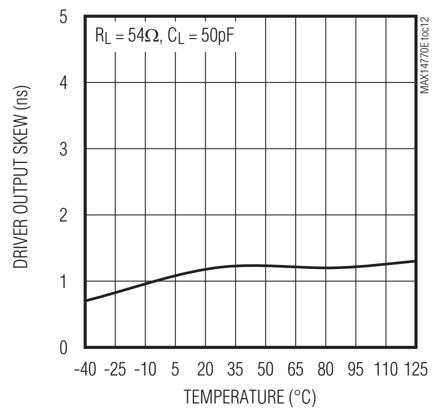
DRIVER OUTPUT CURRENT vs. OUTPUT LOW VOLTAGE



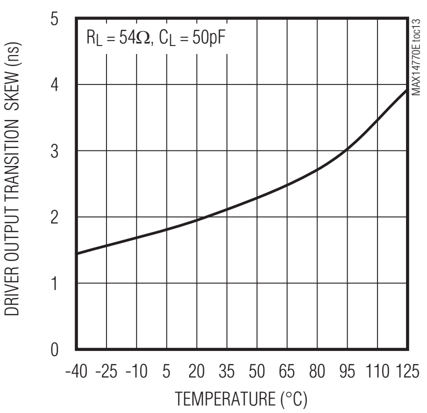
DRIVER OUTPUT CURRENT vs. OUTPUT HIGH VOLTAGE



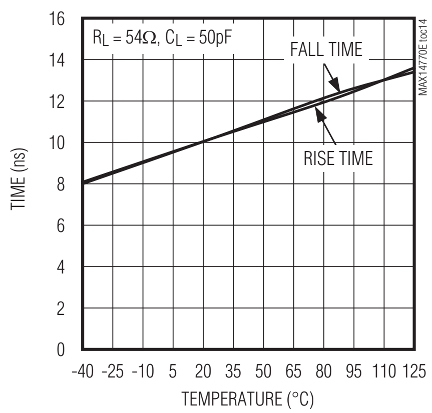
DRIVER DIFFERENTIAL SKEW t_{DSKEW} vs. TEMPERATURE



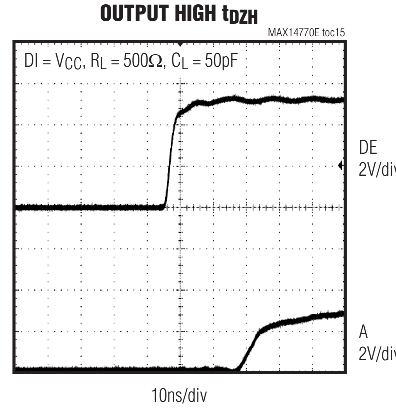
DRIVER OUTPUT TRANSITION SKEW vs. TEMPERATURE



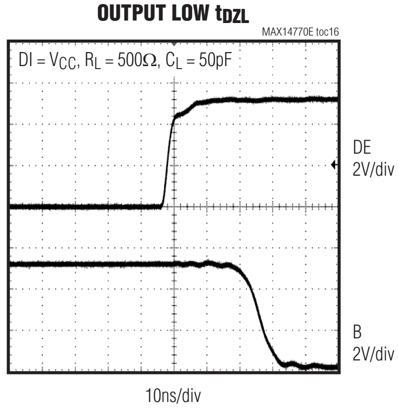
DRIVER OUTPUT RISE AND FALL TIME vs. TEMPERATURE



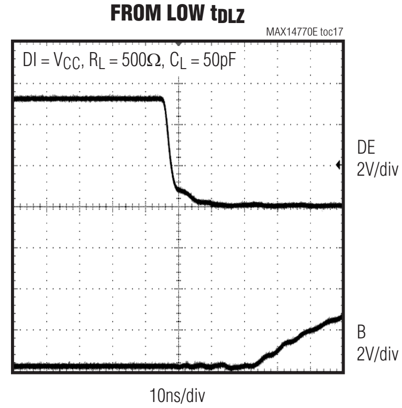
DRIVER ENABLE TO OUTPUT HIGH t_{DZH}



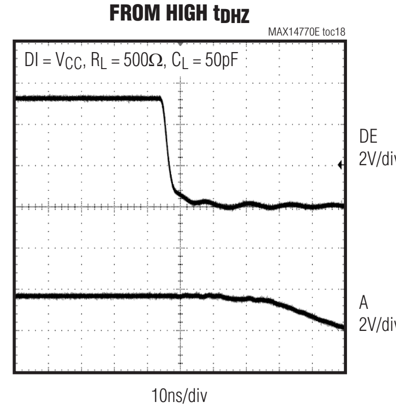
DRIVER ENABLE TO OUTPUT LOW t_{DZL}



DRIVER DISABLE TIME FROM LOW t_{DLZ}



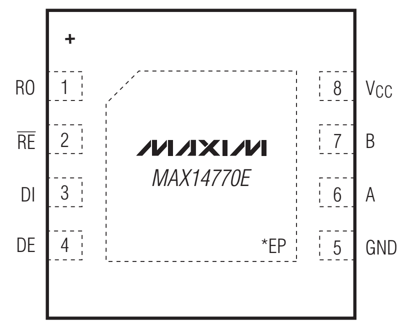
DRIVER DISABLE TIME FROM HIGH t_{DHZ}



Pin Configurations

TOP VIEW

SO



TDFN
(3mm × 3mm)

*CONNECT EXPOSED PAD TO GND.

Pin Description

PIN	NAME	FUNCTION
1	RO	Receiver Output. When $\overline{RE}$ is low and (A - B) ≥ -50mV, RO is high; if (A - B) ≤ -200mV, RO is low.
2	$\overline{RE}$	Receiver Enable. Drive $\overline{RE}$ low to enable RO; RO is high impedance when $\overline{RE}$ is high. Drive $\overline{RE}$ high and DE low to enter low-power shutdown mode.
3	DE	Driver Enable. Drive DE high to enable driver output. The driver outputs are high impedance when DE is low. Drive $\overline{RE}$ high and DE low to enter low-power shutdown mode.
4	DI	Driver Input. With DE high, a low on DI forces the noninverting output, A, low and the inverting output, B, high. Similarly, a high on DI forces the noninverting output, A, high and the inverting output, B, low.
5	GND	Ground
6	A	Noninverting Receiver Input and Noninverting Driver Output
7	B	Inverting Receiver Input and Inverting Driver Output
8	V_{CC}	Positive Supply. Bypass V_{CC} to GND with a 0.1µF ceramic capacitor as close as possible to the device.
—	EP	Exposed Pad (TDFN Only). Connect EP to GND.

High-ESD Profibus RS-485 Transceiver

Detailed Description

The MAX14770E is a half-duplex, ±35kV high ESD-protected transceiver for Profibus-DP, RS-485, and RS-422 communications. The device features true fail-safe circuitry that guarantees a logic-high receiver output when the receiver inputs are open or shorted, or when they are connected to a terminated transmission line with all drivers disabled (see the *True Fail-Safe* section). The MAX14770E supports data rates up to 20Mbps.

The MAX14770E operates from a single +4.5V to +5.5V supply. Drivers are output short-circuit current limited. Thermal-shutdown circuitry protects drivers against excessive power dissipation. When activated, the thermal-shutdown circuitry places the driver outputs into a high-impedance state. The MAX14770E has a hot-swap input structure that prevents disturbances on the differential signal lines when the MAX14770E is powered up (see the *Hot-Swap Capability* section).

True Fail-Safe

The MAX14770E guarantees a logic-high receiver output when the receiver inputs are shorted or open, or when they are connected to a terminated transmission line with all drivers disabled. This is done by having the receiver threshold between -50mV and -200mV. If the differential receiver input voltage (A - B) is greater than or equal to -50mV, RO is logic-high. If (A - B) is less than or equal to -200mV, RO is logic-low. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to 0V by the termination. With the receiver thresholds of the MAX14770E, this results in a logic-high with a 50mV minimum noise margin. The -50mV to -200mV threshold complies with the ±200mV EIA/TIA-485 standard.

Table 1. Functional Table (Transmitting)

TRANSMITTING				
INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	High-Z and shutdown	

X = Don't care.

Table 2. Functional Table (Receiving)

RECEIVING			
INPUTS			OUTPUT
$\overline{RE}$	DE	A-B	RO
0	X	≥ -0.05V	1
0	X	≤ -0.2V	0
0	X	Open/shorted	1
1	1	X	High-Z
1	0	X	High-Z and shutdown

X = Don't care.

Hot-Swap Capability

Hot-Swap Inputs

When circuit boards are inserted into a hot or powered backplane, disturbances to the enable inputs and differential receiver inputs can lead to data errors. Upon initial circuit board insertion, the processor undergoes its power-up sequence. During this period, the processor output drivers are high impedance and are unable to drive the DE and $\overline{RE}$ inputs of the MAX14770E to a defined logic level. Leakage currents up to 10µA from the high-impedance output of a controller could cause DE and $\overline{RE}$ to drift to an incorrect logic state. Additionally, parasitic circuit board capacitance could cause coupling of V_{CC} or GND to DE and $\overline{RE}$. These factors could improperly enable the driver or receiver. However, the MAX14770E has hot-swap inputs that avoid these potential problems.

When V_{CC} rises, an internal pulldown circuit holds DE low and $\overline{RE}$ high. After the initial power-up sequence, the pulldown circuit becomes transparent, resetting the hot-swap-tolerable inputs.

Hot-Swap Input Circuitry

The MAX14770E DE and $\overline{RE}$ enable inputs feature hot-swap capability. At the input, there are two NMOS devices, M1 and M2 (Figure 11). When V_{CC} ramps from 0, an internal 15µs timer turns on M2 and sets the SR latch that also turns on M1. Transistors M2, a 1mA current sink, and M1, a 100µA current sink, pull DE to GND through a 5.6kΩ resistor. M2 is designed to pull DE to the disabled state against an external parasitic capacitance up to 100pF that can drive DE high. After 15µs, the timer deactivates M2 while M1 remains on, holding DE low against three-state leakages that can drive DE high. M1 remains on until an external source overcomes the required input current. At this time, the SR latch resets and M1 turns off. When M1 turns off, DE reverts to a standard, high-impedance CMOS input. Whenever V_{CC} drops below 1V, the hot-swap input is reset.

For $\overline{RE}$, there is a complementary circuit employing two PMOS devices pulling $\overline{RE}$ to V_{CC}.

Thermal-Shutdown Protection

The MAX14770E features thermal-shutdown circuitry. The internal switch turns off when the junction temperature exceeds +160°C (typ) and immediately goes into a fault mode. The device exits thermal shutdown after the junction temperature cools by 15°C (typ).

Applications Information

128 Transceivers on the Bus

The standard RS-485 receiver input impedance is one unit load, and a standard driver can drive up to 32 unit loads. The MAX14770E transceiver has a 1/4 unit load receiver, which allows up to 128 transceivers connected in parallel on one communication line. Connect any combination of these devices, and/or other RS-485 devices, for a maximum of 32 unit loads to the line.

Low-Power Shutdown Mode

Low-power shutdown mode is initiated by bringing both $\overline{RE}$ high and DE low. In shutdown, the devices draw only 15µA (max) of supply current. $\overline{RE}$ and DE can be driven simultaneously; the devices are guaranteed not to enter shutdown if $\overline{RE}$ is high and DE is low for less than 50ns. If the inputs are in this state for at least 800ns, the devices are guaranteed to enter shutdown.

Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. The first, a foldback current limit on the output stage, provides immediate protection against short circuits over the whole common-mode voltage range (see the *Typical Operating Characteristics*). The second, a thermal-shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature exceeds +160°C (typ).

Typical Application

The MAX14770E transceivers are designed for bidirectional data communications on multipoint bus transmission lines. Figure 12 shows a typical network applications circuit. To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible.

Profibus Termination

The MAX14770E is designed for driving Profibus-DP termination networks. With a worst-case loading of two termination networks with 220Ω termination impedance and 390Ω pullups/pulldowns, the drivers can drive $V_{(A - B)}$ > 2.1V output.

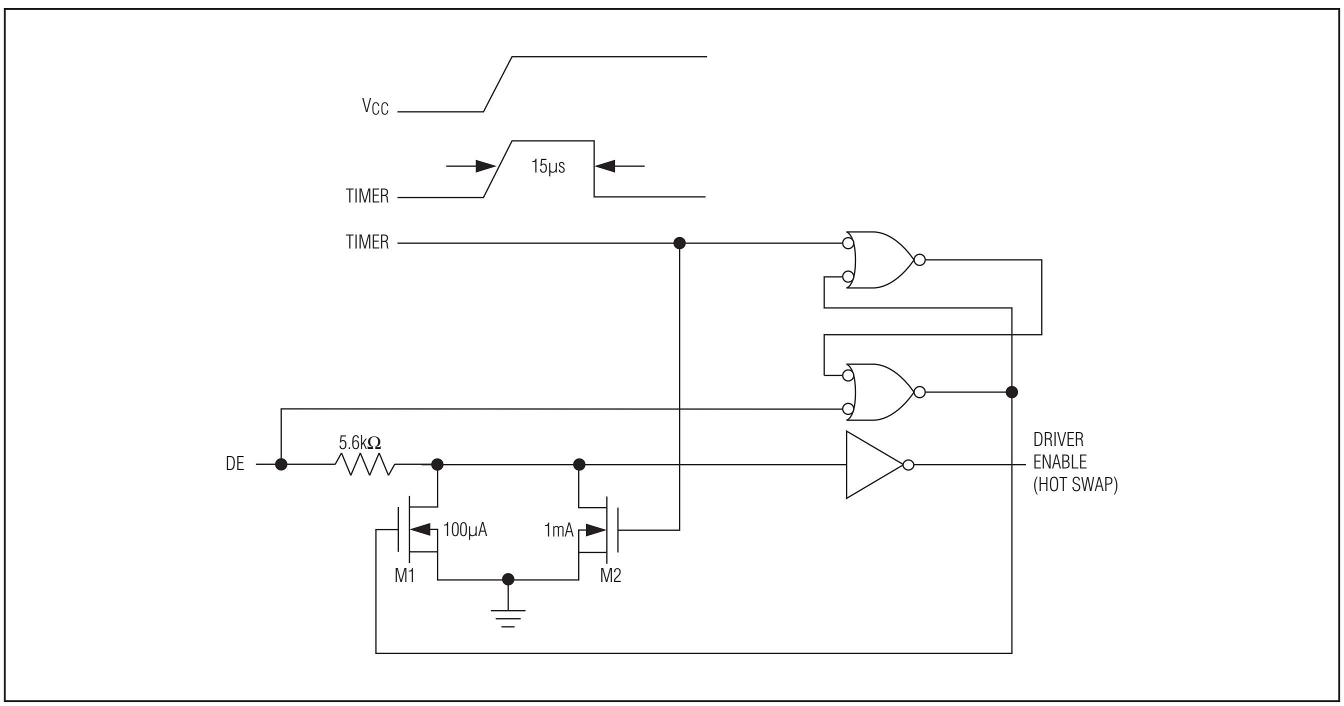


Figure 11. Simplified Structure of the Driver Enable Pin (DE)

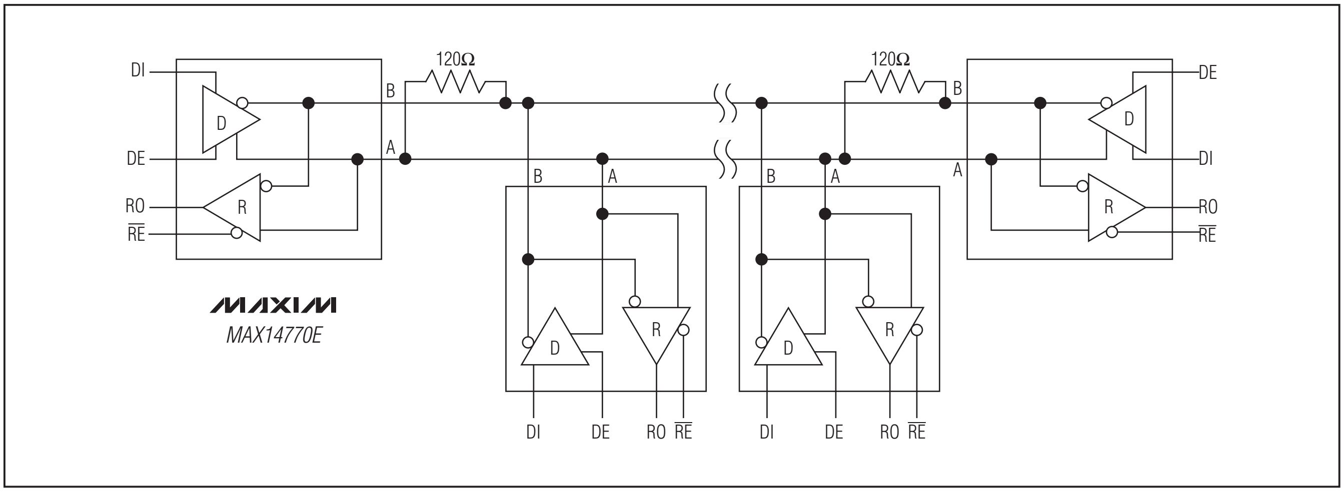


Figure 12. Typical Half-Duplex RS-485 Network

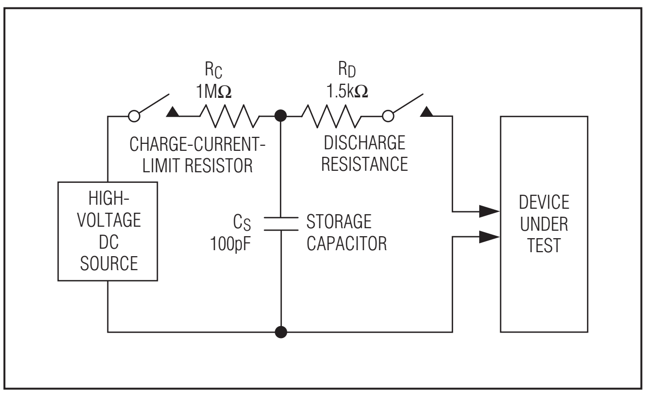


Figure 13. Human Body ESD Test Model

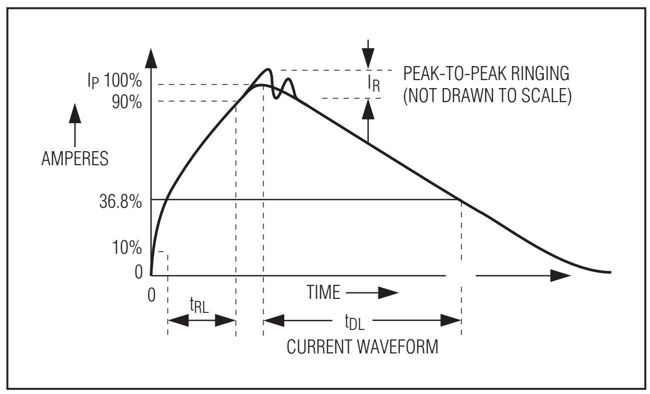


Figure 14. Human Body Current Waveform

Extended ESD Protection

ESD protection structures are incorporated on all pins to protect against electrostatic discharges up to ±2kV (HBM) encountered during handling and assembly. A and B are further protected against high ESD up to ±35kV (HBM) without damage. The A and B pins are also protected against ±20kV Air-Gap and ±10kV Contact IEC61000-4-2 ESD events. The ESD structures withstand high ESD both in normal operation and when the device is powered down. After an ESD event, the MAX14770E continues to function without latchup.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 13 shows the HBM. Figure 14 shows the current waveform it generates when discharged into a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. It does not specifically refer to integrated circuits. The MAX14770E is specified for ±20kV Air-Gap Discharge and ±10kV Contact Discharge IEC 61000-4-2 on the A and B pins.

The main difference between tests done using the HBM and IEC 61000-4-2 is higher peak current in IEC 61000-4-2. Because series resistance is lower in the IEC 61000-4-2

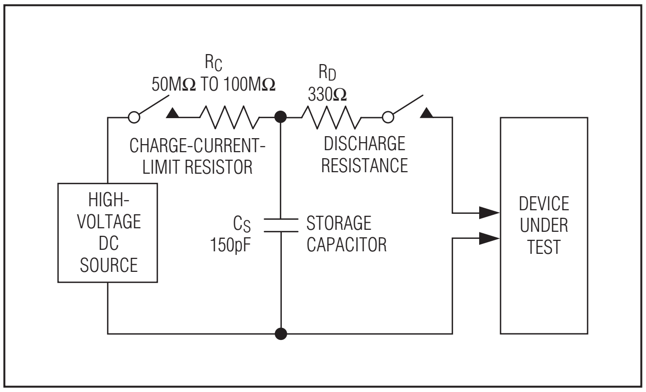


Figure 15. IEC61000-4-2 ESD Test Model

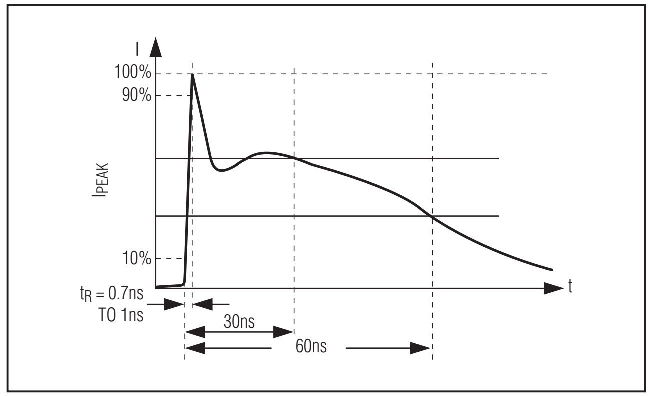
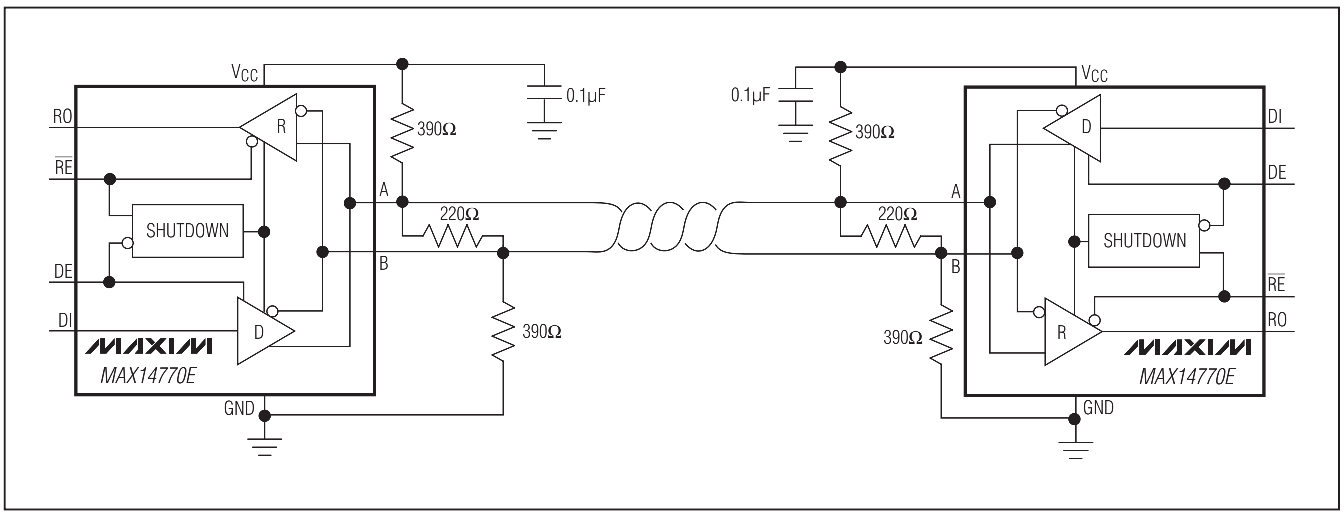


Figure 16. IEC61000-4-2 ESD Generator Current Waveform

Typical Profibus-DP Operating Circuit



ESD test model (Figure 15), the ESD-withstand voltage measured to this standard is generally lower than that measured using the HBM. Figure 16 shows the current waveform for the ±10kV IEC 61000-4-2 Level 4 ESD Contact Discharge test. The Air-Gap Discharge test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+," "#," or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 SO	S8+4	**21-0041**
8 TDFN-EP	T833+2	**21-0137**