BlueCore™3-ROM CSP

Single Chip Bluetooth® v1.2 System

Production Information Data Sheet for

BC313141A (UART) and BC313143A (USB)

November 2006

Device Features

- Fully Qualified Bluetooth System
- Bluetooth v1.1 and v1.2 Specification Compliant
- 1.8V core, 1.8 to 3.6V I/O
- Ultra Low Power Consumption
- Excellent Compatibility with Cellular Telephones
- Minimum External Components
- Integrated 1.8V Regulator
- Dual UART Ports (BC313141A only)
- Available in UART and USB Versions
- Built-In Self-Test Reduces Production Test Times
- RoHS Compliant

General Description

BlueCore3-ROM CSP is a single chip radio and baseband chip for Bluetooth wireless technology 2.4GHz systems. It is implemented in 0.18µm CMOS technology.

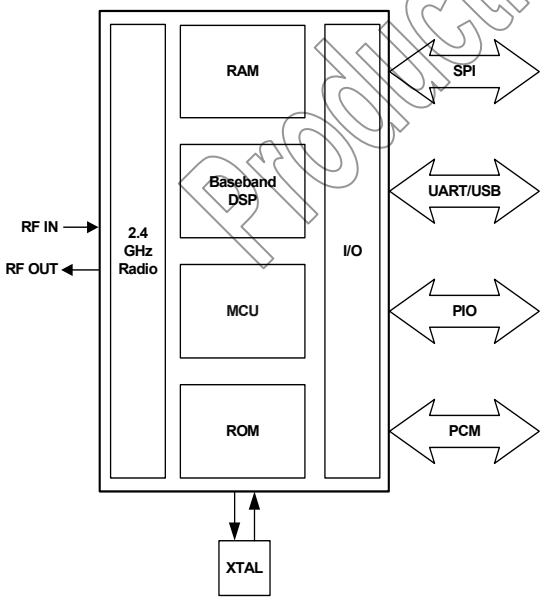
The 4Mbit ROM is metal programmable, which enables an eight week turn-around from approval of firmware to production samples.

Applications

- Cellular Handsets
- Personal Digital Assistants
- Digital cameras and other high volume consumer products
- Space critical applications

BlueCore3-ROM CSP has been designed to reduce the number of external components required, which ensures production costs are minimised.

The device incorporates auto-calibration and built-in self-test (BIST) routines to simplify development, type approval and production test. All hardware and device firmware is fully compliant with the Bluetooth specification v1.2.



BlueCore3-ROM CSP System Architecture

BlueCore™3-ROM CSP Product Data Sheet

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Status Information

The status of this Data Sheet is **Production Information.**

CSR Product Data Sheets progress according to the following format:

Advance Information

Information for designers concerning CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

Pre-Production Information

Pinout and mechanical dimension specifications finalised. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All electrical specifications may be changed by CSR without notice.

Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications. Production Data Sheets supersede all previous document versions.

RoHS Compliance

BlueCore3-ROM devices meet the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS).

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While every care has been taken to ensure the accuracy of the contents of this document, CSR cannot accept responsibility for any errors.

CSR's products are not authorised for use in life-support or safety-critical applications.

1 Key Features

Radio

- Common TX/RX terminals simplifies external matching; eliminates external antenna switch
- BIST minimises production test time. No external trimming is required in production
- Full RF reference designs are available
- Bluetooth v1.2 specification compliant

Transmitter

- +6dBm RF transmit power with level control from on-chip 6-bit DAC over a dynamic range >30dB
- Class 2 and Class 3 support without the need for an external power amplifier or TX/RX switch

Receiver

- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real time digitised RSSI available on HCI interface
- Fast AGC for enhanced dynamic range

Synthesiser

- Fully integrated synthesizer requires no external VCO varactor diode, resonator or loop filter
- Compatible with crystals between 8 and 40MHz (in multiples of 250kHz) or an external clock
- Accepts 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz TCXO frequencies for GSM and CDMA devices with either sinusoidal or logic level signals

Auxiliary Features

- Crystal oscillator with built-in digital trimming
- Power management includes digital shut down and wake up commands with an integrated low power oscillator for ultra-low Park/Sniff/Hold mode
- 'Clock request' output to control an external clock source
- Device can run in low power modes from an external 32KHz clock signal Auto Baud Rate setting for different TCXO frequencies
- Auto Baud Rate setting for different TCXO frequencies
- On-chip low dropout linear regulator, producing 1.8V output from 2.2-4.2V input
- Power-on-reset cell detects low supply voltage
- Arbitrary sequencing of power supplies is permitted

Baseband and Software

- Internal programmed 4Mbit ROM for complete system solution
- 32kbyte on-chip RAM allows full speed Bluetooth data transfer, mixed voice and data, plus full seven slave Piconet operation
- Dedicated logic for forward error correction, header error control, access code correlation, demodulation, cyclic redundancy check, encryption bit stream generation, whitening and transmit pulse shaping. Supports all Bluetooth 1.2 features including eSCO
- Transcoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air

Physical Interfaces

- Synchronous serial interface up to 4M Baud for system debugging
- UART interface with programmable Baud rate up to 1.5M Baud with an optional bypass mode (BC313141A only)
- Full speed USB interface supports OHCI and UHCI host interfaces. Compliant with USB v2.0 (BC3131143A only)
- Synchronous bi-directional serial programmable audio interface

Bluetooth Stack Running on an Internal Microcontroller

CSR's Bluetooth protocol stack runs on-chip in a variety of configurations:

- Standard HCI (UART or USB)
- Fully embedded to RFCOMM
- Customer specific builds with embedded application code

Package Options

- 42-ball CSP 3.8 x 3.4 x 0.7mm 0.5mm pitch

2 CSP Package Information

2.1 BC313141AXX-IXF and BC313143AXX-IXF Pinout Diagram

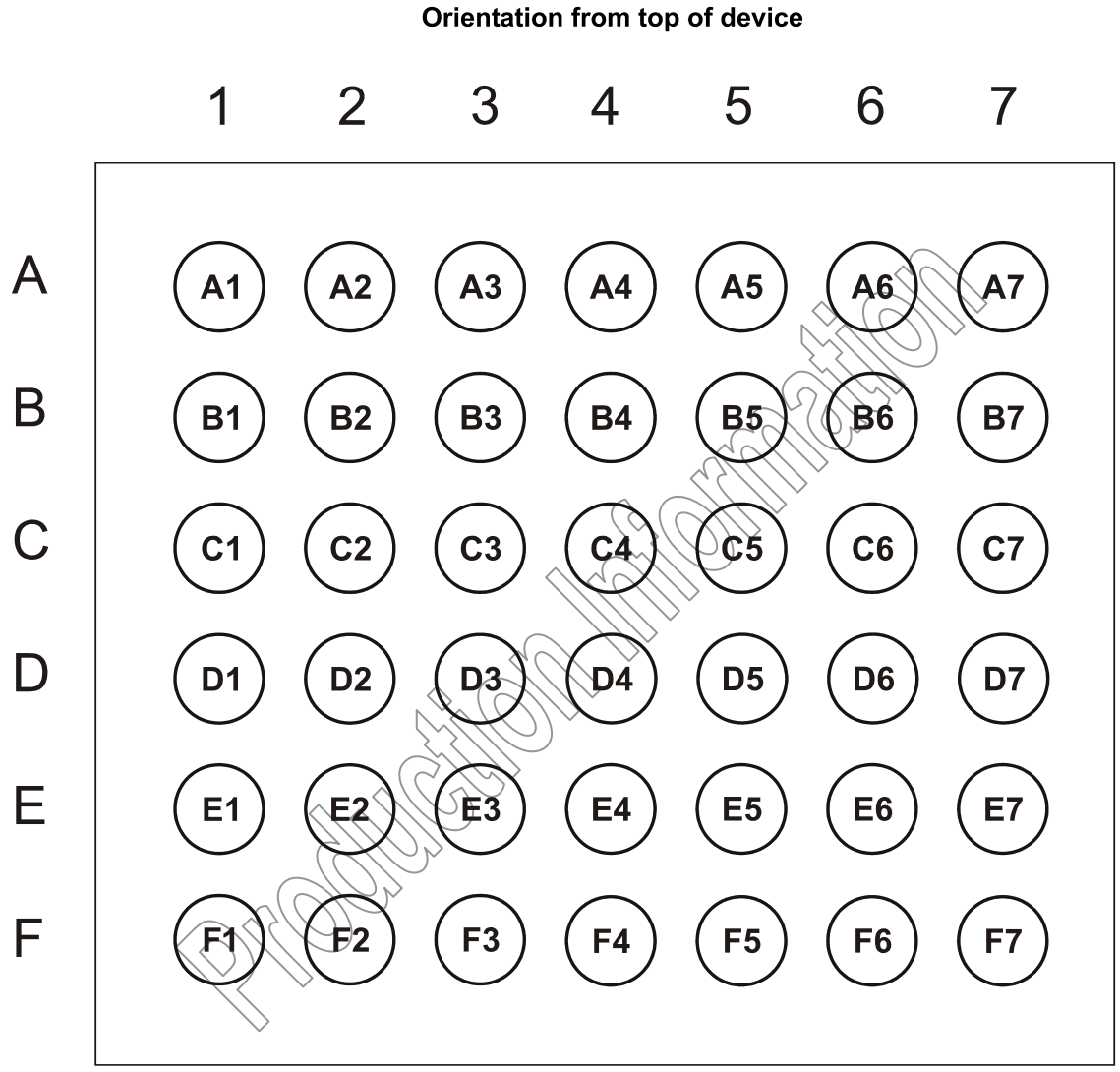

Figure 2.1: BlueCore3-ROM CSP Package (BC313141AXX-IXF and BC313143AXX-IXF)

2.2 BC313141AXX-IXF Device Terminal Functions

Radio	Ball	Pad Type	Description
TX_A	D1	Analogue	Transmitter output/Switched Receiver input
TX_B	E1	Analogue	Complement of TX_A

Synthesiser and Oscillator	Ball	Pad Type	Description
XTAL_IN	A1	Analogue	For crystal or external clock input
XTAL_OUT	A3	Analogue	Drive for crystal

PCM Interface	Ball	Pad Type	Description
PCM_OUT	D5	CMOS output, tri-state with weak internal pull-down	Synchronous data output
PCM_IN	B7	CMOS input, with weak internal pull-down	Synchronous data input
PCM_SYNC	C5	Bi-directional with weak internal pull-down	Synchronous data sync
PCM_CLK	B6	Bi-directional with weak internal pull-down	Synchronous data clock

UART	Ball	Pad Type	Description
UART_TX	D4	CMOS output, tri-state with weak internal pull-up	UART data output active high
UART_RX	B5	CMOS input with weak internal pull-down	UART data input active high
UART_RTS	A7	CMOS output, tri-state with weak internal pull-up	UART request to send active low
UART_CTS	C4	CMOS input with weak internal pull-down	UART clear to send active low

Test and Debug	Ball	Pad Type	Description
RESETB	E6	CMOS input with weak internal pull-up	Reset if low. Input debounced so must be low for >5ms to cause a reset
SPI_CSB	F6	CMOS input with weak internal pull-up	Chip select for Synchronous Serial Interface active low
SPI_CLK	F5	CMOS input with weak internal pull-down	Serial Peripheral Interface clock
SPI_MOSI	F4	CMOS input with weak internal pull-down	Serial Peripheral Interface data input
SPI_MISO	F7	CMOS output, tri-state with weak internal pull-down	Serial Peripheral Interface data output
TEST_EN	F3	CMOS input with strong internal pull-down	For test purposes only (leave unconnected)

PIO Port	Ball	Pad Type	Description
PIO[0]	D3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[1]	C3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[2]	E3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[3]	F2	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[4]	E5	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[5]	E4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[6]	D7	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[7]	D6	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
AIO[0]	C2	Bi-directional	Programmable input/output line
AIO[2]	A5	Bi-directional	Programmable input/output line

Power Supplies and Control	Ball	Pad Type	Description
VREG_IN	A2	Regulator input	Regulator input
VDD_USB	B4	VDD	Positive supply for UART ports
VDD_PIO	F1	VDD	Positive supply for PIO [3:0]
VDD_PADS	E7	VDD	Positive supply for all other digital input/output ports
VDD_CORE	C6	VDD	Positive supply for internal digital circuitry
VDD_VCO	B1	VDD	Positive supply for VCO and synthesiser circuitry
VDD_RADIO	C1	VDD	Positive supply for RF circuitry
VDD_ANA	A4	VDD/Regulator output	Positive supply for analogue circuitry and 1.8V regulated output
VSS_DIG	C7	VSS	Ground connection for internal digital circuitry and digital ports
VSS_PIO	E2	VSS	Ground connection for digital ports
VSS_PADS	A6	VSS	Ground connection for digital ports
VSS_VCO	B2	VSS	Ground connections for VCO and synthesiser
VSS_RADIO	D2	VSS	Ground connections for RF circuitry
VSS_ANA	B3	VSS	Ground connections for analogue circuitry

2.3 BC313143AXX-IXF Device Terminal Functions

Radio	Ball	Pad Type	Description
TX_A	D1	Analogue	Transmitter output/Switched Receiver input
TX_B	E1	Analogue	Complement of TX_A

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XTAL_IN	A1	Analogue	For crystal or external clock input
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PCM Interface	Ball	Pad Type	Description
PCM_OUT	D5	CMOS output, tri-state with weak internal pull-down	Synchronous data output
PCM_IN	B7	CMOS input, with weak internal pull-down	Synchronous data input
PCM_SYNC	C5	Bi-directional with weak internal pull-down	Synchronous data sync
PCM_CLK	B6	Bi-directional with weak internal pull-down	Synchronous data clock

UART and USB	Ball	Pad Type	Description
UART_TX	D4	CMOS output, tri-state with weak internal pull-up	UART data output active high
UART_RX	B5	CMOS input with weak internal pull-down	UART data input active high
USB_DP	C4	Bi-directional	USB data plus with selectable internal 1.5kΩ pull-up resistor
USB_DN	A7	Bi-directional	USB data minus

Test and Debug	Ball	Pad Type	Description
RESETB	E6	CMOS input with weak internal pull-up	Reset if low. Input debounced so must be low for >5ms to cause a reset
SPI_CSB	F6	CMOS input with weak internal pull-up	Chip select for Synchronous Serial Interface active low
SPI_CLK	F5	CMOS input with weak internal pull-down	Serial Peripheral Interface clock
SPI_MOSI	F4	CMOS input with weak internal pull-down	Serial Peripheral Interface data input
SPI_MISO	F7	CMOS output, tri-state with weak internal pull-down	Serial Peripheral Interface data output
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PIO[2]	E3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[3]	F2	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[4]	E5	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[5]	E4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[6]	D7	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[7]	D6	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
AIO[0]	C2	Bi-directional	Programmable input/output line
AIO[2]	A5	Bi-directional	Programmable input/output line

Power Supplies and Control	Ball	Pad Type	Description
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VDD_PIO	F1	VDD	Positive supply for PIO [3:0]
VDD_PADS	E7	VDD	Positive supply for all other digital input/output ports
VDD_CORE	C6	VDD	Positive supply for internal digital circuitry
VDD_VCO	B1	VDD	Positive supply for VCO and synthesiser circuitry
VDD_RADIO	C1	VDD	Positive supply for RF circuitry
VDD_ANA	A4	VDD/Regulator output	Positive supply for analogue circuitry and 1.8V regulated output
VSS_DIG	C7	VSS	Ground connection for internal digital circuitry and digital ports
VSS_PIO	E2	VSS	Ground connection for digital ports
VSS_PADS	A6	VSS	Ground connection for digital ports
VSS_VCO	B2	VSS	Ground connections for VCO and synthesiser
VSS_RADIO	D2	VSS	Ground connections for RF circuitry
VSS_ANA	B3	VSS	Ground connections for analogue circuitry

3 Electrical Characteristics

Absolute Maximum Ratings		
Rating	**Minimum**	**Maximum**
Storage Temperature	-40°C	150°C
Supply Voltage: VDD_RADIO, VDD_VCO, VDD_ANA, and VDD_CORE	-0.40V	2.20V
Supply Voltage: VDD_PADS, VDD_PIO, VDD_USB	-0.40V	3.70V
Supply Voltage: VREG_IN	-0.40V	5.60V
Other Terminal Voltages	VSS-0.4V	VDD+0.4V

Recommended Operating Conditions		
Operating Condition	**Minimum**	**Maximum**
Operating Temperature Range	-40°C	105°C
Guaranteed RF performance range	-40°C	105°C
Supply Voltage: VDD_RADIO, VDD_VCO, VDD_ANA, and VDD_CORE	1.70V	1.90V
Supply Voltage: VDD_PADS, VDD_PIO, VDD_USB	1.70V	3.60V
Supply Voltage: VREG_IN	2.20V	4.20V(1)

Note:

(1) The device will operate without damage with VREG_IN as high as 5.6V, however the RF performance is not guaranteed above 4.20V.

Input/Output Terminal Characteristics					
Linear Regulator		**Minimum**	**Typical**	**Maximum**	**Unit**
Normal Operation					
Output Voltage (I_{load} = 70mA / Vreg_IN = 3.0V)		1.70	1.78	1.85	V
Temperature Coefficient		-250	-	250	ppm/C
Output Noise(1)(2)		-	-	1	mV rms
Load Regulation (I_{load} < 100 mA)		-	-	50	mV/A
Settling Time(1)(3)		-	-	50	µs
Output current:	Maximum output current	70	-	-	mA
	Minimum load current	5	-	-	µA
Input Voltage		-	-	4.2(6)	V
Dropout Voltage (I_{load} = 70 mA)		-	-	350	mV
Quiescent Current (excluding load, I_{load} < 1mA)		25	35	50	µA
Low Power Mode(4)					
Quiescent Current (excluding load, I_{load} < 100µA)		4	7	10	µA
Disabled Mode(5)					
Quiescent Current		1.5	2.5	3.5	µA

Notes:

(1) Regulator output connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors

(2) Frequency range 100Hz to 100kHz

(3) 1mA to 70mA pulsed load

(4) Low power mode is entered and exited automatically when the chip enters/leaves Deep Sleep mode

(5) Regulator is disabled when VREG_EN is pulled low. It is also disabled when VREG_IN is either open circuit or driven to the same voltage as VDD_ANA

(6) Operation up to 5.6V is permissible without damage and without the output voltage rising sufficiently to damage the rest of BlueCore3, but output regulation and other specifications are no longer guaranteed at input voltages in excess of 4.2V.

Input/Output Terminal Characteristics (Continued)					
Digital Terminals		**Minimum**	**Typical**	**Maximum**	**Unit**
Input Voltage Levels					
V_{IL} input logic level low	VDD=3.0V	-0.4	-	0.8	V
	VDD=1.8V	-0.4	-	0.4	V
V_{IH} input logic level high		0.7VDD	-	VDD+0.4	V
Output Voltage Levels					
V_{OL} output logic level low, (I_O = 4.0mA), VDD=3.0V		-	-	0.2	V
V_{OL} output logic level low, (I_O = 4.0mA), VDD=1.8V		-	-	0.4	V
V_{OH} output logic level high, (I_O = -4.0mA), VDD=3.0V		VDD-0.2	-	-	V
V_{OH} output logic level high, (I_O = -4.0mA), VDD=1.8V		VDD-0.4	-	-	V
Input and Tri-State Current with:					
Strong pull-up		-100	-20	-10	µA
Strong pull-down		10	20	100	µA
Weak pull-up		-5	-1	-0.5	µA
Weak pull-down		0.5	1	5	µA
I/O pad leakage current		-1	0	1	µA
C_I Input Capacitance		1.0	-	5.0	pF

USB Terminals	**Minimum**	**Typical**	**Maximum**	**Unit**
Input threshold				
V_{IL} input logic level low	-	-	0.3VDD_USB	V
V_{IH} input logic level high	0.57VDD_USB	-	-	V
Input leakage current				
VSS_USB< V_{IN}< VDD_USB [1]	-1	-	1	µA
C_I Input capacitance	2.5	-	10.0	pF
Output Voltage levels				
To correctly terminated USB Cable				
V_{OL} output logic level low	0.0	-	0.2	V
V_{OH} output logic level high	2.8	-	VDD_USB	V

Crystal Oscillator	Minimum	Typical	Maximum	Unit
Crystal frequency [2]	8.0	-	40.0	MHz
Digital trim range [3]	5.0	6.2	8.0	pF
Trim step size [3]	-	0.1	-	pF
Transconductance	2.0	-	-	mS
Negative resistance[4]	870	1500	2400	Ω
External Clock				
Input frequency[5]	8.0	-	40.0	MHz
Clock input level[6]	0.4	-	VDD_ANA	V pk-pk
Allowable jitter	-	-	15	ps rms
XTAL_IN input impedance	-	≥10	-	kΩ
XTAL_IN input capacitance	-	□4	-	pF
Power-on reset				
VDD_CORE falling threshold	1.40	1.50	1.60	V
VDD_CORE rising threshold	1.50	1.60	1.70	V
Hysteresis	0.05	0.10	0.15	V

Notes:

VDD_CORE, VDD_RADIO, VDD_VCO and VDD_ANA are at 1.8V unless shown otherwise

VDD_PADS, VDD_PIO and VDD_USB are at 3.0V unless shown otherwise

The same setting of the digital trim is applied to both XTAL_IN and XTAL_OUT

Current drawn into a pin is defined as positive; current supplied out of a pin is defined as negative

(1) Internal USB pull-up disabled

(2) Integer multiple of 250kHz

(3) The difference between the internal capacitance at minimum and maximum settings of the internal digital trim

(4) XTAL frequency = 16MHz; XTAL C0 = 0.75pF; XTAL load capacitance = 8.5pF

(5) Clock input can be any frequency between 8 and 40MHz in steps of 250kHz + CDMA/3G TCXO frequencies of 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz

(6) Clock input can either be sinusoidal or square wave if the peaks of the signal are below VSS_ANA or above VDD_ANA a DC blocking capacitor is required between the signal and XTAL_IN

4 Radio Characteristics

BlueCore3-ROM CSP meets the Bluetooth specification v1.2 when used in a suitable application circuit between -40°C and +105°C. Tx output is guaranteed to be unconditionally stable over the guaranteed temperature range.

4.1 Temperature +20°C

4.1.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +20°C					
	Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power(1)(2)	-	5.0	-	-6 to +4(3)	dBm
Variation in RF power over temperature range with compensation enabled (±)(4)	-	1.0	-	-	dB
Variation in RF power over temperature range with compensation disabled (±)(4)	-	2	-	-	dB
RF power control range	-	35	-	≥16	dB
RF power range control resolution (5)	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	780	-	≤1000	kHz
Adjacent channel transmit power F=F_0 ±2MHz(6)(7)	-	-35	-	≤-20	dBm
Adjacent channel transmit power F=F_0 ±3MHz(6)(7)	-	-45	-	≤-40	dBm
Adjacent channel transmit power F=F_0>±3MHz(6)(7)	-	-55	-	≤-40	dBm
Δf1avg “Maximum Modulation”	-	165	-	140<$\Delta f1_{avg}$<175	kHz
Δf2max “Minimum Modulation”	-	140	-	≥115	kHz
Δf2avg / Δf1avg	-	0.91	-	≥0.80	-
Initial carrier frequency tolerance	-	6	-	±75	kHz
Drift Rate	-	8	-	≤20	kHz/50μs
Drift (single slot packet)	-	8	-	≤25	kHz
Drift (five slot packet)	-	9	-	≤40	kHz
2nd Harmonic content	-	-40	-	≤30	dBm
3rd Harmonic content	-	-50	-	≤30	dBm

Note

(1) BlueCore3-ROM CSP firmware maintains the transmit power to be within the Bluetooth specification v1.2 limits.

(2) Measurement made using a PSKEY_LC_MAX_TX_POWER setting corresponds to a PSKEY_LC_POWER_TABLE power table entry of 63.

(3) Class 2 RF transmit power range, Bluetooth specification v1.2.

(4) To some extent these parameters are dependent on the matching circuit used, and its behaviour over temperature. Therefore these parameters may be beyond CSR’s direct control.

(5) Resolution guaranteed over the range -5dB to -25dB relative to maximum power for Tx Level >20.

(6) Measured at F_0 = 2441MHz.

(7) Up to three exceptions are allowed in v1.2 of the Bluetooth specification. BlueCore3-ROM CSP is guaranteed to meet the ACP performance as specified by the Bluetooth specification v1.2.

Radio Characteristics VDD = 1.8V Temperature = +20°C (Continued)						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Cellular Band**	**Unit**
Emitted power in cellular bands measured at the unbalanced port of the balun. Output power ≤4dBm	0.869 – 0.894[1]	-	-135	-	GSM 850	dBm /Hz
	0.869 – 0.894[2]	-	-134	-	CDMA 850	
	0.925 – 0.960[1]	-	-137	-	GSM 900	
	1.570 – 1.580[3]	-	-140	-	GPS	
	1.805 – 1.880[1]	-	-141	-	GSM 1800 / DCS 1800	
	1.930 – 1.990[4]	-	-134	-	PCS 1900	
	1.930 – 1.990[1]	-	-136	-	GSM 1900	
	1.930 – 1.990[2]	-	-135	-	CDMA 1900	
	2.110 – 2.170[2]	-	-132	-	W-CDMA 2000	
	2.110 – 2.170[5]	-	-135	-	W-CDMA 2000	

Notes:

(1) Integrated in 200kHz bandwidth and then normalised to a 1Hz bandwidth.

(2) Integrated in 1.2MHz bandwidth and then normalised to a 1Hz bandwidth.

(3) Integrated in 1MHz bandwidth. and then normalised to a 1Hz bandwidth

(4) Integrated in 30kHz bandwidth and then normalised to a 1Hz bandwidth.

(5) Integrated in 5MHz bandwidth and then normalised to a 1Hz bandwidth.

4.1.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = +20°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER for all packet types	2.402	-	-82	-	≤-70	dBm
	2.441	-	-85	-		
	2.480	-	-83	-		
Maximum received signal at 0.1% BER		-	>10	-	≥-20	dBm
	Frequency (MHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Continuous power required to block Bluetooth reception (for sensitivity of -67dBm with 0.1% BER) measured at the unbalanced port of the balun.	30 – 2000	-	>0	-	-10	dBm
	2000 – 2400	-	>-10	-	-27	
	2500 – 3000	-	>-12	-	-27	
	3000 – 3300	-	>3	-	-10	
C/I co-channel		-	8	-	≤11	dB
Adjacent channel selectivity C/I $F=F_0+1MHz$ (1) (2)		-	-3	-	≤0	dB
Adjacent channel selectivity C/I $F=F_0-1MHz$ (1) (2)		-	-4	-	≤0	dB
Adjacent channel selectivity C/I $F=F_0+2MHz$ (1) (2)		-	-35	-	≤-30	dB
Adjacent channel selectivity C/I $F=F_0-2MHz$ (1) (2)		-	-21	-	≤-20	dB
Adjacent channel selectivity C/I $F\geq F_0+3MHz$ (1) (2)		-	-44	-	≤-40	dB
Adjacent channel selectivity C/I $F\leq F_0-5MHz$ (1) (2)		-	-43	-	≤-40	dB
Adjacent channel selectivity C/I $F=F_{Image}$ (1) (2)		-	-23	-	≤-9	dB
Maximum level of intermodulation interferers (3)		-	-34	-	≥-39	dBm
Spurious output level (4)		-	-160	-	-	dBm/Hz

Notes:

(1) Up to five exceptions are allowed in v1.2 of the Bluetooth specification. BlueCore3-ROM CSP is guaranteed to meet the C/I performance as specified by the Bluetooth specification v1.2.

(2) Measured at F_0 = 2441MHz

(3) Measured at f1-f2 = 5MHz. Measurement is performed in accordance with Bluetooth RF test RCV/CA/05/c. i.e. wanted signal at -64dBm

(4) Measured at the unbalanced port of the balun. Integrated in 100kHz bandwidth and then normalized to 1Hz. Actual figure is typically below -160dBm/Hz except for peaks of -57dBm at 1.6GHz, -48dBm inband at 2.4GHz and -60dBm at 3.2GHz

Radio Characteristics VDD = 1.8V Temperature = +20°C (Continued)						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Cellular Band**	**Unit**
Continuous power in cellular bands required to block Bluetooth reception (for sensitivity of -67dBm with 0.1% BER) measured at the unbalanced port of the balun.	0.824 – 0.849	-	>4[1]	-	GSM 850	dBm
	0.824 – 0.849	-	-8	-	CDMA	
	0.880 – 0.915	-	1	-	GSM 900	
	1.710 – 1.785	-	>4	-	GSM 1800 / DCS 1800	
	1.850 – 1.910	-	>4	-	GSM 1900 / PCS 1900	
	1.850 – 1.910	-	-8	-	CDMA 1900	
	1.920 – 1.980	-	-10	-	W-CDMA 2000	
Continuous power in cellular bands required to block Bluetooth reception (for sensitivity of -72dBm with 0.1% BER) measured at the unbalanced port of the balun.	0.824 – 0.849	-	>0	-	GSM 850	dBm
	0.824 – 0.849	-	-13	-	CDMA	
	0.880 – 0.915	-	0	-	GSM 900	
	1.710 – 1.785	-	>4	-	GSM 1800 / DCS 1800	
	1.850 – 1.910	-	>4	-	GSM 1900 / PCS 1900	
	1.850 – 1.910	-	-13	-	CDMA 1900	
	1.920 – 1.980	-	-16	-	W-CDMA 2000	

Note:

(1) 0dBm if $f_{BLOCKING}$ <0.831GHz

4.2 Temperature -40°C

4.2.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = -40°C					
	Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power(1)	-	5.5	-	-6 to +4(2)	dBm
RF power control range	-	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	780	-	≤1000	kHz
Adjacent channel transmit power $F=F_0 \pm 2MHz$(3) (4)	-	-35	-	≤-20	dBm
Adjacent channel transmit power $F=F_0 \pm 3MHz$(3) (4)	-	-41	-	≤-40	dBm
$\Delta f1avg$ "Maximum Modulation"	-	165	-	$140<\Delta f1_{avg}<175$	kHz
$\Delta f2max$ "Minimum Modulation"	-	135	-	115	kHz
$\Delta f2avg / \Delta f1avg$	-	0.85	-	≥0.80	-
Initial carrier frequency tolerance	-	10	-	±75	kHz
Drift Rate	-	8	-	≤20	kHz/50µs
Drift (single slot packet)	-	8	-	≤25	kHz
Drift (five slot packet)	-	10	-	≤40	kHz

Notes:

(1) BlueCore3-ROM CSP firmware maintains the transmit power to be within the Bluetooth specification v1.2 limits

(2) Class 2 RF transmit power range, Bluetooth specification v1.2

(3) Measured at F_0 = 2441MHz

(4) Up to three exceptions are allowed in v1.2 of the Bluetooth specification

4.2.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = -40°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER for all packet types	2.402	-	-82.5	-	≤-70	dBm
	2.441	-	-85.5	-		
	2.480	-	-84	-		
Maximum received signal at 0.1% BER		-	>10	-	≥-20	dBm

4.3 Temperature -25°C

4.3.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = -25°C					
	Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power(1)	-	5.5	-	-6 to +4(2)	dBm
RF power control range	-	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	780	-	≤1000	kHz
Adjacent channel transmit power $F=F_0 \pm 2MHz$(3) (4)	-	-35	-	≤-20	dBm
Adjacent channel transmit power $F=F_0 \pm 3MHz$(3) (4)	-	-45	-	≤-40	dBm
Δf1avg “Maximum Modulation”	-	165	-	$140<\Delta f1_{avg}<175$	kHz
Δf2max “Minimum Modulation”	-	135	-	115	kHz
Δf2avg / Δf1avg	-	0.87	-	≥0.80	-
Initial carrier frequency tolerance	-	8	-	±75	kHz
Drift Rate	-	8	-	≤20	kHz/50µs
Drift (single slot packet)	-	7	-	≤25	kHz
Drift (five slot packet)	-	8	-	≤40	kHz

Notes:

(1) BlueCore3-ROM CSP firmware maintains the transmit power to be within the Bluetooth specification v1.2 limits

(2) Class 2 RF transmit power range, Bluetooth specification v1.2

(3) Measured at F_0 = 2441MHz

(4) Up to three exceptions are allowed in v1.2 of the Bluetooth specification

4.3.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = -25°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER for all packet types	2.402	-	-82.5	-	≤-70	dBm
	2.441	-	-85.5	-		
	2.480	-	-83.5	-		
Maximum received signal at 0.1% BER		-	>10	-	≥-20	dBm

4.4 Temperature +85°C

4.4.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +85°C					
	Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power(1)	-	3	-	-6 to +4(2)	dBm
RF power control range	-	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	800	-	≤1000	kHz
Adjacent channel transmit power $F=F_0 \pm 2MHz$(3) (4)	-	-40	-	≤-20	dBm
Adjacent channel transmit power $F=F_0 \pm 3MHz$(3) (4)	-	-45	-	≤-40	dBm
Δf1avg “Maximum Modulation”	-	165	-	$140<\Delta f1_{avg}<175$	kHz
Δf2max “Minimum Modulation”	-	130	-	≥115	kHz
Δf2avg / Δf1avg	-	0.90	-	≥0.80	-
Initial carrier frequency tolerance	-	10	-	±75	kHz
Drift Rate	-	8	-	≤20	kHz/50µs
Drift (single slot packet)	-	11	-	≤25	kHz
Drift (five slot packet)	-	10	-	≤40	kHz

Notes:

(1) BlueCore3-ROM CSP firmware maintains the transmit power to be within the Bluetooth specification v1.2 limits

(2) Class 2 RF transmit power range, Bluetooth specification v1.2

(3) Measured at F_0 = 2441MHz

(4) Up to three exceptions are allowed in v1.2 of the Bluetooth specification

4.4.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = +85°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER for all packet types	2.402	-	-80.5	-	≤-70	dBm
	2.441	-	-82.5	-		
	2.480	-	-81.5	-		
Maximum received signal at 0.1% BER		-	>10	-	≥-20	dBm

4.5 Temperature +105°C

4.5.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +105°C					
	Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power(1)	-	1	-	-6 to +4(2)	dBm
RF power control range	-	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	820	-	≤1000	kHz
Adjacent channel transmit power $F=F_0 \pm 2MHz$(3) (4)	-	-40	-	≤-20	dBm
Adjacent channel transmit power $F=F_0 \pm 3MHz$(3) (4)	-	-45	-	≤-40	dBm
Δf1avg "Maximum Modulation"	-	165	-	$140<\Delta f1_{avg}<175$	kHz
Δf2max "Minimum Modulation"	-	130	-	115	kHz
Δf2avg / Δf1avg	-	0.87	-	≥0.80	-
Initial carrier frequency tolerance	-	15	-	±75	kHz
Drift Rate	-	9	-	≤20	kHz/50µs
Drift (single slot packet)	-	12	-	≤25	kHz
Drift (five slot packet)	-	12	-	≤40	kHz

Notes:

(1) BlueCore3-ROM CSP firmware maintains the transmit power to be within the Bluetooth specification v1.2 limits.

(2) Class 2 RF transmit power range, Bluetooth specification v1.2

(3) Measured at F_0 = 2441MHz.

(4) Up to three exceptions are allowed in v1.2 of the Bluetooth specification.

4.5.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = +105°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER for all packet types	2.402	-	-79	-	≤-70	dBm
	2.441	-	-81	-		
	2.480	-	-79.5	-		
Maximum received signal at 0.1% BER		-	>10	-	≥-20	dBm

4.6 Power Consumption

Operation Mode	Connection Type	UART Rate (kbps)	Average	Unit
Page scan	-	115.2	0.37	mA
Inquiry and page scan	-	115.2	0.68	mA
ACL No traffic	Master	115.2	6.46	mA
ACL With file transfer	Master	115.2	11.73	mA
ACL No traffic	Slave	115.2	13.90	mA
ACL With file transfer	Slave	115.2	17.19	mA
ACL No traffic	Master	921.6	6.49	mA
ACL With file transfer	Master	921.6	32.91	mA
ACL No traffic	Slave	921.6	13.87	mA
ACL With file transfer	Slave	921.6	30.59	mA
ACL 40ms sniff	Master	38.4	1.59	mA
ACL 1.28s sniff	Master	38.4	0.20	mA
SCO HV1	Master	38.4	34.00	mA
SCO HV3	Master	38.4	17.33	mA
SCO HV3 30ms sniff	Master	38.4	17.00	mA
ACL 40ms sniff	Slave	38.4	1.60	mA
ACL 1.28s sniff	Slave	38.4	0.24	mA
Parked 1.28s beacon	Slave	38.4	0.18	mA
SCO HV1	Slave	38.4	34.02	mA
SCO HV3	Slave	38.4	20.94	mA
SCO HV3 30ms sniff	Slave	38.4	16.80	mA
Standby Host connection	-	38.4	29	µA
Reset (RESETB low)	-	-	50	µA

Notes:

Firmware used: 17.11.

(1) Low power mode on the linear regulator is entered and exited automatically when the chip enters/leaves Deep Sleep mode. For more information about the electrical characteristics of the linear regulator, see Electrical Characteristics in this document.

Typical Peak Current @ -20°C to +85°C	
Device Activity/State	**Current (mA)**
Peak current during cold boot	50.7
Peak Tx current Master	42.8
Peak Rx current Master	35.1
Peak Tx current Slave	43.5
Peak Rx current Slave	39.4
Conditions	
Firmware	**HCI 17.11**
REG_IN, VDD_PIO, VDD_PADS	3.15V
Host Interface	UART
Baud Rate	115200
Clock Source	26MHz crystal
Output Power	0dBm

5 Device Diagram

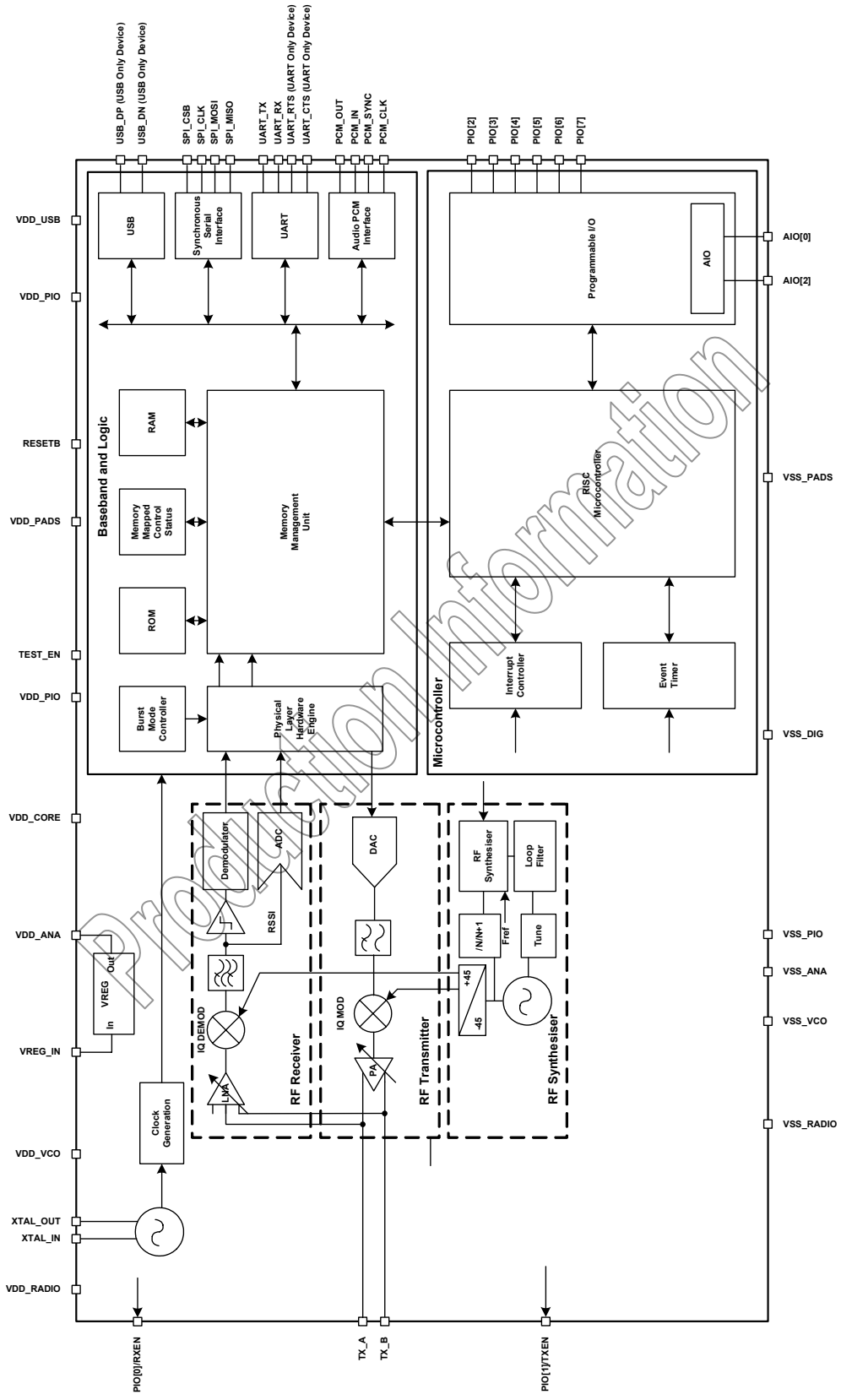


Figure 5.1: BlueCore3-ROM CSP Device Diagram for CSP Package

6 Description of Functional Blocks

6.1 RF Receiver

The receiver features a near-zero Intermediate Frequency (IF) architecture that allows the channel filters to be integrated on to the die. Sufficient out-of-band blocking specification at the Low Noise Amplifier (LNA) input allows the radio to be used in close proximity to Global System for Mobile Communications (GSM) and Wideband Code Division Multiple Access (W-CDMA) cellular phone transmitters without being desensitised. The use of a digital Frequency Shift Keying (FSK) discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BlueCore3-ROM CSP to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

6.1.1 Low Noise Amplifier

The LNA operates in differential mode and is used for Class 2 operation.

6.1.2 Analogue to Digital Converter

The Analogue to Digital Converter (ADC) is used to implement fast Automatic Gain Control (AGC). The ADC samples the Received Signal Strength Indicator (RSSI) voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference limited environments.

6.2 RF Transmitter

6.2.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise the frequency drift during a transmit timeslot which results in a controlled modulation index. A digital baseband transmit filter provides the required spectral shaping.

6.2.2 Power Amplifier

The internal Power Amplifier (PA) has a maximum output power of +6dBm allowing BlueCore3-ROM CSP to be used in Class 2 and Class 3 radios without an external RF PA.

6.3 RF Synthesiser

The radio synthesiser is fully integrated onto the die with no requirement for an external Voltage Controlled Oscillator (VCO) screening can, varactor tuning diodes or LC resonators. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth specification V1.2.

6.4 Clock Input and Generation

The reference clock for the system is generated from a TCXO or crystal input between 8MHz and 40MHz. All internal reference clocks are generated using a phase locked loop, which is locked to the external reference frequency.

6.5 Baseband and Logic

6.5.1 Memory Management Unit

The Memory Management Unit (MMU) provides a number of dynamically allocated ring buffers that hold the data which is in transit between the host and the air or vice versa. The dynamic allocation of memory ensures efficient use of the available Random Access Memory (RAM) and is performed by hardware MMU to minimise the overheads on the processor during data/voice transfers.

6.5.2 Burst Mode Controller

During radio transmission the Burst Mode Controller (BMC) constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During radio reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

6.5.3 Physical Layer Hardware Engine DSP

Dedicated logic is used to perform the following:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

The following voice data translations and operations are performed by firmware:

- A-law/μ-law/linear voice data (from host)
- A-law/μ-law/Continuously Variable Slope Delta (CVSD) (over the air)
- Voice interpolation for lost packets
- Rate mismatches

The hardware supports all optional and mandatory features of Bluetooth v1.2 including AFH and eSCO.

6.5.4 RAM

32Kbytes of on-chip RAM is provided and is shared between the ring buffers used to hold voice/data for each active connection and the general purpose memory required by the Bluetooth stack.

6.5.5 ROM

4Mbits of metal programmable ROM is provided for system firmware implementation.

6.5.6 USB (BC313143A only)

This is a full speed Universal Serial Bus (USB) interface for communicating with other compatible digital devices. BlueCore3-ROM CSP acts as a USB peripheral, responding to requests from a master host controller such as a PC.

6.5.7 Synchronous Serial Interface

This is a synchronous serial port interface (SPI) for interfacing with other digital devices. The SPI port can be used for system debugging.

6.5.8 UART (BC313141A only)

This is a standard Universal Asynchronous Receiver Transmitter (UART) interface for communicating with other serial devices.

6.5.9 Audio PCM Interface

The Audio Pulse Code Modulation (PCM) Interface supports continuous transmission and reception of PCM encoded audio data over Bluetooth.

6.6 Microcontroller

The microcontroller, interrupt controller and event timer run the Bluetooth software stack and control the radio and host interfaces. A 16-bit Reduced Instruction Set Computer (RISC) microcontroller is used for low power consumption and efficient use of memory.

6.6.1 Programmable I/O

BlueCore3-ROM CSP has a total of 10 (8 digital and 2 analogue) programmable I/O terminals. These are controlled by firmware running on the device.

7 CSR Bluetooth Software Stacks

BlueCore3-ROM CSP is supplied with Bluetooth v1.2 compliant stack firmware which runs on the internal RISC microcontroller.

The BlueCore3-ROM CSP software architecture allows Bluetooth processing and the application program to be shared in different ways between the internal RISC microcontroller and an external host processor (if any). The upper layers of the Bluetooth stack (above HCI) can be run either on-chip or on the host processor.

7.1 BlueCore HCI Stack

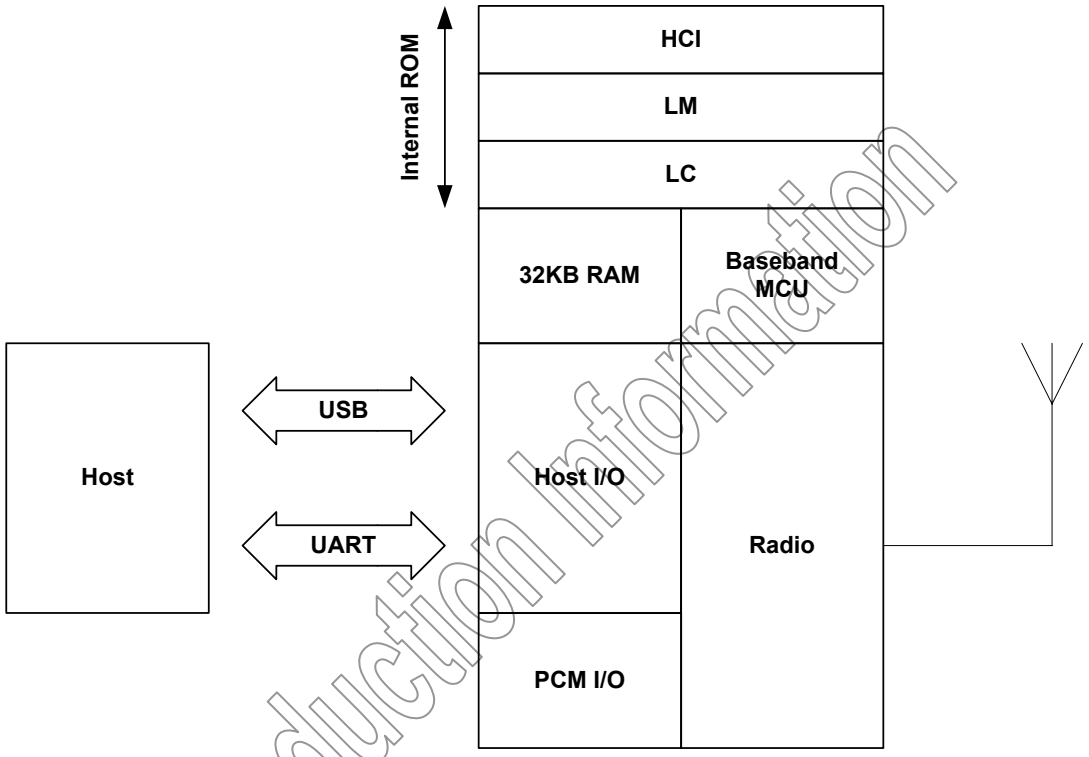


Figure 7.1: BlueCore HCI Stack

In this implementation the internal processor runs the Bluetooth stack up to the Host Controller Interface (HCI). The Host processor must provide all upper layers including the applications.

7.1.1 Key Features of the HCI Stack – Standard Bluetooth Functionality

New Bluetooth v1.2 Mandatory Functionality

- Adaptive Frequency Hopping (AFH)
- Faster Connections
- Flow and Flush Timeout
- LMP Improvements
- Parameter Ranges

Optional v1.2 functionality supported

- Extended SCO (eSCO), eV3 +CRC, eV4, eV5
- Scatter mode
- LMP Absence Masks ,Quality of service and SCO handle
- L2CAP flow and error control
- Synchronisation

Standard Bluetooth Functionality

The firmware has been written against the Bluetooth Core Specification v1.2.

- Bluetooth components:
  - Baseband (including LC)
  - LM
  - HCI
- Standard USB v2.0 and UART (H5) HCI Transport Layers
- All standard radio packet types
- Full Bluetooth data rate, up to 723.2kbps asymmetric(1)
- Operation with up to seven active slaves (1)
- Maximum number of simultaneous active ACL connections: 7(2)
- Maximum number of simultaneous active SCO connections: 3(2)
- Operation with up to three SCO links, routed to one or more slaves
- Scatternet 2.5 operation
- All standard SCO voice coding, plus “transparent SCO”
- Standard operating modes: page, inquiry, page-scan and inquiry-scan
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power saving mechanisms: Hold, Sniff and Park modes, including “Forced Hold”
- Dynamic control of peers’ transmit power via LMP
- Master/slave switch
- Broadcast
- Channel quality driven data rate
- All standard Bluetooth Test Modes

Notes:

(1) Maximum allowed by Bluetooth specification v1.2

(2) Supports all combinations of active ACL and SCO channels, per Bluetooth specification v1.2

The firmware's supported Bluetooth features are detailed in the standard Protocol Implementation Conformance Statement (PICS) documents, available from www.csr.com.

7.1.2 Key Features of the HCI Stack - Extra Functionality

The firmware extends the standard Bluetooth functionality with the following features:

- Supports BlueCore Serial Protocol (BCSP) – a proprietary, reliable alternative to the standard Bluetooth UART Host Transport.
- Provides a set of approximately 50 manufacturer-specific HCI extension commands. This command set, called BCCMD (BlueCore Command), provides:
- Access to the chip's general-purpose PIO port
  - The negotiated effective encryption key length on established Bluetooth links
  - Access to the firmware's random number generator
  - Controls to set the default and maximum transmit powers. These can help minimise interference between overlapping, fixed-location piconet
  - Dynamic UART configuration
  - Radio transmitter enable/disable (a simple command connects to a dedicated hardware switch that determines whether the radio can transmit)
- The firmware can read the voltage on a pair of the chip's external pins. This is normally used to build a battery monitor, using either VM or host code.
- A block of BCCMD commands provides access to the chip's "persistent store" configuration database (PS). The database sets the device's Bluetooth address, Class of Device, radio (transmit class) configuration, SCO routing, LM, USB and DFU constants, etc.
- A UART break condition can be used in three ways:
  1.1. Presenting a UART break condition to the chip can force the chip to perform a hardware reboot
  1.2. Presenting a break condition at boot time can hold the chip in a low power state, preventing normal initialisation while the condition exists
  1.3. With H5, the firmware can be configured to send a break to the host before sending data (normally used to wake the host from a Deep Sleep state)
- A block of "radio test" or BIST commands allows direct control of the chip's radio. This aids the development of modules' radio designs, and can be used to support Bluetooth qualification.
- Virtual Machine (VM). The firmware provides the VM environment in which to run application-specific code. Although the VM is mainly used with BlueLab and "RFCOMM builds" (alternative firmware builds providing L2CAP, SDP and RFCOMM), the VM can be used with this build to perform simple tasks such as flashing LEDs via the chip's PIO port.
- Hardware low power modes: shallow sleep and deep sleep. The chip drops into modes that significantly reduce power consumption when the software goes idle.
- SCO channels are normally routed over HCI over BCSP, H5 or USB. However, up to three SCO channels can be routed over the chip's single PCM port at the same time as routing any other SCO channels over HCI.
- Co-operative existence with 802.11b chipsets

Always refer to the Firmware Release Note for the specific functionality of a particular build.

7.2 BlueCore RFCOMM Stack

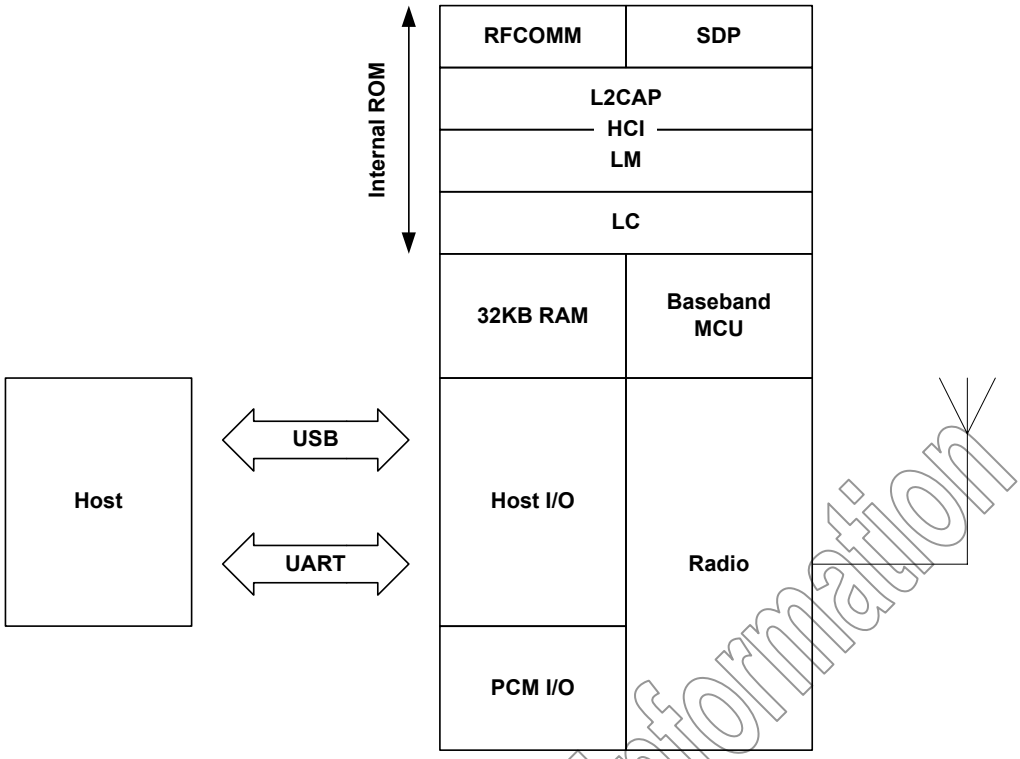


Figure 7.2: BlueCore RFCOMM Stack

In this version of the firmware the upper layers of the Bluetooth stack up to RFCOMM are run on-chip. This reduces host-side software and hardware requirements at the expense of some of the power and flexibility of the HCI only stack.

7.2.1 Key Features of the BlueCore3-ROM CSP RFCOMM Stack

Interfaces to Host

- RFCOMM, an RS-232 serial cable emulation protocol
- SDP, a service database look-up protocol

Connectivity

- Maximum number of active slaves: 3
- Maximum number of simultaneous active ACL connections: 3
- Maximum number of simultaneous active SCO connections: 3
- Data Rate: up to 350Kb/s

Security

- Full support for all Bluetooth security features up to and including strong (128-bit) encryption.

Power Saving

- Full support for all Bluetooth power saving modes (Park, Sniff and Hold).

Data Integrity

- CQDDR increases the effective data rate in noisy environments.
- RSSI used to minimise interference to other radio devices using the ISM band.

7.3 BCHS Software

BlueCore Embedded Host Software is designed to enable CSR customers to implement Bluetooth functionality into embedded products quickly, cheaply and with low risk.

BCHS is developed to work with CSR's family of BlueCore IC's. BCHS is intended for embedded products that have a host processor for running BCHS and the Bluetooth application e.g. a mobile phone or a PDA. BCHS together with the BlueCore IC with embedded Bluetooth core stack (L2CAP, RFCOMM and SDP) is a complete Bluetooth system solution from RF to profiles.

BCHS includes most of the Bluetooth intelligence and gives the user a simple API. This makes it possible to develop a Bluetooth product without in-depth Bluetooth knowledge.

The BlueCore Embedded Host Software contains three elements:

- Example Drivers (BCSP and proxies)
- Bluetooth Profile Managers
- Example Applications

The profiles are qualified which makes the qualification of the final product very easy. BCHS is delivered with source code (ANSI C). With BCHS also come example applications in ANSI C, which makes the process of writing the application easier.

7.4 Additional Software for Other Embedded Applications

When the upper layers of the Bluetooth protocol stack are run as firmware on BlueCore3-ROM CSP, a UART software driver is supplied that presents the L2CAP, RFCOMM and Service Discovery (SDP) APIs to higher Bluetooth stack layers running on the host. The code is provided as 'C' source or object code.

7.5 CSR Development Systems

CSR's BlueLab and Casira development kits are available to allow the evaluation of the BlueCore3 hardware and software, and as toolkits for developing on-chip and host software.

8 Device Terminal Descriptions

8.1 RF Ports

The BlueCore3-ROM CSP has common differential RF input and output ports as shown in Figure 8.1, the internal common connections between the transmitter and receiver are described in Section 8.1.1 and shown in. The operational mode is determined by setting the PS Key PSKEY_TXRX_PIO_CONTROL (0x209).

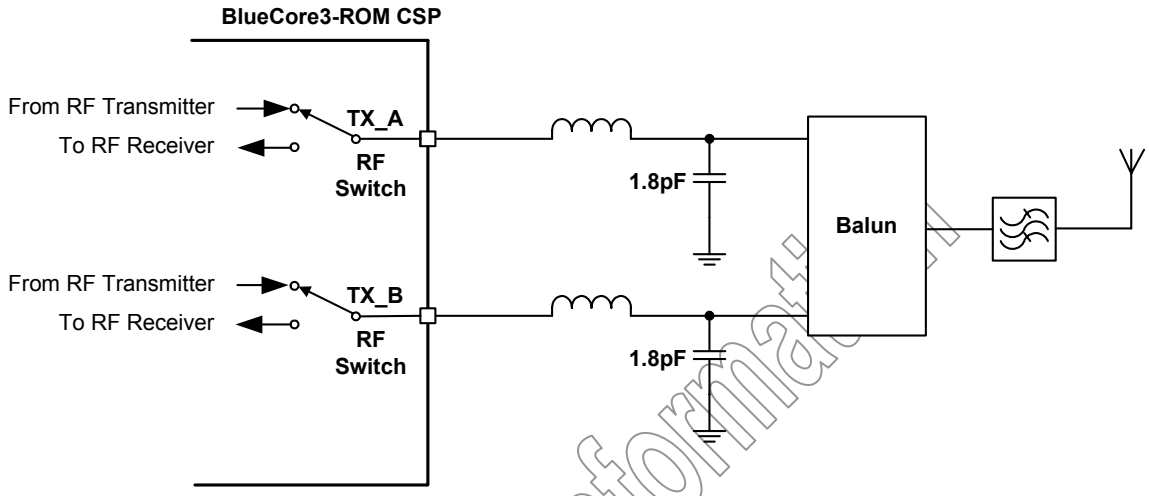


Figure 8.1: Common Differential RF Input and Output Ports (Class 2)

8.1.1 TX_A and TX_B

TX_A and TX_B are balanced RF ports which are used for both transmitting and receiving. Selection of transmit or receive mode is under software control. The TX measurements in the following section refer to the device being put into transmit modes and the RX measurements refer to the device being put into receive modes.

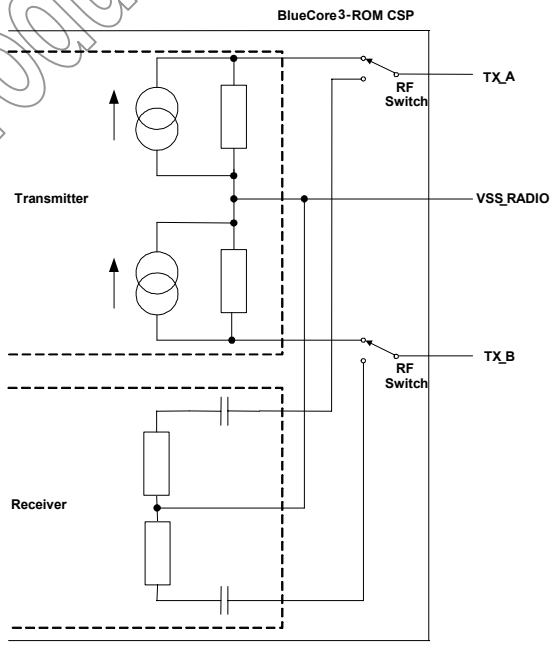


Figure 8.2: RF Input/Output Diagram

8.1.2 Transmitter S-Parameters

Port 1: TX_A

Port 2: TX_B

Temperature: +20°C

Power Level: 63

GHZ S MP R 50

Freq (MHz)	S11		S21		S12		S22	
	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.
2.4	0.778992	-110.502	0.089221	53.090667	0.095407	76.015437	0.765223	-111.621238
2.41	0.778216	-110.488	0.08835	53.138275	0.096211	74.898228	0.765626	-111.955226
2.42	0.77645	-110.507	0.087776	53.082489	0.097171	73.823056	0.765605	-112.259735
2.43	0.774543	-110.59	0.086733	53.190804	0.098066	72.806983	0.765635	-112.625792
2.44	0.774082	-110.644	0.085721	52.978288	0.097855	71.945326	0.76746	-113.100529
2.45	0.772337	-110.798	0.08466	53.826097	0.099093	71.402956	0.770942	-113.31683
2.46	0.776561	-110.974	0.085574	55.47352	0.096084	68.284531	0.775047	-113.456241
2.47	0.773134	-110.998	0.085125	53.860453	0.10329	70.063979	0.772324	-113.702371
2.48	0.787564	-110.922	0.101769	56.756751	0.081487	69.515479	0.749537	-114.239531
2.49	0.770775	-111.086	0.085522	54.24436	0.103871	66.737566	0.771541	-114.281514
2.5	0.771305	-111.27	0.084643	54.319244	0.102864	65.651072	0.772812	-114.523037

Table 8.1: Transmit Mode S-Parameters

8.1.3 Transmit Port Impedances

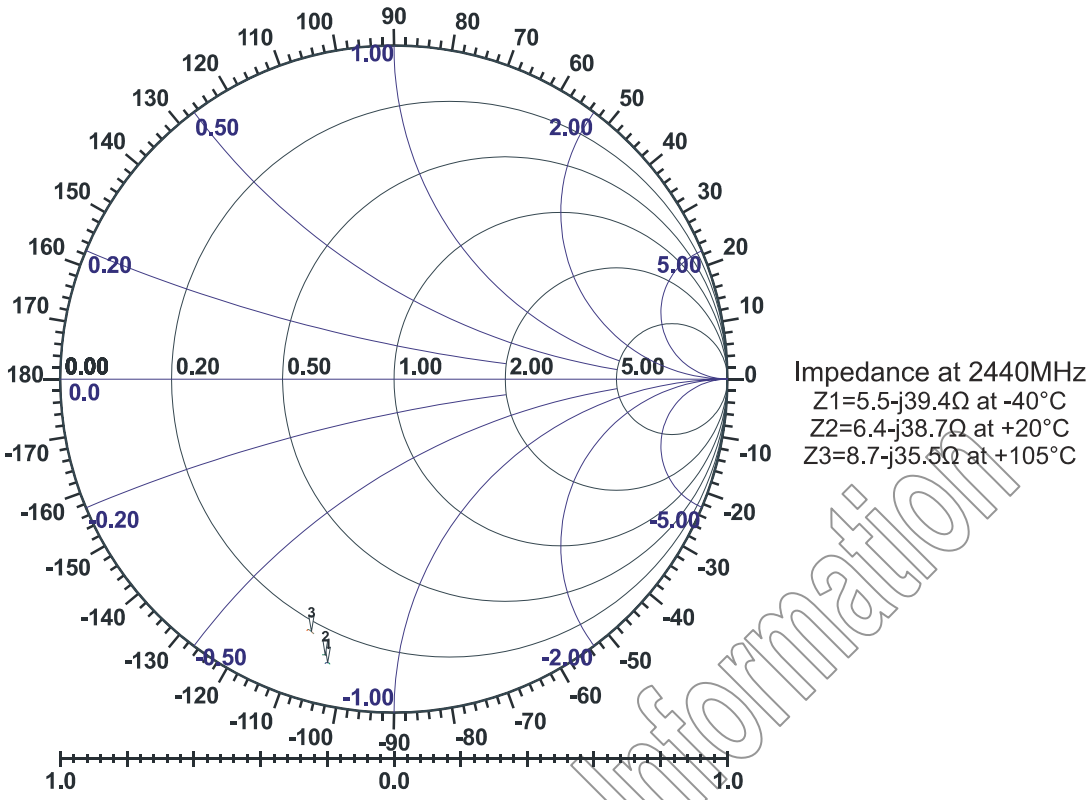


Figure 8.3: TX_A Output at Power Setting 35

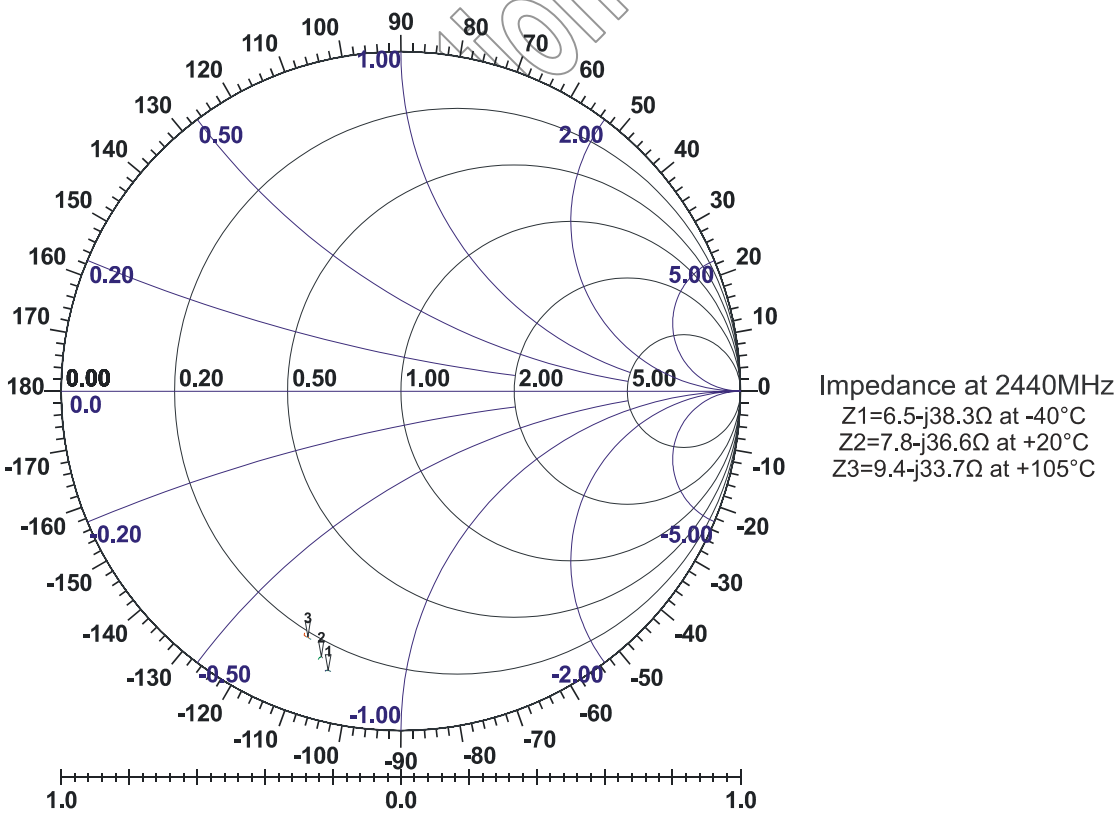


Figure 8.4: TX_A Output at Power Setting 50

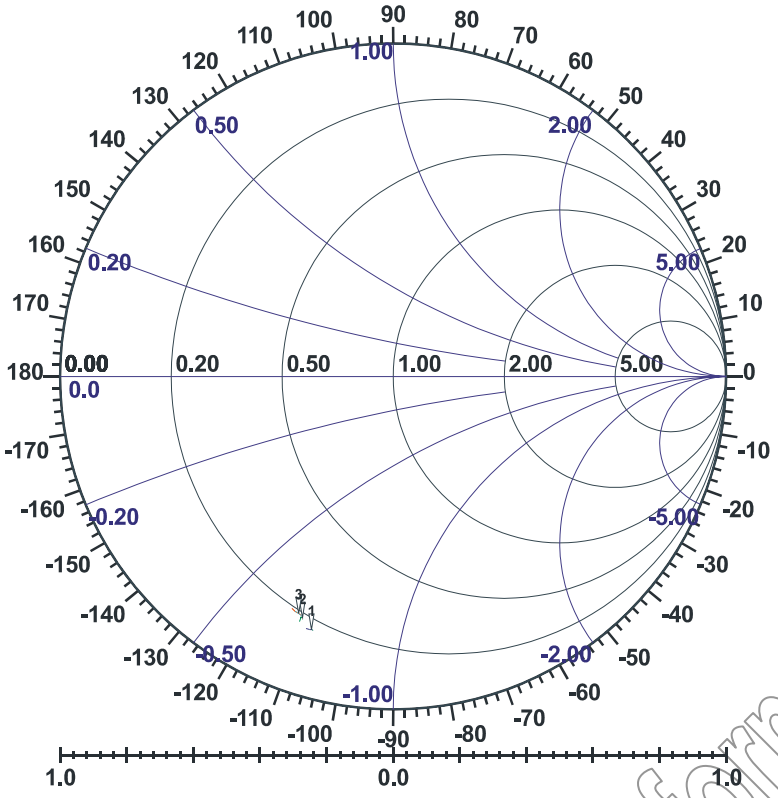


Figure 8.5: TX_A Output at Power Setting 63

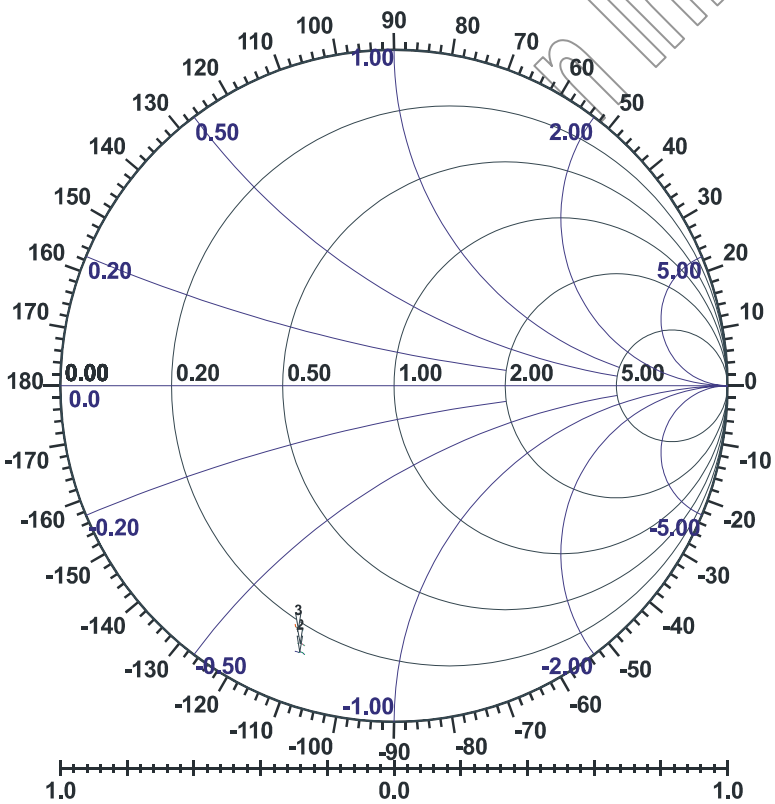


Figure 8.6: TX_B Output at Power Setting 35

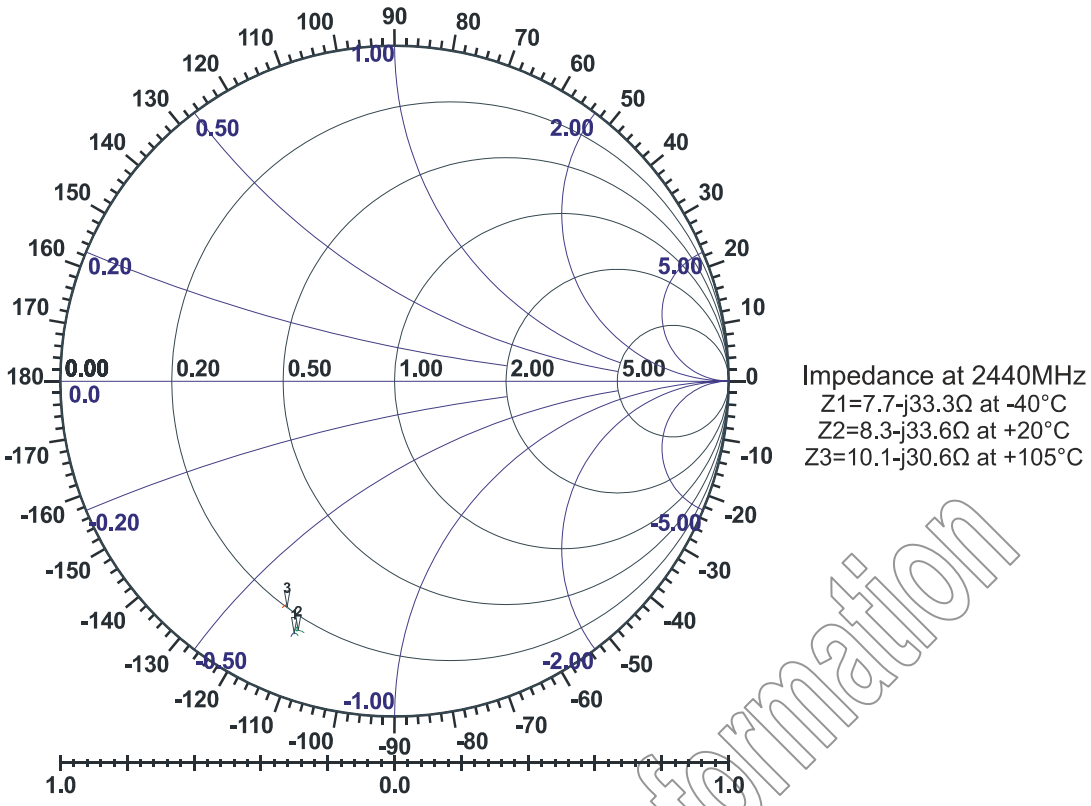


Figure 8.7: TX_B Output at Power Setting 50

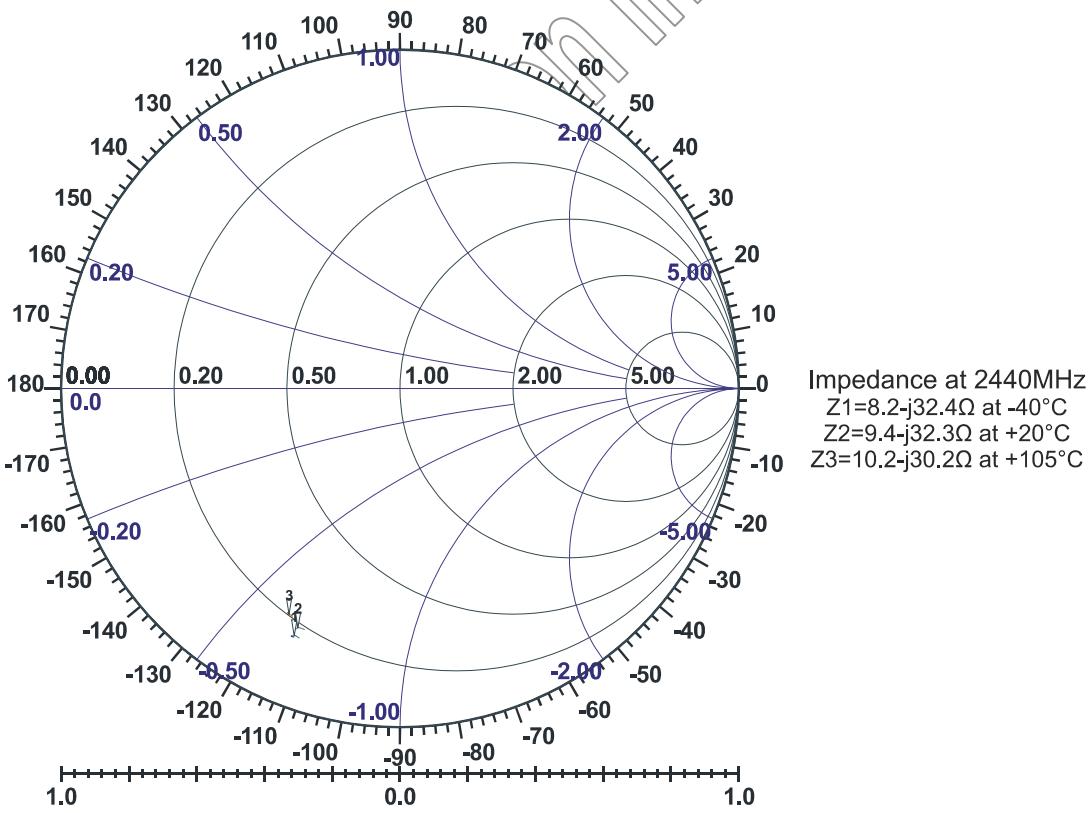


Figure 8.8: TX_B Output at Power Setting 63

8.1.4 Receiver S-Parameters

Port 1: TX_A

Port 2: TX_B

Temperature: +20°C

GHZ S MP R 50

Freq (MHz)	S11		S21		S12		S22	
	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.
2.4	0.731957	-83.6007	0.098114	59.46505	0.130935	74.86366	0.651799	-88.5651
2.41	0.728306	-84.3174	0.097465	59.09911	0.132772	72.84295	0.646684	-89.7553
2.42	0.722299	-85.0836	0.096811	58.55238	0.13363	71.09473	0.641781	-90.827
2.43	0.714729	-86.0815	0.095667	58.12089	0.134139	69.54935	0.636354	-92.0823
2.44	0.711343	-87.0754	0.094944	57.52449	0.134045	68.11455	0.63506	-93.5674
2.45	0.704912	-88.0926	0.094097	57.71248	0.136614	66.62563	0.634593	-94.7098
2.46	0.70591	-89.2094	0.094708	58.64331	0.136792	63.42167	0.633279	-95.8576
2.47	0.700536	-90.2489	0.094607	57.00482	0.14231	63.94967	0.626289	-97.0576
2.48	0.708689	-91.3032	0.106625	59.86385	0.126132	60.06994	0.604609	-98.3874
2.49	0.689339	-92.4534	0.093223	56.44381	0.143789	60.1473	0.619555	-99.3865
2.5	0.686515	-93.7781	0.092186	56.24232	0.143386	58.2896	0.619004	-100.649

Table 8.2: Receive Mode S-Parameters

8.1.5 Receive Port Impedances

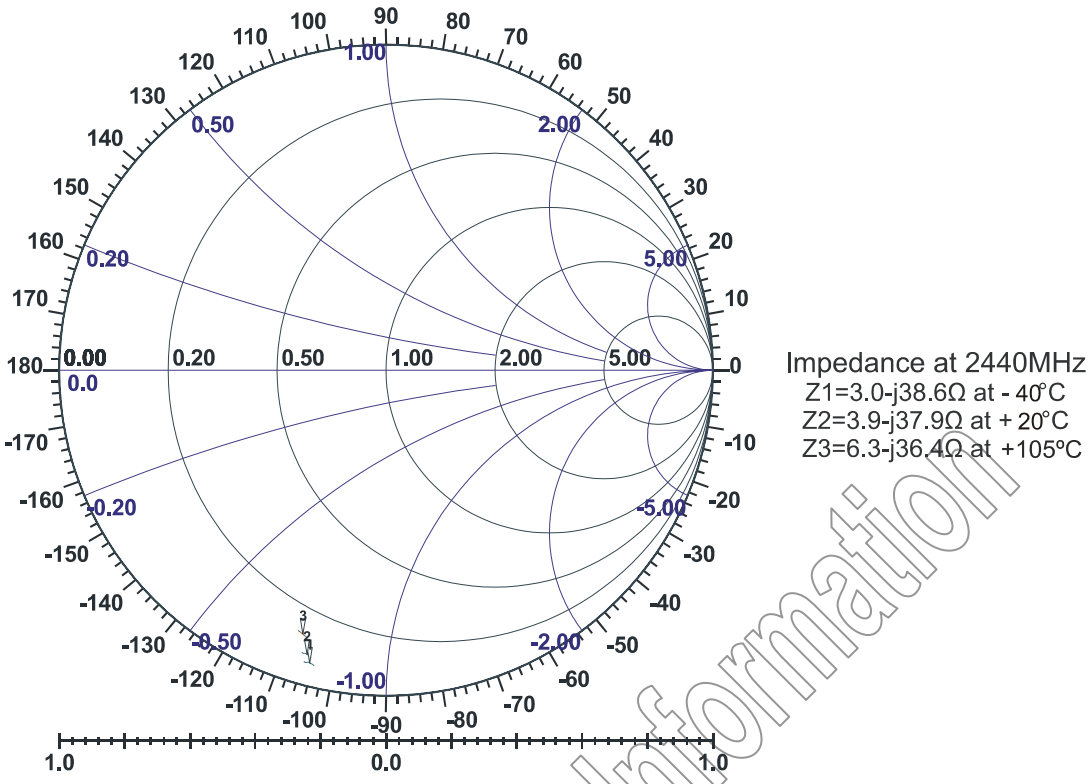


Figure 8.9: RX_A Balanced Receive Input Impedance

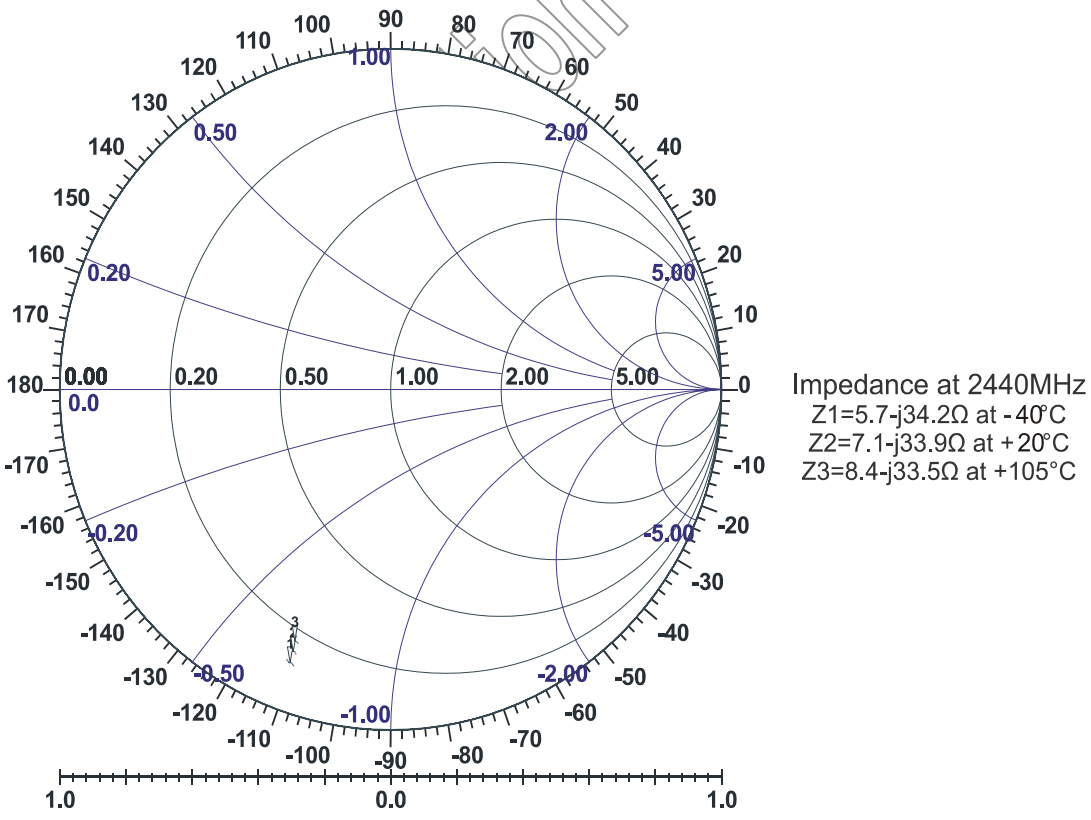


Figure 8.10: RX_B Balanced Receive Input Impedance

8.2 External Reference Clock Input (XTAL_IN)

The BlueCore3-ROM CSP RF local oscillator and internal digital clocks are derived from the reference clock at the BlueCore3-ROM CSP XTAL_IN input. This reference may be either an external clock or from a crystal connected between XTAL_IN and XTAL_OUT. The crystal mode is described in Section 8.3.

8.2.1 External Mode

BlueCore3-ROM CSP can be configured to accept an external reference clock (from another device, such as TCXO) at XTAL_IN by connecting XTAL_OUT to ground. The external clock can either be a digital level square wave or sinusoidal and this may be directly coupled to XTAL_IN without the need for additional components. If the peaks of the reference clock are below VSS_ANA or above VDD_ANA, it must be driven through a DC blocking capacitor (~33pF) connected to XTAL_IN. A digital level reference clock gives superior noise immunity as the high slew rate clock edges have lower voltage to phase conversion.

The external clock signal should meet the specifications in Table 8.3:

	Min	Typ	Max
Frequency[1]	7.5MHz	16MHz	40MHz
Duty cycle	20:80	50:50	80:20
Edge Jitter (At Zero Crossing)	-	-	15ps rms
Signal Level	400mV pk-pk	-	VDD_ANA[2][3]

Table 8.3: External Clock Specifications

Notes:

(1) The frequency should be an integer multiple of 250kHz except for the CDMA/3G frequencies

(2) VDD_ANA is 1.8V nominal

(3) If the external clock is driven through a DC blocking capacitor then maximum allowable amplitude is reduced from VDD_ANA to 800mV pk-pk

8.2.2 XTAL_IN Impedance in External Mode

The impedance of the XTAL_IN will not change significantly between operating modes, typically 10fF. When transitioning from deep sleep to an active state a spike of up to 1pC may be measured. For this reason it is recommended that a buffered clock input be used.

8.2.3 Clock Timing Accuracy

As Figure 8.11 indicates, the 250ppm timing accuracy on the external clock is required 7ms after the assertion of the system clock request line. This is to guarantee that the firmware can maintain timing accuracy in accordance with the Bluetooth v1.2 specification. Radio activity may occur after 11ms, therefore at this point, the timing accuracy of the external clock source must be within 20ppm.

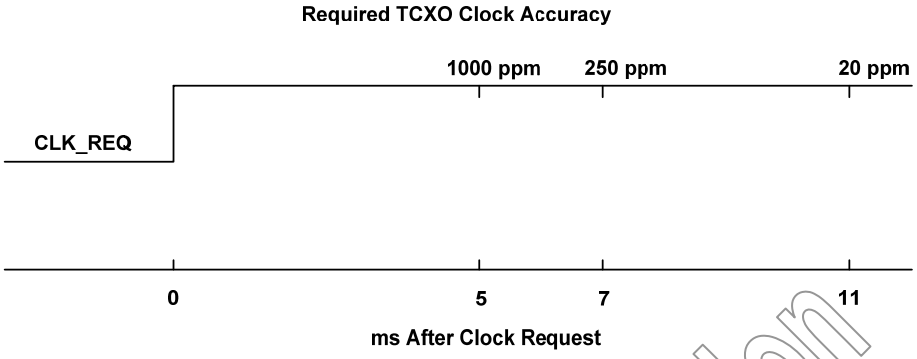


Figure 8.11: TCXO Clock Accuracy

8.2.4 Clock Start-Up Delay

BlueCore3-ROM CSP hardware incorporates an automatic 5ms delay after the assertion of the system clock request signal before running firmware. This is suitable for most applications using an external clock source. However, there may be scenarios where the clock cannot be guaranteed to either exist or be stable after this period. Under these conditions, BlueCore3-ROM CSP firmware provides a software function which will extend the system clock request signal by a period stored in PSKEY_CLOCK_STARTUP_DELAY. This value is set in milliseconds from 5-31ms.

This PS Key allows the designer to optimise a system where clock latencies may be longer than 5ms while still keeping the current consumption of BlueCore3-ROM CSP as low as possible. BlueCore3-ROM CSP will consume about 2mA of current for the duration of PSKEY_CLOCK_STARTUP_DELAY before activating the firmware.

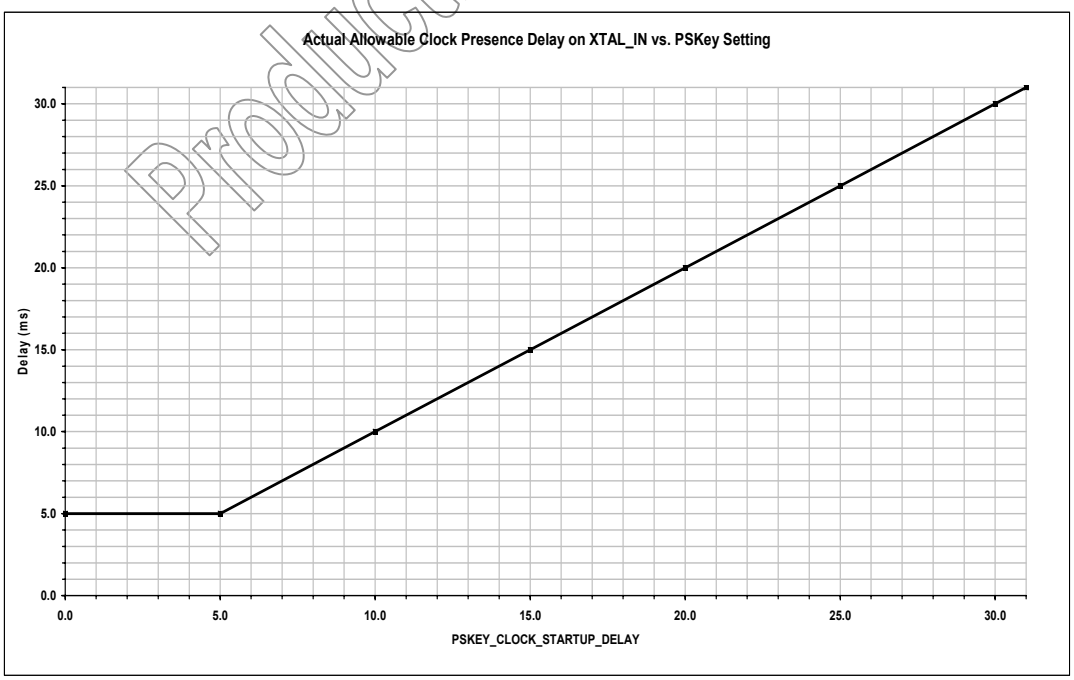


Figure 8.12: Actual Allowable Clock Presence Delay on XTAL_IN vs. PS Key Setting

8.2.5 Input Frequencies and PS Key Settings

BlueCore3-ROM CSP should be configured to operate with the chosen reference frequency. This is accomplished by setting the PS Key PSKEY_ANA_FREQ (0x1fe) for all frequencies with an integer multiple of 250KHz. The input frequency default setting in BlueCore3-ROM CSP is 26MHz.

The following CDMA/3G TCXO frequencies are also catered for: 7.68, 14.4, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz.

Reference Crystal Frequency (MHz)	PSKEY_ANA_FREQ (0x1fe) (Units of 1kHz)
7.68	7680
14.40	14400
15.36	15360
16.20	16200
16.80	16800
19.20	19200
19.44	19440
19.68	19680
19.80	19800
38.40	38400
n x 250kHz	-
+26.00 Default	26000

Table 8.4: PS Key Values for CDMA/3G phone TCXO Frequencies

8.3 Crystal Oscillator (XTAL_IN, XTAL_OUT)

The BlueCore3-ROM CSP RF local oscillator and internal digital clocks are derived from the reference clock at the BlueCore3-ROM CSP XTAL_IN input. This reference may be either an external clock or from a crystal connected between XTAL_IN and XTAL_OUT. The external reference clock mode is described in Section 8.1.

8.3.1 XTAL Mode

BlueCore3-ROM CSP contains a crystal driver circuit. This operates with an external crystal and capacitors to form a Pierce oscillator.

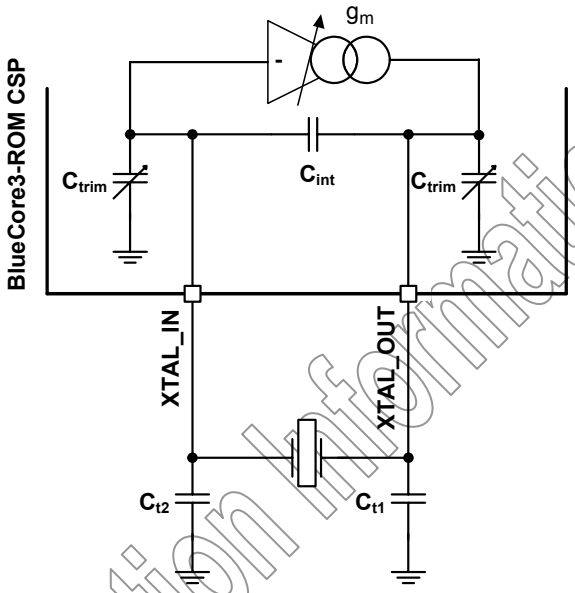


Figure 8.13: Crystal Driver Circuit

Figure 8.14 shows an electrical equivalent circuit for a crystal. The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors.

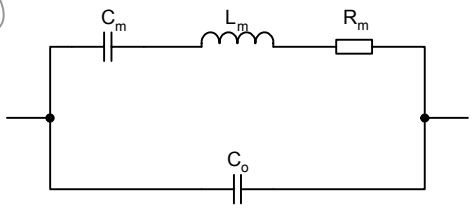


Figure 8.14: Crystal Equivalent Circuit

The resonant frequency may be trimmed with the crystal load capacitance. BlueCore3-ROM CSP contains variable internal capacitors to provide a fine trim.

The BlueCore3-ROM CSP driver circuit is a transconductance amplifier. A voltage at XTAL_IN generates a current at XTAL_OUT. The value of transconductance is variable and may be set for optimum performance.

8.3.2 Load Capacitance

For resonance at the correct frequency the crystal should be loaded with its specified load capacitance, which is defined for the crystal. This is the total capacitance across the crystal viewed from its terminals. BlueCore3-ROM CSP provides some of this load with the capacitors C_{trim} and C_{int}. The remainder should be from the external capacitors labelled C_{t1} and C_{t2}. C_{t1} should be three times the value of C_{t2} for best noise performance. This maximises the signal swing, hence slew rate at XTAL_IN, to which all on chip clocks are referred. Crystal load capacitance, C_l is calculated with the following equation:

$$C_l = C_{int} + \frac{C_{trim}}{2} + \frac{C_{t1} \cdot C_{t2}}{C_{t1} + C_{t2}}$$

Equation 8.1: Load Capacitance

Where:

C_{trim} = 3.4pF nominal (Mid range setting)

C_{int} = 1.5pF

Note:

C_{int} does not include the crystal internal self capacitance, it is the driver self capacitance

8.3.3 Frequency Trim

BlueCore3-ROM CSP enables frequency adjustments to be made. This feature is typically used to remove initial tolerance frequency errors associated with the crystal. Frequency trim is achieved by adjusting the crystal load capacitance with on chip trim capacitors, C_{trim}. The value of C_{trim} is set by a 6-bit word in the Persistent Store Key PSKEY_ANA_FTRIM (0x1f6). Its value is calculated thus:

$$C_{trim} = 110\ \text{fF} \times \text{PSKEY\_ANA\_FTRIM}$$

Equation 8.2: Trim Capacitance

There are two C_{trim} capacitors, which are both connected to ground. When viewed from the crystal terminals, they appear in series so each least significant bit (LSB) increment of frequency trim presents a load across the crystal of 55fF.

The frequency trim is described by Equation 8.3:

$$\frac{\Delta(F_x)}{F_x} = \text{pullability} \times 55 \times 10^{-3} (\text{ppm/LSB})$$

Equation 8.3: Frequency Trim

Where F_x is the crystal frequency and pullability is a crystal parameter with units of ppm/pF. Total trim range is 63 times the value above.

If not specified, the pullability of a crystal may be calculated from its motional capacitance with Equation 8.4:

$$\frac{\partial(F_x)}{\partial(C)} = F_x \cdot \frac{C_m}{4(C_l + C_0)^2}$$

Equation 8.4: Pullability

Where:

C_0 = Crystal self capacitance (shunt capacitance)

C_m = Crystal motional capacitance (series branch capacitance in crystal model). See Figure 8.14.

Note:

It is a Bluetooth requirement that the frequency is always within ±20ppm. The trim range should be sufficient to pull the crystal within ±5ppm of the exact frequency. This leaves a margin of ±15ppm for frequency drift with ageing and temperature. A crystal with an ageing and temperature drift specification of better than ±15ppm is required.

8.3.4 Transconductance Driver Model

The crystal and its load capacitors should be viewed as a transimpedance element, whereby a current applied to one terminal generates a voltage at the other. The transconductance amplifier in BlueCore3-ROM CSP uses the voltage at its input, XTAL_IN, to generate a current at its output, XTAL_OUT. Therefore, the circuit will oscillate if the transconductance, transimpedance product is greater than unity. For sufficient oscillation amplitude, the product should be greater than 3. The transconductance required for oscillation is defined by the following relationship:

$$g_m > \frac{3(C_{t1}+C_{trim})(C_{t2}+C_{trim})}{(2\pi F_x)^2 R_m((C_0+C_{int})(C_{t1}+C_{t2}+2C_{trim})+(C_{t1}+C_{trim})(C_{t2}+C_{trim}))^2}$$

Equation 8.5: Transconductance Required for Oscillation

BlueCore3-ROM CSP guarantees a transconductance value of at least 2mA/V at maximum drive level.

Notes:

More drive strength is required for higher frequency crystals, higher loss crystals (larger Rm) or higher capacitance loading.

Optimum drive level is attained when the level at XTAL_IN is approximately 1V pkpk. The drive level is determined by the crystal driver transconductance, by setting the Persistent Store KEY_XTAL_LVL (0x241).

8.3.5 Negative Resistance Model

An alternative representation of the crystal and its load capacitors is a frequency dependent resistive element. The driver amplifier may be considered as a circuit that provides negative resistance. For oscillation, the value of the negative resistance must be greater than that of the crystal circuit equivalent resistance. Although the BlueCore3-ROM CSP crystal driver circuit is based on a transimpedance amplifier, an equivalent negative resistance may be calculated for it with the following formula in Equation 8.6:

$$R_{neg} > \frac{3(C_{t1}+C_{trim})(C_{t2}+C_{trim})}{g_m(2\pi F_x)^2(C_0+C_{int})((C_{t1}+C_{t2}+2C_{trim})+(C_{t1}+C_{trim})(C_{t2}+C_{trim}))^2}$$

Equation 8.6: Equivalent Negative Resistance

This formula shows the negative resistance of the BlueCore3-ROM CSP driver as a function of its drive strength.

The value of the driver negative resistance may be easily measured by placing an additional resistance in series with the crystal. The maximum value of this resistor (oscillation occurs) is the equivalent negative resistance of the oscillator.

	Min	Typ	Max
Frequency	8MHz	16MHz	40MHz
Initial Tolerance	-	±25ppm	-
Pullability	-	±20ppm/pF	-

Table 8.5: Crystal Oscillator Specification

8.3.6 Crystal PS Key Settings

See tables in Section 8.2.5.

8.3.7 Crystal Oscillator Characteristics

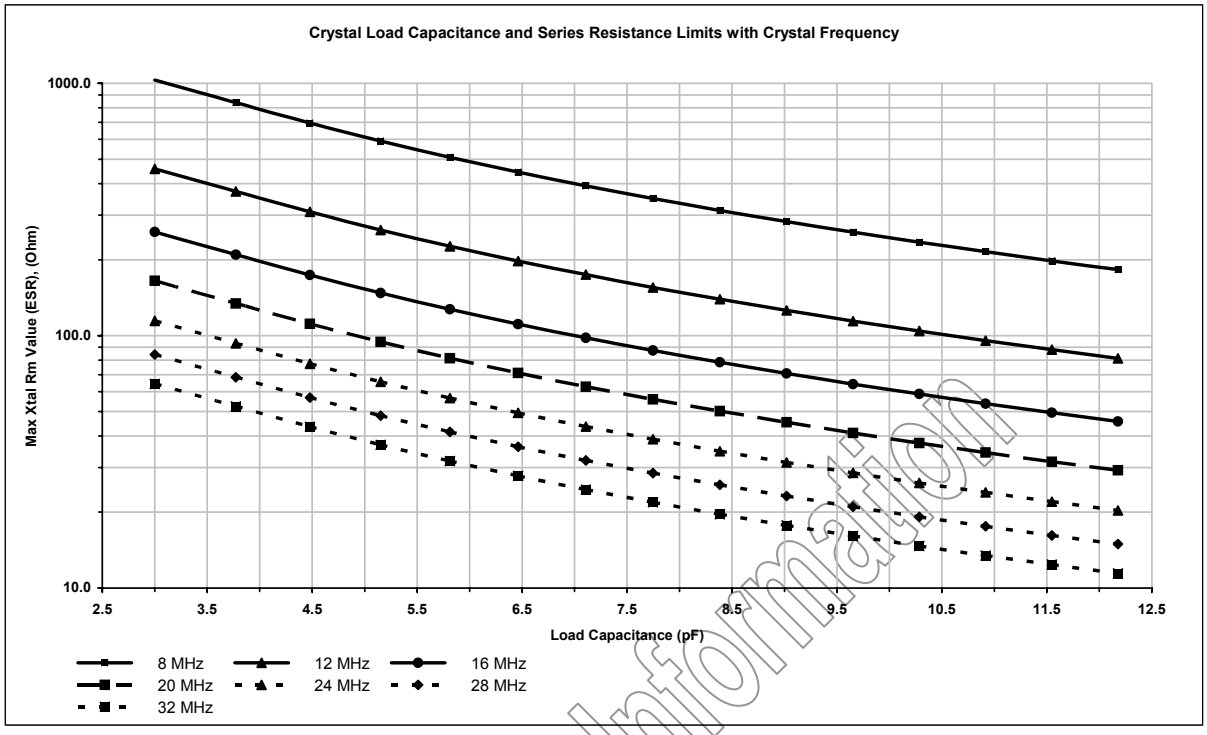


Figure 8.15: Crystal Load Capacitance and Series Resistance Limits with Crystal Frequency

Note:

Graph shows results for BlueCore3-ROM CSP crystal driver at maximum drive level.

Conditions:

C_{trim} = 3.4pF centre value

Crystal C_o = 2pF

Transconductance setting = 2mA/V

Loop gain = 3

C_{t1}/C_{t2} = 3

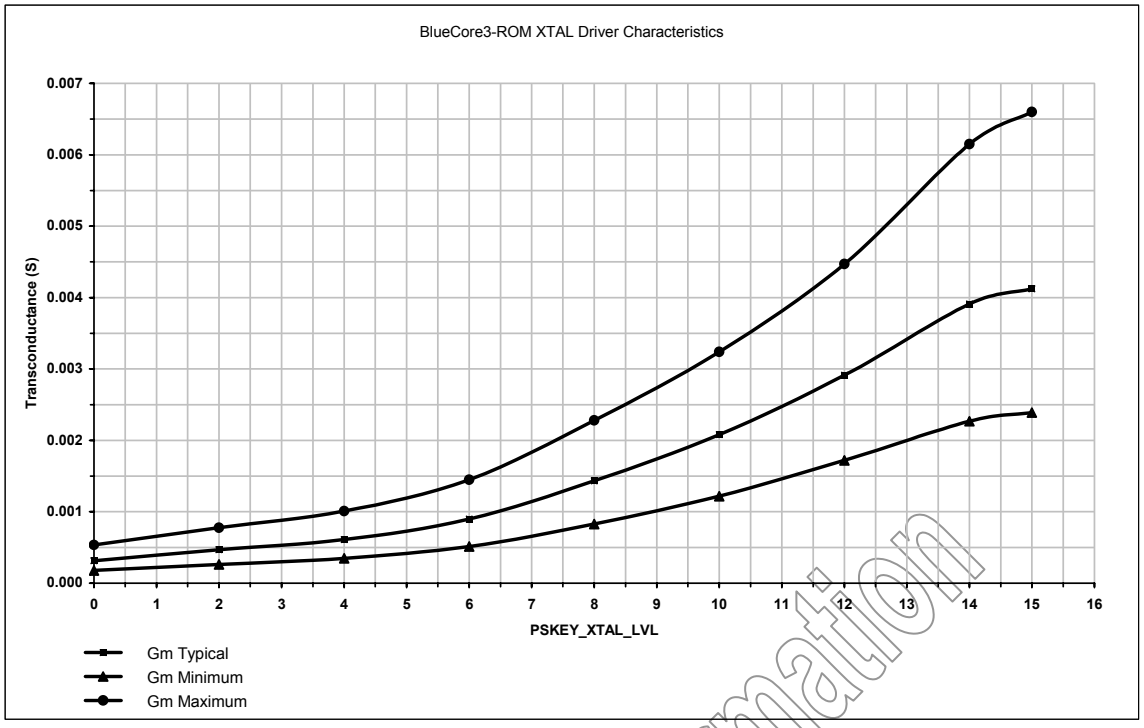


Figure 8.16: Crystal Driver Transconductance vs. Driver Level Register Setting

Note:

Drive level is set by Persistent Store Key PSKEY_XTAL_LVL (0x241).

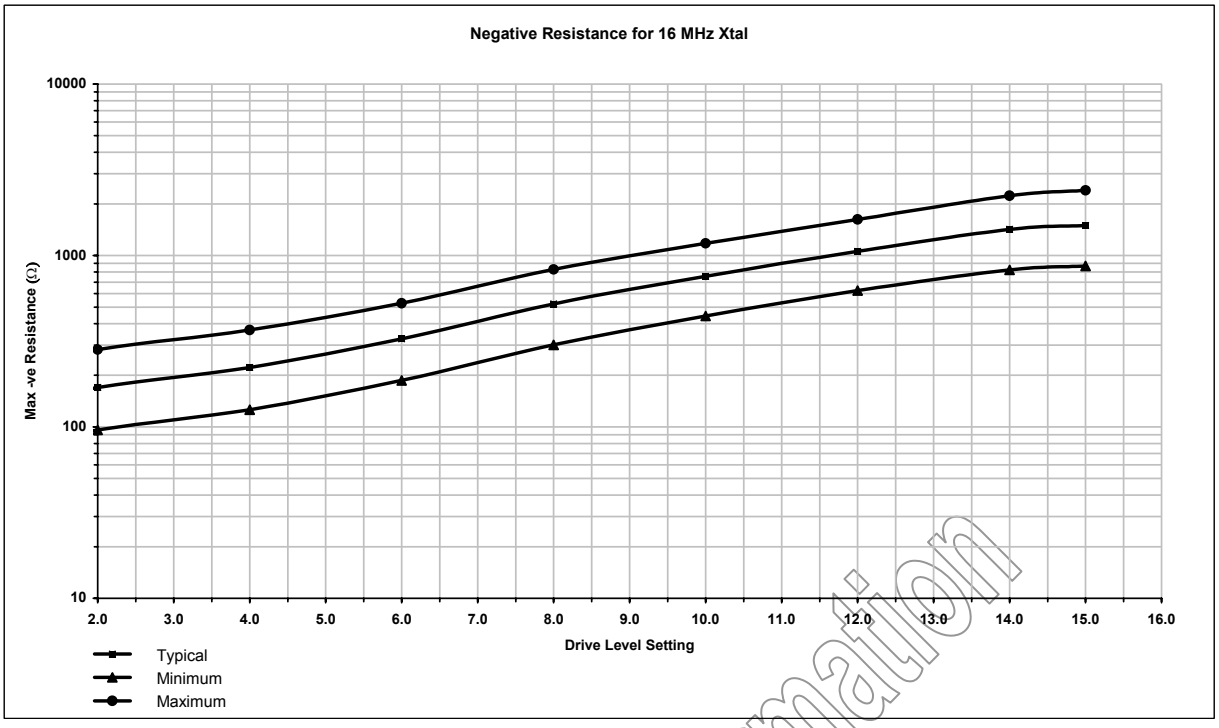


Figure 8.17: Crystal Driver Negative Resistance as a Function of Drive Level Setting

Crystal parameters:

Crystal frequency 16MHz (Please refer to your software build release note for frequencies supported);

Crystal C_0 = 0.75pF

Circuit parameters:

C_{trim} = 8pF, maximum value

C_{t1},C_{t2} = 5pF (3.9pF plus 1.1 pF stray)

(Crystal total load capacitance 8.5pF)

Note:

This is for a specific crystal and load capacitance.

8.4 UART Interface (BC313141A only)

BlueCore3-ROM CSP Universal Asynchronous Receiver Transmitter (UART) interface provides a simple mechanism for communicating with other serial devices using the RS232 standard (1).

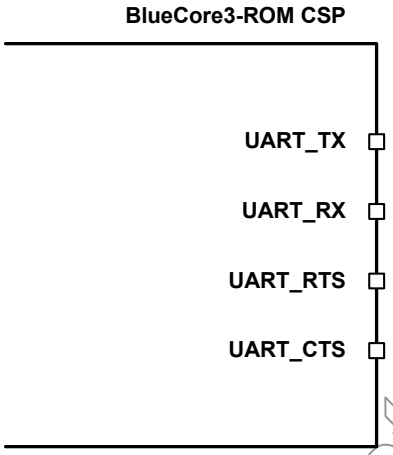


Figure 8.18: Universal Asynchronous Receiver

Four signals are used to implement the UART function, as shown in Figure 8.18. When BlueCore3-ROM CSP is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators. All UART connections are implemented using CMOS technology and have signalling levels of 0V and VDD_PADS.

UART configuration parameters, such as Baud rate and packet format, are set using BlueCore3-ROM CSP software.

Notes:

In order to communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

(1) Uses RS232 protocol but voltage levels are 0V to VDD_USB, (requires external RS232 transceiver chip)

Parameter		Possible Values
Baud Rate	Minimum	1200 Baud (≤2%Error)
		9600 Baud (≤1%Error)
	Maximum	1.5MBaud (≤1%Error)
Flow Control		RTS/CTS or None
Parity		None, Odd or Even
Number of Stop Bits		1 or 2
Bits per channel		8

Table 8.6: Possible UART Settings

The UART interface is capable of resetting BlueCore3-ROM CSP upon reception of a break signal. A Break is identified by a continuous logic low (0V) on the UART_RX terminal, as shown in Figure 8.19. If t_{BRK} is longer than the value, defined by the PS Key PSKEY_HOST_IO_UART_RESET_TIMEOUT, (0x1a4), a reset will occur. This feature allows a host to initialise the system to a known state. BlueCore3-ROM CSP can also emit a Break character that may be used to wake the Host.

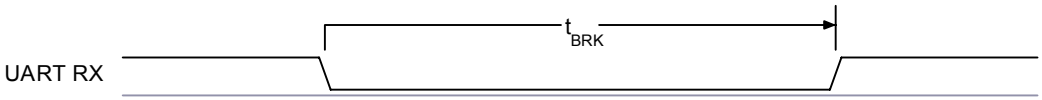


Figure 8.19: Break Signal

Note:

The DFU boot loader must be loaded into the Flash device before the UART or USB interfaces can be used. This initial flash programming can be done via the SPI.

Table 8.7 shows a list of commonly used Baud rates and their associated values for the Persistent Store Key PSKEY_UART_BAUD_RATE (0x204). There is no requirement to use these standard values. Any Baud rate within the supported range can be set in the Persistent Store Key according to the formula in Equation 8.7.

$$\text{Baud Rate} = \frac{\text{PSKEY\_UART\_BAUD\_RATE}}{0.004096}$$

Equation 8.7: Baud Rate

Baud Rate	Persistent Store Value		Error
	Hex	Dec	
1200	0x0005	5	1.73%
2400	0x000a	10	1.73%
4800	0x0014	20	1.73%
9600	0x0027	39	-0.82%
19200	0x004f	79	0.45%
38400	0x009d	157	-0.18%
57600	0x00ec	236	0.03%
76800	0x013b	315	0.14%
115200	0x01d8	472	0.03%
230400	0x03b0	944	0.03%
460800	0x075f	1887	-0.02%
921600	0x0ebf	3775	0.00%
1382400	0x161e	5662	-0.01%

Table 8.7: Standard Baud Rates

8.4.1 UART Bypass

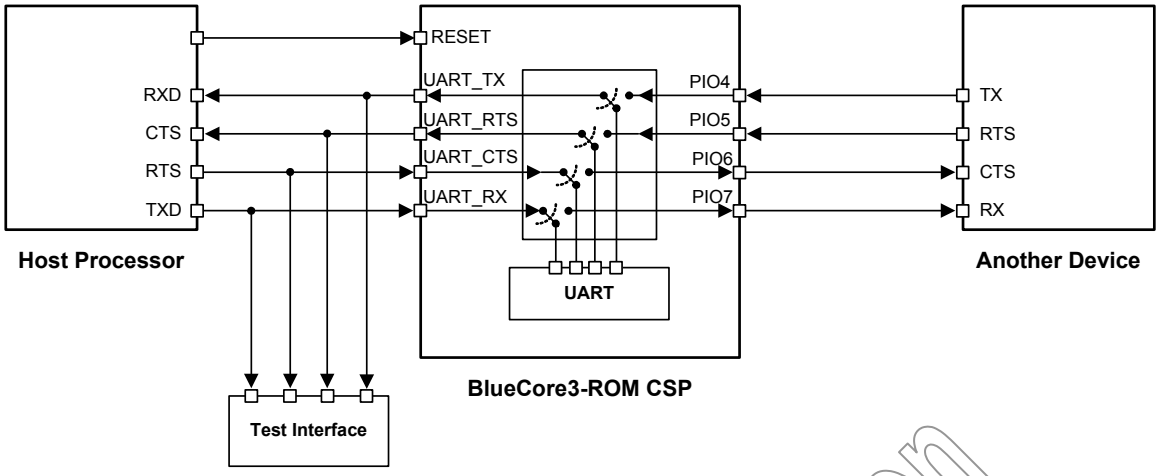


Figure 8.20: UART Bypass Architecture

8.4.2 UART Configuration while RESET is Active

The UART interface for BlueCore3-ROM CSP while the chip is being held in reset is tri-state. This will allow the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tri-state when BlueCore3-ROM CSP reset is de-asserted and the firmware begins to run.

8.4.3 UART Bypass Mode

Alternatively, for devices that do not tri-state the UART bus, the UART bypass mode on BlueCore3-ROM CSP can be used. The default state of BlueCore3-ROM CSP after reset is de-asserted is for the host UART bus to be connected to the BlueCore3-ROM CSP UART, thereby allowing communication to BlueCore3-ROM CSP via the UART.

In order to apply the UART bypass mode, a BCCMD command will be issued to BlueCore3-ROM CSP upon this, it will switch the bypass to PIO[7:4] as shown in Figure 8.20. Once the bypass mode has been invoked, BlueCore3-ROM CSP will enter the deep sleep state indefinitely.

In order to re-establish communication with BlueCore3-ROM CSP, the chip must be reset so that the default configuration takes affect.

It is important for the host to ensure a clean Bluetooth disconnection of any active links before the bypass mode is invoked. Therefore it is not possible to have active Bluetooth links while operating the bypass mode.

8.4.4 Current Consumption in UART Bypass Mode

The current consumption for a device in UART Bypass Mode is equal to the values quoted for a device in standby mode.

8.5 USB Interface (BC313143A only)

BlueCore3-ROM CSP devices contain a full speed (12Mbits/s) USB interface that is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented can behave as specified in the USB section of the Bluetooth specification v1.2 or alternatively can appear as a set of endpoints appropriate to USB audio devices such as speakers.

As USB is a Master/Slave oriented system (in common with other USB peripherals), BlueCore3-ROM CSP only supports USB Slave operation.

8.5.1 USB Data Connections

The USB data lines emerge as pins USB_DP and USB_DN. These terminals are connected to the internal USB I/O buffers of the BlueCore3-ROM CSP and therefore have a low output impedance. To match the connection to the characteristic impedance of the USB cable, resistors must be placed in series with USB_DP / USB_DN and the cable.

8.5.2 USB Pull-Up Resistor

BlueCore3-ROM CSP features an internal USB pull-up resistor. This pulls the USB_DP pin weakly high when BlueCore3-ROM CSP is ready to enumerate. It signals to the PC that it is a full speed (12Mbit/s) USB device.

The USB internal pull-up is implemented as a current source, and is compliant with Section 7.1.5 of the USB specification v1.2. The internal pull-up pulls USB_DP high to at least 2.8V when loaded with a 15kΩ ±5% pull-down resistor (in the hub/host) when VDD_PADS=3.1V. This presents a Thevenin resistance to the host of at least 900Ω. Alternatively, an external 1.5kΩ pull-up resistor can be placed between a PIO line and D+ on the USB cable. The firmware must be alerted to which mode is used by setting PS Key PSKEY_USB_PIO_PULLUP appropriately. The default setting uses the internal pull-up resistor.

8.5.3 Power Supply

The USB specification dictates that the minimum output high voltage for USB data lines is 2.8V. To safely meet the USB specification, the voltage on the VDD_USB supply terminals must be an absolute minimum of 3.1V. CSR recommends 3.3V for optimal USB signal quality.

8.5.4 Self Powered Mode

In self powered mode, the circuit is powered from its own power supply and not from the VBUS (5V) line of the USB cable. It draws only a small leakage current (below 0.5mA) from VBUS on the USB cable. This is the easier mode for which to design for, as the design is not limited by the power that can be drawn from the USB hub or root port. However, it requires that VBUS be connected to BlueCore3-ROM CSP via a resistor network (R_{vb1} and R_{vb2}), so BlueCore3-ROM CSP can detect when VBUS is powered up. BlueCore3-ROM CSP will not pull USB_DP high when VBUS is off.

Self powered USB designs (powered from a battery or PSU) must ensure that a PIO line is allocated for USB pull-up purposes. A 1.5KΩ 5% pull-up resistor between USB_DP and the selected PIO line should be fitted to the design. Failure to fit this resistor may result in the design failing to be USB compliant in self powered mode. The internal pull-up in BlueCore is only suitable for bus powered USB devices i.e. dongles.

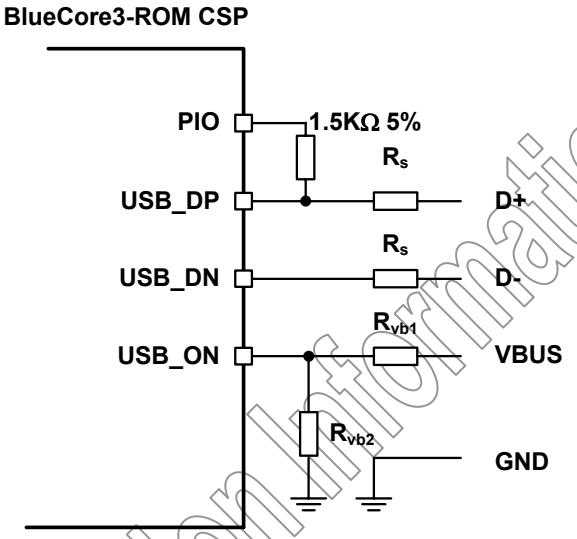


Figure 8.21: USB Connections for Self Powered Mode

The terminal marked USB_ON can be any free PIO pin. The PIO pin selected must be registered by setting PSKEY_USB_PIO_VBUS to the corresponding pin number.

8.5.5 Bus Powered Mode

In bus powered mode the application circuit draws its current from the 5V VBUS supply on the USB cable. BlueCore3-ROM CSP negotiates with the PC during the USB enumeration stage about how much current it is allowed to consume.

For Class 2 Bluetooth applications, CSR recommends that the regulator used to derive 3.3V from VBUS is rated at 100mA average current and should be able to handle peaks of 120mA without foldback or limiting. In bus powered mode, BlueCore3-ROM CSP requests 100mA during enumeration.

When selecting a regulator, be aware that VBUS may go as low as 4.4V. The inrush current (when charging reservoir and supply decoupling capacitors) is limited by the USB specification (see USB specification v1.1, Section 7.2.4.1). Some applications may require soft start circuitry to limit inrush current if more than 10μF is present between VBUS and GND.

The 5V VBUS line emerging from a PC is often electrically noisy. As well as regulation down to 3.3V and 1.8V, applications should include careful filtering of the 5V line to attenuate noise that is above the voltage regulator bandwidth. Excessive noise on the 1.8V supply to the analogue supply pins of BlueCore3-ROM CSP will result in reduced receive sensitivity and a distorted RF transmit signal.

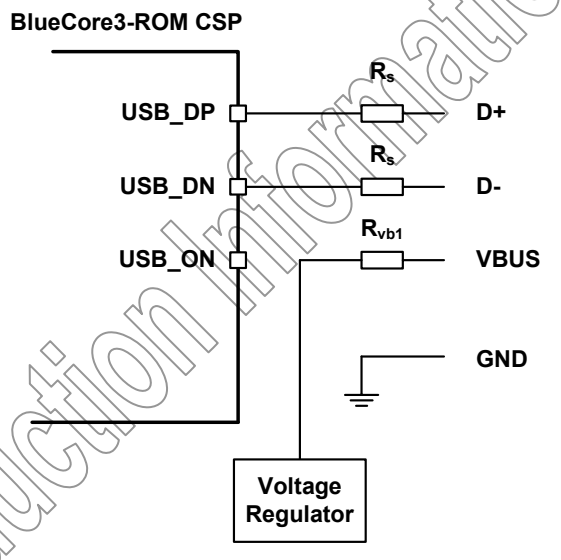


Figure 8.22: USB Connections for Bus Powered Mode

Note:

USB_ON is shared with BlueCore3-ROM CSP PIO terminals

Identifier	Value	Function
R_s	27Ω nominal	Impedance matching to USB cable
R_{vb1}	22kΩ 5%	VBUS ON sense divider
R_{vb2}	47kΩ 5%	VBUS ON sense divider

Table 8.8: USB Interface Component Values

8.5.6 Suspend Current

All USB devices must permit the USB controller to place them in a USB Suspend mode. While in USB Suspend, bus powered devices must not draw more than 0.5mA from USB VBUS (self powered devices may draw more than 0.5mA from their own supply). This current draw requirement prevents operation of the radio by bus powered devices during USB Suspend.

The voltage regulator circuit itself should draw only a small quiescent current (typically less than 100μA) to ensure adherence to the suspend current requirement of the USB specification. This is not normally a problem with modern regulators. Ensure that external LEDs and/or amplifiers can be turned off by BlueCore3-ROM CSP. The entire circuit must be able to enter the suspend mode. (For more details on USB Suspend, see separate CSR documentation).

8.5.7 Detach and Wake_Up Signalling

BlueCore3-ROM CSP can provide out-of-band signalling to a host controller by using the control lines called 'USB_DETACH' and 'USB_WAKE_UP'. These are outside the USB specification (no wires exist for them inside the USB cable), but can be useful when embedding BlueCore3-ROM CSP into a circuit where no external USB is visible to the user. Both control lines are shared with PIO pins and can be assigned to any PIO pin by setting the PS Keys PSKEY_USB_PIO_DETACH and PSKEY_USB_PIO_WAKEUP to the selected PIO number.

USB_DETACH is an input which, when asserted high, causes BlueCore3-ROM CSP to put USB_DN and USB_DP in a high impedance state and turned off the pull-up resistor on DP. This detaches the device from the bus and is logically equivalent to unplugging the device. When USB_DETACH is taken low, BlueCore3-ROM CSP will connect back to USB and await enumeration by the USB host.

USB_WAKE_UP is an active high output (used only when USB_DETACH is active) to wake up the host and allow USB communication to recommence. It replaces the function of the software USB WAKE_UP message (which runs over the USB cable), and cannot be sent while BlueCore3-ROM CSP is effectively disconnected from the bus.

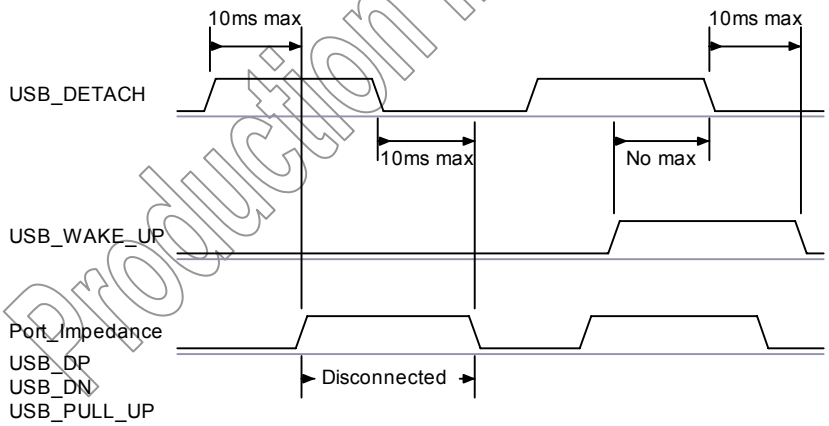


Figure 8.23: USB_DETACH and USB_WAKE_UP Signal

8.5.8 USB Driver

A USB Bluetooth device driver is required to provide a software interface between BlueCore3-ROM CSP and Bluetooth software running on the host computer. Suitable drivers are available from www.csrsupport.com.

8.5.9 USB 1.1 Compliance

BlueCore3-ROM CSP is qualified to the USB specification v1.1, details of which are available from http://www.usb.org. The specification contains valuable information on aspects such as PCB track impedance, supply inrush current and product labelling.

Although BlueCore3-ROM CSP meets the USB specification, CSR cannot guarantee that an application circuit designed around the chip is USB compliant. The choice of application circuit, component choice and PCB layout all affect USB signal quality and electrical characteristics. The information in this document is intended as a guide and should be read in association with the USB specification, with particular attention being given to Chapter 7. Independent USB qualification must be sought before an application is deemed USB compliant and can bear the USB logo. Such qualification can be obtained from a USB plugfest or from an independent USB test house.

Terminals USB_DP and USB_DN adhere to the USB specification 2.0 (Chapter 7) electrical requirements.

8.5.10 USB 2.0 Compatibility

BlueCore3-ROM CSP is compatible with USB v2.0 host controllers; under these circumstances the two ends agree the mutually acceptable rate of 12Mbits/s according to the USB v2.0 specification.

8.6 Serial Peripheral Interface

BlueCore3-ROM CSP uses 16-bit data and 16-bit address serial peripheral interface, where transactions may occur when the internal processor is running or is stopped. This section details the considerations required when interfacing to BlueCore3-ROM CSP via the four dedicated serial peripheral interface terminals. Data may be written or read one word at a time or the auto increment feature may be used to access blocks.

8.6.1 Instruction Cycle

The BlueCore3-ROM CSP is the slave and receives commands on SPI_MOSI and outputs data on SPI_MISO. The instruction cycle for a SPI transaction is shown in Table 8.9.

1	Reset the SPI interface	Hold SPI_CSB high for two SPI_CLK cycles
2	Write the command word	Take SPI_CSB low and clock in the 8 bit command
3	Write the address	Clock in the 16-bit address word
4	Write or read data words	Clock in or out 16-bit data word(s)
5	Termination	Take SPI_CSB high

Table 8.9: Instruction Cycle for an SPI Transaction

With the exception of reset, SPI_CSB must be held low during the transaction. Data on SPI_MOSI is clocked into the BlueCore3-ROM CSP on the rising edge of the clock line SPI_CLK. When reading, BlueCore3-ROM CSP will reply to the master on SPI_MISO with the data changing on the falling edge of the SPI_CLK. The master provides the clock on SPI_CLK. The transaction is terminated by taking SPI_CSB high.

Sending a command word and the address of a register for every time it is to be read or written is a significant overhead, especially when large amounts of data are to be transferred. To overcome this BlueCore3-ROM CSP offers increased data transfer efficiency via an auto increment operation. To invoke auto increment, SPI_CSB is kept low, which auto increments the address, while providing an extra 16 clock cycles for each extra word to be written or read.

8.6.2 Writing to BlueCore3-ROM CSP

To write to BlueCore3-ROM CSP, the 8-bit write command (00000010) is sent first (C[7:0]) followed by a 16-bit address (A[15:0]). The next 16-bits (D[15:0]) clocked in on SPI_MOSI are written to the location set by the address (A). Thereafter for each subsequent 16-bits clocked in, the address (A) is incremented and the data written to consecutive locations until the transaction terminates when SPI_CSB is taken high.

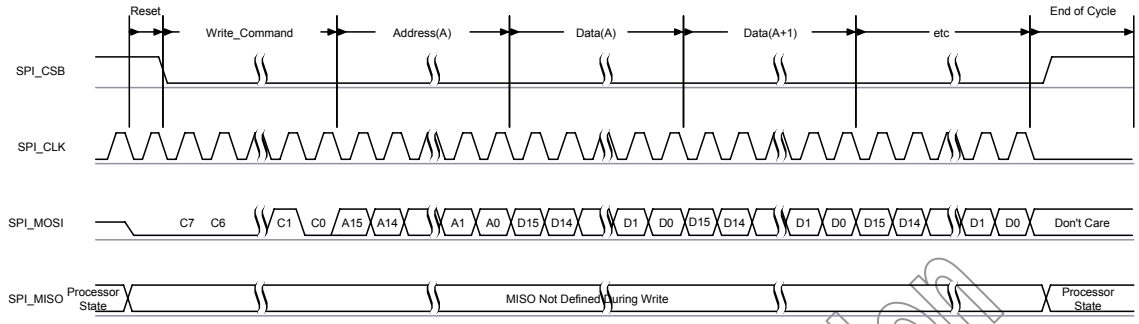


Figure 8.24: Write Operation

8.6.3 Reading from BlueCore3-ROM CSP

Reading from BlueCore3-ROM CSP is similar to writing to it. An 8-bit read command (00000011) is sent first (C[7:0]), followed by the address of the location to be read (A[15:0]). BlueCore3-ROM CSP then outputs on SPI_MISO a check word during T[15:0] followed by the 16-bit contents of the addressed location during bits D[15:0].

The check word is composed of {command, address [15:8]}. The check word may be used to confirm a read operation to a memory location. This overcomes the problems encountered with typical serial peripheral interface slaves, whereby it is impossible to determine whether the data returned by a read operation is valid data or the result of the slave device not responding.

If SPI_CSB is kept low, data from consecutive locations is read out on SPI_MISO for each subsequent 16 clocks, until the transaction terminates when SPI_CSB is taken high.

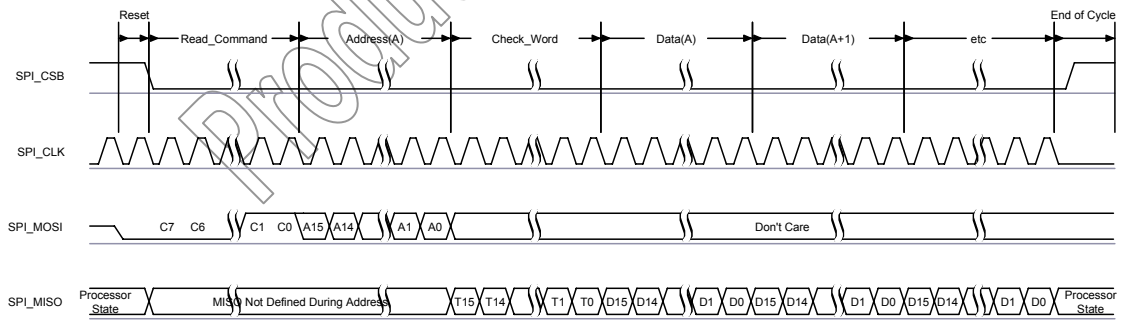


Figure 8.25: Read Operation

8.6.4 Multi Slave Operation

BlueCore3-ROM CSP should not be connected in a multi slave arrangement by simple parallel connection of slave MISO lines. When BlueCore3-ROM CSP is deselected (SPI_CSB = 1), the SPI_MISO line does not float, instead, BlueCore3-ROM CSP outputs 0 if the processor is running or 1 if it is stopped.

8.7 PCM CODEC Interface

Pulse Code Modulation (PCM) is a standard method used to digitise human voice patterns for transmission over digital communication channels. Through its PCM interface, BlueCore3-ROM CSP has hardware support for continual transmission and reception of PCM data, thus reducing processor overhead for wireless headset applications. BlueCore3-ROM CSP offers a bi directional digital audio interface that routes directly into the baseband layer of the on chip firmware. It does not pass through the HCI protocol layer.

Hardware on BlueCore3-ROM CSP allows the data to be sent to and received from a SCO connection.

Up to three SCO connections can be supported by the PCM interface at any one time(1).

BlueCore3-ROM CSP can operate as the PCM interface Master generating an output clock of 128, 256 or 512kHz. When configured as PCM interface slave it can operate with an input clock up to 2048kHz. BlueCore3-ROM CSP is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13 or 16-bit linear, 8-bit μ-law or A-law companded sample formats at 8ksamples/s and can receive and transmit on any selection of three of the first four slots following PCM_SYNC. The PCM configuration options are enabled by setting the PS Key PS KEY_PCM_CONFIG (0x1b3).

BlueCore3-ROM CSP interfaces directly to PCM audio devices including the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 four channel A-law and μ-law CODEC
- Motorola MC145481 8-bit A-law and μ-law CODEC
- Motorola MC145483 13-bit linear CODEC
- STW 5093 and 5094 14-bit linear CODECs
- BlueCore3-ROM CSP is also compatible with the Motorola SSI™ interface

Note:

(1) Subject to firmware support, contact CSR for current status.

8.7.1 PCM Interface Master/Slave

When configured as the Master of the PCM interface, BlueCore3-ROM CSP generates PCM_CLK and PCM_SYNC.

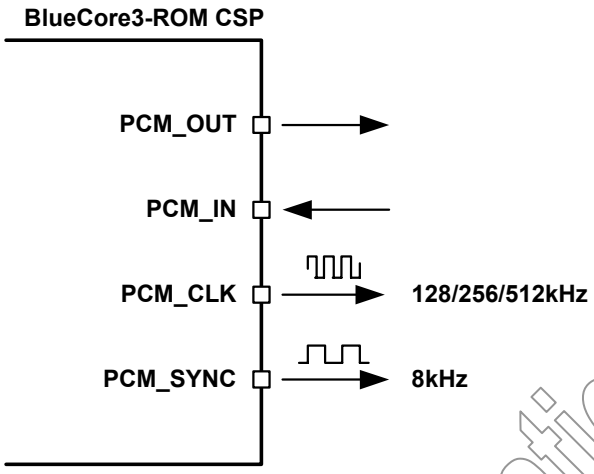


Figure 8.26: BlueCore3-ROM CSP as PCM Interface Master

When configured as the Slave of the PCM interface, BlueCore3-ROM accepts PCM_CLK rates up to 2048kHz.

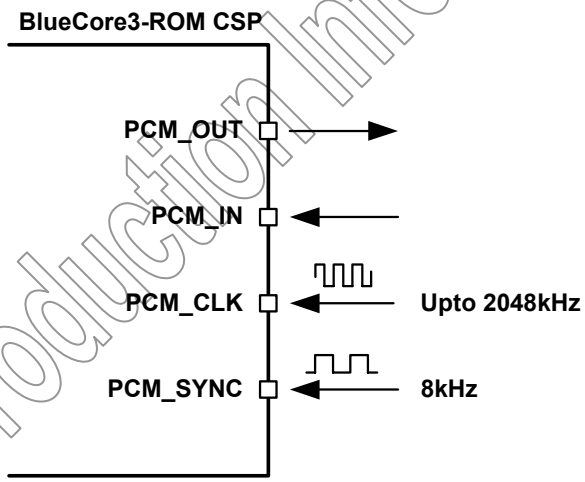


Figure 8.27: BlueCore3-ROM CSP as PCM Interface Slave

8.7.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When BlueCore3-ROM CSP is configured as PCM Master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8-bits long. When BlueCore3-ROM CSP is configured as PCM Slave, PCM_SYNC may be from two consecutive falling edges of PCM_CLK to half the PCM_SYNC rate, i.e. 62.5µs long.

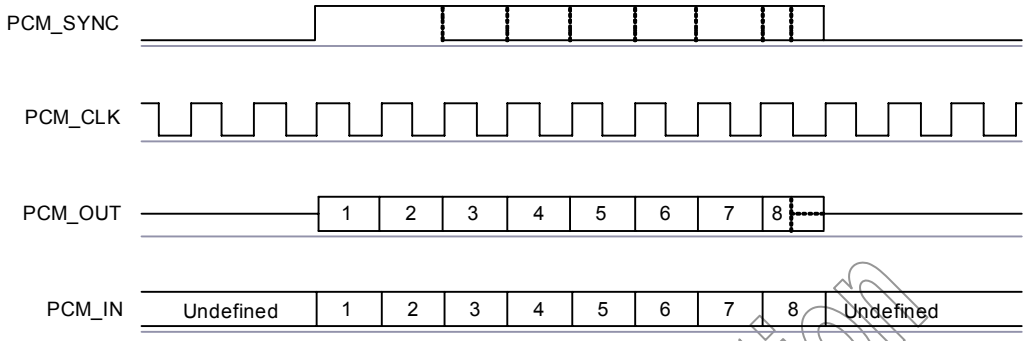


Figure 8.28: Long Frame Sync (Shown with 8-bit Companded Sample)

BlueCore3-ROM CSP samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

8.7.3 Short Frame Sync

In Short Frame Sync the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

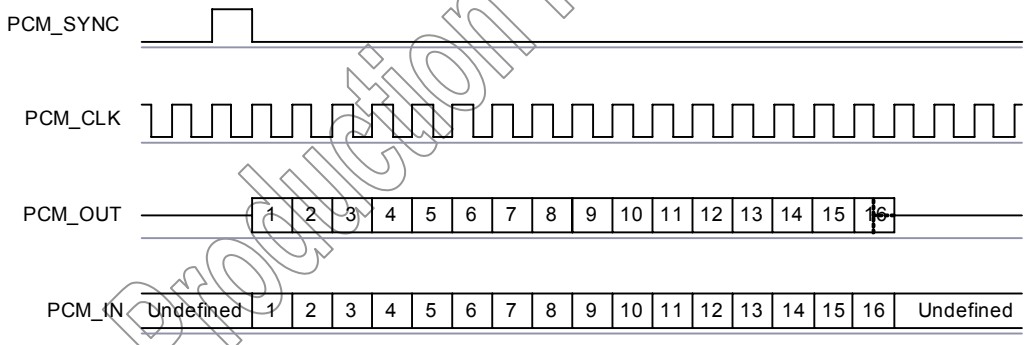


Figure 8.29: Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, BlueCore3-ROM CSP samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

8.7.4 Multi Slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots.

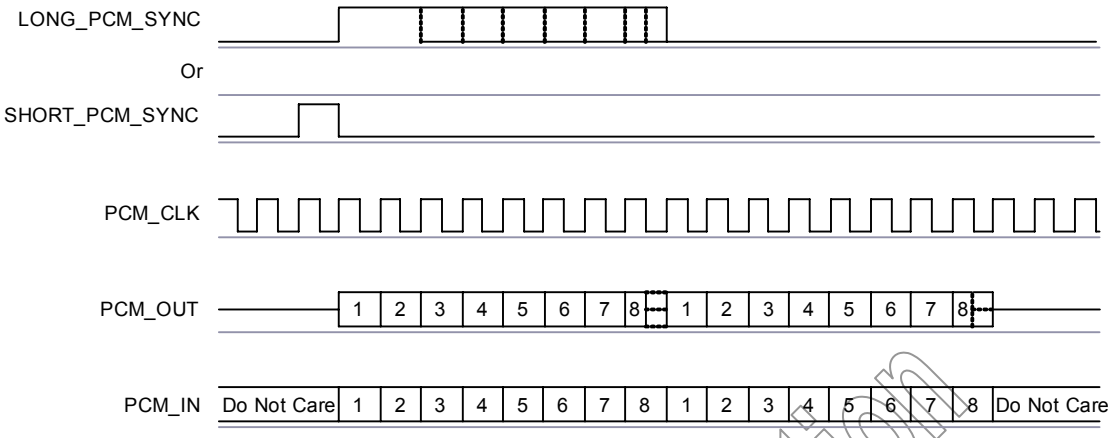


Figure 8.30: Multi Slot Operation with Two Slots and 8-bit Companded Samples

8.7.5 GCI Interface

BlueCore3-ROM CSP is compatible with the General Circuit Interface, a standard synchronous 2B+D ISDN timing interface. The two 64Kbps B channels can be accessed when this mode is configured.

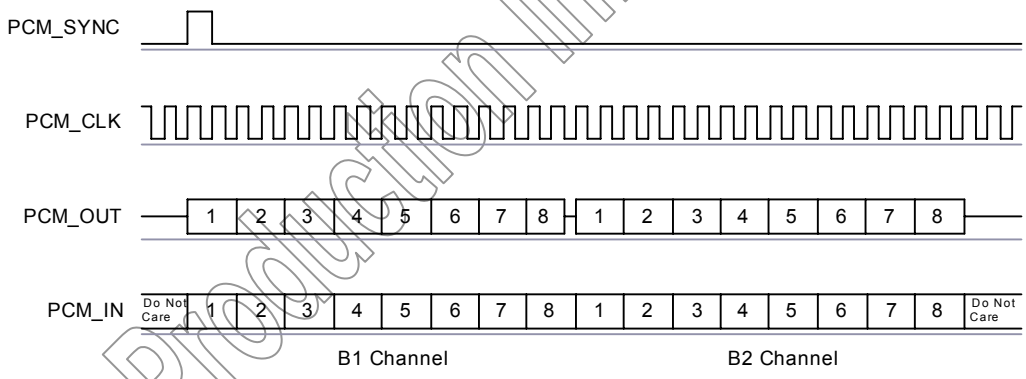


Figure 8.31: GCI Interface

The start of frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz. With BlueCore3-ROM CSP in Slave mode, the frequency of PCM_CLK can be up to 4.096MHz.

8.7.6 Slots and Sample Formats

BlueCore3-ROM CSP can receive and transmit on any selection of the first four slots following each sync pulse. Slot durations can be either 8 or 16 clock cycles. Duration's of 8 clock cycles may only be used with 8-bit sample formats. Durations of 16 clocks may be used with 8, 13 or 16-bit sample formats.

BlueCore3-ROM CSP supports 13-bit linear, 16-bit linear and 8-bit μ-law or A-law sample formats. The sample rate is 8ksamples/s. The bit order may be little or big endian. When 16-bit slots are used, the 3 or 8 unused bits in each slot may be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola CODECs.

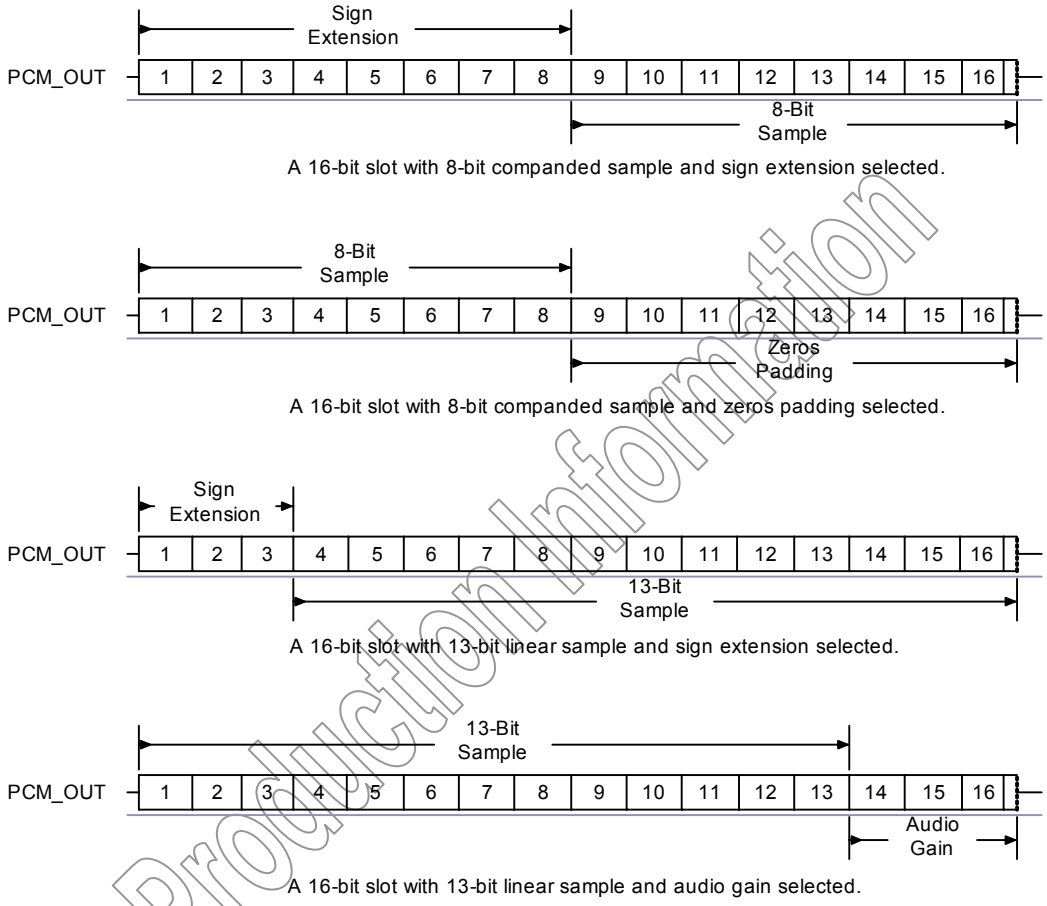


Figure 8.32: 16-Bit Slot Length and Sample Formats

8.7.7 Additional Features

BlueCore3-ROM CSP has a mute facility that forces PCM_OUT to be 0. In Master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running which some CODECS use to control power down.

8.7.8 PCM Timing Information

Symbol	Parameter		Min	Typ	Max	Unit
f_{mclk}	PCM_CLK frequency	4MHz DDS generation. Selection of frequency is programmable, see Table 8.12	-	128 256 512	-	kHz
		48MHz DDS generation. Selection of frequency is programmable, see Table 8.13 and Section 8.7.10	2.9		-	kHz
-	PCM_SYNC frequency		-	8		kHz
t_{mclkh} (1)	PCM_CLK high	4MHz DDS generation	980	-	-	ns
t_{mclkl} (1)	PCM_CLK low	4MHz DDS generation	730	-		ns
-	PCM_CLK jitter	48MHz DDS generation			21	ns pk-pk
$t_{dmclksynch}$	Delay time from PCM_CLK high to PCM_SYNC high		-	-	20	ns
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT		-	-	20	ns
$t_{dmclklsyncl}$	Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only)		-	-	20	ns
$t_{dmclkhsyncl}$	Delay time from PCM_CLK high to PCM_SYNC low		-	-	20	ns
$t_{dmclklpoutz}$	Delay time from PCM_CLK low to PCM_OUT high impedance		-	-	20	ns
$t_{dmclkhpoutz}$	Delay time from PCM_CLK high to PCM_OUT high impedance		-	-	20	ns
$t_{supinclkl}$	Set-up time for PCM_IN valid to PCM_CLK low		30	-	-	ns
$t_{hpinclkl}$	Hold time for PCM_CLK low to PCM_IN invalid		10	-	-	ns

Table 8.10: PCM Master Timing

Note:

(1) Assumes normal system clock operation. Figures will vary during low power modes, when system clock speeds are reduced.

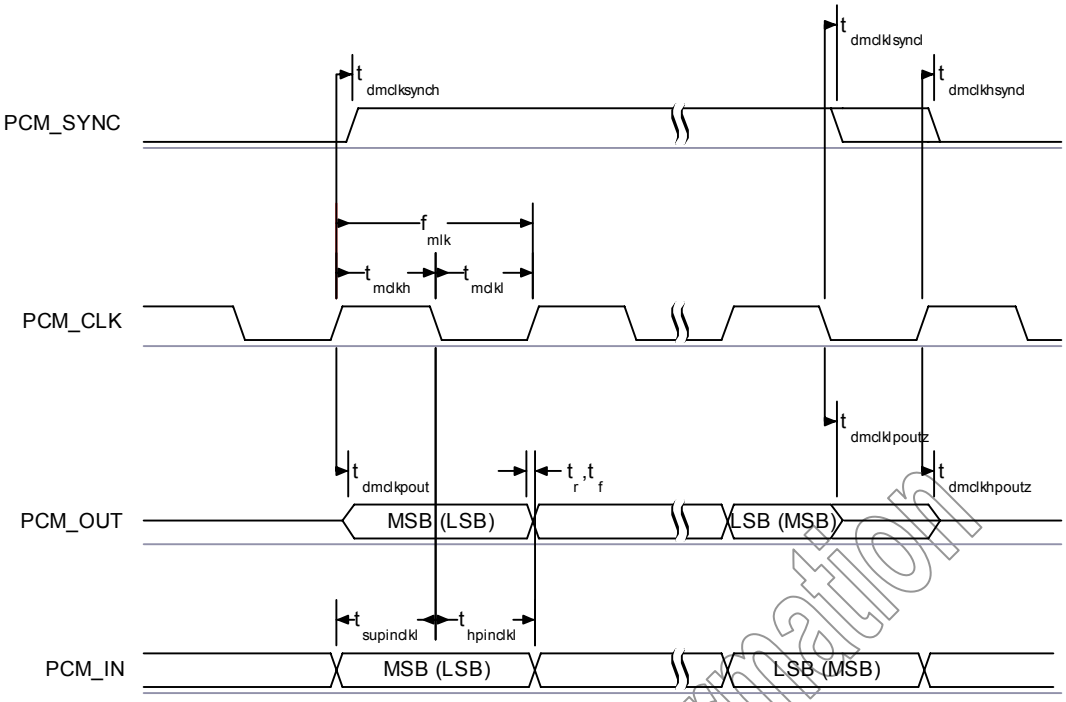


Figure 8.33: PCM Master Timing Long Frame Sync

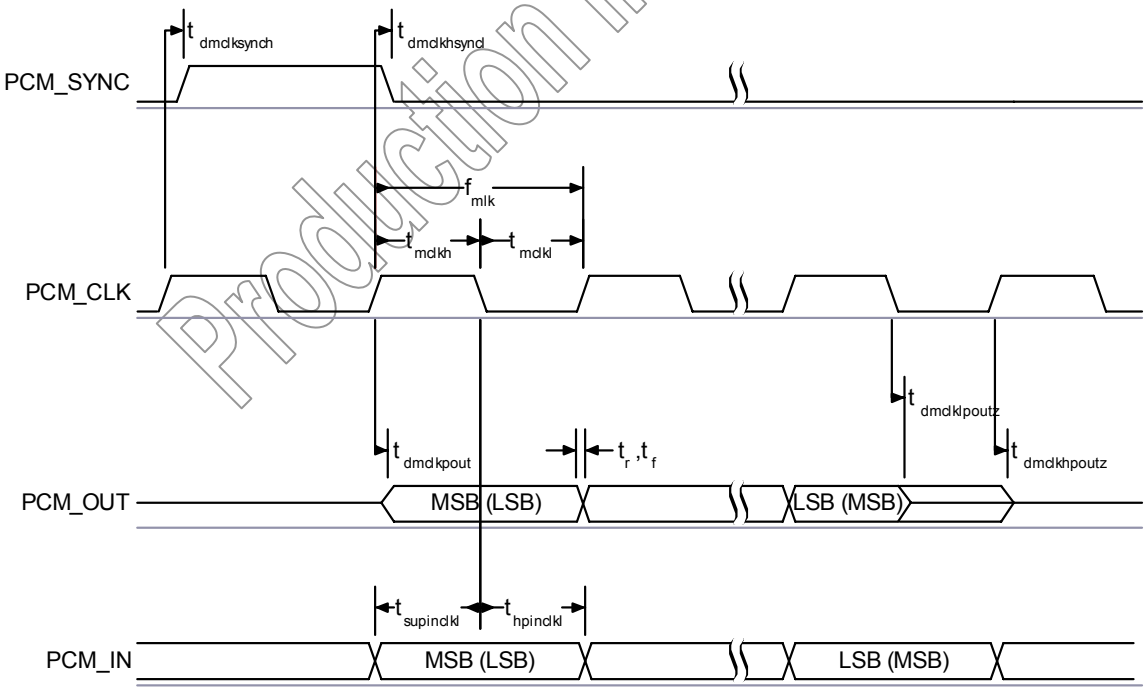


Figure 8.34: PCM Master Timing Short Frame Sync

8.7.9 PCM Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
f_{sclk}	PCM clock frequency (Slave mode: input)	64	-	2048	kHz
f_{sclk}	PCM clock frequency (GCI mode)	128	-	4096	kHz
t_{sclkl}	PCM_CLK low time	200	-	-	ns
t_{sclkh}	PCM_CLK high time	200	-	-	ns
$t_{hsclksynch}$	Hold time from PCM_CLK low to PCM_SYNC high	30	-	-	ns
$t_{susclksynch}$	Set-up time for PCM_SYNC high to PCM_CLK low	30	-	-	ns
t_{dpout}	Delay time from PCM_SYNC or PCM_CLK whichever is later, to valid PCM_OUT data (Long Frame Sync only)	-	-	20	ns
$t_{dsclkhpout}$	Delay time from CLK high to PCM_OUT valid data	-	-	20	ns
t_{dpoutz}	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
$t_{supinsclkl}$	Set-up time for PCM_IN valid to CLK low	30	-	-	ns
$t_{hpinsclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	30	-		ns

Table 8.11: PCM Slave Timing

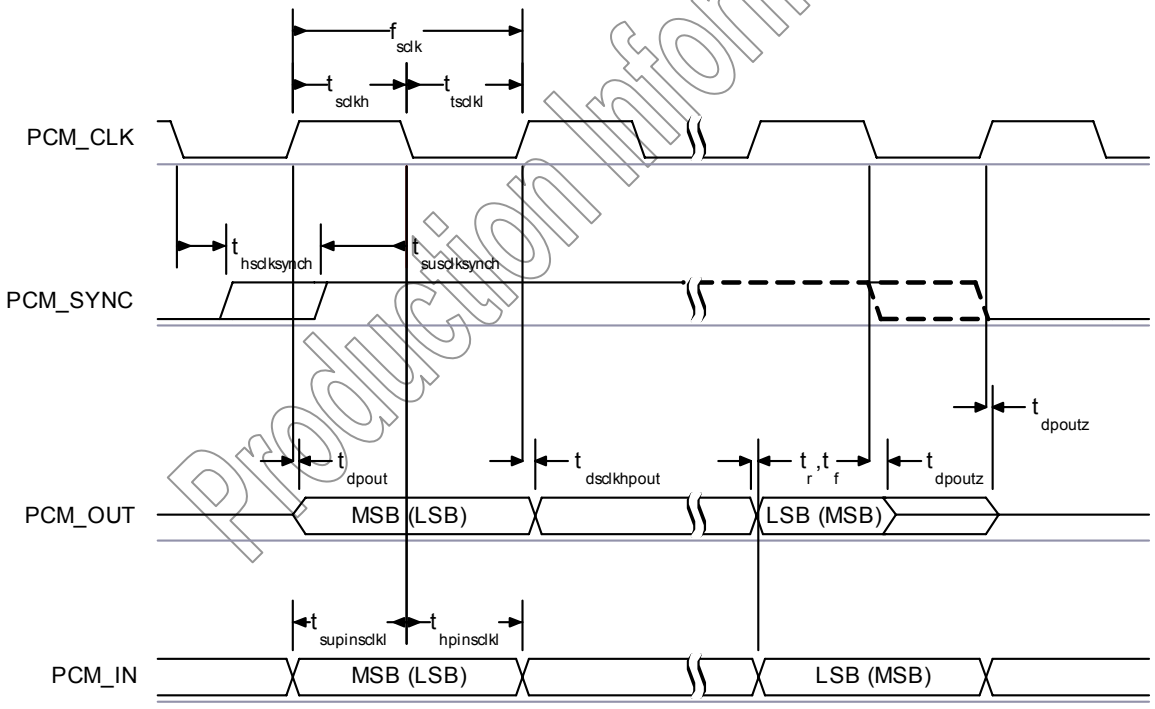


Figure 8.35: PCM Slave Timing Long Frame Sync

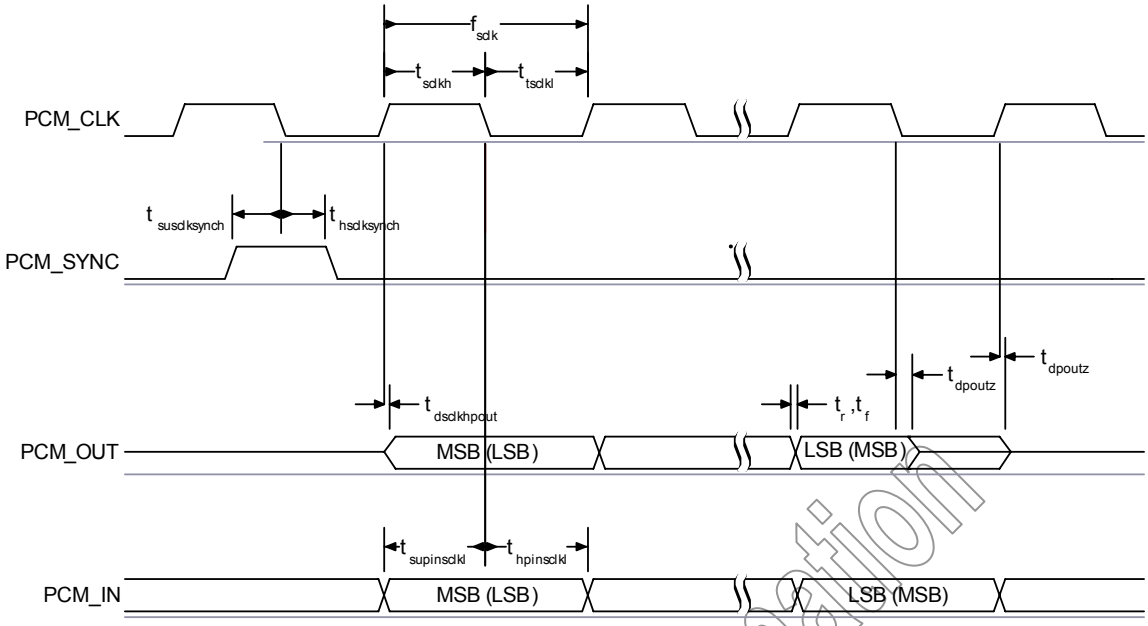


Figure 8.36: PCM Slave Timing Short Frame Sync

8.7.10 PCM_CLK and PCM_SYNC Generation

BlueCore3-ROM CSP has two methods of generating PCM_CLK and PCM_SYNC in master mode. The first is generating these signals by Direct Digital Synthesis (DDS) from BlueCore3-ROM CSP internal 4MHz clock (which is used in BlueCore3-ROM CSP). Using this mode limits PCM_CLK to 128, 256 or 512kHz and PCM_SYNC to 8kHz. The second is generating PCM_CLK and PCM_SYNC by DDS from an internal 48MHz clock which allows a greater range of frequencies to be generated with low jitter but consumes more power. This second method is selected by setting bit '48M_PCM_CLK_GEN_EN' in PSKEY_PCM_CONFIG32.

Note:

The bit 'SLAVE_MODE_EN' should also be set. When in this mode and with long frame sync, the length of PCM_SYNC can be either 8 or 16 cycles of PCM_CLK, determined by 'LONG_LENGTH_SYNC_EN' in PSKEY_PCM_CONFIG32.

The Equation 8.8 describes PCM_CLK frequency when being generated using the internal 48MHz clock:

$$f = \frac{CNT\_RATE}{CNT\_LIMIT} \times 24MHz$$

Equation 8.8: PCM_CLK Frequency When Being Generated Using the Internal 48MHz clock

The frequency of PCM_SYNC relative to PCM_CLK can be set using following equation:

$$f = \frac{PCM\_CLK}{SYNC\_LIMIT \times 8}$$

Equation 8.9: PCM_SYNC Frequency Relative to PCM_CLK

CNT_RATE, CNT_LIMIT and SYNC_LIMIT are set using PSKEY_PCM_LOW_JITTER_CONFIG. As an example, to generate PCM_CLK at 512kHz with PCM_SYNC at 8kHz, set PSKEY_PCM_LOW_JITTER_CONFIG to 0x08080177.

8.7.11 PCM Configuration

The PCM configuration is set using two PS Keys, PSKEY_PCM_CONFIG32 and PSKEY_PCM_LOW_JITTER_CONFIG. The following tables detail these PS Keys. PSKEY_PCM_CONFIG32. The default for this key is 0x00800000 i.e. first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tristating of PCM_OUT. PSKEY_PCM_LOW_JITTER_CONFIG is described in Table 8.13.

Name	Bit Position	Description
-	0	Set to 0.
SLAVE_MODE_EN	1	0 selects Master mode with internal generation of PCM_CLK and PCM_SYNC. 1 selects Slave mode requiring externally generated PCM_CLK and PCM_SYNC. This should be set to 1 if 48M_PCM_CLK_GEN_EN (bit 11) is set.
SHORT_SYNC_EN	2	0 selects long frame sync (rising edge indicates start of frame), 1 selects short frame sync (falling edge indicates start of frame).
-	3	Set to 0.
SIGN_EXTEND_EN	4	0 selects padding of 8 or 13-bit voice sample into a 16-bit slot by inserting extra LSBs, 1 selects sign extension. When padding is selected with 13-bit voice sample, the 3 padding bits are the audio gain setting; with 8-bit samples the 8 padding bits are zeroes.
LSB_FIRST_EN	5	0 transmits and receives voice samples MSB first, 1 uses LSB first.
TX_TRISTATE_EN	6	0 drives PCM_OUT continuously, 1 tri-states PCM_OUT immediately after the falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is not active.
TX_TRISTATE_RISING_EDGE_EN	7	0 tristates PCM_OUT immediately after the falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is also not active. 1 tristates PCM_OUT after the rising edge of PCM_CLK.
SYNC_SUPPRESS_EN	8	0 enables PCM_SYNC output when master, 1 suppresses PCM_SYNC whilst keeping PCM_CLK running. Some CODECS utilise this to enter a low power state.
GCI_MODE_EN	9	1 enables GCI mode.
MUTE_EN	10	1 forces PCM_OUT to 0.
48M_PCM_CLK_GEN_EN	11	0 sets PCM_CLK and PCM_SYNC generation via DDS from internal 4 MHz clock, as for BlueCore3-ROM CSP. 1 sets PCM_CLK and PCM_SYNC generation via DDS from internal 48 MHz clock.
LONG_LENGTH_SYNC_EN	12	0 sets PCM_SYNC length to 8 PCM_CLK cycles and 1 sets length to 16 PCM_CLK cycles. Only applies for long frame sync and with 48M_PCM_CLK_GEN_EN set to 1.
-	[20:16]	Set to 0b00000.
MASTER_CLK_RATE	[22:21]	Selects 128 (0b01), 256 (0b00), 512 (0b10) kHz PCM_CLK frequency when master and 48M_PCM_CLK_GEN_EN (bit 11) is low.
ACTIVE_SLOT	[26:23]	Default is '0001'. Ignored by firmware.
SAMPLE_FORMAT	[28:27]	Selects between 13 (0b00), 16 (0b01), 8 (0b10) bit sample with 16 cycle slot duration or 8 (0b11) bit sample with 8 cycle slot duration.

Table 8.12: PSKEY_PCM_CONFIG32 Description

Name	Bit Position	Description
CNT_LIMIT	[12:0]	Sets PCM_CLK counter limit.
CNT_RATE	[23:16]	Sets PCM_CLK count rate.
SYNC_LIMIT	[31:24]	Sets PCM_SYNC division relative to PCM_CLK.

Table 8.13: PSKEY_PCM_LOW_JITTER_CONFIG Description

8.8 I/O Parallel Ports

Ten lines of programmable bi-directional input/outputs (I/O) are provided. PIO[3:0] are powered from VDD_PIO. PIO[7:4] are powered from VDD_PADS. AIO [2:0] are powered from VDD_USB.

PIO lines can be configured through software to have either weak or strong pull-ups or pull-downs. All PIO lines are configured as inputs with weak pull-downs at reset. See section 2 CSP Package Information for details.

Any of the PIO lines can be configured as interrupt request lines or as wake-up lines from sleep modes. PIO[6] or PIO[2] can be configured as a request line for an external clock source. This is useful when the clock to BlueCore3-ROM CSP is provided from a system application specific integrated circuit (ASIC).

BlueCore3-ROM CSP has two general purpose analogue interface pins, AIO[0] and AIO[2]. These are used to access internal circuitry and control signals. One pin is allocated to decoupling for the on-chip bandgap reference voltage, the other two may be configured to provide additional functionality.

Auxiliary functions available via these pins include an 8-bit ADC and an 8-bit DAC. Typically the ADC is used for battery voltage measurement. Signals selectable at these pins include the bandgap reference voltage and a variety of clock signals; 48, 24, 16, 8MHz and the XTAL clock frequency. When used with analogue signals the voltage range is constrained by the analogue supply voltage (1.8V). When configured to drive out digital level signals (clocks) generated from within the analogue part of the device, the output voltage level is determined by VDD_MEM (1.8V).

8.9 TCXO Enable OR Function

An OR function exists for clock enable signals from a host controller and BlueCore3-ROM CSP where either device can turn on the clock without having to wake up the other device. PIO[3] can be used as the Host clock enable input and PIO[2] can be used as the OR output with the TCXO enable signal from BlueCore3-ROM CSP.

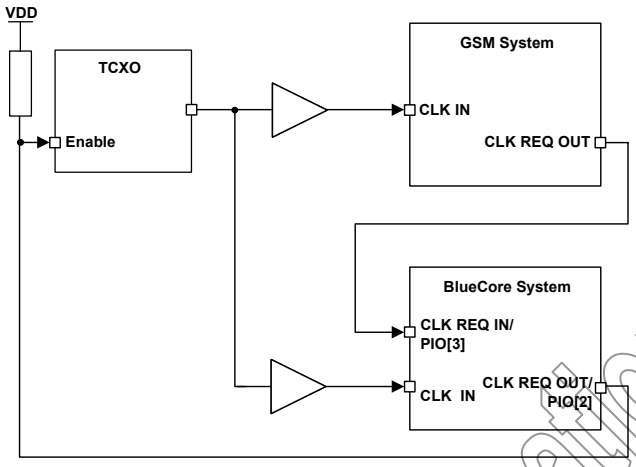


Figure 8.37: Example TXCO Enable OR Function

On reset and up to the time the PIO has been configured, PIO[2] will be tri-stated. Therefore, the developer must ensure that the circuitry connected to this pin is pulled via a 470k resistor to the appropriate power rail. This ensures that the TCXO is oscillating at start up.

8.10 RESETB

BlueCore3-ROM CSP may be reset from several sources: RESETB pin, power on reset, a UART break character or via a software configured watchdog timer.

The RESETB pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESETB being active. CSR recommends that RESETB is applied for a period greater than 5ms.

The power on reset occurs when the VDD_CORE supply falls below typically 1.5V and is released when VDD_CORE rises above typically 1.6V.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-stated. The PIOs have weak pull-downs.

Following a reset, BlueCore3-ROM CSP assumes the maximum XTAL_IN frequency which ensures that the internal clocks run at a safe (low) frequency until BlueCore3-ROM CSP is configured for the actual XTAL_IN frequency. If no clock is present at XTAL_IN, the oscillator in BlueCore3-ROM CSP free runs, again at a safe frequency.

8.10.1 Pin States on Reset

Table 8.14 shows the pin states of BlueCore3-ROM CSP on reset.

Pin name	State: BlueCore3-ROM CSP
PIO[7:0]	Input with weak pull-down
PCM_OUT	Tri-stated with weak pull-down
PCM_IN	Input with weak pull-down
PCM_SYNC	Input with weak pull-down
PCM_CLK	Input with weak pull-down
UART_TX	Output tri-stated with weak pull-up
UART_RX	Input with weak pull-down
UART_RTS (BC313143A only)	Output tri-stated with weak pull-up
UART_CTS (BC313143A only)	Input with weak pull-down
USB_DP (BC313141A only)	Input with weak pull-down
USB_DN (BC313141A only)	Input with weak pull-down
SPI_CSB	Input with weak pull-up
SPI_CLK	Input with weak pull-down
SPI_MOSI	Input with weak pull-down
SPI_MISO	Output tri-stated with weak pull-down
AIO[2]	Output, driving low
RESET	Input with weak pull-down
RESETB	Input with weak pull-up
TEST_EN	Input with strong pull-down
XTAL_IN	High impedance, 250k to XTAL_OUT
XTAL_OUT	High impedance, 250k to XTAL_IN

Table 8.14: Pin States of BlueCore3-ROM CSP on Reset

8.10.2 Status after Reset

The chip status after a reset is as follows:

- Warm Reset: Baud rate and RAM data remain available
- Cold Reset[1]: Baud rate and RAM data not available

Note:

(1) Cold Reset constitutes one of the following:

- Power cycle
- System reset (firmware fault code)
- Reset signal, see Section 8.10

8.11 Power Supply

8.11.1 Voltage Regulator

An on-chip linear voltage regulator can be used to power the 1.8V dependant supplies. It is advised that a smoothing circuit using a 2.2μF low ESR capacitor and 2.2Ω resistor be placed on the output VDD_ANA.

The regulator is switched into a low power mode when the device is sent into deep sleep mode. When the on-chip regulator is not required VDD_ANA is a 1.8V input and VREG_IN must be either open circuit or tied to VDD_ANA.

8.11.2 Sequencing

It is recommended that VDD_CORE, VDD_RADIO and VDD_VCO are powered at the same time, this is true when these supplies are powered from the internal regulator on BlueCore3-ROM CSP. The order of powering supplies for VDD_PIO, VDD_PADS and VDD_USB is not important. However, if VDD_CORE is not present all inputs have a weak pull-down irrespective of the reset state.

8.11.3 Sensitivity to Disturbances

It is recommended that if you are supplying BlueCore3-ROM CSP from an external voltage source that VDD_VCO, VDD_ANA and VDD_RADIO should have less than 10mV rms noise levels between 0 to 10MHz. Single tone frequencies are also to be avoided. A simple RC filter is recommended for VDD_CORE as this isoloates the power supply rails from on-chip transients.

The transient response of the regulator is also important as at the start of a packet, power consumption will jump to the levels defined in average current consumption section. It is essential that the power rail recovers quickly, so the regulator should have a response time of 20μs or less.

9 Application Schematic

9.1 BC313141AXX (UART) CSP Package

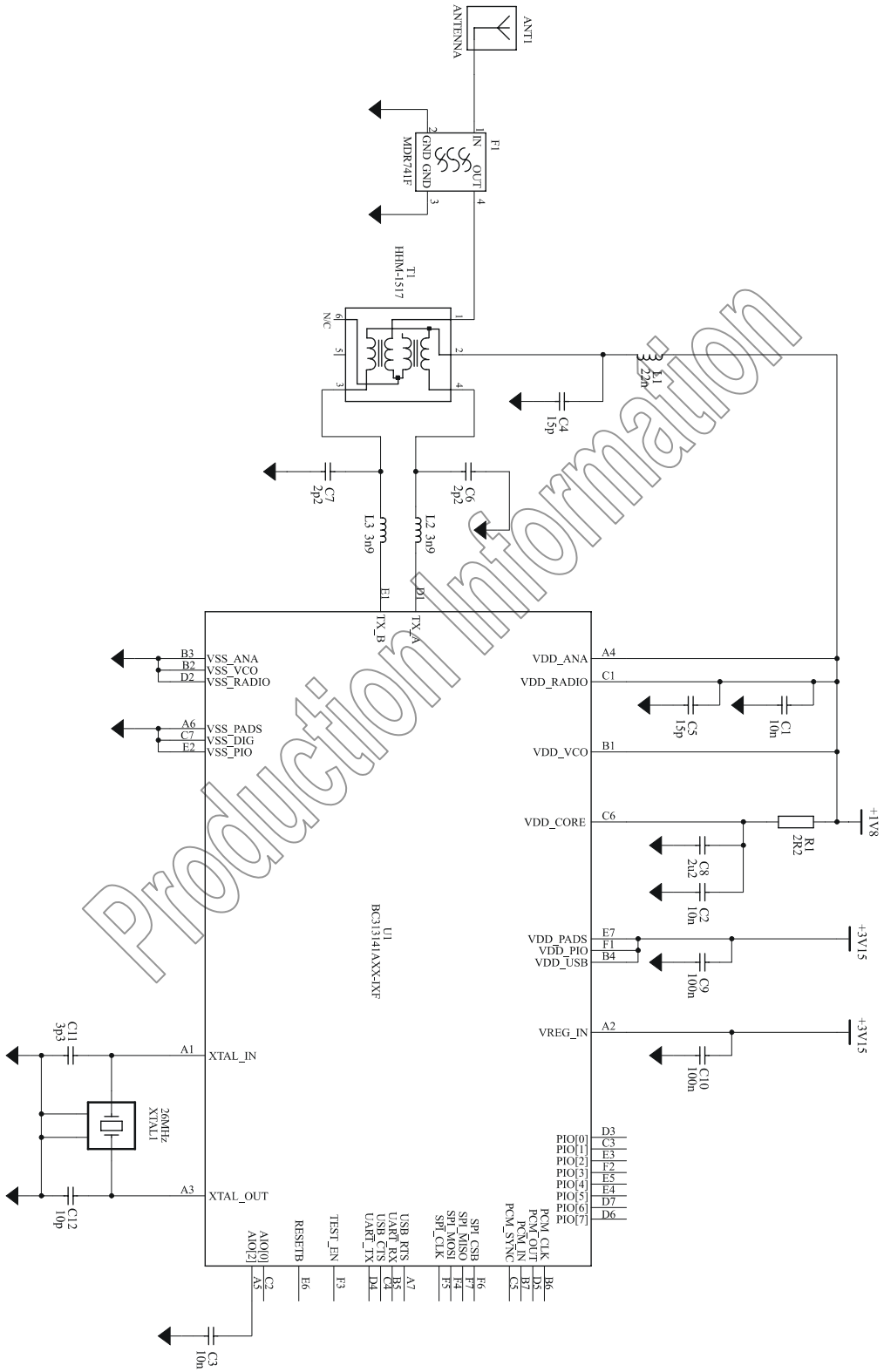


Figure 9.1: Application Circuit for CSP Package

9.2 BC313143AXX (USB) CSP Package

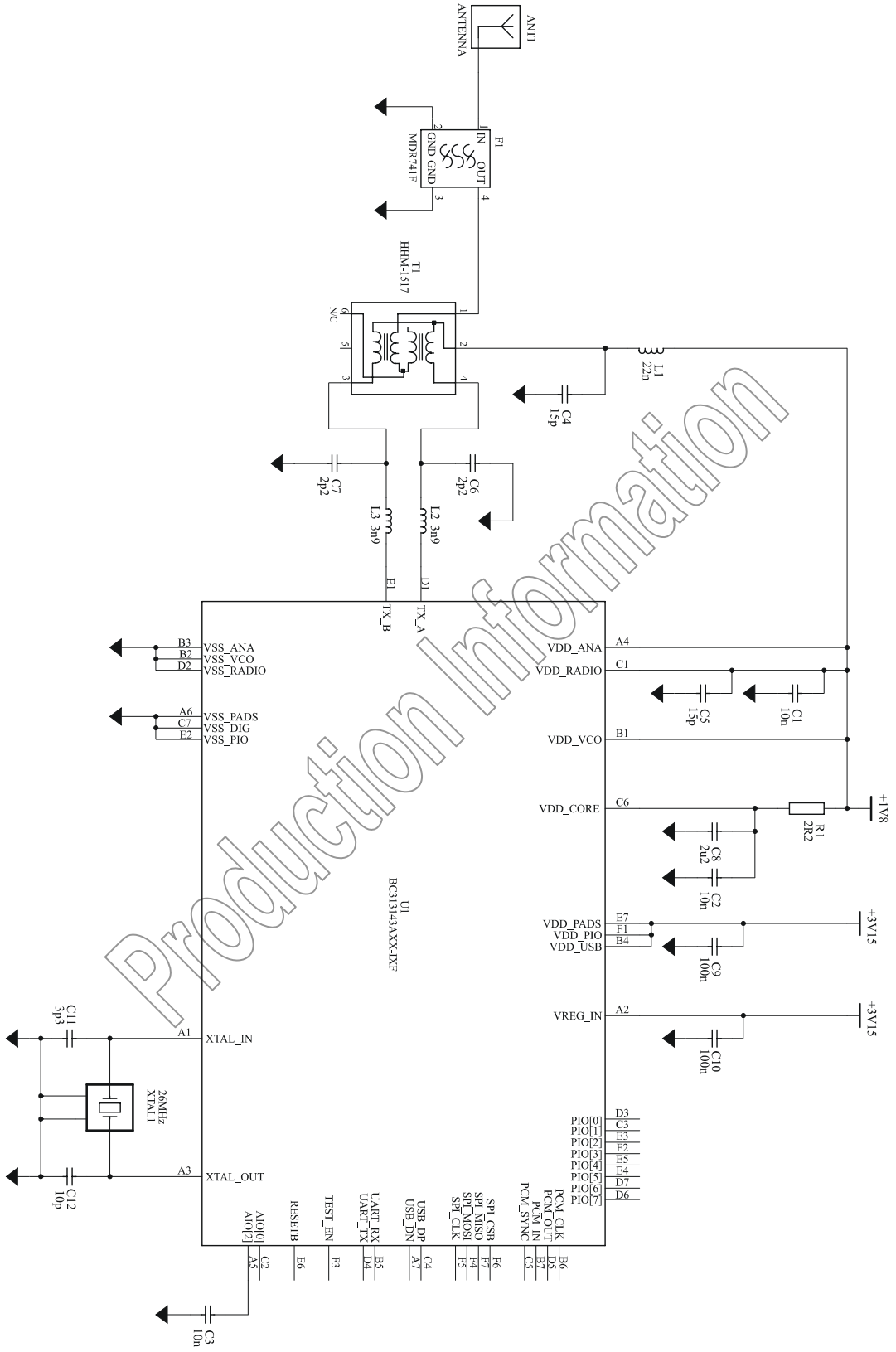


Figure 9.2: Application Circuit for CSP Package

10 PCB Design and Assembly Considerations

10.1 3.8mm x 3.4mm CSP 42-Ball Package

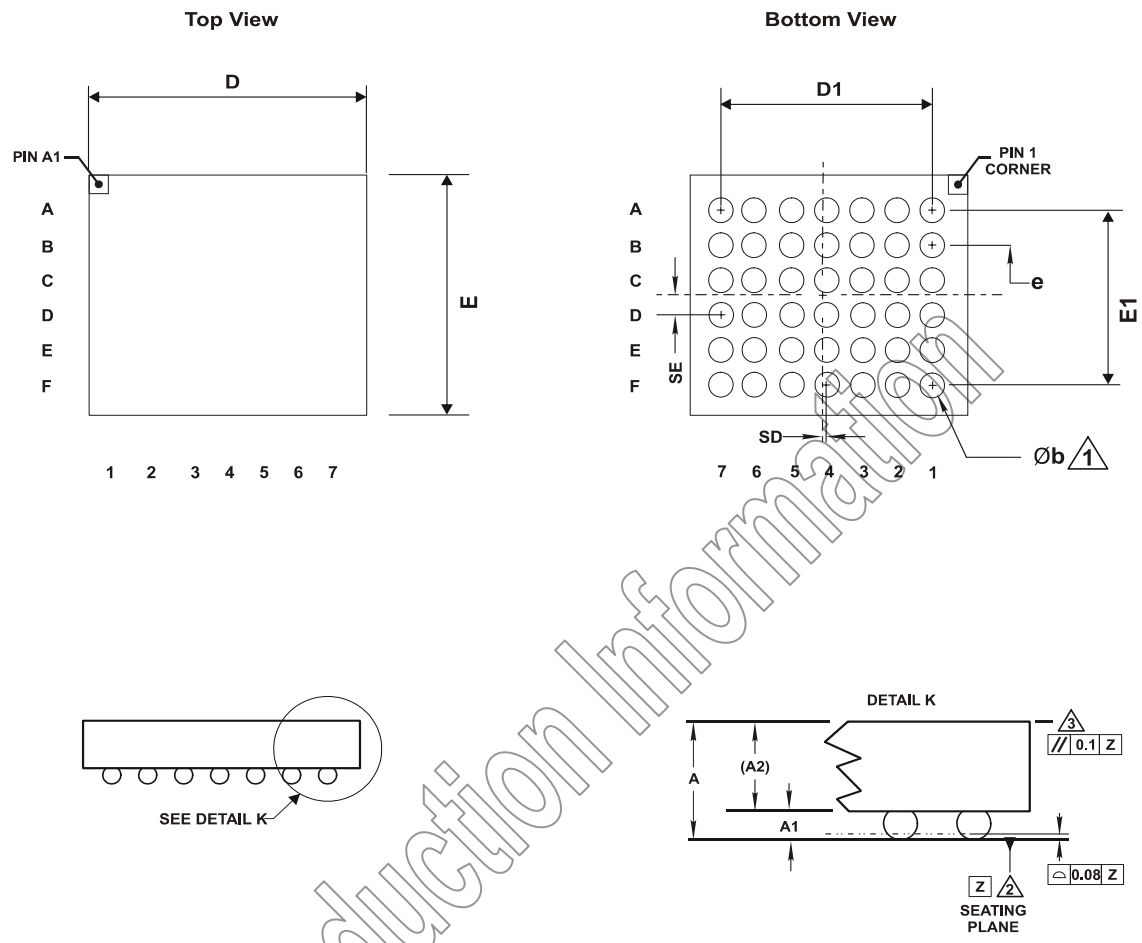
The following list details the recommendations to achieve maximum board-level reliability of the BlueCore3-ROM CSP 3.8mm x 3.4mm CSP 42-ball package:

- Non-solder mask defined (NSMD) lands – lands smaller than the solder mask aperture – are preferred, because of the greater accuracy of the metal definition process compared to the solder mask process. With solder mask defined pads, the overlap of the solder mask on the land creates a step in the solder at the land interface, which can cause stress concentration and act as a point for crack initiation
- Ideally, via-in-pad technology should be employed to achieve truly NSMD lands. Where this is not possible, a maximum of one trace connected to each land is preferred and this trace should be as thin as possible – taking into consideration its current carrying and the radio frequency (RF) requirements
- 35 micron thick (1 oz.) copper lands are recommended rather than 17 micron thick (1/2 oz.), because this results in a greater standoff, which has been proven to provide greater reliability during thermal cycling
- Land diameter should be 275 microns +/-10 microns to achieve optimum reliability
- Solder paste is preferred to flux during the assembly process, as this adds to the final volume of solder in the joint, increasing its reliability
- Where possible, the lands should be finished with organic solderability preservative (OSP). Were a nickel gold plating finish is used, the gold thickness should be kept below 0.5 microns in order to prevent brittle gold/tin intermetallics forming in the solder

CSP devices have been proven to be reliable. However, by their nature they are more susceptible to handling damage than plastic packaged devices. Care should be taken to optimise placement equipment settings for CSPs and care should be taken when handling PCBs with CSPs attached.

11 Package Dimensions

11.1 BC313141AXX-IXF and BC313143AXX-IXF CSP 42-Ball Package



Package: 3.8 x 3.4 x 0.7mm 0.5mm Pitch 42-Ball CSP				
DIM	MIN	TYP	MAX	NOTES
A	0.61	0.67	0.70	1 DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM PLANE Z.
A1	0.21	0.24	0.27	
A2		0.43		2 DATUM Z IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
b	0.25	0.30	0.35	
D	3.74	3.79	3.84	3 PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
E	3.30	3.35	3.40	
e		0.50		
D1		3.00		
E1		2.50		
SD		0.02		
SE		0.35		
42-Ball CSP 3.8 x 3.4 x 0.7mm				UNIT MM

Figure 11.1: BlueCore3-ROM CSP Package Dimensions

12 Tape and Reel Information

12.1 Tape Information

12.1.1 WLCSP Tape Orientation

Figure 12.1 shows the general orientation of the CSP package in the carrier tape.

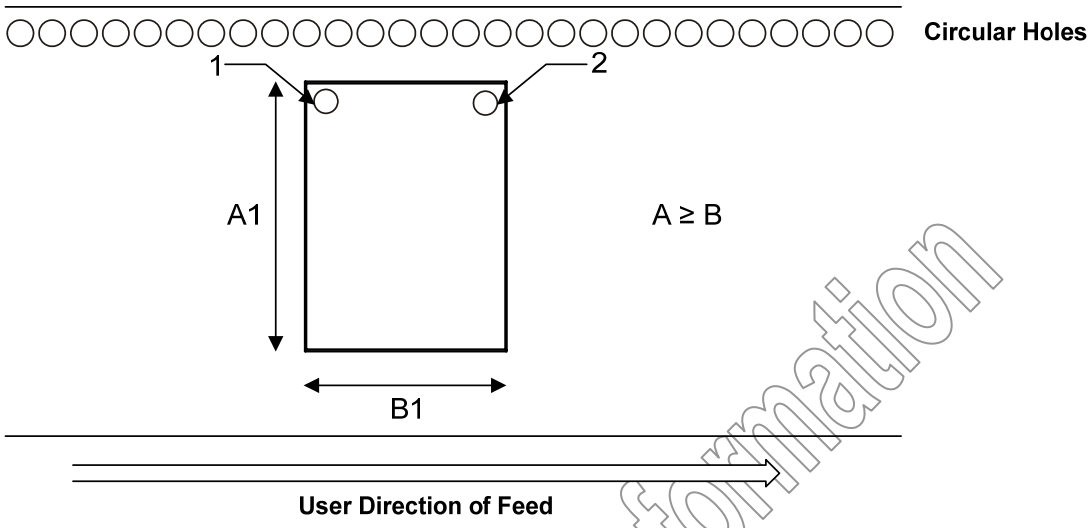
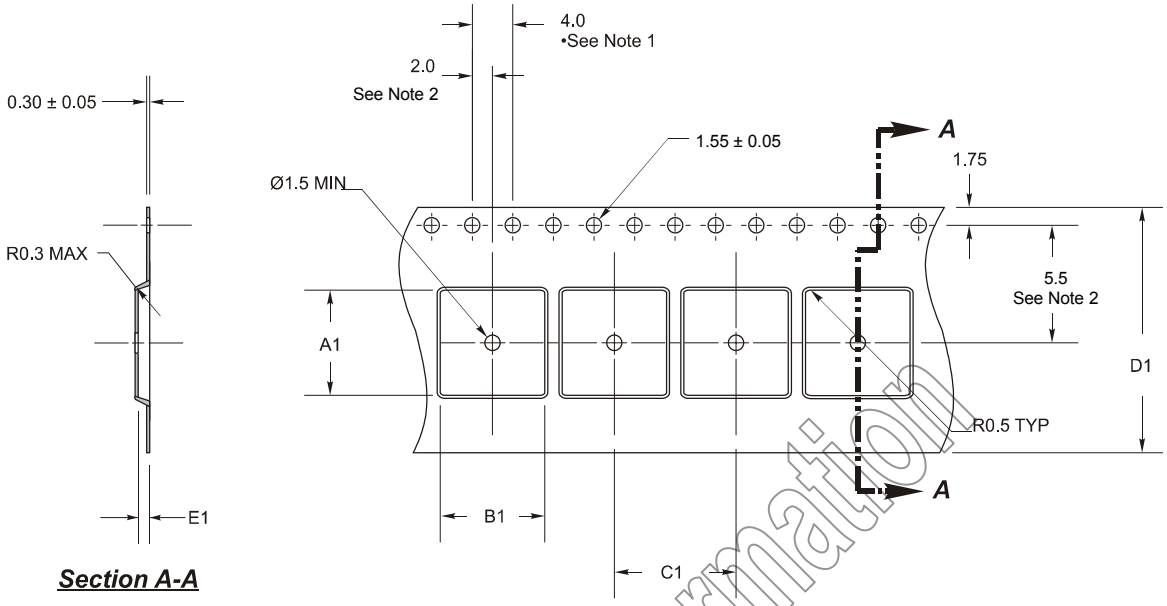


Figure 12.1: CSP Tape and Reel Orientation

Where possible the Pin A1 marker will be placed at position 1. Where the aspect ratio of the CSP does not make this possible, the Pin 1 marker will be placed at position 2. For BlueCore3-ROM CSP the marker is in position 2.

12.1.2 Package Tape Dimensions

The diagram shown in Figure 12.2 outlines the dimensions of the tape used for the various packages:



Notes:

1. 10 sprocket hole pitch cumulative tolerance ± 0.1.
2. Pocket position relative to sprocket hole measured as true position of pocket , not pocket hole.

Figure 12.2: Package Tape Dimensions

Package Type	A1	B1	C1	D1	E1
3.8 x 3.4 x 0.7mm CSP	4.01mm	3.55mm	8mm	12mm	0.87mm

Figure 12.3: Tape Dimensions

The cover tape has a total peel strength of 0.1N to 1.3N. The direction of the pull should be opposite the direction of the carrier tape such that the cover tape makes an angle of between 165° and 180° with the top of the carrier tape. The carrier and/or cover tape should be pulled with a velocity of 300±10mm during peeling.

Maximum component rotation inside the cavity is 10°. The cavity pitch tolerance (dimension P1) is ±0.1mm.

The reel is made of high impact injection molded polystyrene. The carrier tape is made of polystyrene with carbon. The cover tape is made of antistatic polyester film and an antistatic heat activated adhesive coating.

12.2 Reel Information

Reel dimensions
(All dimensions in millimeters)

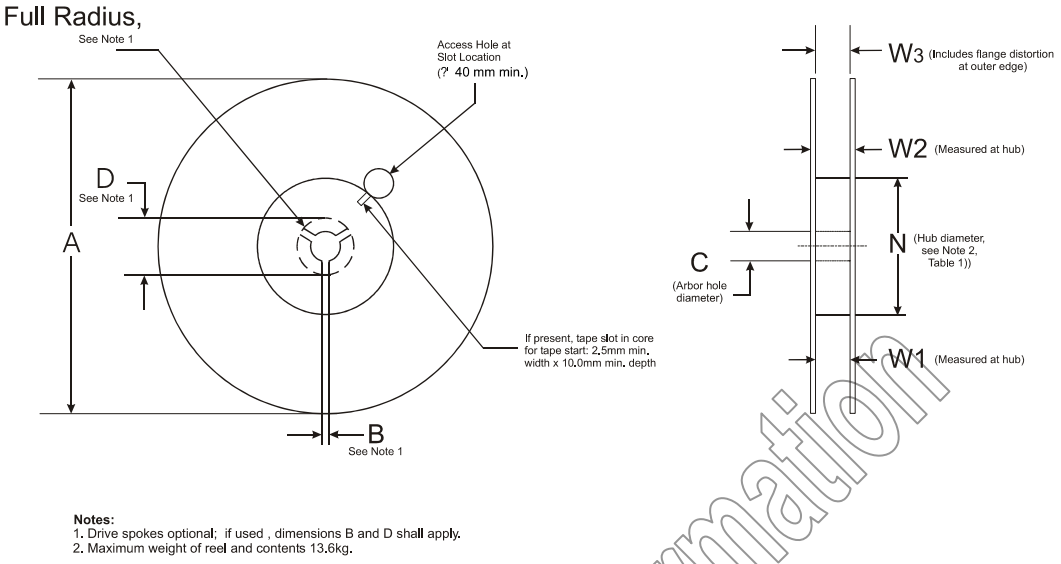


Figure 12.4: Reel Dimensions

Package Type	Tape Width	A Max	B Max	C	D Min	N Min	W1	W2 Max	W3		Units
									Min	Max	
CSP	12	330	1.5	13.0 (+0.5/-0.2)	20.2	50	12.4 (+2.0/-0.0)	18.4	11.9	15.4	mm

Table 12.1: Reel Dimensions

13 Solder Profile

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder re-flow. There are four zones:

1. **Preheat Zone:** This zone raises the temperature at a controlled rate, typically 1-2.5°C/s.
2. **Equilibrium Zone:** This zone brings the board to a uniform temperature and also activates the flux. The duration in this zone (typically 2-3 minutes) will need to be adjusted to optimise the out gassing of the flux.
3. **Reflow Zone:** The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint.
4. **Cooling Zone:** The cooling rate should be fast, to keep the solder grains small which will give a longer lasting joint. Typical rates will be 2-5°C/s.

13.1 Typical Solder Re-flow Profile for Devices with Lead-Free Solder Balls

Composition of the solder ball: Sn 96.8%, Ag 2.6%, Cu 0.6% or Sn 95.5%, Ag 4.0%, Cu 0.5%.

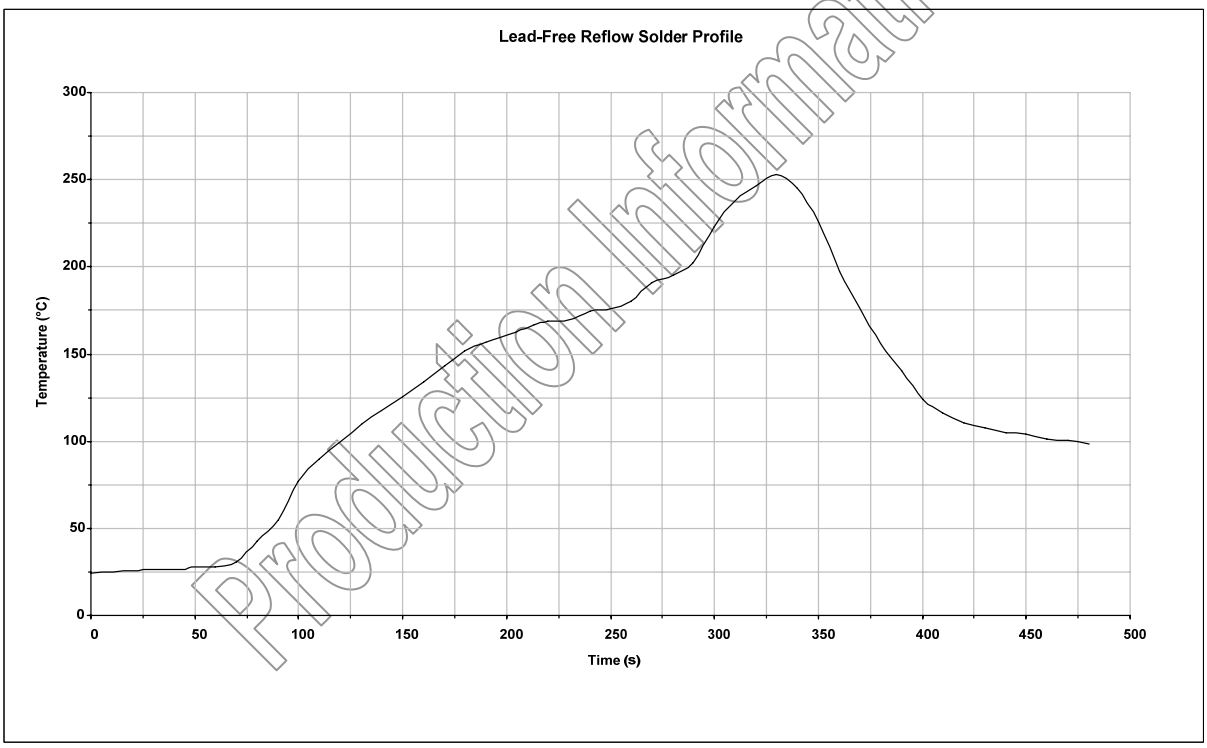


Figure 13.1: Typical Lead-Free Re-flow Solder Profile

Key features of the profile:

- Initial Ramp = 1-2.5°C/sec to 175°C±25°C equilibrium
- Equilibrium time = 60 to 180 seconds
- Ramp to Maximum temperature (250°C) = 3°C/sec max.
- Time above liquidus temperature (217°C): 45-90 seconds
- Device absolute maximum reflow temperature: 260°C
- Devices will withstand the specified profile.
- Lead-free devices will withstand up to 3 reflows to a maximum temperature of 260°C.

14 Ordering Information

14.1 BlueCore3-ROM CSP

Interface Version	Package			Order Number
	Type	Size	Shipment Method	
UART Only (4 wire)	42-Ball CSP (Pb free)	3.8 x 3.4 x 0.7mm	Tape and reel	BC313141AXX-IXF-E4
USB and UART 3 wire UART (H5) and BCSP	42-Ball CSP (Pb free)	3.8 x 4.0 x 0.7mm	Tape and reel	Discontinued

Note:

XX denotes firmware type and firmware version status. These are determined on a customer and project basis.

Minimum Order Quantity:

2kpcs Taped and Reeled

15 Contact Information

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16 Document References

Document	Reference
Specification of the Bluetooth system	v1.2, 0.95, 10 October 2002
Universal Serial Bus Specification	v1.1, 23 September 1998
Restrictions of Hazardous Substances	RoHS directive 2002/95/EC

Terms and Definitions

BlueCore	Group term for CSR's range of Bluetooth chips
Bluetooth	A set of technologies providing audio and data transfer over short-range radio connections
ACL	Asynchronous Connection-Less. A Bluetooth data packet
AC	Alternating Current
ADC	Analogue to Digital Converter
AGC	Automatic Gain Control
A-law	Audio encoding standard
API	Application Programming Interface
BCSP	BlueCore™ Serial Protocol
BER	Bit Error Rate. Used to measure the quality of a link
BGA	Ball Grid Array
BIST	Built-In Self-Test
BOM	Bill of Materials. Component part list and costing for a product
BMC	Burst Mode Controller
C/I	Carrier Over Interferer
CDMA	Code Division Multiple Access
CMOS	Complementary Metal Oxide Semiconductor
CODEC	Coder Decoder
CPU	Central Processing Unit
CQDDR	Channel Quality Driven Data Rate
CSB	Chip Select (Active Low)
CSP	Chip Scale Package
CSR	Cambridge Silicon Radio
CTS	Clear to Send
CVSD	Continuous Variable Slope Delta Modulation
DAC	Digital to Analogue Converter
dBm	Decibels relative to 1mW
DC	Direct Current
DFU	Device Firmware Upgrade
eSCO	Extended Synchronous Connection-Oriented
FSK	Frequency Shift Keying
GSM	Global System for Mobile communications
HCI	Host Controller Interface
HV	Header Value
I/O	Input Output
IQ Modulation	In-Phase and Quadrature Modulation
IF	Intermediate Frequency
ISDN	Integrated Services Digital Network
ISM	Industrial, Scientific and Medical
ksamples/s	kilosamples per second
L2CAP	Logical Link Control and Adaptation Protocol (protocol layer)
LC	Link Controller

LCD	Liquid Crystal Display
LNA	Low Noise Amplifier
LSB	Least-Significant Bit
μ-law	Audio Encoding Standard
MMU	Memory Management Unit
MISO	Master In Serial Out
OHCI	Open Host Controller Interface
PA	Power Amplifier
PCB	Printed Circuit Board
PCM	Pulse Code Modulation. Refers to digital voice data
PDA	Personal Digital Assistant
PICS	Protocol Implementation Conformance Statement
PIO	Parallel Input Output
PLL	Phase Lock Loop
ppm	parts per million
PS Key	Persistent Store Key
RAM	Random Access Memory
REB	Read enable (Active Low)
RF	Radio Frequency
RFCOMM	Protocol layer providing serial port emulation over L2CAP
RISC	Reduced Instruction Set Computer
rms	root mean squared
ROM	Read Only Memory
RoHS	Restrictions of Hazardous Substances
RSSI	Receive Signal Strength Indication
RTS	Ready To Send
RX	Receive or Receiver
SCO	Synchronous Connection-Oriented. Voice oriented Bluetooth packet
SDK	Software Development Kit
SDP	Service Discovery Protocol
SIG	Special Interest Group
SPI	Serial Peripheral Interface
SSI	Signal Strength Indication
TBA	To Be Announced
TBD	To Be Defined
TCXO	Temperature Controlled crystal Oscillator
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
UHCI	Upper Host Control Interface
USB	Universal Serial Bus or Upper Side Band (depending on context)
VCO	Voltage Controlled Oscillator
VFBGA	Very Fine Ball Grid Array
VM	Virtual Machine
W-CDMA	Wideband Code Division Multiple Access
WEB	Write Enable (Active Low)

Document History

Date	Revision	Reason for Change
MAY 04	a	Original publication of Advance Information Product Data Sheet (CSR reference BC313143ACS-ds-001Pa)
AUG 04	b	Changes made to package diagram.
FEB 05	c	Production radio characteristics added
MAR 05	d	Typical peak current @20°C added to Power Consumption
APR 05	e	Updated Power Consumption. Transmitter/Receiver S-Parameters and Transmit/Receive Impedances added to Device Terminal Descriptions.
JUN 05	f	Amendment to note concerning VREG_EN and VREG_IN in Linear Regulator table of Electrical Characteristics section. Changed title of Record of Changes to Document History; changed title of Acronyms and Abbreviations to Terms and Definitions Changed copyright information on Status Information page
JUL 05	g	Tape and reel information updated
JUL 05	h	Changes to reflect obsolete part BC313143A. Solder ball composition clarified.
NOV 06	i	Key features section updated for consistency

BlueCore™3-ROM CSP

Product Data Sheet

BC313143ACS-db-001Pi

November 2006