AMIS-49587

Product Preview
Power Line Carrier Modem

ON Semiconductor's AMIS−49587 is an IEC1334 compliant power line carrier modem using spread−FSK (S−FSK) modulation for robust low data rate communication over power lines. AMIS−49587 is built around an ARM 7TDMI processor core, and includes the MAC layer. With this robust modulation technique, signals on the power lines can pass long distances. The half−duplex operation is automatically synchronized to the mains, and can be up to 2400 bits/sec.

The product configuration is done via its serial interface, which allows the user to concentrate on the development of the application.

The AMIS−49587 is implemented in ON Semiconductor mixed signal technology, combining both analog circuitry and digital functionality on the same IC.

Features

- Power Line Carrier Modem for 50 and 60 Hz Mains
- Fully Compliant to IEC1334−5−1 IEC 1334−4−32 / EN50065
- Complete Handling of Protocol Layers Physical to MAC
- Programmable Carrier Frequencies from 9 to 95 kHz in 10 Hz Steps
- Half Duplex
- Data Rate Selectable: 300 – 600 – 1200 – 2400 baud (50 Hz)
- Synchronization on Mains
- Repetition Algorithm Boost the Robustness of Communication
- Other Features Under Development / Validation
- SCI Port to Application Microcontroller
- SCI Baudrate Selectable: 4.8 – 9.6 – 19.2 – 34.4 kb
- Power Supply 3.3 V
- Ambient Temperature Range: −40°C to +80°C
- These Devices are Pb−Free and are RoHS Compliant*

Typical Applications

- AMR: Automated Remote Meter Reading (Télérelevé)
- Remote Security Control
- Streetlight Control
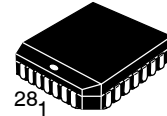- Transmission of Alerts (Fire, Gas Leak, Water Leak)

ON Semiconductor®

http://onsemi.com

**PLCC 28 Lead
CASE 776AA**

MARKING DIAGRAM

ON   **ARM**

XXXXYZZ
AMIS49587
C587-NAF   e3
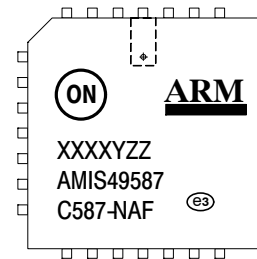
xx	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
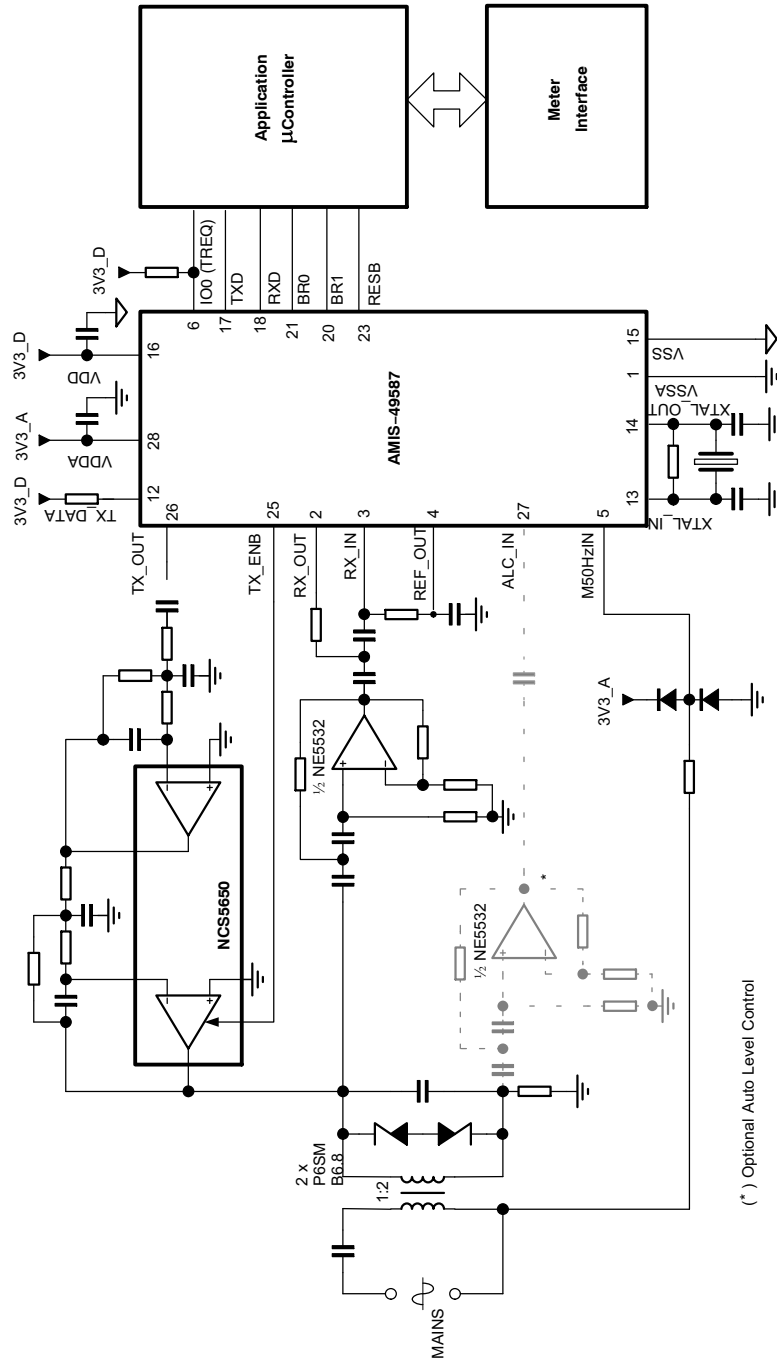
APPLICATION

APPLICATION EXAMPLE

Figure 1. Typical Application for the AMIS−49587 S−FSK Modem

A typical application example is given above. The example shows the AMIS−49587 with its companion devices. Namely the power line driver NCS5650, the application controller and a meter device interface.

Between the modem chip and the line driver, an active band pass filter is used to reduce the noise outside the transmission band. The filter is realized with external passive components.

From the line driver, the connection to the mains is done through a line transformer and a capacitive coupling.

From the application side, the interface between the modem and the application is done through the SCI. The link to the meter device will be done easily by using the meter device interface chip. This device is used to realize the physical interface between the controller and the standard S0 pulse (DIN 19234) generator output of the meter device.

AMIS−49587

Table 1. ORDERING INFORMATION

Part No.	Package	Shipping[†]
AMIS49587C5871R	PLCC−28 (Pb−Free)	Rail
AMIS49587C5871RG	PLCC−28 (Pb−Free)	Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Table of Contents

ABSOLUTE MAXIMUM RATINGS

Stresses above those listed in this clause may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Power Supply Pins VDD, VDDA, VSS, VSSA

Table 2. ABSOLUTE MAXIMUM RATINGS SUPPLY

Rating	Symbol	Min	Max	Unit
Absolute maximum digital power supply	V_{DD_ABSM}	$V_{SS}−0.3$	3.9	V
Absolute maximum analog power supply	V_{DDA_ABSM}	$V_{SSA}−0.3$	3.9	V
Absolute maximum difference between digital and analog power supply	$V_{DD}−V_{DDA\_ABSM}$	−0.3	0.3	V
Absolute maximum difference between digital and analog ground	$V_{SS}−V_{SSA\_ABSM}$	−0.3	0.3	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Non 5V Safe Pins: TX_OUT, ALC_IN, RX_IN, RX_OUT, REF_OUT, M50HZ_IN, XIN, XOUT, TDO, TDI, TCK, TMS, TRSTB, TEST

Table 3. ABSOLUTE MAXIMUM RATINGS NON 5V SAFE PINS

Rating	Symbol	Min	Max	Unit
Absolute maximum input for normal digital inputs and analog inputs	V_{IN_ABSM}	$V_{SS*}−0.3$	$V_{DD*}+0.3$	V
Absolute maximum voltage at any output pin	V_{OUT_ABSM}	$V_{SS*}−0.3$	$V_{DD*}+0.3$	V

5V Safe Pins: TX_ENB, TXD, RXD, BR0, BR1, IO0, IO2, RESB

Table 4. ABSOLUTE MAXIMUM RATINGS 5V SAFE PINS

Rating	Symbol	Min	Max	Unit
Absolute maximum input for digital 5 V safe inputs	V_{5VS_ABSM}	$V_{SS}−0.3$	6.0	V
Absolute maximum voltage at 5 V safe output pin	V_{OUT5V_ABSM}	$V_{SS}−0.3$	3.9	V

Normal Operating Conditions

Operating ranges define the limits for functional operation and parametric characteristics of the device as described in the Receiver Block Diagram Section and for the reliability specifications as listed in the Local Transfer and Configuration Commands (LTC) Section. Functionality outside these limits is not implied.

Total cumulative dwell time outside the normal power supply voltage range or the ambient temperature under bias, must be less than 0.1% of the useful life as defined in the Local Transfer and Configuration Commands (LTC) Section.

Table 5. OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Power Supply Voltage Range	V_{DD}	3.0	3.6	V
Ambient Temperature	T_A	−25	70	°C

AMIS−49587

PIN DESCRIPTION
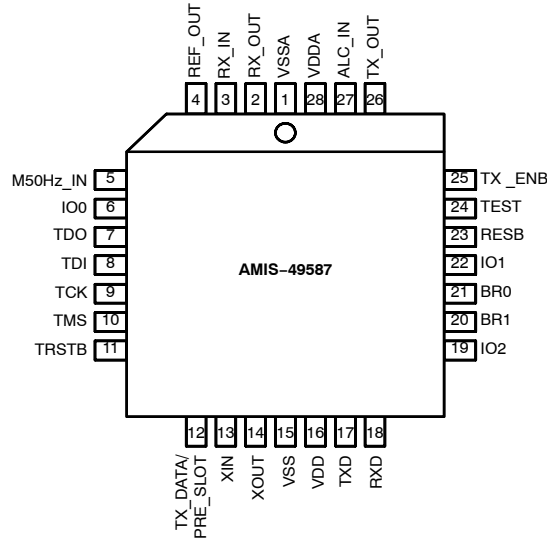
Figure 2. Pinout

Table 6. PIN DESCRIPTION

Pin No.	Pin Name	I/O	Type	Description
1	VSSA		P	Analog ground
2	RX_OUT	Out	A	Output of input stage opamp
3	RX_IN	In	A	Positive input of input stage opamp
4	REF_OUT	Out	A	Reference output for stabilization
5	M50HZ_IN	In	A	50.60 Hz input
6	IO0	In/Out	D,5V Safe	Programmable IO pin (open drain)
7	TDO	Out	D, 5V Safe	Test data output
8	TDI	In	D, 5V Safe	Test data input (internal pulldown)
9	TCK	In	D, 5V Safe	Test clock (internal pull down)
10	TMS	In	D, 5V Safe	Test mode select (internal pulldown)
11	TRSTB	In	D, 5V Safe	Test reset bar (internal pull down, active low)
12	TX_DATA	Out	D, 5V Safe	Data output corresponding to transmitted frequency
13	XIN	In	A	Xtal input (can be driven by an internal clock)
14	XOUT	Out	A	Xtal output (output floating when XIN driven by external clock)
15	VSS		P	Digital ground
16	VDD		P	3.3 V digital supply
17	TXD	Out	D, 5V Safe	SCI transmit output (open drain)
18	RXD	In	D, 5V Safe	SCI receive input (Schmitt trigger output)
19	IO2	In/Out	D, 5V Safe	Programmable IO pin + interrupt (open drain)
20	BR1	In	D, 5V Safe	SCI baud rate selection
21	BR0	In	D, 5V Safe	SCI baud rate selection
22	IO1	In/Out	D, 5V Safe	Programmable IO pin (open drain)
23	RESB	In	D, 5V Safe	Master reset bar (Schmitt trigger input, active low)
24	TEST	In	D	Test enable (internal pulldown)
25	TX_ENB	Out	D, 5V Safe	TX enable bar (open drain)
26	TX_OUT	Out	A	Transmitter output
27	ALC_IN	In	A	Automatic level control input
28	VDDA		P	3.3 V analog supply

P: Power pin
A: Analog pin
D: Digital pin
5V Safe: IO that support the presence of 5V on bus line
Out: Output signal
In: Input signal
In/Out: Bi−directional pin

ELECTRICAL CHARACTERISTICS

DC AND AC CHARACTERISTICS

Oscillator: Pin XIN, XOUT

In production the actual oscillation of the oscillator and duty cycle will not be tested. The production test will be based on the static parameters and the inversion from XIN to XOUT in order to guarantee the functionality of the oscillator.

Table 7. OSCILLATOR

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Crystal frequency	(Note 1)	f_{CLK}	−100 ppm	24	+100 ppm	MHz
Duty cycle with quartz connected	(Note 1)		40		60	%
Start−up time	(Note 1)	$T_{startup}$			50	ms
Maximum Capacitive load on XOUT	XIN used as clock input	CL_{XOUT}			50	pF
Low input threshold voltage	XIN used as clock input	VIL_{XOUT}	$0.3\,V_{DD}$			V
High input threshold voltage	XIN used as clock input	VIH_{XOUT}			$0.7\,V_{DD}$	V
Low output voltage	XIN used as clock input, XOUT = 2 mA	VOL_{XOUT}			0.3	V
High input voltage	XIN used as clock input	VOH_{XOUT}			V_{DD}−0.3	V

1. For the design of the oscillator crystal parameters have been taken from the data sheet [8]. The series loss resistance for this type of crystal is maximum 50 Ω. However the oscillator cell has been designed with some margin for series loss resistance up to 80 Ω.

Zero Crossing Detector and 50/60Hz PLL: Pin M50HZ_IN

Table 8. ZERO CROSSING DETECTOR AND 50/60HZ PLL

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Maximum peak input current		$Imp_{M50HZIN}$	−20		20	mA
Maximum average input current	During 1 ms	$Imavg_{M50HZIN}$	−2		2	mA
Mains voltage (ms) range	With protection resistor at M50HZIN	V_{MAINS}	90		550	V
Rising threshold level	(Note 2)	$VIRM_{50HZIN}$			1.9	V
Falling threshold level	(Note 2)	$VIFM_{50HZIN}$	0.9			V
Hysteresis	(Note 2)	VHY_{50HZIN}	0.4			V
Lock range for 50 Hz (Note 3)	MAINS_FREQ = 0 (50 Hz)	$Flock_{50Hz}$	45		55	Hz
Lock range for 60 Hz (Note 3)	MAINS_FREQ = 0 (60 Hz)	$Flock_{60Hz}$	54		66	Hz
Lock time (Note 3)	MAINS_FREQ = 0 (50 Hz)	$Tlock_{50Hz}$			15	s
Lock time (Note 3)	MAINS_FREQ = 0 (60 Hz)	$Tlock_{60Hz}$			20	s
Frequency variation without going out of lock (Note 3)	MAINS_FREQ = 0 (50 Hz)	DF_{60Hz}			0.1	Hz/s
Frequency variation without going out of lock (Note 3)	MAINS_FREQ = 0 (60 Hz)	DF_{50Hz}			0.1	Hz/s
Jitter of CHIP_CLK (Note 3)		$Jitter_{CHIP\_CLK}$	−25		25	μs

2. Measured relative to V_{SS}.
3. These parameters will not be measured in production since the performance is totally dependent of a digital circuit which will be guaranteed by the digital test patterns.

Transmitter External Parameters: Pin TX_OUT, ALC_IN, TX_ENB

To guarantee the transmitter external specifications the TX_CLK frequency must be 12 MHz ± 100 ppm.

Table 9. TRANSMITTER EXTERNAL PARAMETERS

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Maximum peak output level	fTX_OUT = 23.75 kHz fTX_OUT = 95 kHz Level control at max. output	V_{TX_OUT}	0.85 0.76		1.15 1.22	Vp
Second order harmonic distortion	fTX_OUT = 95 kHz Level control at max. output	HD2			−56	dB
Third order harmonic distortion	fTX_OUT = 95 kHz Level control at max. output	HD3			−58	dB
Frequency accuracy of the generated sine wave	(Notes 4 and 6)	Df_{TX_OUT}			30	Hz
Capacitive output load at pin TX_OUT	(Note 4)	CL_{TX_OUT}			20	pF
Resistive output load at pin TX_OUT		RL_{TX_OUT}	5			kΩ
Turn off delay of TX_ENB output	(Note 5)	Td_{TX_ENB}	0.25		0.5	ms
Automatic level control attenuation step		ALC_{step}	2.9		3.1	dB
Maximum attenuation		ALC_{range}	20.3		21.7	dB
Low threshold level on ALC_IN		VTL_{ALC_IN}	−0.46		−0.36	V
High threshold level on ALC_IN		VTH_{ALC_IN}	−0.68		−0.54	V
Input impedance of ALC_IN pin		R_{ALC_IN}	111		189	kΩ
Power supply rejection ration of the transmitter section		$PSRR_{TX\_OUT}$	10 (Note 7)		35 (Note 8)	dB

4. This parameter will not be tested in production.
5. This delay corresponds to the internal transmit path delay and will be defined during design.
6. Taking into account the resolution of the DDS and an accuracy of 100 ppm of the crystal.
7. A sinusoidal signal of 10 kHz and 100 mV ptp is injected between VDDA and VSSA. The digital AD converter generates an idle pattern. The signal level at TX_OUT is measured to determine the parameter.
8. A sinusoidal signal of 50 Hz and 100 mV ptp is injected between VDDA and VSSA. The digital AD converter generates an idle pattern. The signal level at TX_OUT is measured to determine the parameter.

The LPF filter + amplifier must have a frequency characteristic between the limits listed below. The absolute output level depends on the operating condition. In production the measurement will be done for relative output levels where the 0 dB reference value is measured at 50 kHz with a signal amplitude of 100 mV.

Table 10. TRANSMITTER FREQUENCY CHARACTERISTICS

| Frequency (kHz) | Attenuation | | Unit |
	Min	Max	
10	−0.5	0.5	dB
95	−1.3	0.5	dB
130	−4.5	−2.0	dB
165		−3.0	dB
330		−18.0	dB
660		−36.0	dB
1000		−50	dB
2000		−50	dB

Table 11. RECEIVER EXTERNAL PARAMETERS: Pin RX_IN, RX_OUT, REF_OUT

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Input offset voltage 42 dB	AGC gain = 42 dB	$V_{OFFS\_RX\_IN}$			5	mV
Input offset voltage 0 dB	AGC gain = 0 dB	$V_{OFFS\_RX\_IN}$			50	mV
Max. peak input voltage (corresponding to 62.5% of the SD full scale)	AGC gain = 0 dB (Note 9)	$V_{MAX\_RX\_IN}$	0.85		1.15	V_p
Input referred noise of the analog receiver path	AGC gain = 42 dB (Notes 9 and 10)	NF_{RX_IN}			150	nV/√Hz
Input leakage current of receiver input		$I_{LE\_RX\_IN}$	−1		1	μA
Max. current delivered by REF_OUT		$I_{Max\_REF\_OUT}$	−300		300	mA
Power supply rejection ratio of the receiver input section	AGC gain = 42 dB	$PSRR_{LPF\_OUT}$	10 (Note 11) 35 (Note 12)			dB
AGC gain step		AGC_{step}	5.7		6.3	dB
AGC range		AGC_{range}	39.9		44.1	dB
Analog ground reference output voltage		V_{REF_OUT}	1.52		1.78	V
Signal to noise ratio at 62.5% of the SD full scale	(Notes 9 and 13)	SN_{AD_OUT}	54			dB
Clipping level at the output of the gain stage		$V_{CLIP\_AGC\_IN}$	1.15		1.65	Vp

9. Input at RX_IN, no other external components.
10. This parameter will be characterized on a limited number of prototypes and will not be tested in production.
11. A sinusoidal signal of 10 kHz and 100 mV ptp is injected between VDDA and VSSA. The signal level at the differential LPF_OUT and REF_OUT output is measured to determine the parameter.
12. A sinusoidal signal of 50 Hz and 100mV ptp is injected between VDDA and VSSA. The signal level at the differential LPF_OUT output is measured to determine the parameter.
13. These parameters will be tested in production with an input signal of 95 kHz and 1 Vp by reading out the digital samples at the point AD_OUT with the default settings of T_RX_MOD[7], SDMOD_TYP, DEC_TYP, and COR_F_ENA. The AGC gain is switched to 0 dB.

The receive LPF filter + AGC + low noise amplifier must have a frequency characteristic between the limits listed below. The absolute output level depends on the operating condition. In production the measurement will be done for relative output levels where the 0 dB reference value is measured at 50 kHz with a signal amplitude of 100 mV.

Table 12. RECEIVER FREQUENCY CHARACTERISTICS

Frequency (kHz)	Attenuation		Unit
	Min	Max	
10	−0.5	0.5	dB
95	−1.3	0.5	dB
130	−4.5	−2.0	dB
165		−3.0	dB
330		−18.0	dB
660		−36.0	dB
1000		−50	dB
2000		−50	dB

Table 13. POWER−ON−RESET (POR)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
POR threshold		V_{POR}	1.7		2.7	V
Power supply rise time	0 V to 3 V	T_{RPOR}	1			ms

Table 14. DIGITAL OUTPUTS: TDO, CLK_OUT

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Low output voltage	I_{XOUT} = 4 mA	V_{OL}			0.4	V
High output voltage	I_{XOUT} = −4 mA	V_{OH}	0.85 V_{DD}			V

Table 15. DIGITAL OUTPUTS WITH OPEN DRAIN: TX_END, TXD

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Low output voltage	I_{XOUT} = 4 mA	V_{OL}			0.4	V

Table 16. DIGITAL INPUTS: BR0, BR1

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Low input level		V_{IL}			0.2 V_{DD}	V
High input level	0 V to 3 V	V_{IH}	0.8 V_{DD}			V
Input leakage current		I_{LEAK}	−10		10	μA

Table 17. DIGITAL INPUTS WITH PULL DOWN: TDI, TMS, TCK, TRSTB, TEST

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Low input level		V_{IL}			0.2 V_{DD}	V
High input level		V_{IH}	0.8 V_{DD}			V
Pull down resistor	(Note 14)	R_{PU}	7		50	kΩ

14. Measured around a bias point of $V_{DD}/2$.

Table 18. DIGITAL SCHMITT TRIGGER INPUTS: RXC, RESB

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Rising threshold level		V_{T+}			2.5	V
Falling threshold level		V_{T-}	0.9			V
Input leakage current		I_{LEAK}	−10		1−	μA

Table 19. DIGITAL INPUT/OUTPUTS OPEN DRAIN: IO0, IO1, IO2

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Low output voltage	I_{COUT} = 4 mA	V_{OL}			0.4	V
Low input level		V_{IL}			0.2 V_{DD}	V
High input level		V_{IH}	0.8 V_{DD}			V
Input leakage current		I_{LEAK}	−10		10	μA

Table 20. CURRENT CONSUMPTION

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Current consumption in receive mode	Current through V_{DD} and V_{DDA} (Note 15)	I_{RX}	60		80	mA
Current consumption in transmit mode	Current through V_{DD} and V_{DDA} (Note 15)	I_{TX}	60		80	mA
Current consumption when RESB = 0	Current through V_{DD} and V_{DDA} (Note 15)	I_{RESET}			4	mA

15. CLKARM is < 12 MHz, fCLK = 24 MHz.

Main Modem Characteristics

Table 21. OPERATING CHARACTERISTICS

Parameter	Value	Unit
Positive supply voltage Negative supply voltage	3.0 to 3.6 −0.7 to + 0.3	V V
Max peak output level	1, 2	Vp
HD2	−60	dB
HD3	−60	dB
ALC Steps	3	dB
ALC Range	(0 ... −21)	dB
Maximum input signal	1, 15	V_p
Input impedance	100	kΩ
Input sensitivity	0.4	mV
AGC steps	6	dB
AGC range	(0 ... +42)	dB
Maximum 50 Hz variation	0, 1	Hz/s
Data rate	300/360 (Note 23) 600/720 (Note 23) 1200/1440 (Note 23) 2400/2880(Note 23)	baud baud baud baud
Programmable carrier (Note 22)		
Frequency band		
Frequency minimum	9	kHz
Frequency maximum	95	kHz
Frequency deviation between pairs	>10	kHz
Dynamic range	40 (Note 17) 60 (Note 18) 80 (Note 19)	dB dB dB
Narrow band interfere BER (Note 20)	10E−5	
Maximum 50 Hz variation	0, 1	Hz/s

16. For the design of the oscillator crystal parameters have been taken from the data sheet [8]. The series loss resistance for this type of crystal is maximum 50 Ω. However the oscillator cell has been designed with some margin for series loss resistance up to 80 Ω.
17. FER = 0%.
18. FER = 0.3%.
19. FER = 8.0%.
20. Signal between −60 dB and 0 dB interference signal level is 30 dB above signal level between 20 kHz and 95 kHz.
21. Input at −40 dB, duty cycle between 10 − 50% pulse noise frequency between 100 to 1000 Hz. BER: Bit error rate FER: Frame error rate (1frame is 288 bits).
22. Carriers frequency is programmable by steps of 10 Hz.
23. 60 Hz mains frequency.

AMIS−49587

INTRODUCTION

GENERAL DESCRIPTION

The AMIS−49587 is a single chip half duplex S−FSK modem dedicated to power line carrier (PLC) data transmission on low− or medium−voltage power lines. The device offers complete handling of the protocol layers from the physical up to the MAC. AMIS−49587 complies with the EN 50065 CENELEC and the IEC 1334−5−1 standards. It operates from a single 3.3 V power supply and is interfaced to the power line by an external power driver and transformer. An internal PLL is locked to the mains frequency (50 Hz or 60 Hz) and is used to synchronize the data transmission at data rates of 300, 600, 1200 and 2400 baud for a 50 Hz mains frequency, corresponding to 3, 6, 12 or 24 data bits per half cycle of the mains frequency (50 Hz or 60 Hz).

S−FSK is a modulation and demodulation technique that combines some of the advantages of a classical spread spectrum system (e.g. immunity against narrow band interferers) with the advantages of the classical FSK system (low complexity). The transmitter assigns the space frequency f_S to "data 0" and the mark frequency f_M to "data 1". The difference between S−FSK and the classical FSK lies in the fact that f_S and f_M are now placed far from each other, making their transmission quality independent from each other (the strengths of the small interferences and the signal attenuation are both independent at the two frequencies). The frequency pairs supported by the AMIS−49587 are in the range of 9−95 kHz with a typical separation of 10 kHz.

The conditioning and conversion of the signal is performed at the analog front−end of the circuit. The further processing of the signal and the handling of the protocol is digital. At the back−end side, the interface to the application is done through a serial interface. The digital processing of the signal is partitioned between hardwired blocks and a microprocessor block. The microprocessor is controlled by firmware. Where timing is most critical, the functions are implemented with dedicated hardware. For the functions where the timing is less critical, typically the higher level functions, the circuit makes use of the ARM 7TDMI microprocessor core.

The processor runs DSP algorithms and, at the same time, handles the communication protocol. The communication protocol, in this application, contains the MAC = Medium Access Control Layer. The program running on the microprocessor is stored into an on−board ROM. The working data necessary for the processing is stored in an internal RAM. At the back−end side the link to the application hardware is provided by a SCI. The SCI is an easy to use serial interface, which allows communication between an external processor used for the application software and the AMIS−49587 modem. The SCI works on two wires: TXD and RXD. Baud rate is programmed by setting 2 bits (BR0, BR1).

Because the low protocol layers are handled in the circuit, the AMIS−49587 provides an innovative architectural split. Thanks to this, the user has the benefit of a higher level interface of the link to the PLC medium. Compared to an interface at the physical level, the AMIS−49587 allows faster development of applications. The user just needs to send the raw data to the AMIS−49587 and no longer has to take care of the protocol detail of the transmission over the specific medium. This last part represents usually 50% of the software development costs.
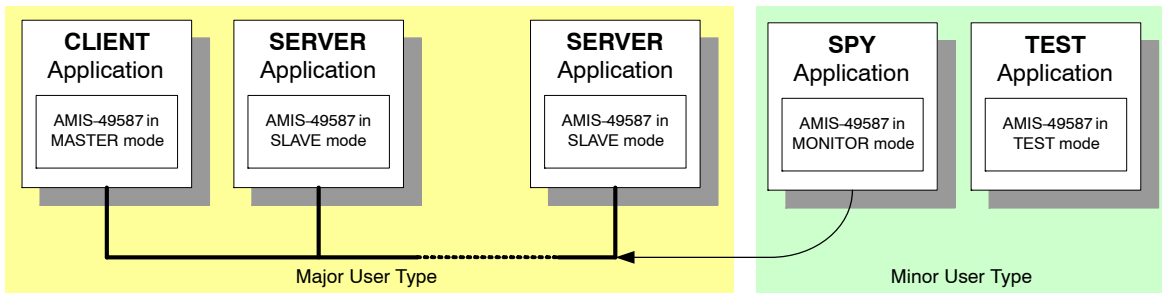

Figure 3. Application Examples

AMIS−49587 is an integrated circuit intended to connect equipment using Distribution Line Carrier (DLC) communication. It serves two major and two minor types of applications:
- Major type:
  - Server Applications which provide resources to a client. A typical application is an electricity meter device equipped for DLC
- Client Applications which exploit remote servers. A typical application is a concentrator system is a
- Minor type:
  - Spy Applications, used to monitor or test DLC communication on the channel.
  - Test Mode, used to test the compliance of a PLC modem conforms to CENELEC. (Continuous broadcast of f_S or f_M).

FUNCTIONAL DESCRIPTION

The block diagram below represents the main functional units of the AMIS−49587:
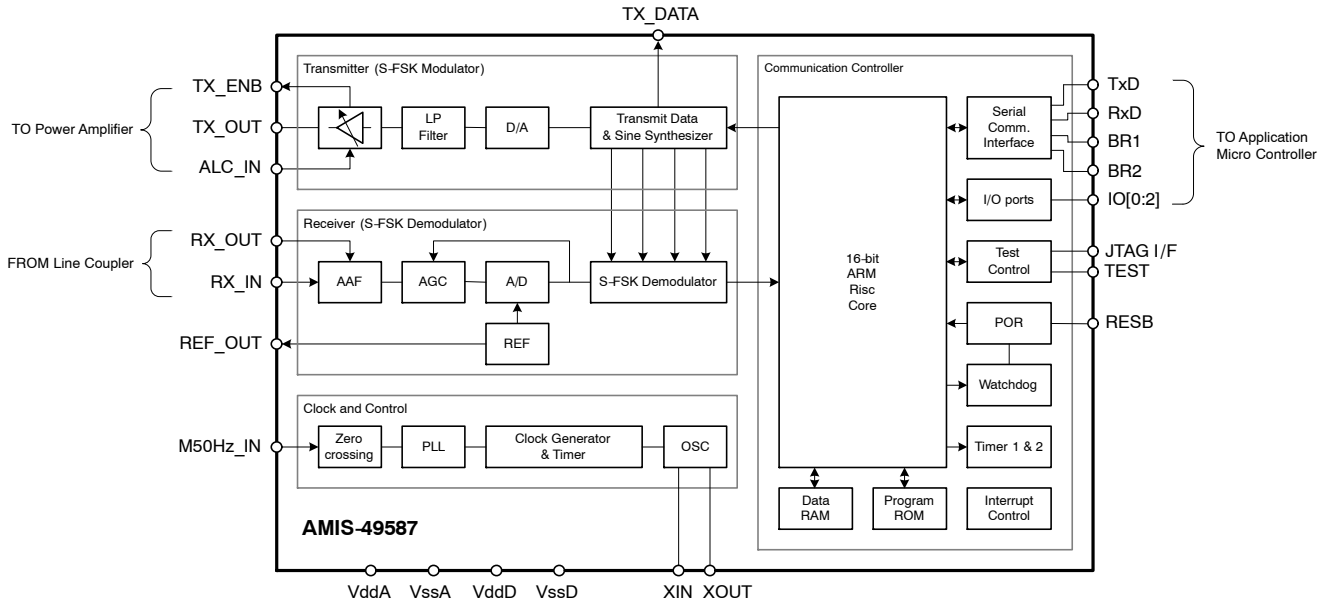

Figure 4. S−FSK Modem AMIS−49587 Block Diagram

Transmitter

The AMIS−49587 Transmitting function block prepares the communication signal which will be sent on the transmitting channel during the transmitting phase. This block is connected to a power amplifier which injects the output signal on the mains through a coupler.

Receiver

The analog signal coming from the line−coupler is low pass filtered in order to avoid aliasing during the conversion. Then the level of the signal is automatically adapted by an automatic gain control (AGC) block. This operation maximizes the dynamic range of the incoming signal. The signal is then converted to its digital representation using sigma delta modulation. From then on, the processing of the data is done in a digital way. By using dedicated hardware, a direct quadrature demodulation is performed. The signal demodulated in the base band is then low pass filtered to reduce the noise and reject the image spectrum.

Clock and Control

According to the IEC standard, the frame data is transmitted at the zero crossing of the mains voltage. In order to recover the information at the zero crossing, a zero crossing detection of the mains is performed. A phase−locked loop (PLL) structure is used in order to allow a more reliable reconstruction of the synchronization. This PLL permits as well a safer implementation of the "repetition with credit" function (also known as chorus transmission). The clock generator makes use of a precise quartz oscillator master. The clock signals are then obtained by the use of a programmed division scheme. The support

circuits are also contained in this block. The support circuits include the necessary blocks to supply the references voltages for the AD and DA converters, the biasing currents and power supply sense cells to generate the right power off and startup conditions.
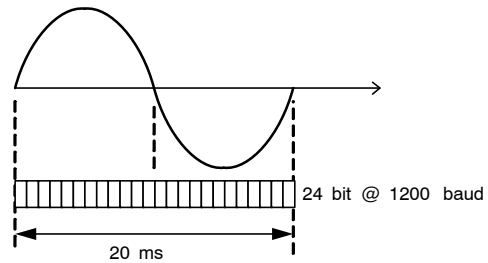

Figure 5. Data Stream is in Sync with Zero Crossings of the Mains

Communication Controller

The Communication Controller block includes the micro−processor, its peripherals: RAM, ROM, UART, TIMER, and the Power on reset. The processor uses the ARM Reduced Instruction Set Computer (RISC) architecture optimized for IO handling. For most of the instructions, the machine is able to perform one instruction per clock cycle. The microcontroller contains the necessary hardware to implement interrupt mechanisms, timers and is able to perform byte multiplication over one instruction cycle. The microcontroller is programmed to handle the physical layer (chip synchronization), and the MAC layer conform to IEC 1334−5−1. The program is stored in a

masked ROM. The RAM contains the necessary space to store the working data. The back−end interface is done through the Serial Communication Interface block. This back−end is used for data transmission with the application micro controller (containing the application layer for concentrator, power meter, or other functions) and for the definition of the modem configuration.

Local Port

The controller uses 3 output ports to inform about the actual status of the PLC communication. IO[0] indicates if Receiving is in progress and is CRC is OK. TX_ENB is an output port for the information about the transmitter enabling. TX_DATA is the output for either the transmitting data (TX_DATA) or a synchronization signal with the time−slots (PRE_SLOT).

Serial Communication Interface

The local communication is a half duplex asynchronous serial link using a receiving input (RxD) and a transmitting output (TxD). The input port IO[2] is used to manage the local communication with the base micro (T_REQ) and the baud rate can be selected depending on the status of two local input ports (BR_0, BR_1). These two inputs are taken in account after a AMIS−49587 reset. Thus when the base micro wants to change the baud rate, it has to set the two inputs and then provoke a reset.

DETAILED HARDWARE DESCRIPTION

TRANSMITTER PATH DESCRIPTION (S−FSK MODULATOR)

For the generation of the tones, the direct digital synthesis of the sine wave frequencies is performed under the control of the microprocessor. After a signal conditioning step, a digital to analog conversion is performed. As for the receive path, a sigma delta modulation technique is used. In the analog domain, the signal is low pass filtered, in order to remove the high frequency quantization noise, and passed to the automatic level controller (ACL) block, where the level of the transmitted signal can be adjusted. The determination of the signal level is done through the sense circuitry.
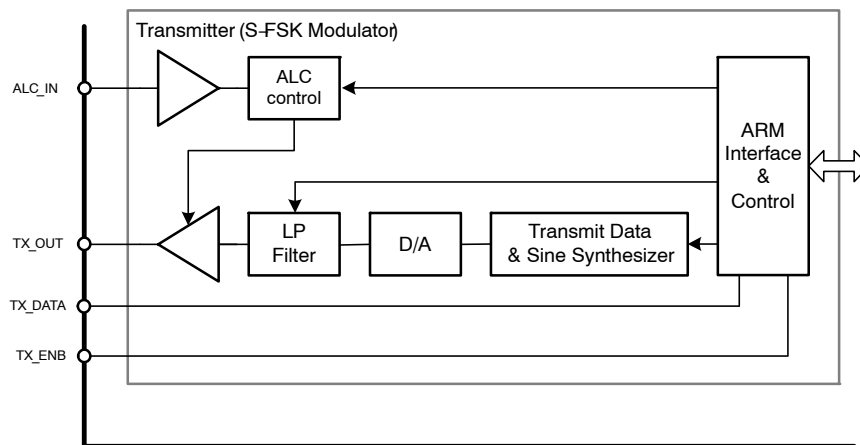

Figure 6. Transmitter Block Diagram

ARM Interface and Control

The interface with the ARM consists in a 8 bit data register, 2 control registers, a flag defining transmit and receive and 2 16 bit wide frequency step registers defining f_M (mark frequency = data 1) and f_S (space frequency = data 0) All these registers are memory mapped.

The transmitter works synchronous with the BIT_CLK and BYTE_CLK signals when the register TX_RXB in R_CONF is logic 1. For good operation TX_RXB must change after an interrupt generated by PRE_BYTE_CLK. The interface between ARM and transmitter is interrupt based. At each BYTE_CLK the data from R_TX_DATA is copied into a buffer register (R_TX_DATA_BUFFER)

The processing of the physical frame (preamble, MAC address, CRC) is done by the ARM

Sine Wave Generator

A sine wave is generated with a direct digital synthesizer DDS. The synthesizer generates in transmission mode a sine wave either for the space frequency (f_S, data 0) or for the mark frequency (f_M, data1). In reception the synthesizer generates the sine and cosine waves for the mixing process, f_{SI}, f_{SQ}, f_{MI}, f_{MQ} (space and mark signals in phase and quadrature). The space and mark frequencies are defined in an individual step 16 bit wide register.

Table 22. SPACE AND MARK FREQUENCY SELECTION (See Appendix C)

ARM Register	Reset	Description
R_FS[15:0]	0000h	Step register for the space frequency f_S
R_FM[15:0]	0000h	Step register for the mark frequency f_M

The space and mark frequency can be calculated as:

• $f_S = R\_FS[15:0]\_dec \times f_{DDS}/2^{18}$

• $f_M = R\_FM[15:0]\_dec \times f_{DDS}/2^{18}$

Or the content of both R_FS[15:0] and R_FM[15:0] are defined as:

• $R\_FS[15:0]\_dec = Round(2^{18} \times f_S/f_{DDS})$

• $R\_FM[15:0]\_dec = Round(2^{18} \times f_M/f_{DDS})$

  ♦ Where f_{DDS} = 3 MHz is the direct digital synthesizer clock frequency.

After a hard or soft reset or at the start of the transmission (when TX_RXB goes from 0 to 1) the phase accumulator must start at it's 0 phase position, corresponding with a 0 V output level. When switching between f_M and f_S the phase accumulator must give a continuous phase and not restart from phase 0.

When AMIS−49587 goes into receive mode (when TX_RXB goes from 1 to 0) the sine wave generator must make sure to complete the active sine period.

The control logic for the transmitter generates a signal TX_ENB to enable the external power amplifier. TX_ENB is 1 when the AMIS−49587 is in receive mode. TX_ENB is 0 when AMIS−49587 is in transmit mode. When going from transmit to receive mode (TX_RXB goes from 1 to 0) the TX_ENB signal is kept active for a short period of t_{dTX_ENB}.

The control logic for the transmitter generates a signal TX_DATA which corresponds to the transmitted SFSK signal. When transmitting f_M TX_DATA is logic 1. When transmitting f_S TX_DATA is logic 0. When the transmitter is not enabled (TX_RXB = 0) TX_DATA goes to logic 1 at the next BIT_CLK.
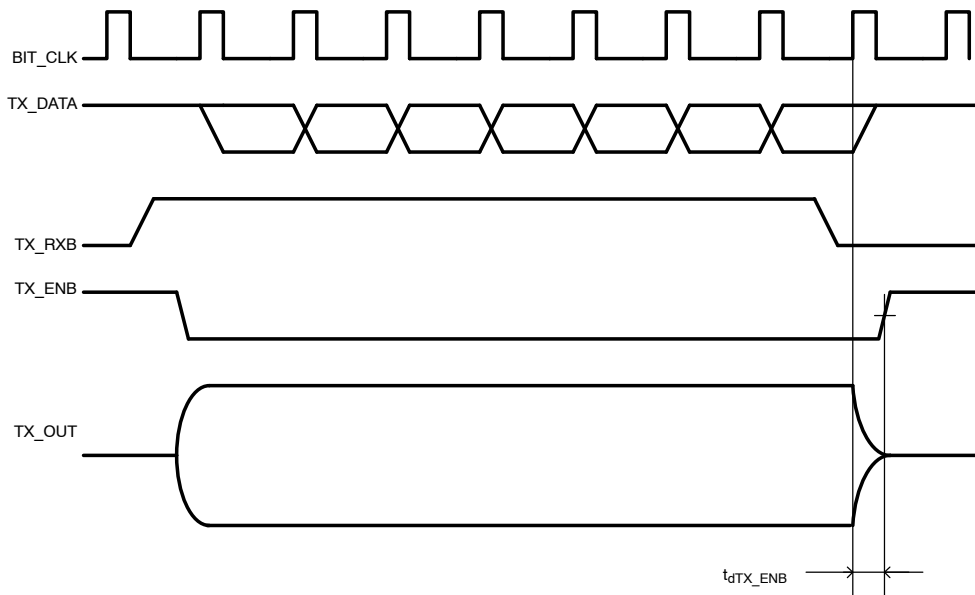

Figure 7. TX_ENB Timing

DA Converter

A digital to analog $\Sigma\Delta$ converter converts the sine wave digital word to a pulse density modulated (PDM) signal. The PDM signal is converted to an analog signal with a first order switched capacitor filter.

Low Pass Filter

A 3rd order continuous time low pass filter in the transmit path filters the quantization noise and noise generated by the $\Sigma\Delta$ DA converter. The low pass filter has a circuit which tunes the RC time constants of the filter towards the process characteristics. The C values for the LPF filter are controlled by the ARM micro controller.

Amplifier with Automatic Level Control (ALC)

The pin ALC_IN is used for level control of the transmitter output level. First a peak detection is done. The peak value is compared to 2 thresholds levels: VTL_{ALC_IN} and VTH_{ALC_IN}. The result of the peak detection is used to control the setting of the level of TX_OUT. The level of TX_OUT can be attenuated in 8 steps of 3 dB typical.

After hard or soft reset the level is set at minimum level (maximum attenuation) When going to reception mode (when TX_RXB goes from 1 to 0) the level is kept in memory so that the next transmit frame starts with the old

level. The evaluation of the level is done during 1 CHIP_CLK period.

Depending on the value of peak level on ALC_IN the attenuation is updated:

− $Vp_{ALC\_IN} < VTL_{ALC}$: Increase the level with 1 step
− $VTL_{ALC} \leq Vp_{ALC\_IN} \leq VTH_{ALC}$: Don't change the level
− $Vp_{ALC\_IN} > VTH_{ALC}$: Decrease the level with 1 step

The gain changes in the next CHIP_CLK period.

An evaluation phase and a level adjustment takes 2 CHIP_CLK periods. ALC operation is enabled only during the first 16 CHIP_CLK cycles after a hard or soft reset or after going into transmit mode.

The automatic level control can be disabled by the ARM by setting R_ALC_CTRL[3] to 1. In case the transmitter outputs the programmed level in the register R_ALC_CTRL[2:0]. See Appendix C.

The analog part of AMIS−49587 works with an analogue ground REF_OUT. When connecting AMIS−49587 to external circuitry working with another ground one must make sure to place a decoupling capacitor.

RECEIVER PATH DESCRIPTION

Receiver Block Diagram

The receiver section is active when TX_RXB = 0. The operation mode and the baud rate are made according to the setting in R_CONF[9:0], R_FS[15:0] and R_FM[15:0]. See Appendix C. The receive signal is applied first to a high pass filter. Therefore AMIS−49587 has a low noise operational amplifier at the input stage which can be used to make a high pass active filter to attenuate the mains frequency. This high pass filter output is followed by a gain stage which is used in an automatic gain control loop. This block also performs a single ended input to differential output conversion. This gain stage is followed by a continuous time low pass filter to limit the bandwidth. A 4th order sigma delta converter converts the analog signal to digital samples. A quadrature demodulation for f_S and f_M is than performed by the ARM micro, as well the handling of the bits and the frames.
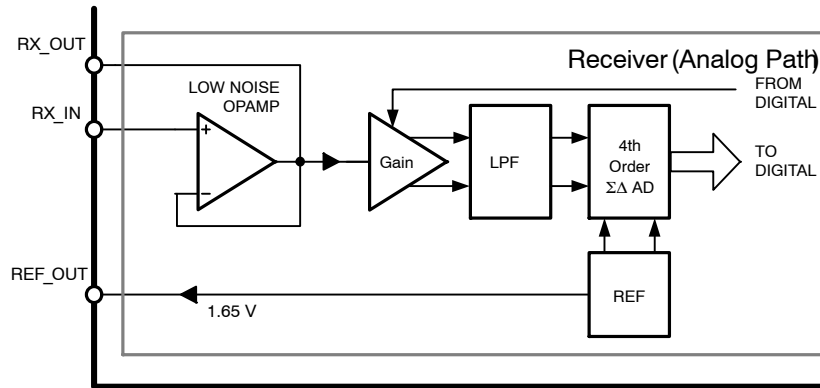

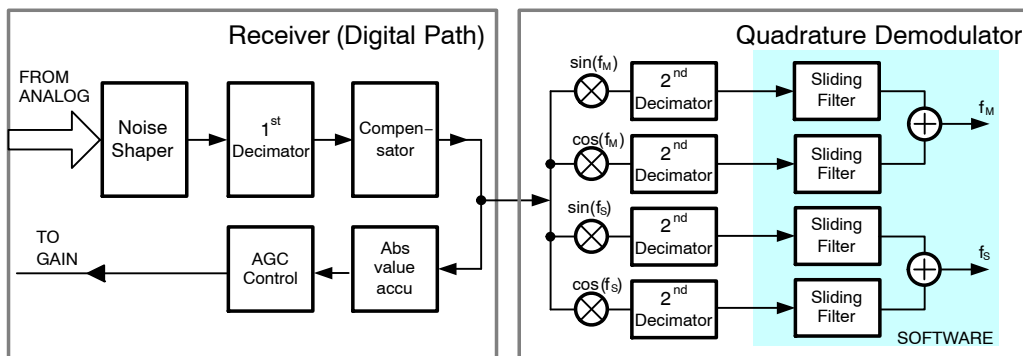**Figure 8. Analog Path of the Receiver**

Figure 9. Digital Path of the Receiver ADC and Quadrature Demodulation

50/60 Hz Suppression Filter

AMIS−49587 receiver input provides a low noise input operational amplifier in a follower configuration which can be used to make a 50/60 Hz suppression filter with a minimum number of external components. This low noise operational amplifier is enabled when R_RX_MOD[7] = 0. See Appendix C. The pin RX_IN is the positive input and RX_OUT is the output of the input low noise operational amplifier. The pin REF_OUT can be use as an analog ground (1.65 V) for the external circuitry.
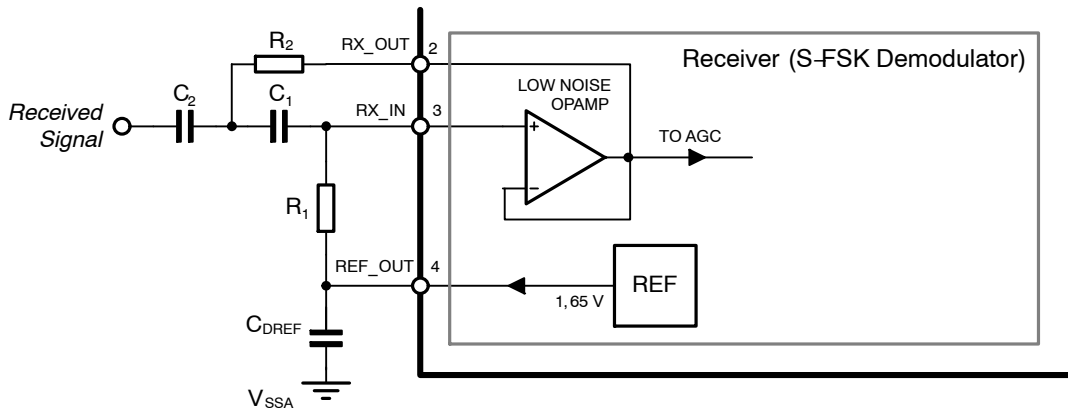
Figure 10. External Component Connection for 50/60 Hz Suppression Filter

RX_IN is the positive analog input pin of the receiver low noise input op−amp. Together with the output RX_OUT an active high pass filter is realized. This filter removes the main frequency (50 Hz or 60 Hz) from the received signal. The filter characteristics are determined by external capacitors and resistors. Typical values are given in Table 23. For these values and after this filter, a typical attenuation of 80 dB at 50 Hz is obtained. Figure 9 represents external components connection. In a typical application the coupling transformer in combination with a parallel capacitance forms a high pass filter with a typical attenuation of 60 dB. The combined effect of the two filters decreases the voltage level of 230 Vrms at the mains frequency well below the sensitivity of the AMIS−49587.
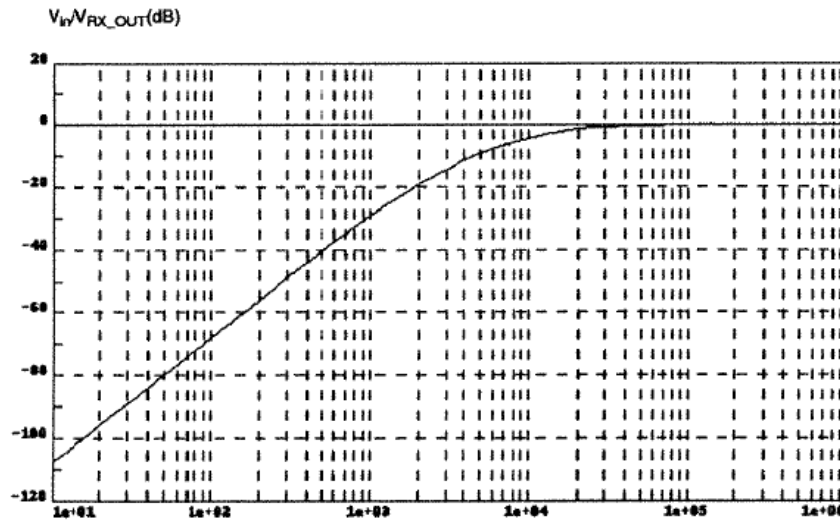

Figure 11. Transfer Function of 50 Hz Suppression Circuit

REF_OUT is the analog output pin which provides the voltage reference used by the A/D converter. This pin must be decoupled from the analog ground by a 1 μF ceramic capacitance (C_{DREF}). It is not allowed to load this pin.

The low noise operational amplifier can be bypassed and powered down by setting the bit R_RX_MOD[7] to 1. In this mode the pin RX_OUT must be used as input of the AGC.

Table 23. VALUE OF THE RESISTORS AND CAPACITORS

Component	Value	Unit
C_1	1.5	nF
C_2	1.5	nF
C_{DREF}	1	μF
R_1	22	kΩ
R_2	11	kΩ

The analog part of AMIS−49587 works with an analog ground of REF_OUT

CLOCK AND CONTROL

Oscillator

The oscillator works with a standard parallel resonance crystal of 24 MHz. XIN is the input to the oscillator inverter gain stage and XOUT is the output.
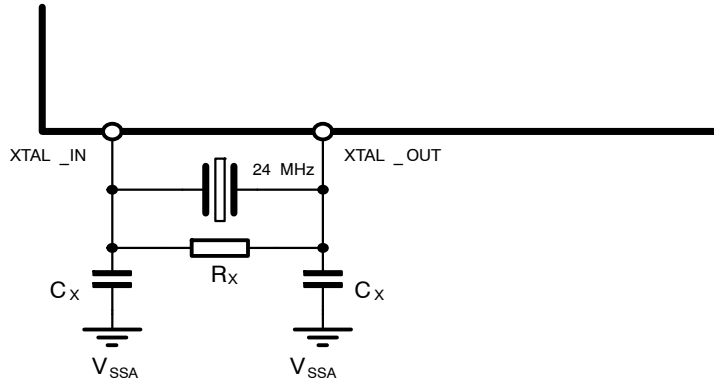

Figure 12. Placement of the Capacitors and Crystal with Clock Signal Generated Internally

For correct functioning the external circuit illustrated in Figure 12 must be connected to the oscillator pins. For a crystal requiring a parallel capacitance of 20 pF C_X must be around 30 pF. (Values of capacitors are indicative only and are given by the crystal manufacturer). To guarantee startup the series loss resistance of the crystal must be smaller than 80 Ω.

A parallel resistor $R_X = 1$ MΩ is recommended to improve the clock symmetry.

Zero Crossing Detector

M50HZ_IN is the mains frequency analog input pin – 50 or 60 Hz. This pin is used to detect the crossing of the zero voltage on one selected phase. This information is used, after filtering with the internal PLL, to synchronize frames with the mains frequency. In case of direct connection to the mains, the use of a series resistor of 1 MΩ is advised in order to limit the current flowing through the external protection diodes. The zero crossing detector output is logic zero when the input is lower than the falling threshold level and a logic one when the input is higher than the rising threshold level. The falling edges of the output of the zero crossing detector are filtered by a period between 0.5 ms and 1 ms. Rising edges are not filtered.

COMMUNICATION CONTROLLER

Serial Communication Interface (SCI)

The SCI allows asynchronous communication. It can communicate with a UART = Universal Asynchronous Receiver Transmitter, ACIA = Asynchronous Communication Interface Adapter and all other chips that employ standard asynchronous serial communication. The serial communication interface allows only half duplex communication.
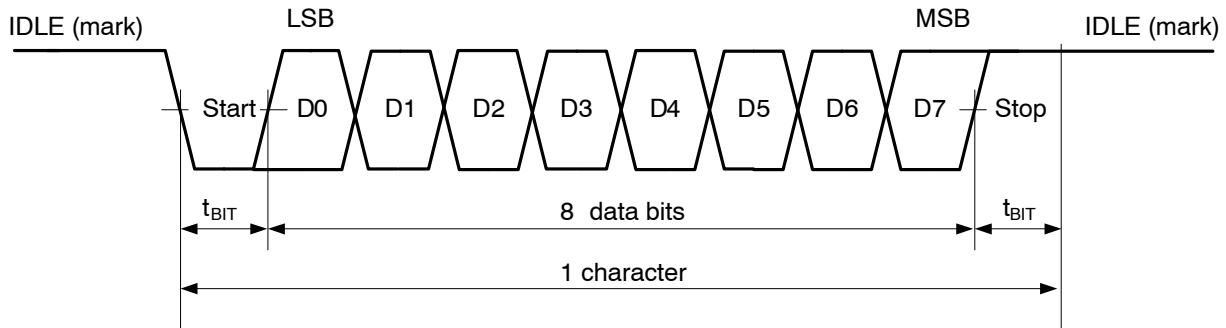

Figure 13. Data Format

The transmitting has the following characteristics:
- Half duplex.
- Standard NRZ format.
- Start bit, 8 data bits and 1 stop bit.

- Hardware programmable baud−rate (4800, 9600, 19200 and 38400 baud).
- 0−5 V levels with open drain for TxD.
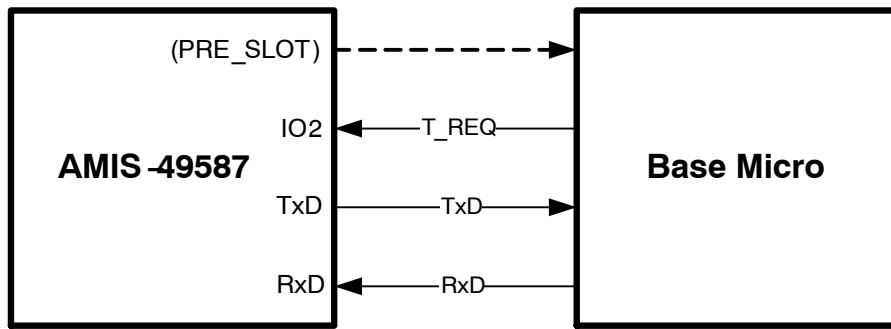- 0−5 V levels for RxD and T_REQ.

Figure 14. Connection to the Application Microcontroller

SCI Physical Layer Description

The following pins control the serial communication interface.

TXD: Transmit data output. It is the data output of the AMIS−49587 and the input of the base micro.

RXD: Receive data input. It is the data input of the AMIS−49587 and the output of the base micro.

BR0, BR1: Baud rate selection inputs. These pins are externally strapped to a value or controlled by the external base microcontroller.

Table 24. BR1, BR0 BAUD RATES

BR_1	BR_0	Baud rate
0	0	4800 baud
0	1	9600 baud
1	0	19200 baud
1	1	38400 baud

Arbitration and Transfer

In order to avoid collisions between the data sent by the AMIS−49587 and the base micro, the AMIS−49587 is chosen as the transmitting controller. This means that when there is no local transfer, the AMIS−49587 can initiate a local communication without taking account of the base micro state. In the other hand, when the base micro wants to send data (using a local frame), it must first send a request for communication through the local input port named T_REQ (Transmitting Request). Then the AMIS−49587 answers with a status message that contains information about the possibility of receiving a MA_Data_Request encapsulated in a local frame. **The AMIS−49587 is the communication controller and has priority in a communication**. This means that as soon as the AMIS−49587 wants to send a local frame (e.g. a local frame including a MA_Data_Indication), if the local communication channel is available (no local transfer has already begun), it can send this local frame.

If the status message indicates a PLC buffer unavailable when the base micro wants to send a MA_Data_Request encapsulated in a local frame, this local frame will be answered by a Confirm « Resource Unavailable » if the base micro insists to send it.

Transfer from Base Micro to AMIS−49587

When the base micro wants to initiate a local transfer, it must pull down the T_REQ signal. The AMIS−49587 answers within the Tpoll delay with the status message in which the base micro can read if the communication channel is available.

If the communication is possible, the base micro can start to send its local frame within the Tsr delay. It should pull up the T_REQ signal as soon as the first character (STX) has been sent. If the beginning of the local frame is not received before the Tsr delay was issued, the AMIS−49587 ignores the local frame.

Remark: If the base micro only wants to know the state of the AMIS−49587, it has just to pull up the T_REQ signal after the reception of the status message.

At the end of the data reception sent by the base micro on the RxD line, the AMIS−49587 sends a byte on the TxD line in order to inform about the status of the transmitting (ACK or NAK).
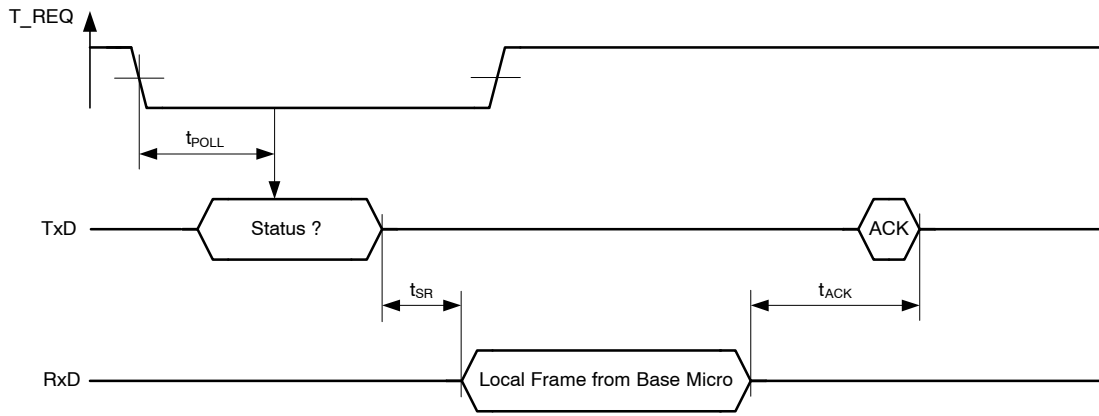
Figure 15. Transfer from Base Micro to AMIS−49587

If the length and the checksum of the local frame are both correct, the AMIS−49587 acknowledges with an <ACK> character. In other cases, it answers with a <NAK> character. In case of <NAK> response, or no acknowledgement from AMIS−49587 in the Tack time−out, a complete sequence must be restarted to repeat the frame.

Transfer from AMIS−49587 to Base Micro

When the AMIS−49587 wants to send a frame, it can directly send it without any previous request.
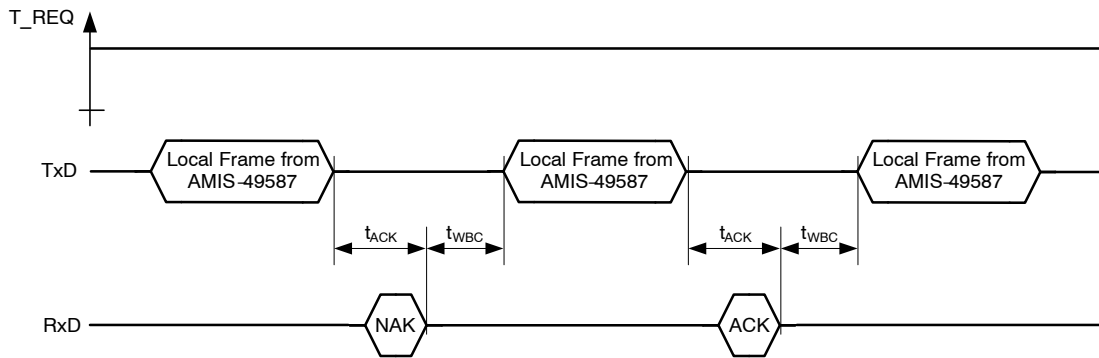

Figure 16. Transfer from AMIS−49587 to Base Micro

If the length and the checksum of the local frame are both correct, the base micro acknowledges with an <ACK> character. In other cases, it answers with a <NAK> character. In case of <NAK> response from the Base Micro, the AMIS−49587 will repeat the frame only once after a delay corresponding to Twbc (Wait Before Continue). A non response from the base micro or a framing error when an

<ACK> character is awaited is considered as an acknowledgment.

Character Time−out in Reception

The time between two consecutive characters in a local frame should not exceed Time−out Inter Character (TIC):
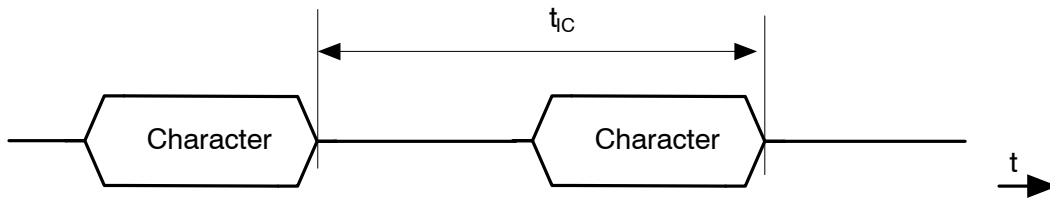

Figure 17. Character Time−Out

After this delay, the frame reception is finished. If the length and the checksum are both correct, the local frame is taken in account otherwise all previous characters are

discarded. The Time−Out Inter Character (TIC) is set by default at 10 ms after a reset. The time out Inter character

(TIC) is modified by the bit 7 of repeater parameter in the configuration frame :

- bit 7 = 1 −> the TIC value is constant at 10 ms,
- bit 7 = 0 −> the TIC value represents 5 characters depending on the communication speed (defined by two local input ports BR0 and BR1).

See Appendix E: timings for Time−out values.

RESET AND LOW POWER

DETAILED SOFTWARE DESCRIPTION

DESCRIPTION

The AMIS−49587 software interface performs the time−out handling, the error checking, the acknowledgment and the reception mechanism. The reception mechanism insures that no collision will occur on the half duplex data channel. The error checking handles several controls (checksum frame, length of the frame and command syntax); an error can provoke repetitions (the base micro has to choose how many repetitions should be done). The AMIS−49587 resources are available via local commands, using the local communication serial interface. All data exchanged between the AMIS−49587 and the users should comply with the local communication protocol.

PROTOCOL

The AMIS−49587 and its base micro share a serial bus to communicate locally. The arbitration of this bus is performed by the AMIS−49587. The AMIS−49587 can directly transmit local frame to the base micro, but the base micro should never transmit local frame without authorization given by the AMIS−49587 (transmitted in the status message).

- A **Not Set AMIS−49587** only accepts the LTC requests (Reset_Request, TestMode_Request, WriteConfig_Request and WriteConfigNew_Request).
- A **Master AMIS−49587** accepts the LTC Reset_Request, WriteConfig_Request and WriteConfigNew_Request, the DB requests, the MAC requests and the ISA requests.
- A **Slave AMIS−49587** has got two different internal states. It could react differently with the base micro requests in function of these states:
  - ♦ Not Synchronized with the mains: it only accepts the LTC Reset_Request, WriteConfig_Request and WriteConfigNew_Request, and the DB requests.
  - ♦ Synchronized: it accepts the LTC Reset_Request, WriteConfig_Request and WriteConfigNew_Request, the DB requests, the MAC requests and the ISA requests.
- A **Monitor AMIS−49587** accepts the LTC Reset_Request, WriteConfig_Request and WriteConfigNew_Request, and the DB requests. When it is synchronized it supplies the SPY local frames.

Remark: On the AMIS−49587 version 4, the WriteConfig_Request or WriteConfigNew_Request can be sent even if the AMIS−49587 is not in the « Not Set » state. It is not necessary to reset the AMIS−49587 before sending a WriteConfig_Request any more (NB: this is only available on AMIS−49587 version 4 and certain conditions must be respected, see Sections WriteConfig_Request (Tag 31h) and WriteConfigNew_Request (Tag 71h)).

STATUS MESSAGE

Time Slot Counter in Status Message

The base micro has no information about the availability of the mains. To solve this problem, the AMIS−49587 supplies a hardware time−slot signal (PRE_SLOT) and a time−slot counter information included in the status message. This time−slot counter allows to the base micro to set its own counter (increased using the hardware time−slot signal). This time−slot counter is reset at the end of a communication (end of receiving, end of transmitting or end of repetition), one time−slot before the first one available for another communication (see figures below). Following time−slots are numbered from 1 to 7. The initial value of the time−slot counter is 7 ("unusable" value). The time−slot counter takes this initial value at the repetition beginning. To obtain a coherent value for the time−slot counter, the reading of the status message must be synchronized with the hardware pre−slot signal. A time−slot counter value equal to zero corresponds to the time−slot just before the first one supposed available (TSC = 1). It informs the base micro that the AMIS−49587 is ready to accept any MA_Data_Request. The following draws show how the time slot counter works:
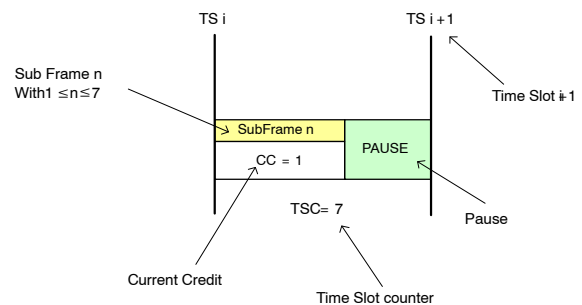

Figure 18. Time Slot Legends

Status Message in NOT SET MODE:

Table 25. STATUS MESSAGE IN NOT SET MODE

Byte	Content	Structure							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Start	0	0	1	1	1	1	1	1
2	Data 1	x	x	x	x	x	x	Not SET	X
3	Data 2	RSV[7:0]							
4	Data 3	SVN[7:4]				SVN[3:0]			

Where:

Not SET	Indication is AMIS 49587 is set
RSV[7:0]	Reserved
SVN[7:4]	Software Version Number: major release
SVN[3:0]	Software Version Number: minor release
x	Not Used

Status Message in SLAVE MODE:

Table 26. STATUS MESSAGE IN SLAVE MODE

Byte	Content	Structure							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Start	0	0	1	1	1	1	1	1
2	Data 1	x	x	x	Not LOCKED	NEW	Not SYNC	Not SET	Buffer BUSY
3	Data 2	TS_Nb[2:0]			x	x	x	ALARM _EN	PLL _LOCK
4	Data 3	DEP[2:0]			MDC[2:0]			REP[1:0]	

Where:

Not LOCKED	Indication if AMIS 49587 is Unlocked
NEW	Indication if AMIS 49587 is New (see definition Section OSI Architecture of AMIS−49587)
Not SYNC	Indication of synchronization with mains
Not SET	Indication if AMIS 49587 is set
Buffer BUSY	Indication if PLC buffer is busy
TS_Nb[2:0]	Time slot counter
Alarm_EN	Alarm detection status
PLL_LOCK	PLL lock status
DEP[2:0]	Delta Electrical Phase
MDC[2:0]	Minimum Delta Credit Value
REP[1:0]	Repeater Mode
x	Not Used

AMIS−49587

Status Message in MASTER MODE:

Table 27. STATUS MESSAGE IN SLAVE MODE

Byte	Content	Structure							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Start	0	0	1	1	1	1	1	1
2	Data 1	x	x	x	x	x	Not SYNC	Not SET	Buffer BUSY
3	Data 2	TS_Nb[2:0]			x	x	x	ALARM _EN	PLL _LOCK
4	Data 3	InvalFrCnt[7:0]							

Where:

Not SYNC	Indication of synchronization with mains
Not SET	Indication is AMIS 49587 is set
Buffer BUSY	Indication if PLC buffer is busy
TS_Nb[2:0]	Time slot counter
Alarm_EN	Alarm detection status
PLL_LOCK	PLL lock status
InvalFrCnt[7:0]	Invalid Frame counter
x	Not Used

Status Message in MONITOR MODE:

Table 28. STATUS MESSAGE IN SLAVE MODE

Byte	Content	Structure							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Start	0	0	1	1	1	1	1	1
2	Data 1	x	x	x	x	x	Not SYNC	Not SET	Buffer BUSY
3	Data 2	TS_Nb[2:0]			x	x	x	ALARM _EN	PLL _LOCK
4	Data 3	DEP[2:0]			x	x	x	x	x

Where:

Not SYNC	Indication of synchronization with mains
Not SET	Indication is AMIS 49587 is set
Buffer BUSY	Indication if PLC buffer is busy
TS_Nb[2:0]	Time slot counter
Alarm_EN	Alarm detection status
PLL_LOCK	PLL lock status
DEP[2:0]	Delta Electrical Phase
x	Not Used

GENERAL DESCRIPTION OF THE FRAME FORMAT

The frame format is the same in both directions:

<STX>	Length	Command	User_Data	CHK
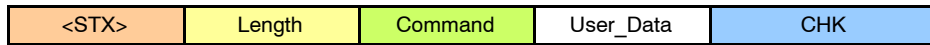
The fields are:

Table 29. LOCAL FRAME DESCRIPTION

Field	Byte Length	Value	Description
<STX>	1	02h	Start of text delimiter
Length	1	03h .. 250	Length of the Command, UserData fields and CHK.
Command	1	00h .. FEh	Command code (Command Codes)
User_Data	0..247	Byte String	Zero to 247 data bytes.
CHK	2	0000h .. 65535	The checksum of the local frame is the result of the addition of the elements of the frame, from length up to the last UserData byte, or up to the Command byte if there is no UserData byte. The CHK is sent with LSB first.

Remark: As soon as a numeric value is greater than one byte (word, long...) it has to be sent in little endian format, that means LSByte first.

AMIS−49587 USERS MODES

NOT SET MODE

In Not Set mode operation the AMIS−49587 software has no configuration and waits for it. The AMIS−49587 is in this mode after a power down or after a reset request.

MASTER MODE (CLIENT)

In MASTER mode operation the AMIS−49587 software should only know its own address (Local MAC address). The Initiator address (Initiator MAC address) is not used and initialized with the NOBODY address (000h).

The Local MAC Address is in the range defined with the WriteConfig_Request command (FIMA/LIMA).

SLAVE MODE (SERVER)

In the Application layer there is a SMAE (system management application entity) which handles the server recording. A server is New when it starts for the first time or when the time−out not addressed has expired without a dedicated call for it. Thus its local MAC address is equal to NEW (FFE hex). After a power−up or a reset the AMIS−49587 does not know its previous setup. Then it informs the base micro it needs to be set by putting the bit « NotSet » in the status message. The base micro has to set the AMIS−49587 with the correct values using the WriteConfig_Request command. When a remote station is New (and then Unlocked), its Initiator MAC address is equal to 000h. After registration this address should be in the range FIMA/LIMA.

MONITOR MODE (SPY)

In MONITOR mode operation the AMIS−49587 software works only in receiving mode and supplies to the base micro all the physical sub−frames which have a good preamble and SSD.

APPLICATION EXAMPLES FOR ADDRESS MAC RANGE

Unlocked means that a Server has an Initiator MAC address equal to NOBODY. Locked means that a Server has a correct Initiator MAC address different from NOBODY. Therefore this slave will only answer to this initiator.

Table 30. MAC ADDRESS RANGE

Application	Mode	Local MAC Address	Initiator MAC Address
AMDES	Client	400 to FEF	000
	Server New & Unlocked Not New & Locked	FFE 1 to 3FF	000 400 to FEF
BMS	Client	C00 to DFF	000
	Server New & Unlocked New & Locked Not New & Locked	FFE FFE 1 to BFF and E00 to FFB	000 C00 to DFF C00 to DFF 000
ICC	**Client**	400 to FEF	000
	Server New & Unlocked New & Locked Not New & Locked	FFE FFE 1 to 3FF	000 400 to FEF 400 to FEF

OSI ARCHITECTURE OF AMIS−49587

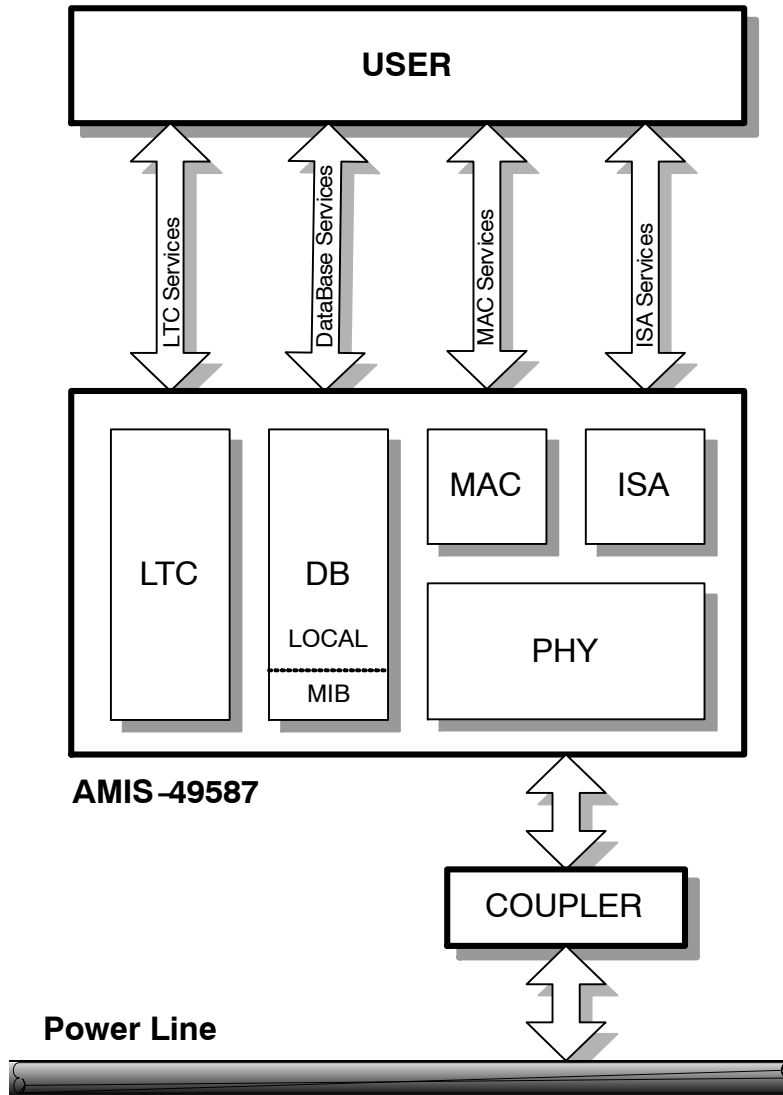The following figure represents the OSI architecture of the AMIS−49587.

Figure 19. OSI Architecture of AMIS−49587

LOCAL TRANSFER AND CONFIGURATION COMMANDS (LTC)

DESCRIPTION

The Local Transfer and Configuration Commands (LTC) supplies the following services:

- **WriteConfigNew_Request**: This command is used by the Base Micro to set the configuration in the AMIS−49587. The AMIS−49587 does not need to be reset before but some parameters cannot be changed without a reset

- **WriteConfigNew_Confirm**: This command is sent by the AMIS−49587 to answer to a correct WriteConfigNew_Request. Its data is the result of the memory and register reading.
  WriteConfigNew_Error: This commands is sent by the AMIS−49587 to answer to an incorrect WriteConfigNew_Request. It contains an Error_Code that indicates which error has been detected.

- **TestMode_Request**: This command is used by the Base Micro to put the AMIS−49587 in a special mode. It is used to perform tests on emission level.

- **Reset_Request**: The Reset_Request is used to reset the AMIS−49587 by software when the Base Micro wants to do it.

- **Synchro_Indication**: This command is sent by the AMIS−49587 to inform about the new synchronization state. Three possibilities could be performed: synchronization found, synchronization confirmed, and synchronization lost. Specific data are associated with each command.

- **Desynchro_Request**: This command is used by the Base Micro to set the AMIS−49587 in the not synchronized state and therefore it starts looking for the synchronization.

CONFIGURATION COMMANDS

Description

The configuration allows to send to AMIS−49587 all the parameters it needs to work correctly. Most of these parameters are also accessible by a WriteDB_request.

The configuration version 3 is the same as the one used on the previous versions of AMIS−49587, but some additional functionalities are available. To ensure a perfect compatibility with the old versions, make sure that:

- the bits corresponding to the number of alarm repetitions are set to 0 (to disable the alarm functionality)

- the bit corresponding to Bad CRC Frame transmitting is set to 0 (to disable this functionality)

- The bits corresponding to the baudrate are set to 10 for 1200 bauds (since 11 will put the AMIS−49587 at 2400 bauds)

- The bits corresponding to the Search Method and SINC Filter are set to 0

- Intelligent synchronization

The configuration version 4 enables is a bit different than the version 3, and it enables one more functionality : the intelligent synchronization. All the new functionalities are also available with this configuration as well as with configuration version 3.

WriteConfigNew_Request (Tag 71h)

Description: The field Data_Config contains the future configuration of the AMIS−49587 (36 bytes). This field is structured as shown in 7.4.4.

Syntax: **Not Set**

Initiator	Command (arguments)	Possible Response
Base Micro	WriteConfigNew_Request (Data_Config)	WriteConfigNew_confirm (Data_Config_Echo) WriteConfigNew_Error (Error_Code)

Since the AMIS−49587 has no non−volatile RAM memory, the information about the chip configuration are lost after each hard or soft reset and also after a power up.

Therefore the AMIS−49587 software waits for a WriteConfig_Request or WriteConfigNew_Request after each reset. The software remains in this state until the configuration is correctly received.

Frame Format:

<STX>	Length	<WriteConfigNew_Request>	Data_Config	CHK
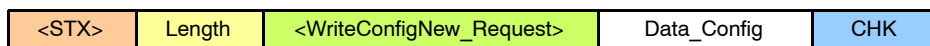
Notice: New Functionality: This command can be used to modify several parameters of the AMIS−49587 at the same time, even if AMIS−49587 is configured yet. This avoids the use of several successive Write_Db.Request. If the AMIS−49587 is set yet, some parameters cannot be changed any more and won't be taken into account. The AMIS−49587 will return a WriteConfig_Error if the Base Micro tries to modify one of these parameters:

Table 31. NON CHANGEABLE PARAMETERS AFTER AMIS 49587 IS SET

| Field	Length	Value	Description
R_CONF_TX_DATA_PRE_SLOT_SEL	1 bit (b7)	x	No action
Pad	1 bit (b6)	x	No action
R_CONF→MODE	3 bits (b5 to b3)	xxx	No action
R_CONF→BAUDRATE	2 bits (b2,b1)	xx	No action
R_CONF→MAINS_FREQ	1 bit (b0)	x	No action

WriteConfigNew_Confirm (Tag 72h)
Description: The WriteConfigNew_Confirm is sent by the AMIS−49587 in order to indicate that the AMIS−49587 configuration has been written in registers and Data Base locations.
The field Data_Config_Echo is the configuration copy read in the AMIS−49587 registers. So the base micro can check if the configuration recorded in the AMIS−49587 is correct. Its structure is the same as Data_Config (see Section WriteConfigNew_Request (Tag 71h)).

Syntax: **Master/Slave/Monitor**

Initiator	Command (arguments)	Possible Response
AMIS−49587	WriteConfigNew_Confirm (Data_Config_Echo)	

Frame Format:

| <STX>	Length	<WriteConfigNew_Confirm>	Data_Config_Echo	CHK
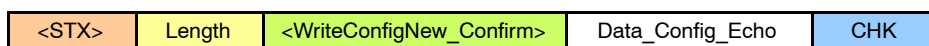
WriteConfigNew_Error (Tag 73h)
Description: The WriteConfigNew_Error is sent by the AMIS−49587 in order to indicate that the previous configuration received by the AMIS−49587 has not been memorized due to an error in its data. This error is due either to a bad MAC address or a Mode test.

Syntax: **Master/Slave/Monitor**

Initiator	Command (arguments)	Possible Response
AMIS−49587	WriteConfigNew_Error (Error_Code)	

Frame Format:

<STX>	Length	< WriteConfigNew_Error>	Error_Code	CHK
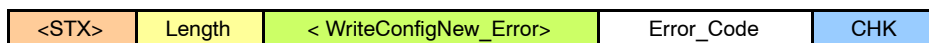
General description of WriteConfigNew_Request
Table 32. GENERAL DESCRIPTION OF WRITECONFIGNEW_REQUEST

Field	Length	Value	Description
First Initiator MAC Address (FIMA)	2 bytes	0001 to 0FFF XXXX	Slave: First value for Initiator MAC address Master & Monitor: don't care
Last Initiator MAC Address (LIMA)	2 bytes	0001 to 0FFF XXXX	Slave: Last value for Initiator MAC address Master & Monitor: don't care
Local MAC Address	2 bytes	0FFE or 0001 to (FIMA−1) FIMA to LIMA XXXX	Slave Mode : New Slave (Registered) Master Monitor
Active Initiator Address	2 bytes	0000 FIMA to LIMA XXXX	Master, Slave (unlocked) Slave (locked on an initiator) Monitor
Time−out−synchro−confirm	2 bytes	0000 to FFFF	Slave: In seconds. (Not used in Master mode)
Time−out−frame−not−ok	2 bytes	0000 to FFFF	Slave: In seconds (Not used in Master mode)
Time−out−not−addressed	2 bytes	0000 to FFFF	Slave : In minutes (Not used in Master & Monitor mode)

Table 32. GENERAL DESCRIPTION OF WRITECONFIGNEW_REQUEST

Field	Length	Value	Description
Mac−group−addresses	10 bytes	0000 to 0FFF	Slave: 5 MAC group addresses (Not used in Master mode)
Fs	2 bytes	0000 to FFFF	Step Register for the Space Frequency Fs
Fm	2 bytes	0000 to FFFF	Step Register for the Mark Frequency Fm
R_ZC_ADJUST	1 byte	00 to FF	Value according to the voltage level of the 50 Hz information for the input of the PLL.
NbAlarm	4 bits (b7 to b4)	XXXX 0000	Number of repetitions of a Phy Alarm Disable Phy Alarm functionality
R_ALC_CTRL→Value Max_Transmistting_Gain→Value	3 bits (b3 to b1)	XXX	Attenuation value in fixed mode
R_ALC_CTRL→Value Max_Transmistting_Gain→Mode	1 bit (b0)	0 1	Automatic level control Fixed mode
R_CONF_TX_DATA_PRE_SLOT_SEL	1 bit (b7)	0 1	The output pin is the PRE_SLOT signal or Mode = Master The output pin is the transmitted DATA (for.Radio)
Pad	1 bit (b6)	0	This bit is not used (adjust length at 1 byte)
R_CONF→MODE	3 bits (b5 to b3)	001 010 011	Master mode for client station Slave mode for server station Monitor mode to spy and test of the DLC communication
R_CONF→BAUDRATE	2 bits (b2,b1)	00 01 10 11	300 baud @ 50 Hz or 360 baud @ 60 Hz 600 baud @ 50 Hz or 720 baud @ 60 Hz 1200 baud @ 50 Hz or 1440 baud @ 60 Hz 2400 baud @ 50 Hz or 2880 baud @ 60 Hz
R_CONF→MAINS_FREQ	1 bit (b0)	0 1	mains frequency = 50 Hz mains frequency = 60 Hz
Pad	1 bit (b7)	0	This bit is not used (adjust length at 1 byte)
Search method	2 bits (b6, b5)	0 1	Method V6 Method V3
SINC Filter	1 bit (b5)	0 1	Disabled (1111) Enabled (1331)
SYNCHRO−Type→Mode	1 bit (b4)	0	Must be set to 0 (Synchronization on sub−frame preamble)
SYNCHRO−Bit→Value	3 bits (b3 to b1)	XXX	Synchro−bit value (in chip clock) in fixed mode
SYNCHRO−Bit→Mode	1 bit (b0)	1	Must be set to 1 (Fixed synchro bit)
SearchInitiatorGain or Min−ReceivingGain Mode	1 bit (b7)	X	0 Search Initiator Gain selected 1 Min Receiving Gain selected
Search Initiator Gain or Min−Receiving Gain	3 bits (b6 to b4)	XXX	Value of the gain for Intelligent Synchronization or Min Receiving Value Min Gain of reception = (value * 6 db)
Max−Receiving−Gain→Value	3 bits (b3to b1)	XXX	Max Receiving gain value in limited mode Range of reception = (value * 6 db)
Max−Receiving−Gain→Mode	1 bit (b0)	0 1	Non limited Max−Receiving−Gain Limited Max−Receiving−Gain
Time out Inter Character TIC	1 bit (b7)	0 1	Constant of 10 ms 5 characters depending on communication speed
Bad CRC transmitting	1 bit (b6)	0 1	Disables the transmitting of bad CRC frames Enables the transmitting of bad CRC frames
Pad correcting	1 bit (b5)	0 1	Enables the Pad correcting Disables the Pad correcting

Table 32. GENERAL DESCRIPTION OF WRITECONFIGNEW_REQUEST

Field	Length	Value	Description
FSK +	1 bit (b4)	0 1	Disables the improvement of FSK Enables the improvement of FSK
Alarm Filter	1 bit (b3)	0 1	Enables the alarm filter Disables the alarm filter
Synchro without Gain Min	1 bit (b2)	x	0 disabled 1 enabled
Repeater	2 bits (b1,b0)	00 01 10 11	Never Repeater or Mode = Master Always Repeater Not Repeater (accept frame ISACall) Repeater (accept frame ISACall)
Time−out−search−initiator	2 bytes	0 to FFFF	In seconds (Not used in Master and Monitor mode)

See Appendix C: SUMMARY of writeconfigNew_request for more details on the data for each mode.

TEST MODE

Description

The test mode is used to perform tests on the emission level of the AMIS−49587 (for CENELEC for example – never used on the field) and on the reception. Six different modes are available:

1. Transmitting 1: the AMIS−49587 transmits the frequency corresponding to the "1" bit value non stop.
2. Transmitting 0: the AMIS−49587 transmits the frequency corresponding to the "0" bit value non stop.
3. Alternative transmission: the AMIS−49587 transmits alternatively the frequencies corresponding to the "1" and "0" bit values.
4. Reception E0/E1 (= no transmission) : the AMIS−49587 is placed in reception mode (but it is not able to interpret what it receives) and it sends on UART the envelop values.
5. Reception I0/Q0 (= no transmission) : the AMIS−49587 is placed in reception mode (but it is not able to interpret what it receives) and it sends on UART the channel 0 values of I and Q.
6. Reception I1/Q1 (= no transmission) : the AMIS−49587 is placed in reception mode (but it is not able to interpret what it receives) and it sends on UART the channel 1 values of I and Q.

TESTMODE_REQUEST (Tag 81h)

Description: The TestMode_Request command is used by the base micro to ask a Transmitting Test to the AMIS−49587. Then the AMIS−49587 is in Not Set mode and its data are all initialized.

Remark: This means that the status will indicate that the AMIS−49587 is not set, but it won't accept WriteConfig_Request and WriteConfigNew_Request without a reset. Be careful with using this mode, since nothing will indicate that the AMIS−49587 is in this mode.

The field DataTx contains the chosen mode (transmitting1, transmitting 0, alternative transmission, E0/E1 reception, I0/Q0 reception, or I1/Q1 reception) (1 byte), the frequencies (2 * 2 bytes) and the MaxTransmisttingGain(1byte)

Table 33. TESTMODES

Mode	Code
Transmitting Fs	00
Transmitting Fm	01
Alternative transmission of Fs and Fm	02
Reception I0/Q0	03
Reception I1/Q1	04
Reception E0/E1	05

Syntax: **Master/Slave/Monitor**

Initiator	Command (arguments)	Possible Response
Base Micro	TestMode_Request (DataTx)	

Frame Format:

<STX>	Length	<TestMode_Request>	DataTx	CHK

RESET AND SYNCHRO COMMANDS

Description

The reset command is used to replace the AMIS−49587 in the Not Set mode. The synchro commands are sent by the AMIS−49587 to the Base Micro to indicate the changes in the synchronization state of the AMIS−49587.

Synchro_Indication (Tag 10h)

Description: The Synchro_Indication is sent by the AMIS−49587 in order to indicate that something has changed in the synchronization state. The field Synchro_Data contains the change reason (see Section Synchronization State Codes) and data corresponding with this change.

Syntax: **Master/Slave**

Initiator	Command (arguments)	Possible Response
AMIS−49587	Synchro_Indication (Synchro_Data)	

Frame Format:

<STX>	Length	<Synchro_Indication>	Synchro_Data	CHK
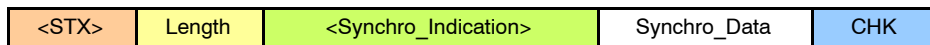
Table 34. GENERAL DESCRIPTION OF SYNCHRO_INDICATION

Change Reason Field	Length and Synchro_data description	Remark
Synchronisation Found (01h)	1 byte: Pad 2 bytes: Signal S0 2 bytes: Noise N0 2 bytes: Signal S1 2 bytes: Noise N1 2 bytes: ASK Threshold or FSK factor 1 byte : Method 1 byte : Synchro−Bit and Gain values	See Table 8: Description of the SpyData field for more details
Synchronisation Confirmed (02h)	1 byte: Pad 2 bytes: Source MAC Address 2 bytes: Destination MAC Address	
Synchronisation Lost (04h)		
Time−out not addressed has expired (01h)	2 bytes: Local MAC Add 2 bytes: Initiator MAC Add	Slave mode
Time−out frame not OK has expired (02h)	2 bytes: Local MAC Add 2 bytes: Initiator MAC Add	Master and Slave mode
Time−out synchro confirm has expired (03h)	2 bytes: Local MAC Add 2 bytes: Initiator MAC Add	Master and Slave mode
Addressed by a wrong initiator (04h)	2 bytes: Source MAC Add 2 bytes: Dest. MAC Add	Slave mode
External desynchro command (05h)	2 bytes: Local MAC Add 2 bytes: Initiator MAC Add	Master and Slave mode
Search Initiator active (06h)	2 bytes: Last initiator MAC Address received 2 bytes: Current initiator MAC Address choice	Slave mode

Desynchro_Request (Tag 11h)

Description: The Desynchro_Request command is used by the base micro to enforce the not synchronized state in the AMIS−49587 and therefore it starts looking for a new synchronization.

Syntax: **Master/Slave/Monitor**

Initiator	Command (arguments)	Possible Response
Base Micro	Desynchro_Request ()	

Frame Format:

| <STX>	Length	<Desynchro_Request>	CHK

Reset_Request (Tag 21h)

Description: The Reset_Request command is used by the base micro to ask a reset to the AMIS−49587. Then the AMIS−49587 is in Not Set mode and its data are all initialized. This command has no data. The base micro can send this command at anytime.

Syntax: **Master/Slave/Monitor**

Initiator	Command (arguments)	Possible Response
Base Micro	Reset_Request ()	

Frame Format:

<STX>	Length	<Reset_Request>	CHK
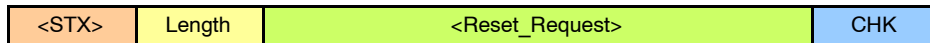
SCENARIO OF STARTING AFTER RESET

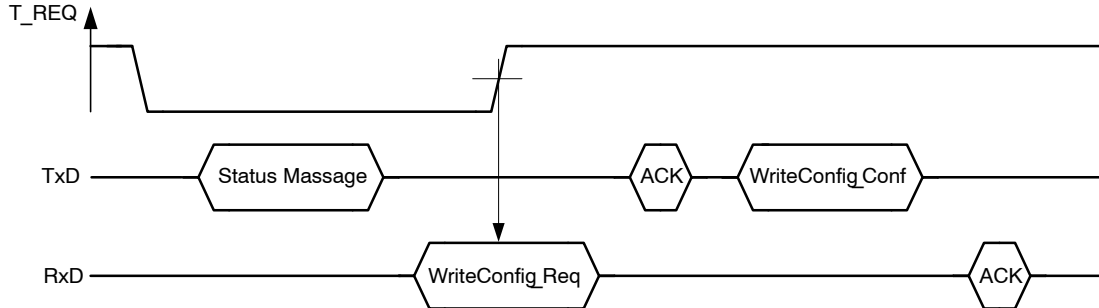This scenario is achieved at the starting time and after a Reset_Request command.

Figure 20. Scenario of starting

DATABASE

DESCRIPTION

These commands allow the access to variables in the Data Base which is constituted by a MIB array and a local data array. The communication between the AMIS−49587 and the base micro is performed through the asynchronous serial interface (UART) by using the WriteDB_Request, the WriteDB_Confirm and the WriteDB_Error commands.

THE COMMANDS AVAILABLE

WriteDB_Request (Tag 41h)

Description: The WriteDB_Request is sent by the base micro in order to write one data in the AMIS−49587 data base. The field **DB_Data_Id** is coded on several bytes in Hex and is structured as follow:
− 2 bytes for the Identifier field (Ident) that indicates which data has to be modified (transmitted LSByte first).
− 0 to 20 bytes for the data depending on the Identifier field.

AMIS−49587

See Section The Objects Available on and The Objects Available Only on AMIS−49587 versions for more details on each object.

Syntax: **Master/Slave**

Initiator	Command (arguments)	Possible Response
Base Micro	WriteDB_Request (DB_Data_Id)	WriteDB_Confirm (DB_Data_Id_Echo) WriteDB_Error (Error_Code)

Frame Format:

<STX>	Length	< WriteDB_Request >	DB_Data_Id	CHK

Table 35. LIST OF WRITEDB ITEMS

Field Name	Ident	Description
FIMA/LIMA	0000	Changes the value of First Initiator MAC Address (FIMA) and Last Initiator MAC Address (LIMA)
LocalMacAdd/InitMacAdd	0001	Changes the value of Local MAC Address and Active Initiator Address
Time−out−synchro−confirm	0002	Changes the value of the TO synchro confirm (In seconds.)
Time−out−frame−not−ok	0003	Changes the value of the TO frame not ok (In seconds)
Time−out−not−addressed	0004	Changes the value of the TO not addressed (In minutes)
Mac−group−addresses	0005	Changes the value of the 5 MAC group addresses
Invalid−frame−counter	0006	Read the value of the invalid−frame counter and then set to 0
Min−delta−credit	0007	Read the value of the Min delta credit and then set to 7
Max_Transmitting_Gain : Mode and Value (R_ALC_CTRL)	0008	Changes the mode and the value of the max transmitting gain
SYNCHRO−Type:Mode SYNCHRO−Bit:Value	0009	Changes sychro mode and the synchro bit value
Max−Receiving−Gain: Mode and Value	000A	Changes the mode and the value of the Max Receiving gain
Repeater	000B	Changes the repeater state
Frequency	000C	Changes the value of the frequencies Fs and Fm
Counters	000D	Read the value of the data counters:Counter Crc Ok, Counter Crc Not Ok, Repeater counter, Transmit counter, corrected frames counter, and then set to 0 or not
PhyAlarmRequest	000F	Request the transmission of a Phy Alarm
DataStats	0010	Read the value of the Data statistics, and then set to 0 or not.
Time−SearchInitiator	0011	Changes the value of the TO Search Initiator (In seconds)
ReadConfig	0012	To get an echo of the current configuration of the FPMA
Read SoftVersion	0013	Read the version of the FPMA
Min−ReceivingGain Value	0014	Changes the value of the Min Receiving Gain
Gain−SearchInitiator	0015	Changes the value of the Gain−SearchInitiator

WriteDB_Confirm (Tag 42h)

Description: The WriteDB_Confirm has to be sent by the FPMA when new data have been correctly recorded. The DB_Data_Id_Echo contains the identifier of the data and the value read at its memory location. It may have the same structure as DB_Data_Id or be different (see Section "The Objects Available" for more details on each object).

Syntax: **Master/Slave**

Initiator	Command (arguments)	Possible Response
AMIS−49587	WriteDB_Confirm (Data_Config_Echo)	

Frame Format:

<STX>	Length	< WriteDB_Confirm >	DB_Data_Id_Echo	CHK

WriteDB_Error (Tag 43h)

Description: The FPMA software checks the MAC addresses, the Synchro−bit and if the modification of that field is allowed. If it detects an error, it sends back a WriteDB_Error command with the corresponding Error_Code (see Section "The Objects Available").

Syntax: **Master/Slave**

Initiator	Command (arguments)	Possible Response
AMIS−49587	WriteDB_Error (Error_Code)	

Frame Format:

<STX>	Length	< WriteDB_Error >	Error_Code	CHK

THE OBJECTS AVAILABLE

FIMA/LIMA

Description: This request is used to modify the value of the FIMA and LIMA addresses. The values of FIMA and LIMA must be in the field 0001 to 0FFF, and must be compatible with current value of LocalMacAdd and InitMacAdd.

Request Format:

<STX>	Length	41h	0000h	FIMA (2 bytes), LIMA (2 bytes)	CHK

Confirm Format:

<STX>	Length	42h	0000h	FIMA (2 bytes), LIMA (2 bytes)	CHK

LocalMacAdd/InitMacAdd

Description: This request is used to modify the value of the Local Mac Address and the Initiator Mac Address. The values of LocalMacAdd and InitMacAdd must be in the field 0001 to 0FFF, and must be compatible with current value of FIMA and LIMA.

Request Format:

<STX>	Length	41h	0100h	LocalMacAdd (2 bytes), InitMacAdd (2 bytes)	CHK

Confirm Format:

<STX>	Length	42h	0100h	LocalMacAdd (2 bytes), InitMacAdd (2 bytes)	CHK

TimeoutSynchro
Description: This request is used to modify the value of the timeout synchro confirmation. The Timeout Synchro Confirm is set in seconds.

Request Format:

<STX>	Length	41h	0200h	TO Synchro Confirm (2 bytes)	CHK

Confirm Format:

<STX>	Length	42h	0200h	TO Synchro Confirm (2 bytes)	CHK

TimeoutNotOK
Description: This request is used to modify the value of the timeout Frame Not OK. The Timeout Frame Not OK is set in seconds.

Request Format:

<STX>	Length	41h	0300h	TO Frame Not OK (2 bytes)	CHK

Confirm Format:

<STX>	Length	42h	0300h	TO Frame Not OK (2 bytes)	CHK

TimeoutNotAddressed
Description: This request is used to modify the value of the timeout Not Addressed. The Timeout Not Addressed is set in minutes.

Request Format:

<STX>	Length	41h	0400h	TO Not Addressed (2 bytes)	CHK

Confirm Format:

<STX>	Length	42h	0400h	TO Not Addressed (2 bytes)	CHK

MacGroupAddress
Description: This request is used to modify the values of the 5 Mac Group Addresses. The Mac Group Addresses must be in the field LIMA(not included) to 0FFB.
If the first address of the 5 MacGroup addresses is set to 0xFFF, every frame with destination MAC address in the field LIMA(not included) to 0FFB will be transmitted by the FPMA. This makes it possible to manage more than 5 MAC address of group by the external micro controller.

Request Format:

<STX>	Length	41h	0500h	Mac Group Addresses (5 *2 bytes)	CHK

Confirm Format:

<STX>	Length	42h	0500h	Mac Group Addresses (5 *2 bytes)	CHK

Invalid Frame Counter
Description: This request is used to read the Invalid Frame Counter of the AMIS−49587. Once the request sent to the AMIS−49587, the Invalid Frame counter is automatically set to 0. The AMIS−49587 answers with the value of the Invalid Frame Counter

Request Format:

<STX>	Length	41h	0600h	Pad (0 to 1 byte)	CHK

Confirm Format:

<STX>	Length	42h	0600h	Invalid Frame Counter (0 to 1 byte)	CHK

Min Delta Credit
Description: This request is used to read the Min Delta Credit in the AMIS−49587. Once the request sent to the AMIS−49587, the Min Delta Credit is automatically set to 7. The AMIS−49587 answers with the value of the Min Delta Credit (before it was set to 7)

Request Format:

<STX>	Length	41h	0700h	Pad (0 to 1 byte)	CHK

Confirm Format:

<STX>	Length	42h	0700h	Min Delta Credit (1 byte)	CHK

MaxTransmittingGain
Description: This request is used to modify the Max Transmitting Gain of the AMIS−49587. The Max Transmitting Gain can be reduced from 0 to 21 dB by step of step 3 dB. The data value for the request is in the field 01 to 0F by step of 2, it indicates an attenuation of $((N − 1) / 2)$ dB. The data value for the Confirm is in the field 00 to 07, indicating an attenuation of $N * 3$ dB.

Request Format:

<STX>	Length	41h	0800h	Transmitting Attenuation (1 byte)	CHK

Confirm Format:

<STX>	Length	42h	0800h	Transmitting Attenuation (1 byte)	CHK

Synchro
Description: This request is used to modify the synchro parameters: the synchro type and the synchro bit. The value of the synchro bit field is 0 if the synchro bit is automatic, or $(2 * N) + 1$ if the synchro bit is fixed, where N is the synchro bit value $(0 < N < 7)$. You can add 16 to this value to enable synchronization on special frame

Request Format:

<STX>	Length	41h	0900h	Synchro−Type−bit (1 byte)	CHK

Confirm Format:

<STX>	Length	42h	0900h	Synchro−Type−bit (1 byte)	CHK

MaxReceivingGain
Description: This request is used to modify the Max Receiving Gain of the AMIS−49587. The Max Receiving Gain can be set from 1 to 42 dB by step of step 6dB, or unlimited. The data value for the request is in the field 01 to 0F by step of 2, it indicates a Max Receiving Gain of $((N − 1) / 2) * 6$ dB; or 00, which indicates an unlimited Max Receiving Gain. The data value for the Confirm is in the field 00 to 07, indicating a Max Receiving Gain of $(N * 6)$ dB, or 08, which indicates an unlimited Max Receiving Gain.

Request Format:

<STX>	Length	41h	0A00h	Max Receiving Gain (1 byte)	CHK

Confirm Format:

<STX>	Length	42h	0A00h	Max Receiving Gain (1 byte)	CHK

Repeater

Description: This request is used to modify the repeater state of the AMIS−49587. The repeater state can be Repeater, No Repeater, Repeater Isacall or No Repeater Isacall. Only the 2 last bits are used for this command, so the value is in the field 00 to 03.

Request Format :

<STX>	Length	41h	0B00h	Repeater State (1 byte)	CHK

Confirm Format:

<STX>	Length	42h	0B00h	Repeater State (1 byte)	CHK

Frequency

Description: This request is used to modify the values of the frequencies Fs and Fm used for the PLC communication. See calculation method Sine Wave Generator on Page 13.

Request Format:

<STX>	Length	41h	0C00h	Fs (2 bytes), Fm (2 bytes)	CHK

Confirm Format:

<STX>	Length	42h	0C00h	Fs (2 bytes), Fm (2 bytes)	CHK

Data Counters

Description: This request is used to read the value of the data counters in the AMIS−49587. It contains one byte which is used to know whether the counters must be reset or not (00: no reset, 01: reset)

There are 6 counters coded on 4 bytes each, which indicates:

− Number of CRC OK frames received
− Number of CRC not OK frames received
− Number of repeated frames
− Number of transmitted frames
− Number of corrected frames (with option Pad Correcting)
− Number of frames with bad Frame Indicator received

Request Format :

<STX>	Length	41h	0D00h	Request Counters (1 byte) + Pad (0 to 19 bytes)	CHK

Confirm Format :

<STX>	Length	42h	0D00h	CRC_OK (4 bytes), CRC_NOK (4 bytes), Rep_Frames (4 bytes), Tr_Frames (4 bytes), Corr_Frames (4 bytes), FI_NOK (4 bytes)	CHK

PhyAlarmRequest

Description: This request is used to send a physical alarm pattern. No data is transmitted to indicate the number of repetitions, the FPMA already knows this number because it is in its config.

Request Format:

<STX>	Length	41h	0F00h	Pad (0 to 1 byte)	CHK

Confirm Format:

<STX>	Length	42h	0F00h	Number of alarm Transmissions (1 byte)	CHK

DataStats

Description: This request is used to read the value of the current data statistics in the AMIS−49587. The request contains one byte which is used to know whether the counters must be reset or not (00: no reset, 01: reset). These statistics are coded this way:

If the AMIS−49587 is synchronized (30 bytes):

− The value of signal and noise (S0, N0, S1, N1) for the last subframe received (4 * 2 bytes) + the method and gain used to demodulate this subframe (2 * 1 byte)
− The method, gain and SNR (S0/N0, S1/N1) on the 5 last time slots in reception mode (5 * 4 bytes) + 1 byte to know the actual position in the table

If the AMIS−49587 is not synchronized (36 bytes):

− The values of the real and imaginary parts of the signal for each frequency (I0, Q0, I1, Q1), for the 4 last calculated time−slots (4 * (4 * 2 bytes))
− The current position in the board (1 byte)
− The software reception gain (1 byte)
− The hardware reception gain (1 byte)
− The R_ALC value (1 byte)

Request Format:

\<STX\>	Length	41h	1000h	Reset Counters (1 byte) + Pad (0 to 35 bytes)	CHK

Confirm Format:

If the AMIS−49587 is synchronized:

\<STX\>	Length	42h	1000h	Signal_noise_subframe (10 bytes), SNRreception (20 bytes)	CHK

If the AMIS−49587 is not synchronized:

\<STX\>	Length	42h	1000h	I0,I1,Q1 (32 bytes), Pos (1 byte), GainSoft (1 byte), GainHard (1 byte), R_ALC (1 byte)	CHK

TimeoutSearchInitiator

Description: This request is used to modify the value of the timeout Search Initiator. The timeout Search Initiator is set in seconds.

Request Format:

\<STX\>	Length	41h	1100h	TO Search Initiator (2 bytes)	CHK

Confirm Format:

\<STX\>	Length	42h	1100h	TO Search Initiator (2 bytes)	CHK

ReadConfig

Description: This request is used to get an echo of the configuration of the AMIS−49587.

Request Format:

\<STX\>	Length	41h	1200h	Pad (0 to 36 bytes)	CHK

Confirm Format:

\<STX\>	Length	42h	1200h	Pad (0 to 36 bytes)	CHK

AMIS−49587

Read Version Soft

Description: This request is used to read the soft version of the AMIS−49587.

Request Format:

<STX>	Length	41h	1300h	Pad (0 to 1 byte)	CHK

Confirm Format:

<STX>	Length	42h	1300h	Soft Version (1 byte)	CHK

Min−ReceivingGain

Description: This request is used to modify the Min Receiving Gain of the AMIS−49587. The Min Receiving Gain can be set from 1 to 42 dB by step of step 6dB, or unlimited. The data value for the request is in the field 01 to 0F by step of 2, it indicates a Min Receiving Gain of $((N - 1) / 2) * 6$ dB; or 00, which indicates that the Min Receiving Gain is not used. The data value for the Confirm is in the field 00 to 07, indicating a Min Receiving Gain of $(N * 6)$ dB, or 08, which indicates an unlimited Max Receiving Gain.

Request Format:

<STX>	Length	41h	1400h	Min Receiving Gain (1 byte)	CHK

Confirm Format:

<STX>	Length	42h	1400h	Min Receiving Gain (1 byte)	CHK

Gain Search Initiator

Description: This request is used to modify the value of the Gain Search Initiator.

Request Format:

<STX>	Length	41h	1500h	Gain Search Initiator (1 byte)	CHK

Confirm Format:

<STX>	Length	42h	1500h	Gain Search Initiator (1 byte)	CHK

MEDIUM ACCESS CONTROL

DESCRIPTION

The local communication exchanges data with the MAC sub−layer. These data (included into local frames) contain information about the DLC frame transmission on the mains (Initial credit, current credit, delta credit, local and destination MAC addresses) and the data field. Other information for transmission such as the Preamble, the Start Sub−frame Delimiter, the Frame Indicator and the Frame Check Sequence are directly managed by the MAC sub−layer and the PHYsical layer. In case of transmission from AMIS−49587 to the mains, if necessary, the MAC sub−layer will separate the frame into one or several sub−frame(s) (maximum 7 sub−frames). In case of frame reception made up of several sub−frames, the AMIS−49587 will send back the complete frame (without Pre, SSD, FI, FCS) to the local communication after the last sub−frame reception and only if the frame is correct and dedicated for this application.

THE COMMANDS AVAILABLE

MA_DATA_Request (Tag 51h)

Description: The MA_Data_Request is sent from the base micro local LLC sub−layer to the AMIS−49587 local MAC sub−layer to request a DLC frame transmission. This request must be received by the AMIS−49587 in the time−slot preceding the transmitting one.

Syntax: **Master/Slave**

Initiator	Command (arguments)	Possible Response
Base Micro	MA_Data_Request (MAC_Frame)	MA_Data_Confirm (Transmission_Status)

Frame Format :

<STX>	Length	< MA_Data_Request >	MAC_Frame	CHK

Table 36. DESCRIPTION OF THE MAC_FRAME FIELD

Field name	Length	Value	Description
Initial Credit Current Credit Delta Credit	3 bits b7−b5 3 bits b4−b2 2 bits b1,b0	0h to 7h 0h to 7h 0h to 3h	Initial Credit Current Credit = Initial Credit Delta Credit = Received Delta Credit (Slave) = 0 (Master)
Source Address	12 bits b23−b12	Not used 000h to FFFh	Slave Mode (Filled by MAC layer) Master Mode
Destination Address	12 bits b11−b0	000h to FFFh	Destination MAC address of the target station DLC
Pad length	1 byte	Not used	Filled by MAC layer
M_sdu	up to 242 bytes		MAC service data unit

MA_DATA_Confirm (Tag 52h)

Description: The MA_DATA_Confirm is sent from AMIS−49587 to a base micro (SLAVE or MASTER) either as positive acknowledgment when a MA_DATA_Request has successfully been transmitted by the physical layer, or as negative acknowledgment when the transmission has been refused. The positive acknowledgment is sent after the frame transmission on the mains and before the beginning of the repetition (if the credit is higher than zero). The Transmission_Status byte contains a value corresponding at this positive or negative acknowledgment. The different values for the Transmission_Status field are described in the Table 45: Transmission Status.

Syntax: **Master/Slave**

Initiator	Command (arguments)	Possible Response
AMIS−49587	MA_Data_Confirm (Transmission_Status)	

Frame Format :

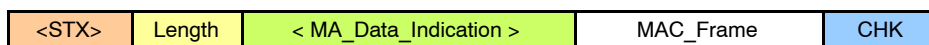| <STX>	Length	< MA_Data_Confirm >	Transmission_Status	CHK

MA_DATA_Indication (Tag 50h)

Description: The MA_Data_Indication is sent from the AMIS−49587 (Client or Server) to the base micro to deliver the received DLC frame to the base micro LLC sub−layer.

Syntax: **Master/Slave**

Initiator	Command (arguments)	Possible Response
AMIS−49587	MA_Data_Indication (MAC_Frame)	

Frame Format :

\<STX\>	Length	< MA_Data_Indication >	MAC_Frame	CHK

See Table 36 Description of the Mac Frame field.

MA_DATA_Indication_Bad_CRC (Tag 53h)

Description: The MA_Data_Indication_Bad_CRC is sent from the AMIS−49587 (Client or Server) to the base micro to deliver an erroneous received DLC frame to the base micro LLC sub−layer. This command is only used if the Bad CRC transmitting option is chosen during the configuration (see Sections WriteConfig_Request (Tag 31h) and WriteConfigNew_Request (Tag 71h))

Syntax: **Master/Slave**

Initiator	Command (arguments)	Possible Response
AMIS−49587	MA_Data_Indication_Bad_CRC (MAC_Frame)	

Frame Format :

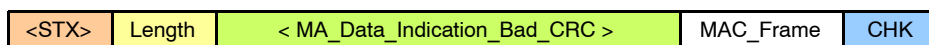| \<STX\>	Length	< MA_Data_Indication_Bad_CRC >	MAC_Frame	CHK

Table 36 − Description of the Mac Frame field.

Caution: The Mac Frame transmitted with this command is erroneous. It may be used by the base Micro to try and rebuild a correct frame (by using the repetitions for example), but is cannot be used just as it is.

REPEATER CALL FUNCTION

ISA_REQUEST (TAG 61H)

Description: In client mode, the ISA_Request command is normally sent by the base micro, when it wants to start a special sequence named « ISACall ». In server mode, the ISA_Request command is normally sent by the base micro, when it has received a MA_Data_Indication corresponding with an ISACall indication. The ISA_Request command is sent from the base micro local LLC sub−layer to the AMIS−49587 local MAC sublayer to switch the AMIS−49587 in special mode called « ISACall ». This service is an internal service and should not be used. Without correct handling at the system level it can disable the communication.

Internal Service Request.

Syntax: **Slave**

Initiator	Command (arguments)	Possible Response
Base Micro	ISA_Request (DataRepeater)	ISA_Confirm (Transmission_Status)

Frame Format :

\<STX\>	Length	< ISA_Request >	Data_ISA	CHK
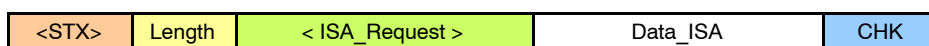
Table 37. FORMAT OF THE DATA_ISA FIELD

Field Name	Length	Value
Level	2 bytes	0 to FFFF
Transmission_Position	2 bytes	0 to FFFF

When ISA_Request command is received, AMIS−49587 enters in RepeaterCall function and is listening for the repeater call pattern, which is 2 bytes long (2E5C), and waiting to transmit this pattern if no other module has transmitted before. So next frames are divided in 21 SubTslots of 2 bytes.

After ISA_Request, if AMIS−49587 is set as Repeater or NoRepeater, it is listening until a pattern is detected, or until the SubTslot counter is equal to the parameter Transmission_Position.

If a pattern is detected, AMIS−49587 is set to NoRepeater and exits RepeaterCall function.

If no pattern detected and SubTslot counter is equal to Transmission_Position, the AMIS−49587 transmits the pattern, is set as Repeater, and exits the function.

If AMIS−49587 is set as AlwaysRepeater, it will always transmit pattern when SubTslot counter is equal to Transmission_Position, even if a pattern has already been transmitted before.

If it is set as NeverRepeater or is in Slave mode, ISA_Request command will not be accepted, and AMIS−49587 will not take part in RepeaterCall function.

Transmission_Position value depends on the mode:
- In Client mode, it is 0: pattern is transmitted at the first SubTslot.
- In Server mode, Transmission_Position is equal to the Mac Adress (values from 1 to MaxAdrMac).

- If Server is "New" (no Mac address defined), a random number is chosen and will determine a position in the reserved Tslots for New at the end of the Repeater Call function. (values from MaxAdrMac to MaxAdrMac + 21*NB_TslotForNew)
(with MaxAdrMac and NB_TslotForNew parameters from CIASE RepeaterCall service)

Level parameter is used when listening for repeater call pattern: at each SubTslot, if the signal is over this level parameter multiplied by the number of bits listened, than the pattern is detected.

So, on the network, there will be more Repeater if this level is set high. The default value is 1000, which is equivalent of a signal on the network between 102 and 106 dBμV.

ISA_CONFIRM (TAG 62H)

Description: The ISA_Confirm is sent by the AMIS−49587 to a base micro (SLAVE or MASTER) either as positive acknowledgment when a ISA_Request has successfully been transmitted by the physical layer, or as negative acknowledgment when the ISA_Request command has been received too late or if the transmitting position is wrong or if the repeater state is equal to never. In both cases the Transmission_Status byte contains a value corresponding with this positive or negative acknowledgment. The different values for the Transmission_Status field are described in the Appendix C (Transmission Status) This service is an internal service and should not be used. Without correct handling at the system level it can disable the communication.

Syntax: Slave

Initiator	Command (arguments)	Possible Response
AMIS−49587	ISA_Confirm (Transmission_Status)	

Frame Format :

<STX>	Length	< ISA_Confirm >	Transmission_Status	CHK

AMIS−49587

MONITOR MODE COMMANDS

DESCRIPTION

The monitor mode is used to spy the exchanged frames on the mains. It allows the user to check the transmission quality in a definite point of the mains. In this mode, all the LTC and DB requests are allowed, but no MAC requests. The Physical layer supplies directly the frames to the base micro.

THE COMMANDS AVAILABLE

SPY_No_SubFrame (Tag A0h)

Description: The SPY_No_SubFrame is sent by the AMIS−49587 local PHY layer to indicate that a sub−frame has not been received correctly, due to either a method not found, or a non recognition of the Start Sub−frame Delimiter (SSD).

Syntax: **Monitor**

Initiator	Command (arguments)	Possible Response
AMIS−49587	SPY_No_SubFrame (SpyData)	

Frame Format :

<STX>	Length	< SPY_No_SubFrame >	SpyData	CHK
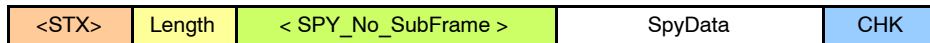
Table 38. DESCRIPTION OF THE SPYDATA FIELD

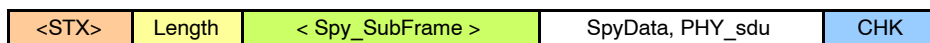| Field Name	Length	Description
S0	2 Bytes	Value of the zero signal envelope
N0	2 Bytes	Value of the zero noise envelope
S1	2 Bytes	Value of the one signal envelope
N1	2 Bytes	Value of the one noise envelope
Threshold	2 Bytes	Indicates the threshold value for ASK method or the FSK factor.
Method	1 Byte	Indicates the found method: $0 \Rightarrow$ No method $1 \Rightarrow$ ASK0 $2 \Rightarrow$ ASK1 $3 \Rightarrow$ FSK ($S0 \cong S1$) $4 \Rightarrow$ FSK0 ($S0 > S1$) 5 FSK1 ($S1 > S0$)
PAD	1 Bit (b7)	0
Synchro_bit Value	3 Bits (b6,b5,b4)	Synchronisation bit value when synchronisation was found
PAD	1 Bit (b3)	0
Reception Gain	3 Bits (b2,b1,b0)	Indicates the gain value (0 to 7) used during the synchronization

SPY_SubFrame (Tag B0h)

Description: The SPY_SubFrame is sent by the AMIS−49587 local PHY layer to indicate that a sub−frame has been correctly received. All information concerning the reception conditions (SpyData) and the data (PHY_sdu) are supplied in this command. Format of the SpyData field: see Table 38: Description of the SpyData field. Format of the PHY_sdu field: see [2] Sections Status Message and Master Mode (Client).

Syntax: **Monitor**

Initiator	Command (arguments)	Possible Response
AMIS−49587	Spy_SubFrame (SpyData, PHY_sdu)	

Frame Format :

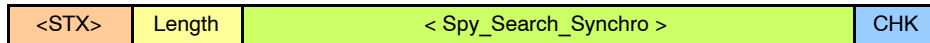| <STX>	Length	< Spy_SubFrame >	SpyData, PHY_sdu	CHK

SPY_Search_Synchro (Tag C0h)

Description: The SPY_Search_Synchro is sent periodically by the AMIS−49587 local MAC sub−layer to indicate synchronization is in progress.

Syntax: **Monitor**

Initiator	Command (arguments)	Possible Response
AMIS−49587	Spy_Search_Synchro ()	

Frame Format :

| <STX>	Length	< Spy_Search_Synchro >	CHK

SPY_Synchro_Found (Tag D0h)

Description: The SPY_Synchro_Found is sent by the AMIS−49587 local MAC sub−layer as soon as it has correctly found synchronization when it was receiving a sub−frame. Thus, it is now synchronized and it is waiting for another correct frame for confirmation.

Format of the SpyData field: see Table 38: Description of the SpyData field

Syntax: **Monitor**

Initiator	Command (arguments)	Possible Response
AMIS−49587	Spy_ Synchro_Found (SpyData)	

Frame Format :

<STX>	Length	< Spy_ Synchro_Found >	SpyData	CHK
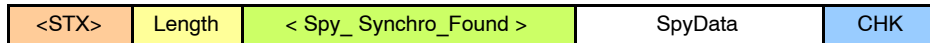
SPY_No_Alarm_Found (Tag E0h)

Description: The SPY_No_Alarm_Found is sent by the AMIS−49587 local MAC sub−layer at the end of a time−slot, when has not found an Alarm indication in the pause time.
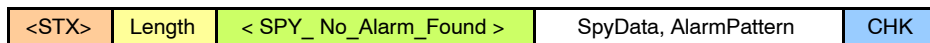
Format of the SpyData field: see Table 38: Description of the SpyData field

Format of the AlarmPattern: 2 bytes

Syntax: **Monitor**

Initiator	Command (arguments)	Possible Response
AMIS−49587	Spy_ Alarm_Found (SpyData,AlarmPattern)	

Frame Format :

<STX>	Length	< SPY_ No_Alarm_Found >	SpyData, AlarmPattern	CHK

SPY_Alarm_Found (Tag F0h)

Description: The SPY_Alarm_Found is sent by the AMIS−49587 local MAC sub−layer as soon as it has correctly found a Alarm indication in the pause time.
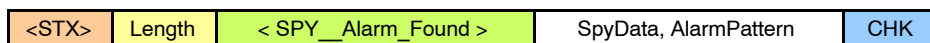
Format of the SpyData field: see Table 38: Description of the SpyData field

Format of the AlarmPattern: 2 bytes

Syntax: **Monitor**

Initiator	Command (arguments)	Possible Response
AMIS−49587	Spy_ Alarm_Found (SpyData,AlarmPattern)	

Frame Format:

<STX>	Length	< SPY__Alarm_Found >	SpyData, AlarmPattern	CHK

APPENDICES

APPENDIX A: SPECIFIC BEHAVOURS

Envelope calculation method

The envelops are calculated using sqrt values or absolute values, depending on the baudrate and on the main frequency. The following table describes the different modes :

	300, 600, 1200 bps		2400 bps	
	50 Hz	**60 Hz**	**50 Hz**	**60 Hz**
Synchro	Sqrt	Sqrt	ABS	ABS
Reception	Sqrt	Sqrt	Sqrt	ABS

Improvement of FSK

When FSK+ option is enabled, new thresholds are calculated. Than if the two envelops are under the threshold, the envelop which has the smallest gap with his threshold is used to determinate which bit is received. Or, if the two envelops are over the threshold, the envelop which has the biggest gap with his threshold is used.

Conflict Between Mains And Base Micro

When the AMIS−49587 receives in the same time (same time−slot) an MA_Data_Request from the base micro and a frame made up of one sub−frame with a repetition credit at zero from the mains, it ignores the frame received from the mains. In all other conflict cases, it refuses the base micro request as described in Section Arbitration and Transfer.

Modifications of Time−Out Values in Slave Mode

When a time−out is written with a **NULL** value using either the WriteConfig_Request or the WriteDB_Request command, this time−out will not be activated.

After a WriteDB_Request for either the Time−out−not−addressed or the Time−out−frame−not−ok, the new value is immediately taken in account (the time−out is restarted) excepted when the local mac address is NEW and the initiator mac address is nobody.

Modifications of MAC−Addresses in Slave Mode

A modification of Local and/or Initiator MAC address using the WriteConfig_Request or the WriteDB_Request, can provoke some modifications of data. It is supposed that the Local MAC address (LMAC) and the Initiator MAC address (IMAC) are both corrects (LMAC < FIMA and FIMA <= IMAC <=LIMA).

The charts below try to summarise these behaviours.

Case of WriteConfig

WriteConfig (always in Not Set mode)		
LMAC	**IMAC**	**Specific Behaviour**
NEW	NOBODY	(Note 24)
NEW	≠ NOBODY	⇒ Start Time−out−not−addressed (Note 24)
≠ NEW	≠ NOBODY	⇒ Start Time−out−not−addressed (Note 24)
≠ NEW	NOBODY	⇒ Start Time−out−not−addressed (Note 24)

24. After receiving the configuration, the AMIS−49587 starts looking for synchronisation.

Case of WriteDB

Values in the WriteDB		
LMAC	**IMAC**	**Specific Behaviour**
NEW	NOBODY	⇒ AMIS 49587 Starts Synchronization & Stop Time−out−not−addressed & Reset MAC Group Address
NEW	≠ NOBODY	⇒ AMIS 49587Starts Synchronization & Start Time−out−not−addressed & Reset MAC Group Address
≠ NEW	≠ NOBODY	⇒ Start Time−out−not−addressed
≠ NEW	NOBODY	⇒ Start Time−out−not−addressed

CASE OF TIME−OUT−NOT−ADDRESSED EXPIRES

LMAC	IMAC	Time−out−not−addressed expires
NEW	NOBODY	Impossible case
NEW	≠ NOBODY	⇒ AMIS 49587Start Synchronization & LMAC=NEW & IMAC=NOBODY & Reset MAC Group Address
≠ NEW	≠ NOBODY	⇒ AMIS 49587Start Synchronization & LMAC=NEW & IMAC=NOBODY & Reset MAC Group Address
≠ NEW	NOBODY	⇒ AMIS 49587Start Synchronization & LMAC=NEW & IMAC=NOBODY & Reset MAC Group Address

APPENDIX B: SUMMARY OF STATUS MESSAGE

STATUS MESSAGE IN NOT SET MODE

Byte	Content	Structure							
		Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	Start	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**
2	Data 1	x	x	x	x	x	x	Not SET	X
3	Data 2	RSV[7:0]							
4	Data 3	SVN[7:4]				SVN[3:0]			

<u>Where</u>:

Not SET   Indication is AMIS 49587 is set
RSV[7:0]   Reserved
SVN[7:4]   Software Version Number: major release
SVN[3:0]   Software Version Number: minor release
x   Not Used

STATUS MESSAGE IN SLAVE MODE

Byte	Content	Structure							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Start	0	0	1	1	1	1	1	1
2	Data 1	x	x	x	Not LOCKED	NEW	Not SYNC	Not SET	Buffer BUSY
3	Data 2	TS_Nb[2:0]			x	x	x	ALARM _EN	PLL _LOCK
4	Data 3	DEP[2:0]			MDC[2:0]			REP[1:0]	

Where:

Not LOCKED	Indication if AMIS 49587 is Unlocked
NEW	Indication if AMIS 49587 is New
Not SYNC	Indication of synchronization with mains
Not SET	Indication if AMIS 49587 is set
Buffer BUSY	Indication if PLC buffer is busy
TS_Nb[2:0]	Time slot counter
Alarm_EN	Alarm detection status
PLL_LOCK	PLL lock status
DEP[2:0]	Delta Electrical Phase
MDC[2:0]	Minimum Delta Credit Value
REP[1:0]	Repeater Mode
x	Not Used

STATUS MESSAGE IN SLAVE MODE

Byte	Content	Structure							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Start	0	0	1	1	1	1	1	1
2	Data 1	x	x	x	x	x	Not SYNC	Not SET	Buffer BUSY
3	Data 2	TS_Nb[2:0]			x	x	x	ALARM _EN	PLL _LOCK
4	Data 3	InvalFrCnt[7:0]							

Where:

Not SYNC	Indication of synchronization with mains
Not SET	Indication is AMIS 49587 is set
Buffer BUSY	Indication if PLC buffer is busy
TS_Nb[2:0]	Time slot counter
Alarm_EN	Alarm detection status
PLL_LOCK	PLL lock status
InvalFrCnt[7:0]	Invalid Frame counter
x	Not Used

Status Message in MONITOR MODE:

STATUS MESSAGE IN SLAVE MODE

Byte	Content	Structure							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Start	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**
2	Data 1	x	x	x	x	x	Not SYNC	Not SET	Buffer BUSY
3	Data 2	TS_Nb[2:0]			x	x	x	ALARM _EN	PLL _LOCK
4	Data 3	DEP[2:0]			x	x	x	x	x

Where:

Not SYNC	Indication of synchronization with mains
Not SET	Indication is AMIS 49587 is set
Buffer BUSY	Indication if PLC buffer is busy
TS_Nb[2:0]	Time slot counter
Alarm_EN	Alarm detection status
PLL_LOCK	PLL lock status
DEP[2:0]	Delta Electrical Phase
x	Not Used

APPENDIX C: SUMMARY OF WRITECONFIG_REQUEST

Table 39. WRITECONFIGNEW_REQUEST FOR MASTER MODE

Field	Length	Value	Description
First Initiator MAC Address (FIMA)	2 bytes	XXXX	Don't care
Last Initiator MAC Address (LIMA)	2 bytes	XXXX	Don't care
Local MAC Address	2 bytes	FIMA to LIMA	Master
Active Initiator Address	2 bytes	0000	Master
Time−out−synchro−confirm	2 bytes	XXXX	Don't care
Time−out−frame−not−ok	2 bytes	0000 to FFFF	Slave: In seconds (Not used in Master mode)
Time−out−not−addressed	2 bytes	XXXX	Don't care
Mac−group−addresses	10 bytes	XXXX	Don't care
Fs	2 bytes	0000 to FFFF	Step Register for the Space Frequency Fs
Fm	2 bytes	0000 to FFFF	Step Register for the Mark Frequency Fm
R_ZC_ADJUST	1 byte	00 to FF	Value according to the voltage level of the 50 Hz information for the input of the PLL.
NbAlarm	4 bits (b7 to b4)	XXXX 0000	Number of repetitions of a Phy Alarm Disable Phy Alarm functionality
R_ALC_CTRL→Value |Max_Transmistting_Gain→Value	3 bits (b3 to b1)	XXX	Attenuation value in fixed mode
R_ALC_CTRL→Value Max_Transmistting_Gain→Mode	1 bit (b0)	0 1	Automatic level control Fixed mode
R_CONF_TX_DATA_PRE_SLOT_SEL	1 bit (b7)	0 1	The output pin is the PRE_SLOT signal or Mode = Master The output pin is the transmitted DATA (for.Radio)
Pad	1 bit (b6)	0	This bit is not used (adjust length at 1 byte)
R_CONF→MODE	3 bits (b5 to b3)	001	Master mode for client station

AMIS−49587

Table 39. WRITECONFIGNEW_REQUEST FOR MASTER MODE

Field	Length	Value	Description
R_CONF→BAUDRATE	2 bits (b2,b1)	00 01 10 11	300 baud @ 50 Hz or 360 baud @ 60 Hz 600 baud @ 50 Hz or 720 baud @ 60 Hz 1200 baud @ 50 Hz or 1440 baud @ 60 Hz 2400 baud @ 50 Hz or 2880 baud @ 60 Hz
R_CONF→MAINS_FREQ	1 bit (b0)	0 1	mains frequency = 50 Hz mains frequency = 60 Hz
Pad	1 bit (b7)	0	This bit is not used (adjust length at 1 byte)
Search method	2 bits (b6, b5)	0 1	Method V5 Method V3
SINC Filter	1 bit (b5)	0 1	Disabled (1111) Enabled (1331)
SYNCHRO−Type→Mode	1 bit (b4)	0	Must be set to 0 (Synchronization on sub−frame preamble)
SYNCHRO−Bit→Value	3 bits (b3 to b1)	XXX	Synchro−bit value (in chip clock) in fixed mode
SYNCHRO−Bit→Mode	1 bit (b0)	1	Must be set to 1 (Fixed synchro bit)
SearchInitiatorGain or Min−ReceivingGain Mode	1 bit (b7)	X	0 Search Initiator Gain selected 1 Min Receiving Gain selected
Search Initiator Gain or Min−Receiving Gain	3 bits (b6 to b4)	XXX	Value of the gain for Intelligent Synchronisation or Min Receiving Value Min Gain of reception = (value * 6db)
Max−Receiving−Gain→Value	3 bits (b3to b1)	XXX	Max Receiving gain value in limited mode Range of reception = (value * 6db)
Max−Receiving−Gain→Mode	1 bit (b0)	0 1	Non limited Max−Receiving−Gain Limited Max−Receiving−Gain
Time out Inter Character TIC	1 bit (b7)	0 1	Constant of 10 ms 5 characters depending on communication speed
Bad CRC transmitting	1 bit (b6)	0 1	Disables the transmitting of bad CRC frames Enables the transmitting of bad CRC frames
Pad correcting	1 bit (b5)	0 1	Enables the Pad correcting Disables the Pad correcting
FSK +	1 bit (b4)	0 1	Disables the improvement of FSK Enables the improvement of FSK
Alarm Filter	1 bit (b3)	0 1	Enables the alarm filter Disables the alarm filter
Synchro without Gain Min	1 bit (b2)	x	0 disabled 1 enabled
Repeater	2 bits (b1,b0)	00 01 10 11	Never Repeater or Mode = Master Always Repeater Not Repeater (accept frame ISACall) Repeater (accept frame ISACall)
Time−out−search−initiator	2 bytes	XXXX	Don't care

WriteConfigNew_Request for Slave Mode

Table 40. DESCRIPTION OF WRITECONFIGNEW_REQUEST IN SLAVE MODE

Field	Length	Value	Description
First Initiator MAC Address (FIMA)	2 bytes	0001 to 0FFF	First value for Initiator MAC address
Last Initiator MAC Address (LIMA)	2 bytes	0001 to 0FFF	Last value for Initiator MAC address
Local MAC Address	2 bytes	0FFE or 0001 to (FIMA−1)	Slave Mode: New Slave (Registered)
Active Initiator Address	2 bytes	0000 FIMA to LIMA	Slave (unlocked) Slave (locked on an initiator)
Time−out−synchro−confirm	2 bytes	0000 to FFFF	In seconds.
Time−out−frame−not−ok	2 bytes	0000 to FFFF	In seconds
Time−out−not−addressed	2 bytes	0000 to FFFF	In minutes (Not used in Master & Monitor mode)
Mac−group−addresses	10 bytes	0000 to 0FFF	5 MAC group addresses (Not used in Master mode)
Fs	2 bytes	0000 to FFFF	Step Register for the Space Frequency Fs
Fm	2 bytes	0000 to FFFF	Step Register for the Mark Frequency Fm
R_ZC_ADJUST	1 byte	00 to FF	Value according to the voltage level of the 50 Hz information for the input of the PLL.
NbAlarm	4 bits (b7 to b4)	XXXX 0000	Number of repetitions of a Phy Alarm Disable Phy Alarm functionality
R_ALC_CTRL→Value Max_Transmistting_Gain→Value	3 bits (b3 to b1)	XXX	Attenuation value in fixed mode
R_ALC_CTRL→Value Max_Transmistting_Gain→Mode	1 bit (b0)	0 1	Automatic level control Fixed mode
R_CONF_TX_DATA_PRE_SLOT_SEL	1 bit (b7)	0 1	The output pin is the PRE_SLOT signal or Mode = Master The output pin is the transmitted DATA (for.Radio)
Pad	1 bit (b6)	0	This bit is not used (adjust length at 1 byte)
R_CONF→MODE	3 bits (b5 to b3)	010	Slave mode for server station
R_CONF→BAUDRATE	2 bits (b2,b1)	00 01 10 11	300 baud @ 50 Hz or 360 baud @ 60 Hz 600 baud @ 50 Hz or 720 baud @ 60 Hz 1200 baud @ 50 Hz or 1440 baud @ 60 Hz 2400 baud @ 50 Hz or 2880 baud @ 60 Hz
R_CONF→MAINS_FREQ	1 bit (b0)	0 1	mains frequency = 50 Hz mains frequency = 60 Hz
Pad	1 bit (b7)	0	This bit is not used (adjust length at 1 byte)
Search method	2 bits (b6, b5)	0 1	Method V6 Method V3
SINC Filter	1 bit (b5)	0 1	Disabled (1111) Enabled (1331)
SYNCHRO−Type→Mode	1 bit (b4)	0	Must be set to 0 (Synchronization on sub−frame preamble)
SYNCHRO−Bit→Value	3 bits (b3 to b1)	XXX	Synchro−bit value (in chip clock) in fixed mode
SYNCHRO−Bit→Mode	1 bit (b0)	1	Must be set to 1 (Fixed synchro bit)
SearchInitiatorGain or Min−ReceivingGain Mode	1 bit (b7)	0	0 Search Initiator Gain selected 1 Min Receiving Gain selected
Search Initiator Gain or Min−Receiving Gain	3 bits (b6 to b4)	XXX	Value of the gain for Intelligent Synchronisation or Min Receiving Value Min Gain of reception = (value * 6 db)
Max−Receiving−Gain→Value	3 bits (b3 to b1)	XXX	Max Receiving gain value in limited mode Range of reception = (value * 6 db)

Table 40. DESCRIPTION OF WRITECONFIGNEW_REQUEST IN SLAVE MODE

Field	Length	Value	Description
Max−Receiving−Gain→Mode	1 bit (b0)	0 1	Non limited Max−Receiving−Gain Limited Max−Receiving−Gain
Time out Inter Character TIC	1 bit (b7)	0 1	Constant of 10ms 5 characters depending on communication speed
Bad CRC transmitting	1 bit (b6)	0 1	Disables the transmitting of bad CRC frames Enables the transmitting of bad CRC frames
Pad correcting	1 bit (b5)	0 1	Enables the Pad correcting Disables the Pad correcting
FSK +	1 bit (b4)	0 1	Disables the improvement of FSK Enables the improvement of FSK
Alarm Filter	1 bit (b3)	0 1	Enables the alarm filter Disables the alarm filter
Synchro without Gain Min	1 bit (b2)	x	0 disabled 1 enabled
Repeater	2 bits (b1,b0)	00 01 10 11	Never Repeater or Mode = Master Always Repeater Not Repeater (accept frame ISACall) Repeater (accept frame ISACall)
Time−out−search−initiator	2 bytes	0 to FFFF	In seconds

WriteConfig_Request for Monitor Mode

Table 41. DESCRIPTION OF WRITECONFIGNEW_REQUEST IN MONITOR MODE

Field	Length	Value	Description
First Initiator MAC Address (FIMA)	2 bytes	XXXX	Don't care
Last Initiator MAC Address (LIMA)	2 bytes	XXXX	Don't care
Local MAC Address	2 bytes	XXXX	Don't care
Active Initiator Address	2 bytes	XXXX	Don't care
Time−out−synchro−confirm	2 bytes	0000 to FFFF	In seconds
Time−out−frame−not−ok	2 bytes	0000 to FFFF	In seconds
Time−out−not−addressed	2 bytes	XXXX	Don't care
Mac−group−addresses	10 bytes	0000 to 0FFF	5 MAC group addresses
Fs	2 bytes	0000 to FFFF	Step Register for the Space Frequency Fs
Fm	2 bytes	0000 to FFFF	Step Register for the Mark Frequency Fm
R_ZC_ADJUST	1 byte	00 to FF	Value according to the voltage level of the 50 Hz information for the input of the PLL.
NbAlarm	4 bits (b7 to b4)	XXXX 0000	Number of repetitions of a Phy Alarm Disable Phy Alarm functionality
R_ALC_CTRL→Value Max_Transmistting_Gain→Value	3 bits (b3 to b1)	XXX	Attenuation value in fixed mode
R_ALC_CTRL→Value Max_Transmistting_Gain→Mode	1 bit (b0)	0 1	Automatic level control Fixed mode
R_CONF_TX_DATA_PRE_SLOT_SEL	1 bit (b7)	0 1	The output pin is the PRE_SLOT signal or Mode = Master The output pin is the transmitted DATA (for.Radio)
Pad	1 bit (b6)	0	This bit is not used (adjust length at 1 byte)
R_CONF→MODE	3 bits (b5 to b3)	011	Monitor mode to spy and test of the DLC communication

Table 41. DESCRIPTION OF WRITECONFIGNEW_REQUEST IN MONITOR MODE

Field	Length	Value	Description
R_CONF→BAUDRATE	2 bits (b2,b1)	00 01 10 11	300 baud @ 50 Hz or 360 baud @ 60 Hz 600 baud @ 50 Hz or 720 baud @ 60 Hz 1200 baud @ 50 Hz or 1440 baud @ 60 Hz 2400 baud @ 50 Hz or 2880 baud @ 60 Hz
R_CONF→MAINS_FREQ	1 bit (b0)	0 1	mains frequency = 50 Hz mains frequency = 60 Hz
Pad	1 bit (b7)	0	This bit is not used (adjust length at 1 byte)
Search method	2 bits (b6, b5)	0 1	Method V6 Method V3
SINC Filter	1 bit (b5)	0 1	Disabled (1111) Enabled (1331)
SYNCHRO−Type→Mode	1 bit (b4)	0	Must be set to 0 (Synchronization on sub−frame pre-amble)
SYNCHRO−Bit→Value	3 bits (b3 to b1)	XXX	Synchro−bit value (in chip clock) in fixed mode
SYNCHRO−Bit→Mode	1 bit (b0)	1	Must be set to 1 (Fixed synchro bit)
SearchInitiatorGain or Min−ReceivingGain Mode	1 bit (b7)	1	1 Min Receiving Gain selected
Search Initiator Gain or Min−Receiving Gain	3 bits (b6 to b4)	XXX	Value of the gain for Intelligent Synchronisation or Min Receiving Value Min Gain of reception = (value * 6 db)
Max−Receiving−Gain→Value	3 bits (b3to b1)	XXX	Max Receiving gain value in limited mode Range of reception = (value * 6 db)
Max−Receiving−Gain→Mode	1 bit (b0)	0 1	Non limited Max−Receiving−Gain Limited Max−Receiving−Gain
Time out Inter Character TIC	1 bit (b7)	0 1	Constant of 10 ms 5 characters depending on communication speed
Bad CRC transmitting	1 bit (b6)	X	Don't care
Pad correcting	1 bit (b5)	X	Don't care
FSK +	1 bit (b4)	0 1	Disables the improvement of FSK Enables the improvement of FSK
Alarm Filter	1 bit (b3)	X	Don't care
Synchro without Gain Min	1 bit (b2)	x	0 disabled 1 enabled
Repeater	2 bits (b1,b0)	XX	Don't care
Time−out−search−initiator	2 bytes	XXXX	Don't care

APPENDIX D: CODING

Pre−Defined Characters
The valid one−byte values for the starting characters in the local frame are listed below :

Table 42. PRE−DEFINED CHARACTERS

Character	Definition	ASCII Code
STX	Start of text first char of frame	02h
ACK	Acknowledgment	06h
NAK	Non Acknowledgment	15h
?	Start of Status Message	3Fh

Synchronization State Codes
The valid one−byte values for the Synchronization state codes are listed below:

Table 43. SYNCHRONIZATION STATE CODES

New Synchronization State	Primary Code	Secondary Code	
Synchronization Found	01	No	
Synchronization Confirmed	02	No	
Synchronization Lost	04	time−out not addressed time−out frame not Ok time−out synchro confirm Wrong Initiator External Command Search Initiator	01 02 03 04 05 06

Error Codes
The valid one−byte values for the Error_Code are listed below:

Table 44. ERROR CODES

Error Identifier	Request Type	Error_Code
ERR_UNAVAILABLE_RESOURCE	MAC	11h
ERR_REQUEST_NOT_ALLOWED	MAC	12h
ERR_UNAVAILABLE_MODE	LTC/MAC	21h
ERR_ILLEGAL_DATA_COMMAND	LTC/DB	22h
ERR_ILLEGAL_LOCAL_MAC_ADR	LTC/DB	23h
ERR_ILLEGAL_INITIATOR_MAC_ADR	LTC/DB	24h
ERR_UNAVAILABLE_COMMAND	LTC	25h

Transmission Status
The valid one−byte values for the *Transmission_Status* field are listed below:

Table 45. TRANSMISSION STATUS

Field Name	Value	Description
OK	FFh	No error has been found
LM_TU1	00d	MA Data Confirm NEG Resources Temporary Unavailable at the MAC sub−layer
LM_SE	03d	Syntax Error at the MAC sub−layer
LM_TU2	10d	Command not authorised or Asic is not synchronised on the mains

Table 45. TRANSMISSION STATUS

Field Name	Value	Description
LM_TU3	20d	PLC buffer not free or Asic is busy Resources Temporary Unavailable at the MAC sub−layer
LM_TU4	30d	PLC buffer not free or Asic is busy Resources Temporary Unavailable at the MAC sub−layer

Command Codes

The valid one−byte value for the *Command* field of the local frame are listed below:

Table 46. COMMAND CODES

Command	Initiator	Mode	Code
Synchro_Indication	AMIS−49587 (Synchro_Data)	Master / Slave	10h
Desynchro_Request	Base Micro()	Master / Slave / Monitor	11h
Reset_Request	Base Micro()	Master / Slave / Monitor/ Not Set	21h
WriteConfigNew_Request	Base Micro (Data_Config)	Master / Slave / Monitor/ Not Set	71h
WriteConfigNew_Confirm	AMIS−49587 (Data_Config_Echo)	Master / Slave / Monitor/ Not Set	72h
WriteConfigNew_Error	AMIS−49587 (Error_Code)	Master / Slave / Monitor/ Not Set	73h
WriteDB_Request	Base Micro (DB_Data_Id)	Master / Slave	41h
WriteDB_Confirm	AMIS−49587 (DB_Data_Id_Echo)	Master / Slave	42h
WriteDB_Error	AMIS−49587 (Error_Code)	Master / Slave	43h
MA_DATA_Indication	AMIS−49587 (MAC_Frame)	Master / Slave	50h
MA_DATA_Request	Base Micro (MAC_Frame)	Master / Slave	51h
MA_DATA_Confirm	AMIS−49587 (Transmission_Status)	Master / Slave	52h
MA_DATA_Indication_Bad_CRC	AMIS−49587 (MAC_Frame)	Master / Slave	53h
ISA_Request	Base Micro (Data_ISA)	Master / Slave	61h
ISA_Confirm	AMIS−49587 (Transmission_Status)	Master / Slave	62h
SPY_No_SubFrame	AMIS−49587 (SpyData)	Monitor	A0h
SPY_SubFrame	AMIS−49587 (SpyData, PHY_sdu)	Monitor	B0h
SPY_Search_Synchro	AMIS−49587 ()	Monitor	C0h
SPY_Synchro_Found	AMIS−49587 (SpyData)	Monitor	D0h
Spy_No_Alarm_Found	AMIS−49587 (SpyData, AlarmPattern)	Monitor	E0h
Spy_Alarm_Found	AMIS−49587 (SpyData, AlarmPattern)	Monitor	F0h

Remark: The highest nibble indicates the service and the lowest nibble indicates the primitive.

SERVICE			PRIMITIVE	
Name	Code		Name	Code
Synchro	1X		Indication	X0
Reset	2X		Request	X1
WriteConfig	3X		Confirm	X2
WriteDB	4X		Error	X3
MA_Data	5X			
ISA_Call	6X			
ISB_Call	7X		Test	X4 .. X9
SPY_No_SubFrame	Ax		Indication	x0
SPY_SubFrame	Bx			
SPY_Search_Synchro	Cx			
SPY_Synchro_Found	Dx			
SPY_No_Alarm_Found	Ex			
SPY_Alarm_Found	Fx			

APPENDIX E : TIMINGS

TIME−OUT VALUES

The values of the AMIS−49587 constant timings are listed below:

Table 47. TIME−OUT VALUES

Time−out	Meaning		Value	
Tpoll	Delay max. awaited by the base micro between the T_REQ pull down and the status message transmission (delay polling)		20 ms	
Tsr	Delay max. awaited by the AMIS−49587 between the end of the status transmitting and the reception of the STX character in the base micro frame (delay status/reception)		200 ms	
Tack	Delay max. awaited by either the AMIS−49587 or the base micro between the end of a transmitting and the reception of the ACK or NAK character sent by the other (delay ack).		40 ms	
Twbc	Delay max. awaited by either the AMIS−49587 or the base micro between the end of a reception and the transmission of the next frame (delay waiting before continue).		5 ms	
Tic	Delay max. awaited by either the AMIS−49587 or the base micro between two characters (delay inter characters) Programmable with the bit 7 of repeater parameter in the configuration frame	Bit 7 = 1	10 ms	
		Bit 7 = 0	4800 baud	10 ms
			9600 baud	5 ms
			19200 baud	2.5 ms
			38400 baud	1.25 ms

APPENDIX F : PHYSICAL FRAMES

Time Slot Example 1

When receiving one frame made up of several sub−frames (2) with current credit = 1
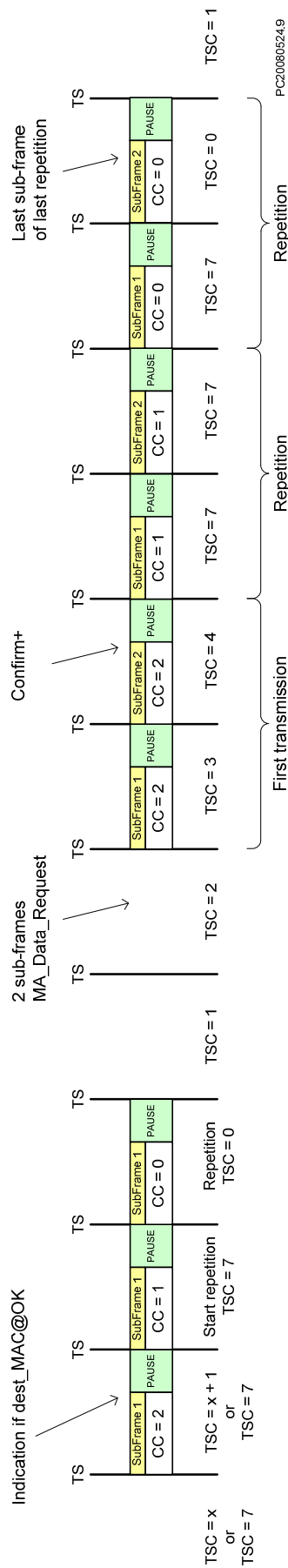Example 1: Receiving one frame made up of 2 sub−frames with current credit = 1
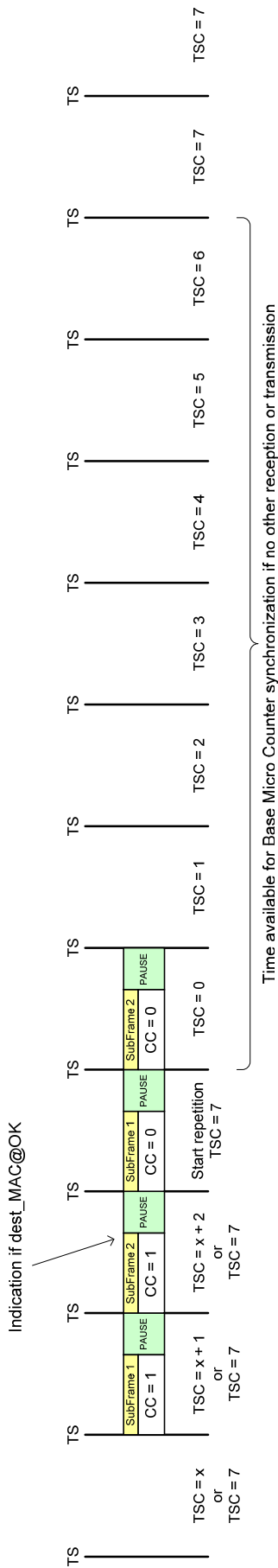
Figure 21. Time Slot Counter Handling: Example 1

Time Slot Example 2

When receiving one frame made up of one sub−frame with current credit = 4
Example 2: Receiving one frame made up of 1 sub−frame with current credit = 4.
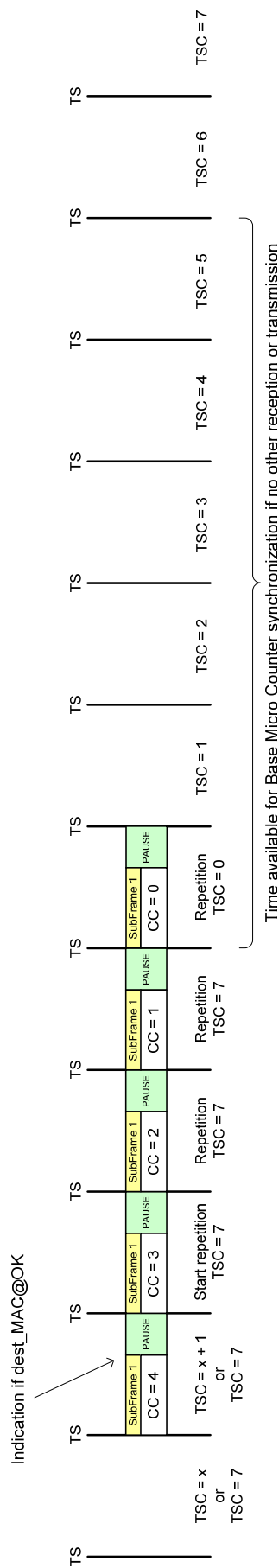
Figure 22. Time Slot Counter Handling: Example 2

Time Slot Example 3

When receiving two consecutives frames with current credit > 0
Example 3: Receiving one sub−frame with current credit = 0

Indication if dest_MAC@OK

SubFrame 1 | CC = 0 | PAUSE

TSC = x or TSC = 7 | TSC = x + 1 or TSC = 7 | TSC = 1 | TSC = 0 | TSC = x + 2 or TSC = 7 | TSC = 2 | TSC = 3 | TSC = 4 | TSC = 5 | TSC = 6 | TSC = 7 | TSC = 7 | TSC = 7

Time available for Base Micro Counter synchronization if no other reception or transmission
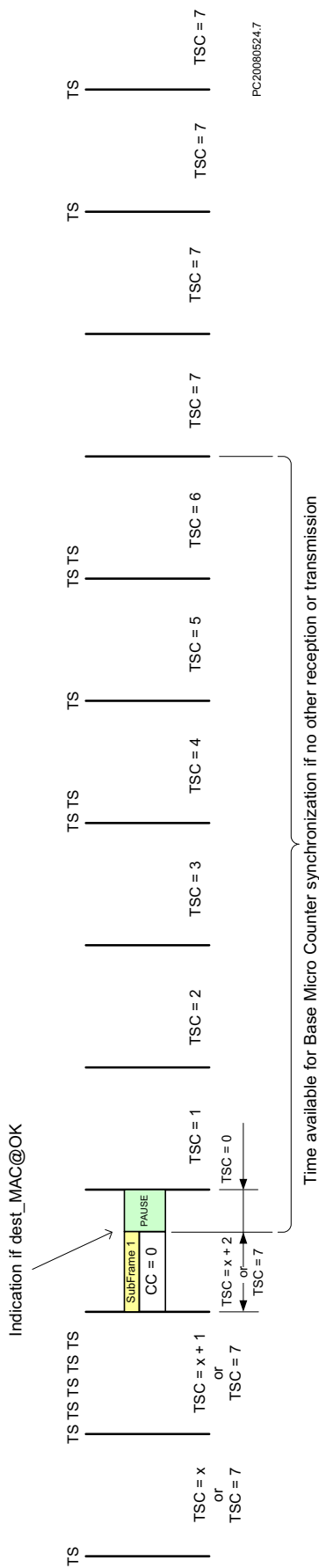
PC20080524.7

Figure 23. Time Slot Counter Handling: Example 3

Time Slot Example 4

When receiving a frame made up of one sub−frame with current credit = 2 and transmitting a frame made up of two sub−frames with the same credit
Example 5: When Receiving a frame made up of 1 sub−frame with current credit = 2 and transmitting a frame made of 2 sub−frames with the same credit

Indication if dest_MAC@OK

SubFrame 1 | CC = 2 | PAUSE
SubFrame 1 | CC = 1 | PAUSE
SubFrame 1 | CC = 0 | PAUSE

TSC = x or TSC = 7 | TSC = x + 1 or TSC = 7 | Start repetition TSC = 7 | Repetition TSC = 0 | TSC = 1 | TSC = 2

2 sub-frames MA_Data_Request

First transmission | Repetition | Repetition

Confirm+

SubFrame 1 | CC = 2 | PAUSE
SubFrame 2 | CC = 2 | PAUSE
SubFrame 1 | CC = 1 | PAUSE
SubFrame 2 | CC = 1 | PAUSE
SubFrame 1 | CC = 0 | PAUSE
SubFrame 2 | CC = 0 | PAUSE

TSC = 3 | TSC = 4 | TSC = 7 | TSC = 7 | TSC = 7 | TSC = 0 | TSC = 1

Last sub-frame of last repetition

PC20080524.9

Figure 24. Time Slot Counter Handling: Example 4

RELATED DOCUMENTS

In this document, reference is made to:

− [2] IEC 61334−5−1 The Spread Frequency Shift Keying (S−FSK) profile (International Electro−Technical Commission)

PACKAGE DIMENSIONS

PLCC 28 LEAD
CASE 776AA−01
ISSUE O
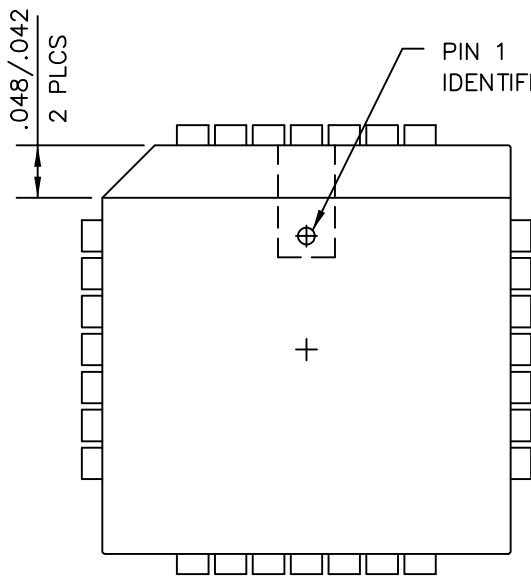
TOP VIEW
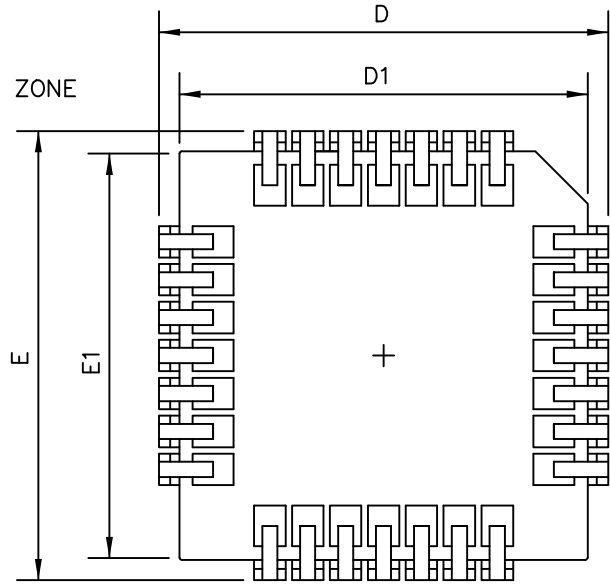
BOTTOM VIEW

SIDE VIEW

SEATING PLANE
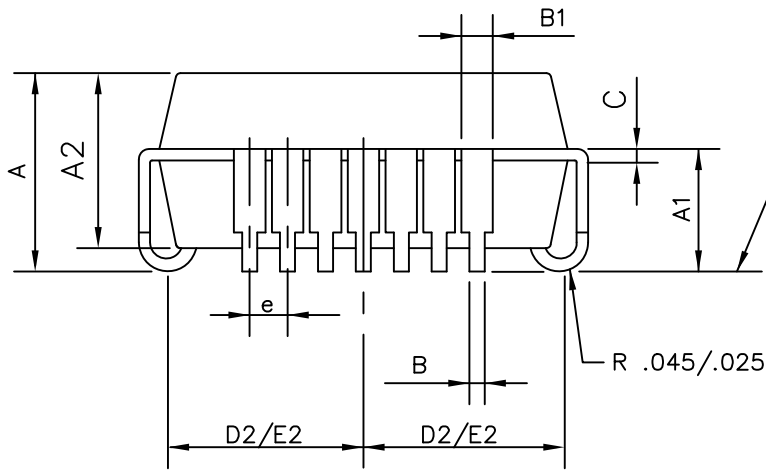
SYMBOL	MIN	NOM	MAX
A	0.165	0.172	0.180
A1	0.090	0.105	0.120
A2	0.148	0.152	0.156
B	0.013	0.017	0.021
B1	0.026	0.029	0.032
C	0.008	0.010	0.012
D	0.485	0.490	0.495
D1	0.450	0.453	0.456
D2	0.195	0.210	0.215
E	0.485	0.490	0.495
E1	0.450	0.453	0.456
E2	0.195	0.210	0.215
e	0.050 REF.		

ALL DIMENSIONS ARE IN INCHES.