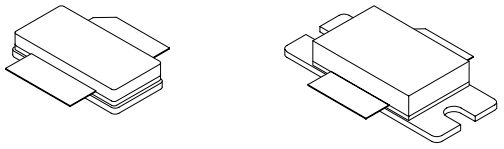
TriQuint SEMICONDUCTOR

AGR21125E
125 W, 2.110 GHz—2.170 GHz, N-Channel E-Mode, Lateral MOSFET

Introduction

The AGR21125E is a high-voltage, gold-metalized, enhancement mode, laterally diffused metal oxide semiconductor (LDMOS) RF power transistor suitable for wideband code division multiple access (W-CDMA), single and multicarrier class AB wireless base station power amplifier applications.



AGR21125EU (unflanged) **AGR21125EF (flanged)**

Figure 1. Available Packages

Features

Typical performance for two carrier 3GPP W-CDMA systems. F1 = 2135 MHz and F2 = 2145 MHz with 3.84 MHz channel BW, adjacent channel BW = 3.84 MHz at F1 – 5 MHz and F2 + 5 MHz. Third-order distortion is measured over 3.84 MHz BW at F1 – 10 MHz and F2 + 10 MHz. Typical P/A ratio of 8.5 dB at 0.01% (probability) CCDF:
- Output power: 28 W.
- Power gain: 14 dB.
- Efficiency: 27%.
- IM3: –34.5 dBc.
- ACPR: –38 dBc.
- Return loss: –10 dB.

High-reliability, gold-metalization process.

Low hot carrier injection (HCI) induced bias drift over 20 years.

Internally matched.

High gain, efficiency, and linearity.

Integrated ESD protection.

Device can withstand a 10:1 voltage standing wave ratio (VSWR) at 28 Vdc, 2140 MHz, 125 W continuous wave (CW) output power.

Large signal impedance parameters available.

Table 1. Thermal Characteristics

Parameter	Sym	Value	Unit
Thermal Resistance, Junction to Case:			
AGR21125EU	$R_{\theta JC}$	0.5	°C/W
AGR21125EF	$R_{\theta JC}$	0.5	°C/W

Table 2. Absolute Maximum Ratings*

Parameter	Sym	Value	Unit
Drain-source Voltage	V_{DSS}	65	Vdc
Gate-source Voltage	V_{GS}	–0.5, +15	Vdc
Total Dissipation at T_C = 25 °C:			
AGR21125EU	P_D	350	W
AGR21125EF	P_D	350	W
Derate Above 25 ˚C:			
AGR21125EU	—	2.0	W/°C
AGR21125EF	—	2.0	W/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{STG}	–65, +150	°C

* Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 3. ESD Rating*

AGR21125E	Minimum (V)	Class
HBM	500	1B
MM	50	A
CDM	1500	4

* Although electrostatic discharge (ESD) protection circuitry has been designed into this device, proper precautions must be taken to avoid exposure to ESD and electrical overstress (EOS) during all handling, assembly, and test operations. PEAK Devices employs a human-body model (HBM), a machine model (MM), and a charged-device model (CDM) qualification requirement in order to determine ESD-susceptibility limits and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in each of the models, as defined by JEDEC's JESD22-A114B (HBM), JESD22-A115A (MM), and JESD22-C101A (CDM) standards.

Caution: MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Electrical Characteristics

Recommended operating conditions apply unless otherwise specified: T_C = 30 °C.

Table 4. dc Characteristics

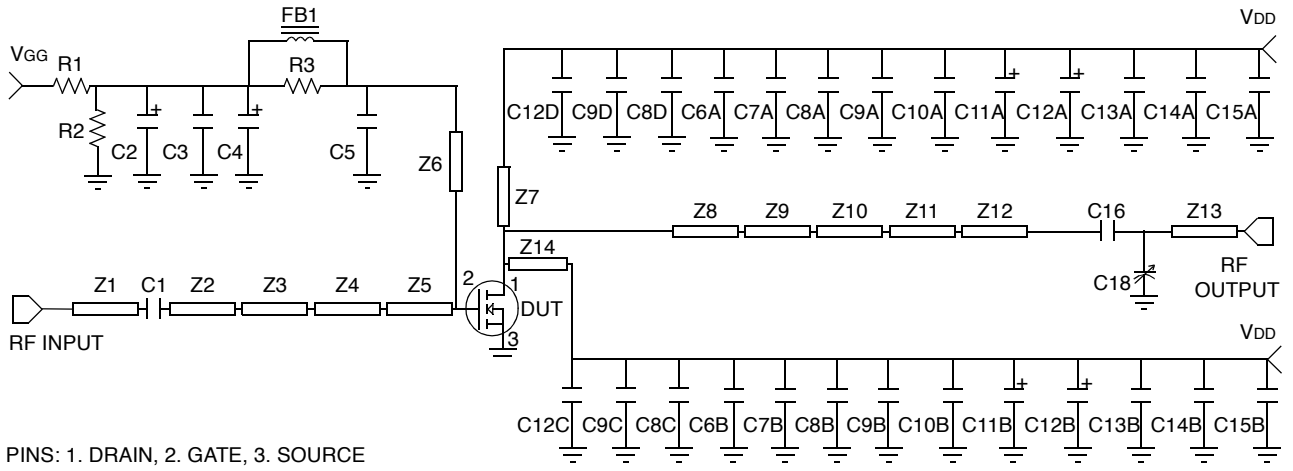
Parameter	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-source Breakdown Voltage (V_{GS} = 0, I_D = 400 μA)	$V_{(BR)DSS}$	65	—	—	Vdc
Gate-source Leakage Current (V_{GS} = 5 V, V_{DS} = 0 V)	I_{GSS}	—	—	4	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	—	—	200	μAdc
On Characteristics					
Forward Transconductance (V_{DS} = 10 V, I_D = 1 A)	G_{FS}	—	9	—	S
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 400 μA)	$V_{GS(TH)}$	—	—	4.8	Vdc
Gate Quiescent Voltage (V_{DS} = 28 V, I_D = 1200 mA)	$V_{GS(Q)}$	—	3.8	—	Vdc
Drain-source On-voltage (V_{GS} = 10 V, I_D = 1 A)	$V_{DS(ON)}$	—	0.08	—	Vdc

Table 5. RF Characteristics

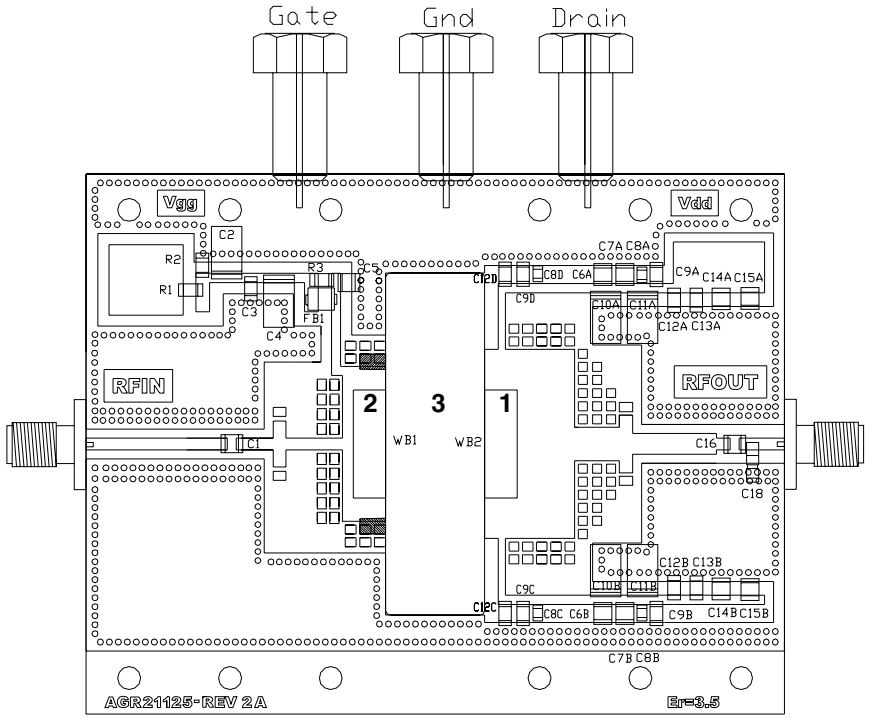
Parameter	Symbol	Min	Typ	Max	Unit
Dynamic Characteristics					
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz) (This part is internally matched on both the input and output.)	C_{RSS}	—	3.0	—	pF
Functional Tests (in Supplied Test Fixture)					
Common-source Amplifier Power Gain*	G_{PS}	12	14	—	dB
Drain Efficiency*	η	25	27	—	%
Third-order Intermodulation Distortion* (IMD3 measured over 3.84 MHz BW @ f1 – 10 MHz and f2 + 10 MHz)	IM3	—	–34.5	–33	dBc
Adjacent Channel Power Ratio* (ACPR measured over BW of 3.84 MHz @ f1 – 5 MHz and f2 + 5 MHz)	ACPR	—	–38	–37	dBc
Input Return Loss*	IRL	—	–10	–9	dB
Power Output, 1 dB Compression Point (V_{DD} = 28 V, f_C = 2140.0 MHz)	P_{1dB}	115	125	—	W
Output Mismatch Stress (V_{DD} = 28 V, P_{OUT} = 125 W (CW), I_{DQ} = 1200 mA, f_C = 2140.0 MHz VSWR = 10:1; [all phase angles])	ψ	No degradation in output power.			

* 3GPP W-CDMA, typical P/A ratio of 8.5 dB at 0.01% CCDF, f1 = 2135.0 MHz, and f2 = 2145 MHz. V_{DD} = 28 Vdc, I_{DQ} = 1200 mA, and P_{OUT} = 28 W avg.

Test Circuit Illustrations for AGR21125E



A. Schematic



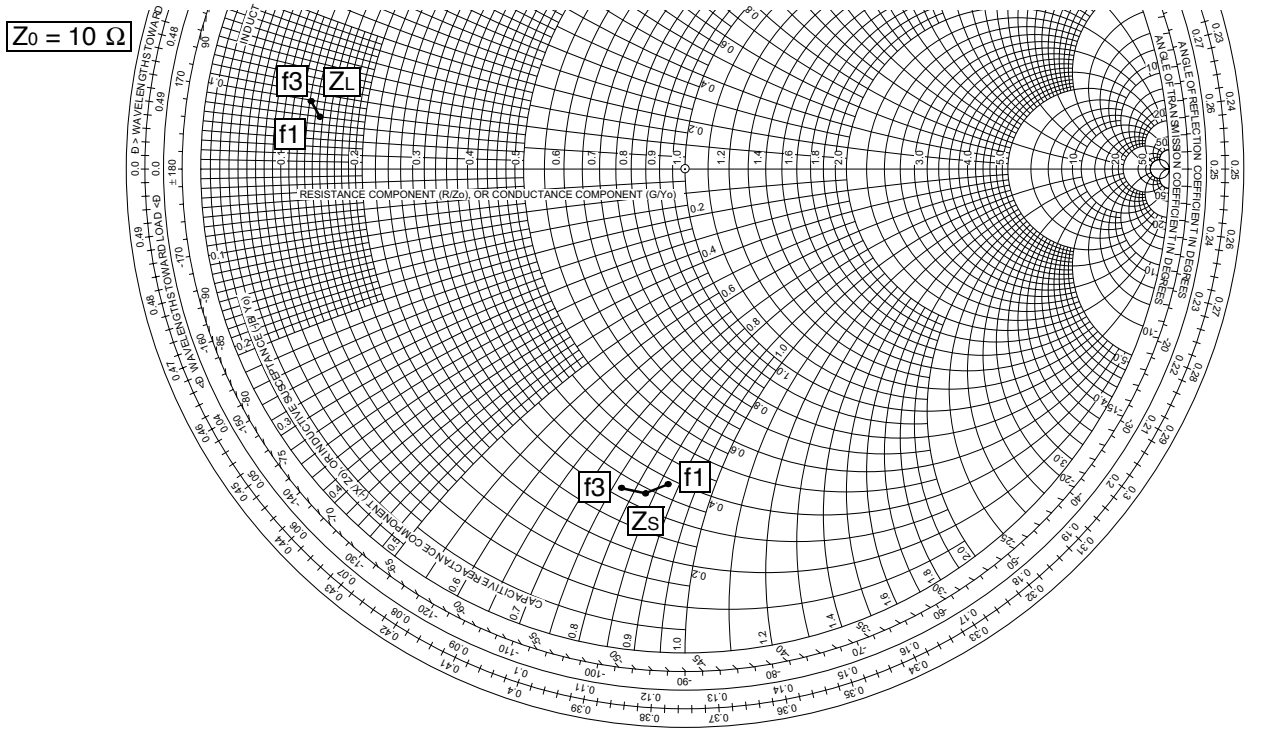
Parts List:

- Microstrip Line:
  Z1 0.785 in. x 0.065 in.
  Z2 0.205 in. x 0.065 in.
  Z3 0.070 in. x 0.255 in.
  Z4 0.315 in. x 0.065 in.
  Z5 0.240 in. x 0.860 in.
  Z6 0.050 in. x 0.467 in.
  Z7 0.050 in. x 0.367 in.
  Z8 0.500 in. x 1.050 in.
  Z9 0.248 in. x 0.185 in.
  Z10 0.075 in. x 0.320 in.
  Z11 0.465 in. x 0.115 in.
  Z12 0.075 in. x 0.065 in.
  Z13 0.252 in. x 0.065 in.
  Z14 0.050 in. x 0.367 in.
- WB1, WB2; 10 mil thick, 0.6 in. x 0.18 in.
- *Fair-Rite*® ferrite bead: FB1 2743019447.
- *Vitramon*® 1206 size chip capacitor:
  C3, C9A, C9B, C9C, C9D 22000 pF.
- 1206 size chip capacitor: 22000 pF
  C12A, C12B, C12C, C12D, C13A, C13B.
- 1206 size chip resistor:
  R1 1 kΩ;
  R2 560 kΩ;
  R3 4.7 Ω.
- *Taconic*® ORCER RF-35 board material, 2 oz. copper, 30 mil thickness, εr = 3.5.
- *ATC*® chip capacitor: C1 10 pF 100B100JW500X; C5, C14A, C14B, C15A, C15B 5.6 pF100B5R6BW500X; C6A, C6B 6.8 pF 100B6R8JW500X; C7A, C7B 1.2 pF 100B1R2BW500X; C16 15 pF 100B150JW500X.
- *Murata*® 0805 size chip capacitor: C8A, C8B, C8C, C8D 0.01 µF GRM40X7R103K100AL.
- *Sprague*® tantalum surface-mount chip capacitor: C2, C4, C10A, C10B, C11A, C11B 22 µF, T491, 35 V.
- *Johanson Giga-Trim*® variable capacitor: C18 0.6 pF to 4.5 pF 27271SL.

B. Component Layout

Figure 2. AGR21125E Test Circuit

Typical Performance Characteristics



MHz (f)	ZS Ω (Complex Source Impedance)	ZL Ω (Complex Optimum Load Impedance)
2110 (f1)	3.8 – j8.7	1.4 + j0.7
2140 (f2)	3.4 – j8.2	1.4 + j0.8
2170 (f3)	3.3 – j7.7	1.3 + j0.9

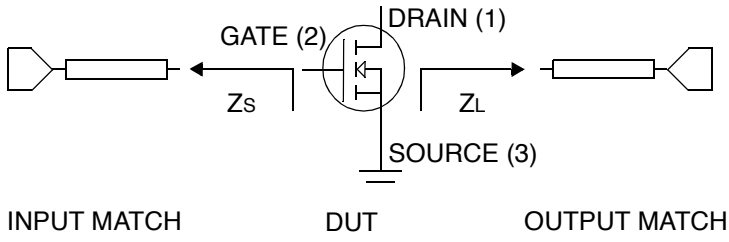


Figure 3. Series Equivalent Input and Output Impedances

Typical Performance Characteristics (continued)

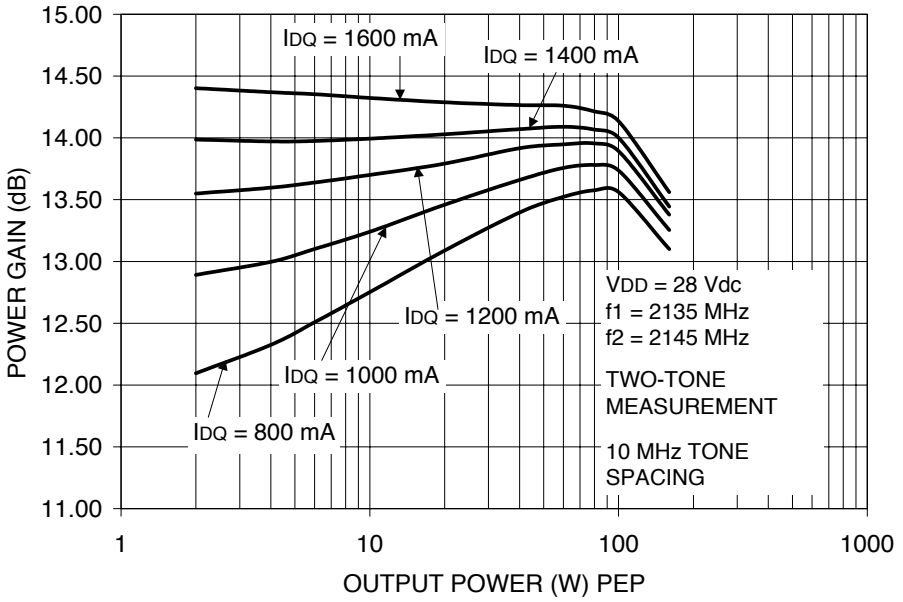


Figure 4. Two-Tone Power Gain vs. Output Power and IDQ

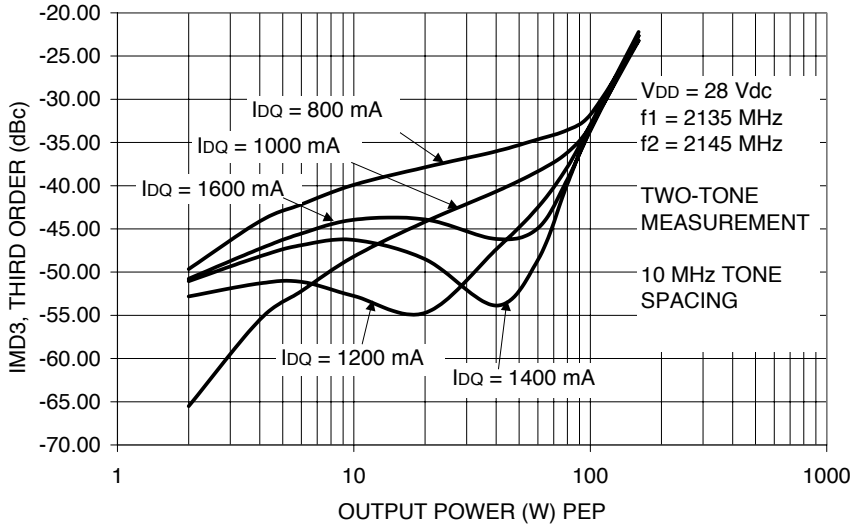


Figure 5. IMD3 vs. Output Power and IDQ

Typical Performance Characteristics (continued)

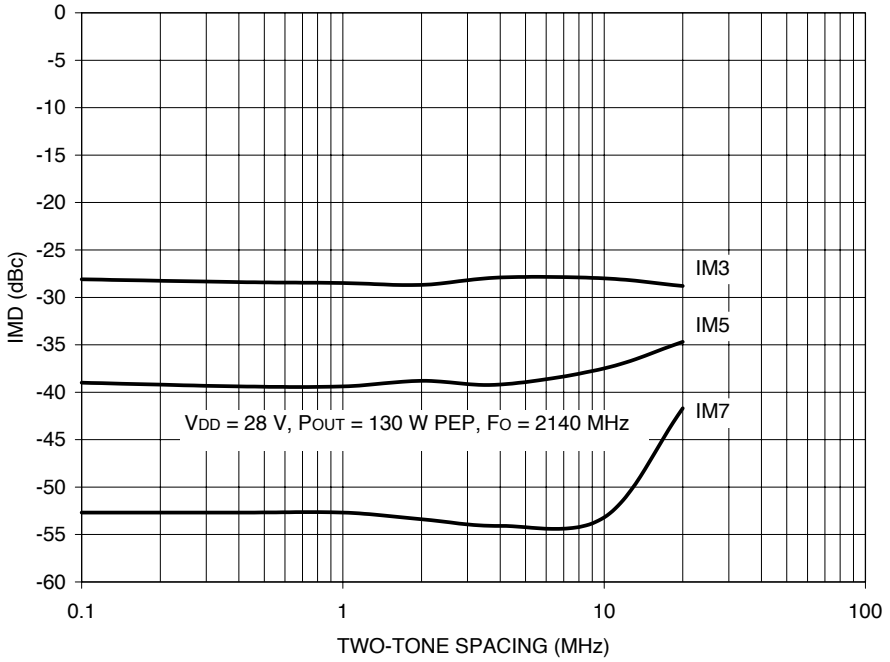


Figure 6. IMD vs. Tone Spacing

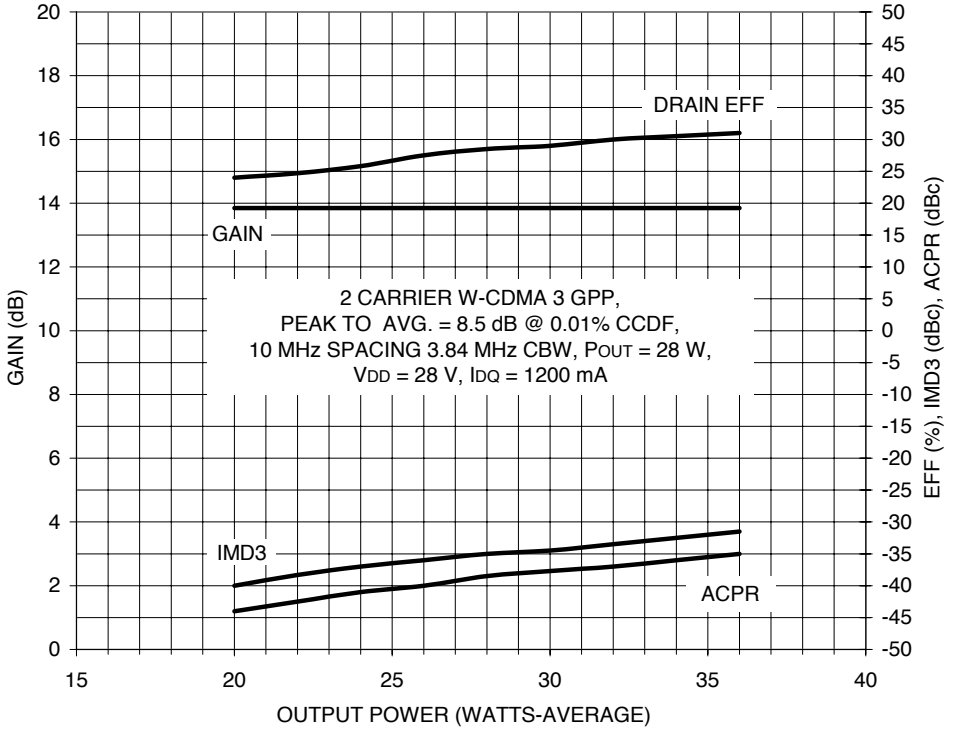


Figure 7. Gain, Efficiency, IMD3, and ACPR vs. Output Power

Typical Performance Characteristics (continued)

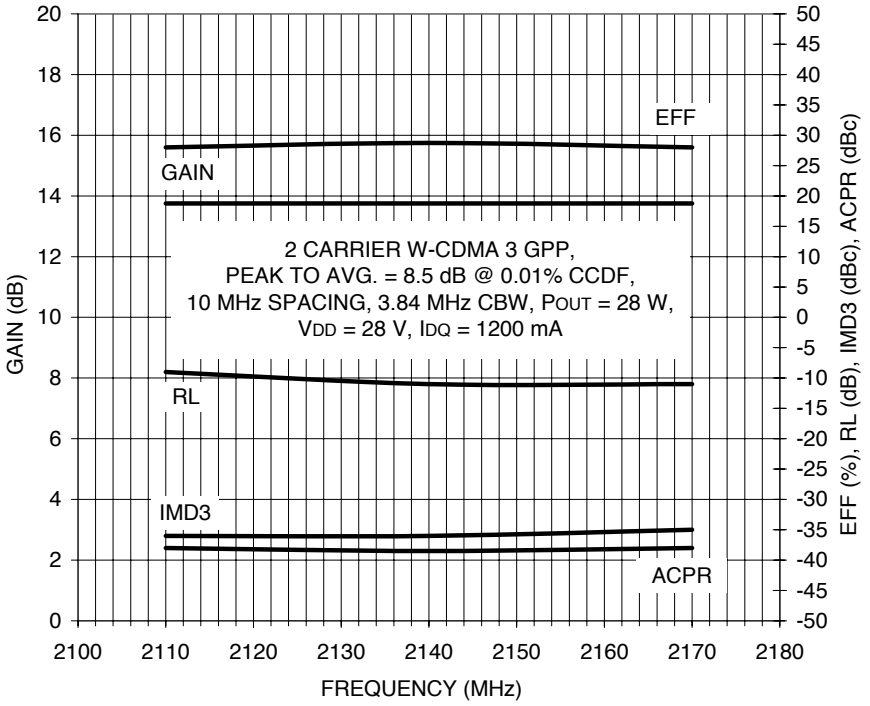


Figure 8. Broadband Performance

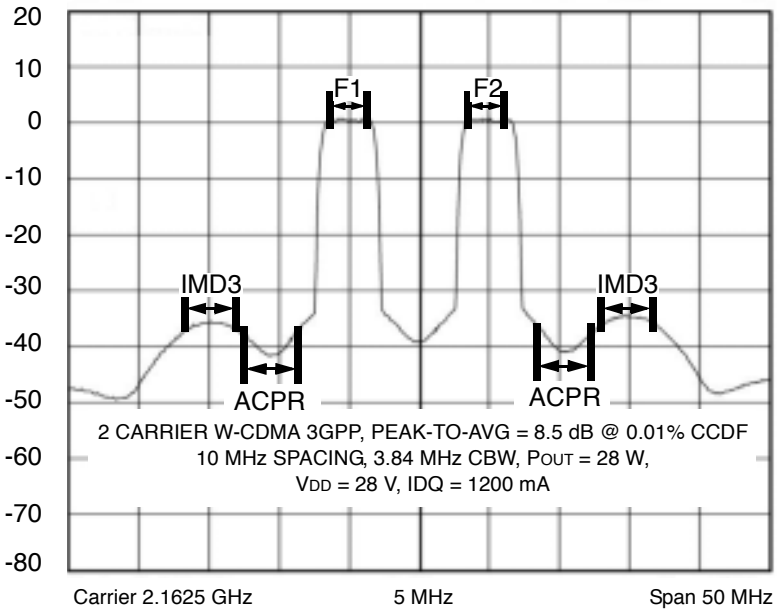


Figure 9. Spectral Plot

Typical Performance Characteristics (continued)

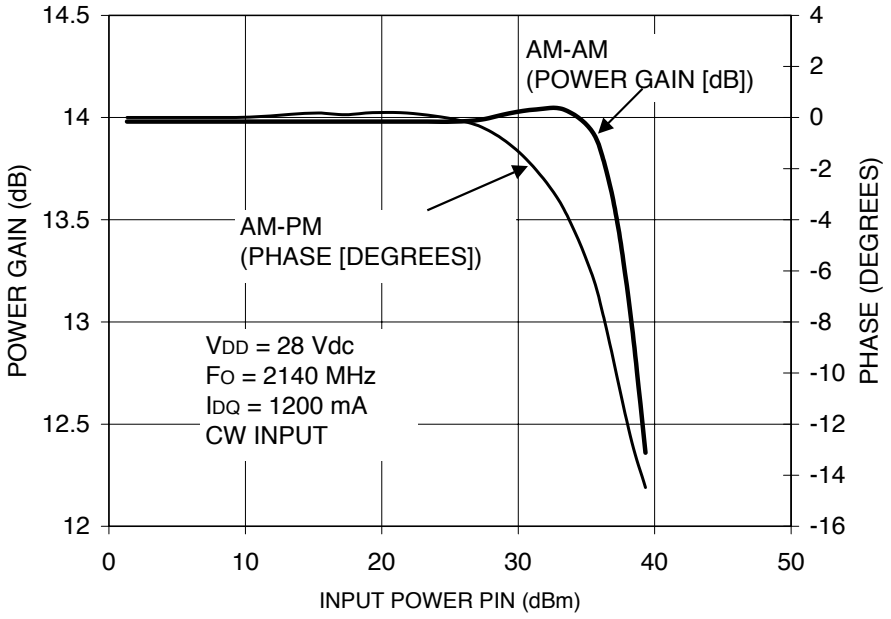
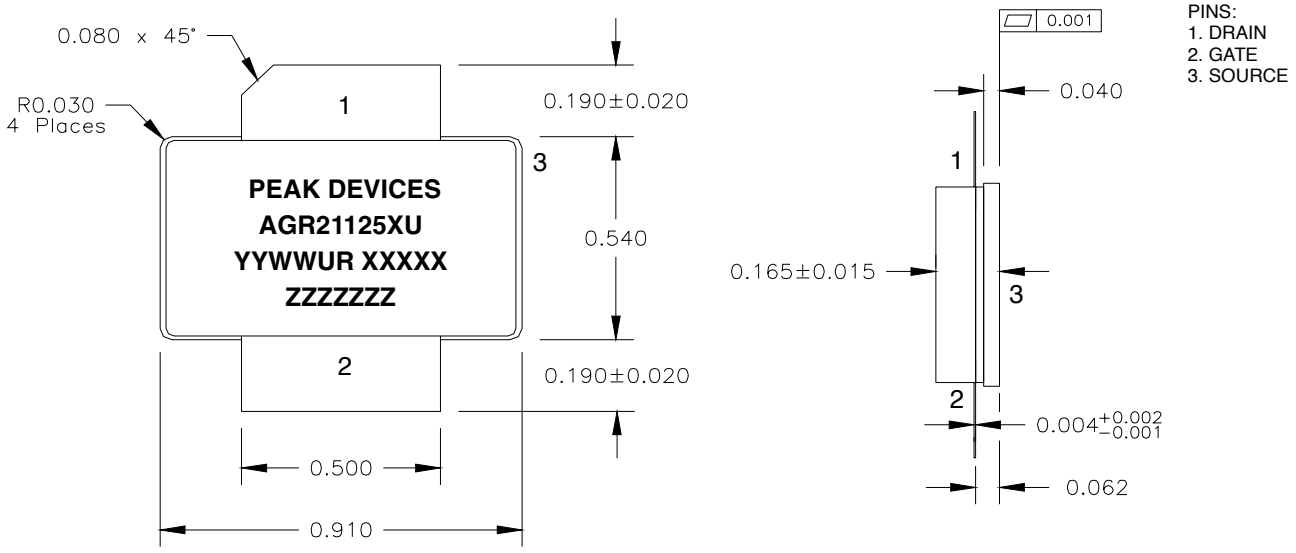


Figure 10. AM-AM and AM-PM Characteristics

Package Dimensions

All dimensions are in inches. Tolerances are ±0.005 in. unless specified. Cut lead indicates drain.

AGR21125EU



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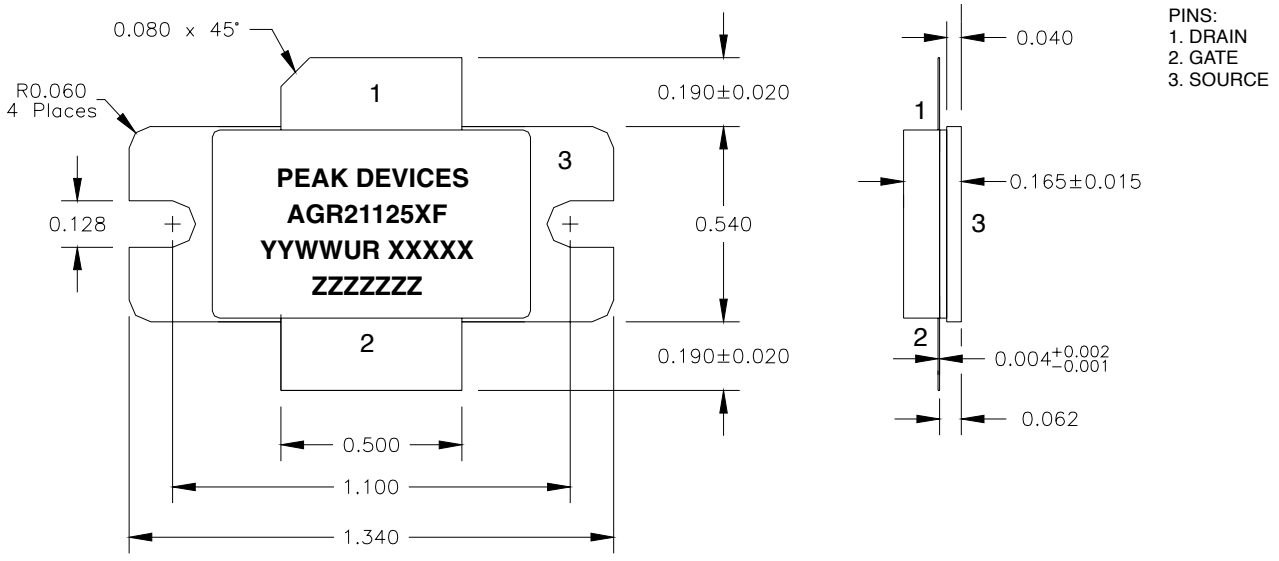

Label Notes:

- M before the part number denotes model program. X before the part number denotes engineering prototype.
- The last two letters of the part number denote wafer technology and package type.
- YYWWLL is the date code including place of manufacture: year year work week (YYWW), LL = location (AL = Allentown, PA; BK = Bangkok, Thailand). XXXXX = five-digit wafer lot number.
- ZZZZZZZ = seven-digit assembly lot number on production parts.
- ZZZZZZZZZZZZ = 12-digit (five-digit lot, two-digit wafer, and five-digit serial number) on models and engineering prototypes.