



System Basis Chip Gen2 with High Speed CAN and LIN Interface

The 33904/5 is the second generation family of System Basis Chips which combine several features and enhance present module designs. The device works as an advanced power management unit for the MCU and additional integrated circuits such as sensors, CAN transceivers. It has a built-in enhanced high speed CAN interface (ISO11898-2 and -5), with local and bus failure diagnostics, protection, and fail safe operation mode. The SBC may include one or two LIN 2.1 interfaces with LIN output pin switches. It includes up to 4 wake-up input pins that can also be configured as output drivers for flexibility.

This device implements multiple Low Power modes, with very low-current consumption. In addition, the device is part of a family concept where pin compatibility, among the various devices with and without LIN interfaces, add versatility to module design.

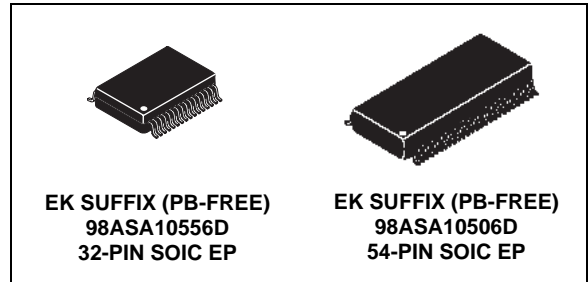
The 33904/5 also implements an innovative and advanced fail-safe state machine and concept solution.

Features

- Protected 5.0V or 3.3V regulators for MCU (part number selectable) and additional ICs (SPI configurable) with optional external PNP usage to increase current capability for MCU.
- Fully-protected embedded 5.0 V regulator for the CAN driver
- Extremely low quiescent current in low power modes
- Multiple under-voltage detections to address various MCU specifications and system operation modes (i.e. cranking)
- Multiple wake-up sources in low power modes: CAN or LIN bus, I/O transition, automatic timer, SPI message, and VDD over-current detection.
- Voltage, current and temperature protection with enhanced diagnostics that can be monitored by system via MUX output
- ISO11898-5 high speed CAN interface compatibility for baud rates of 40 kb/s to 1.0 Mb/s. LIN 2.1 and J2602 LIN interface compatibility
- Pb-free packaging designated by suffix code EK

33904
33905

SBC CAN GEN2



| ORDERING INFORMATION | | |
|----------------------|-------------------------------------|------------|
| Device | Temperature Range (T _A) | Package |
| PCZ33905D3EK/R2 | -40°C to 125°C | 54 SOIC EP |
| MCZ33905D5EK/R2 | | |
| PCZ33905S3EK/R2 | | 32 SOIC EP |
| MCZ33905S5EK/R2 | | |
| PCZ33904A3EK/R2 | | |
| MCZ33904A5EK/R2 | | |

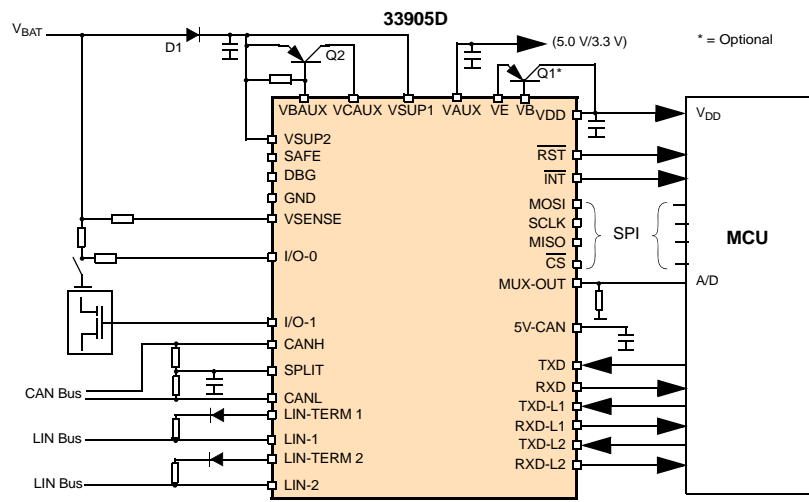


Figure 1. 33905D Simplified Application Diagram

* This document contains certain information on a new product. Specifications and information herein are subject to change without notice.

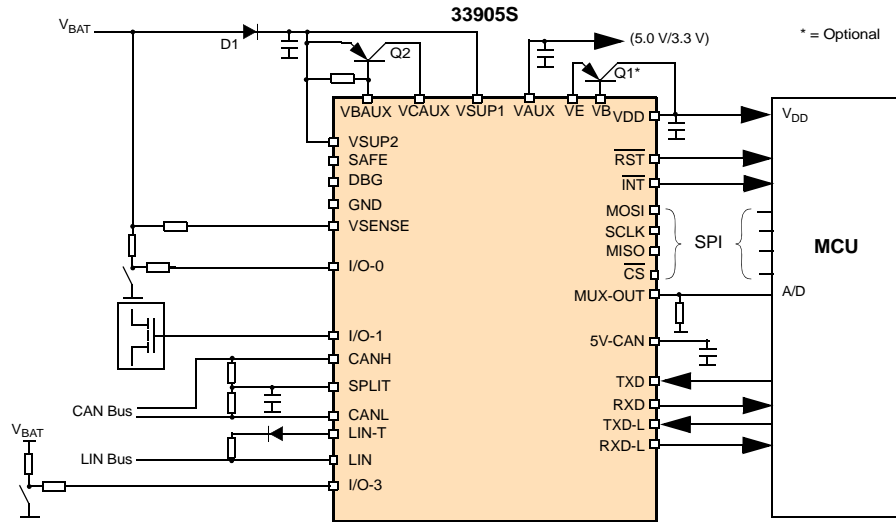


Figure 2. 33905S Simplified Application Diagram

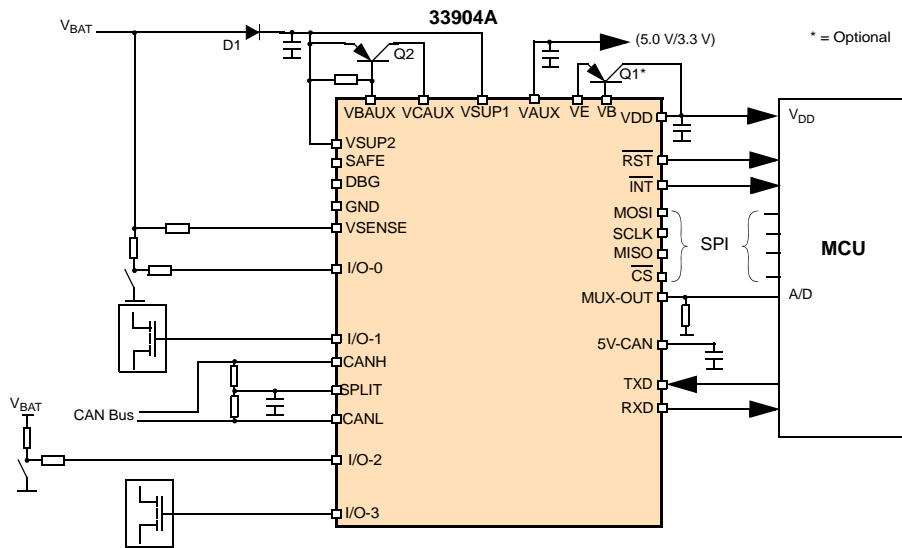


Figure 3. 33904A Simplified Application Diagram

DEVICE VARIATIONS

Table 1. Device Variations

| Freescale Part No. | Vdd output voltage | CAN interface | LIN interface(s) | Wake up input / LIN master termination | Package |
|--------------------|--------------------|--------------------------|------------------|--|--------------------------|
| PCZ33905D3EK/R2 | 3.3V | 1 | 2 | 2 wake up + 2 LIN terms | SOIC 54 pins exposed pad |
| MCZ33905D5EK/R2 | 5V | | | 3 wake up + 1 LIN terms | |
| | | 4 wake up + no LIN terms | | | |
| PCZ33905S3EK/R2 | 3.3V | 1 | 1 | 3 wake up + 1 LIN terms | SOIC 32pins exposed pad |
| MCZ33905S5EK/R2 | 5V | | | 4 wake up + no LIN terms | |
| PCZ33904A3EK/R2 | 3.3V | 1 | no | 4 wake up | SOIC 32pins exposed pad |
| MCZ33904A5EK/R2 | 5V | | | | |

TABLE OF CONTENTS

| | |
|---|----|
| Internal Block Diagram | 5 |
| Pin Connections | 8 |
| Electrical Characteristics | 12 |
| Maximum Ratings | 12 |
| Static Electrical Characteristics | 14 |
| Dynamic Electrical Characteristics | 21 |
| Timing Diagrams | 24 |
| Functional Description | 28 |
| Introduction | 28 |
| Functional Pin Description | 28 |
| Functional Device Operation | 32 |
| Mode and State Description | 32 |
| Low Power Modes | 33 |
| State Diagram | 34 |
| Mode Change | 35 |
| Watchdog Operation | 35 |
| Functional Block Operation Versus Mode | 37 |
| Illustration of Device Mode Transitions | 37 |
| Cyclic Sense Operation During LP Modes | 39 |
| Behavior at Power Up and Power Down | 40 |
| Fail Safe Operation | 42 |
| CAN Interface | 46 |
| CAN Interface Description | 46 |
| CAN Bus Fault Diagnostic | 50 |
| LIN Block | 53 |
| LIN Interface Description | 53 |
| LIN Operational Modes | 53 |
| Serial Peripheral Interface | 55 |
| High Level Overview | 55 |
| Detail Operation | 56 |
| Detail of Control Bits And Register Mapping | 59 |
| Flags | 75 |
| Typical Applications | 80 |
| Packaging | 84 |

INTERNAL BLOCK DIAGRAM

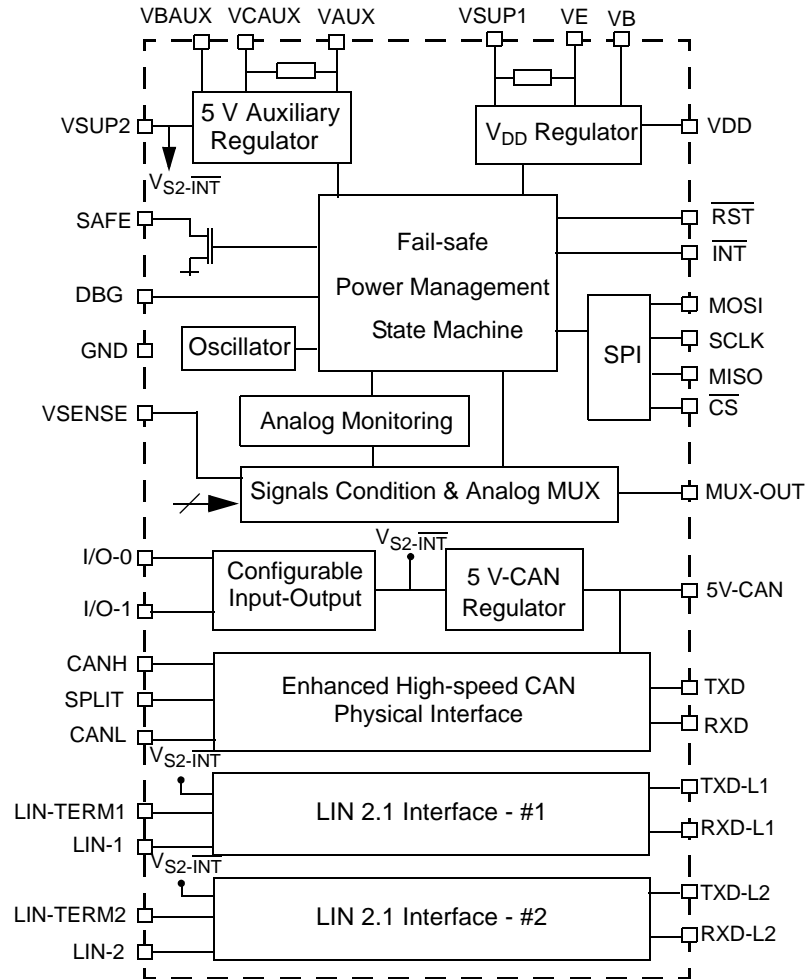


Figure 4. 33905D Internal Block Diagram

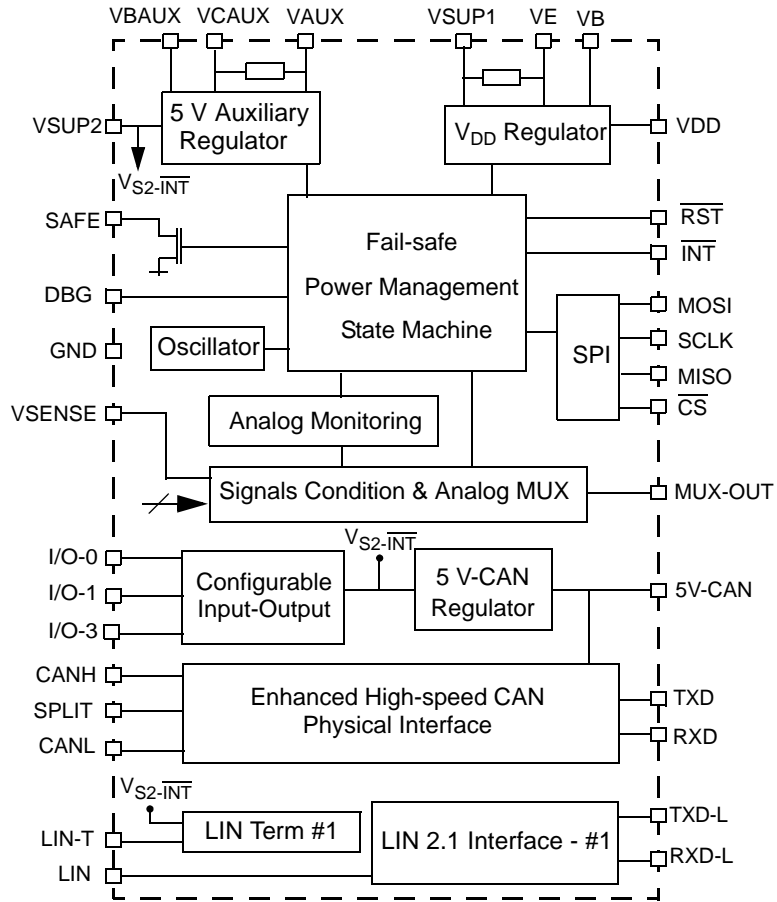


Figure 5. 33905S Internal Block Diagram

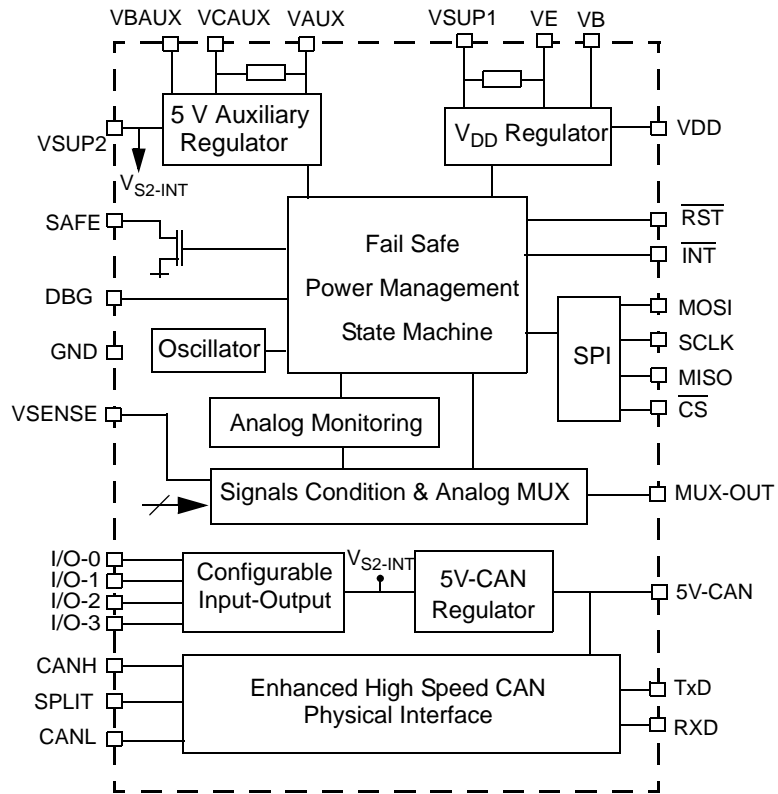


Figure 6. 33904A Internal Block Diagram

PIN CONNECTIONS

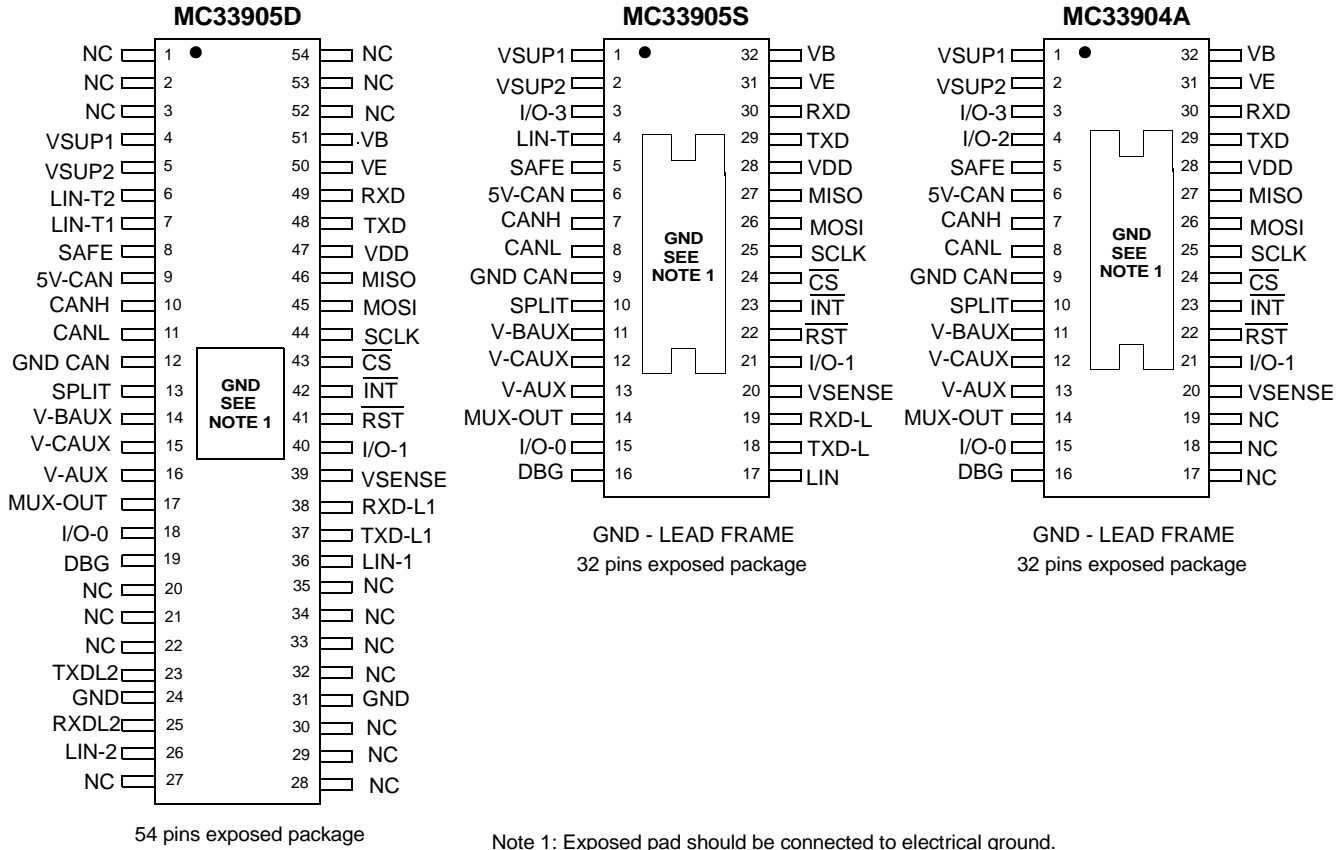


Figure 7. 33904/5 Pin Connections

Table 2. 33904/5 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on [page 28](#).

| Pin # 33905D | Pin # 33905S | Pin # 33904A | Pin Name | Pin Function | Formal Name | Definition |
|-----------------------------|--------------|--------------|----------|--------------|--------------------------|--|
| 1-3,20-22,27-30,32-35,52-54 | N/A | 17, 18, 19 | N/C | No Connect | - | No Connection |
| 4 | 1 | 1 | VSUP1 | Power | Battery Voltage Supply 1 | Supply input for the device internal supplies, power on reset circuitry and the VDD regulator. |
| 5 | 2 | 2 | VSUP2 | Power | Battery Voltage Supply 2 | Supply input for 5 V-CAN regulator, VAUX regulator, I/O and LIN Terminals. |

Table 2. 33904/5 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on [page 28](#).

| Pin # 33905D | Pin # 33905S | Pin # 33904A | Pin Name | Pin Function | Formal Name | Definition |
|-----------------|-----------------|-----------------|------------------------------------|------------------------------|---|--|
| 6 | 3 | 3 | LIN-T2 or I/O-3 | Output or Input/Output | LIN Termination 2 or Input/Output 3 | 33905D, Output pin for the LIN2 master node termination resistor. or 33904A/33905S, Configurable pin as an input or high side output, for connection to external circuitry (switched or small load). The input can be used as a programmable wake-up input in Low Power mode. When used as a high side, no over-temperature protection is implemented. A basic short to GND protection function, based on switch drain-source over-voltage detection, is available. |
| 7 | 4 | 4 | LIN-T1 or LIN-T I/O-2 | Output or Input/Output | LIN Termination 1 or Input/Output 2 I/O-2 | 33905D, Output pin for the LIN1 master node termination resistor. or 33905S, 33905D, Configurable pin as an input or high side output, for connection to external circuitry (switched or small load). The input can be used as a programmable wake-up input in Low Power mode. When used as a high side, no over-temperature protection is implemented. A basic short to GND protection function, based on switch drain-source over-voltage detection, is available. 33904, Configurable terminal as input or high side output, for connection to external circuitry (switched or small load). Input can be used as a programmable wake-up input from Low Power Mode. When used as high side, no over-temperature protection is implemented. A basic short to GND protection function based on switch drain-source over-voltage detection is available. |
| 8 | 5 | 5 | SAFE | Output | Safe Output (Active LOW) | Output of the safe circuitry. The pin is asserted LOW in case of a safe condition is detected (e.g.: software watchdog is not triggered, V_{DD} low, issue on reset pin etc.). Open drain structure. |
| 9 | 6 | 6 | 5 V-CAN | Output | 5V-CAN | Output voltage for the embedded CAN interface. A capacitor must be connected to this pin. |
| 10 | 7 | 7 | CANH | Output | CAN High | CAN high output. |
| 11 | 8 | 8 | CANL | Output | CAN Low | CAN low output. |
| 12 | 9 | 9 | GND-CAN | Ground | GND-CAN | Power GND of the embedded CAN interface |
| 13 | 10 | 10 | SPLIT | Output | SPLIT Output | Output pin for connection to the middle point of the split CAN termination |
| 14 | 11 | 11 | VBAUX | Output | VB Auxiliary | Output pin for external path PNP transistor base |
| 15 | 12 | 12 | VCAUX | Output | VCOLLECTOR Auxiliary | Output pin for external path PNP transistor collector |
| 16 | 13 | 13 | VAUX | Output | VOUT Auxiliary | Output pin for the auxiliary voltage. |
| 17 | 14 | 14 | MUX-OUT | Output | Multiplex Output | Multiplexed output to be connected to an MCU A/D input. Selection of the analog parameter available at MUX-OUT is done via the SPI. A switchable internal pull-down resistor is integrated for V_{DD} current sense measurements. |

Table 2. 33904/5 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on [page 28](#).

| Pin # 33905D | Pin # 33905S | Pin # 33904A | Pin Name | Pin Function | Formal Name | Definition |
|-----------------|-----------------|-----------------|-------------------------------|--------------|-------------------------------|--|
| 18 | 15 | 15 | I/O-0 | Input/Output | Input/Output 0 | Configurable pin as an input or output, for connection to external circuitry (switched or small load). The voltage level can be read by the SPI and via the MUX output pin. The input can be used as a programmable wake-up input in Low Power Mode. In low power, when used as an output, the high side or low side can be activated for a cyclic sense function. |
| 19 | 16 | 16 | DBG | Input | Debug | Input to activate the Debug Mode. In Debug Mode, no watchdog refresh is necessary. Outside of Debug Mode, connection of a resistor between DBG and GND allows the selection of Safe Mode functionality. |
| 23 | N/A | N/A | TXD-L2 | Input | LIN Transmit Data 2 | LIN bus transmit data input. Includes an internal pull-up resistor to V_{DD} . |
| 24,31 | N/A | N/A | GND | Ground | Ground | Ground of the IC. |
| 25 | N/A | N/A | RXD-L2 | Output | LIN Receive Data | LIN bus receive data output. |
| 26 | N/A | N/A | LIN2 | Input/Output | LIN bus | LIN bus input output connected to the LIN bus. |
| 36 | 17 | 17 | 33905D LIN-1 33905S LIN | Input/Output | LIN bus | LIN bus input output connected to the LIN bus. |
| 37 | 18 | 18 | 33905D TXD-L1 33905S TXD-L | Input | LIN Transmit Data | LIN bus transmit data input. Includes an internal pull-up resistor to V_{DD} . |
| 38 | 19 | 19 | 33905D RXD-L1 33905S RXD-L | Output | LIN Receive Data | LIN bus receive data output. |
| 39 | 20 | 20 | VSENSE | Input | Sense input | Direct battery voltage input sense. A serial resistor is required to limit the input current during high voltage transients. |
| 40 | 21 | 21 | I/O-1 | Input/Output | Input Output 1 | Configurable pin as an input or output, for connection to external circuitry (switched or small load). The voltage level can be read by the SPI and via the MUX output pin. The input can be used as a programmable wake-up input in Low Power Mode. Can be used in association with I/O-0 for a cyclic sense function in Low Power Mode. |
| 41 | 22 | 22 | RST | Output | Reset Output (Active LOW) | This is the device reset output whose main function is to reset the MCU. This pin has an internal pull-up to V_{DD} . The reset input voltage is also monitored in order to detect external reset and safe conditions. |
| 42 | 23 | 23 | INT | Output | Interrupt Output (Active LOW) | This output is asserted low when an enabled interrupt condition occurs. The output is a push-pull structure. |
| 43 | 24 | 24 | CS | Input | Chip Select (Active LOW) | Chip select pin for the SPI. When the \overline{CS} is low, the device is selected. In Low Power Mode with V_{DD} ON, a transition on \overline{CS} is a wake-up condition |
| 44 | 25 | 25 | SCLK | Input | Serial Data Clock | Clock input for the Serial Peripheral Interface (SPI) of the device |
| 45 | 26 | 26 | MOSI | Output | Master Out/ Slave In | SPI data received by the device |
| 46 | 27 | 27 | MISO | Input | Master In/Slave Out | SPI data sent to the MCU. When the \overline{CS} is high, MISO is high-impedance |
| 47 | 28 | 28 | VDD | Output | Voltage Digital Drain | 5.0 V or 3.3 V output pin of the main regulator for the Microcontroller supply. |

Table 2. 33904/5 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on [page 28](#).

| Pin # 33905D | Pin # 33905S | Pin # 33904A | Pin Name | Pin Function | Formal Name | Definition |
|-----------------|-----------------|-----------------|----------|--------------|-----------------|--|
| 48 | 29 | 29 | TXD | Input | Transmit Data | CAN bus transmit data input. Internal pull-up to V_{DD} |
| 49 | 30 | 30 | RXD | Output | Receive Data | CAN bus receive data output |
| 50 | 31 | 31 | VE | | Voltage Emitter | Connection to the external PNP path transistor. This is an intermediate current supply source for the V_{DD} regulator |
| 51 | 32 | 32 | VB | Output | Voltage Base | Base output pin for connection to the external PNP pass transistor |
| EX PAD | EX PAD | EX PAD | GND | Ground | Ground | Ground |

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 3. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Ratings | Symbol | Value | Unit |
|--|----------------------|------------------------|------|
| ELECTRICAL RATINGS⁽²⁾ | | | |
| Supply Voltage at V_{SUP1} and V_{SUP2} | | | V |
| Normal Operation (DC) | $V_{SUP1/2}$ | -0.3 to 27 | |
| Transient Conditions (Load Dump) | $V_{SUP1/2TR}$ | -0.3 to 40 | |
| DC voltage on LIN, LIN1 and LIN2 | | | V |
| Normal Operation (DC) | V_{BUSLIN} | -27 to 27 | |
| Transient Conditions (Load Dump) | $V_{BUSLINTR}$ | -27 to 40 | |
| DC voltage on CANL, CANH, SPLIT | | | V |
| Normal Operation (DC) | V_{BUS} | -32 to 27 | |
| Transient Conditions (Load Dump) | V_{BUSTR} | -32 to 40 | |
| DC Voltage at SAFE | | | V |
| Normal Operation (DC) | V_{SAFE} | -0.3 to 27 | |
| Transient Conditions (Load Dump) | V_{SAFETR} | -0.3 to 40 | |
| DC Voltage at I/O-0, I/O-1, I/O-2, I/O-3 (LIN-Terminal Pins) | | | V |
| Normal Operation (DC) | $V_{I/O}$ | -0.3 to 27 | |
| Transient Conditions (Load Dump) | $V_{I/OTR}$ | -0.3 to 40 | |
| DC voltage on TXDL1 TXDL2, RXDL2, RXDL2 | V_{DIGLIN} | -0.3 to $V_{DD} + 0.3$ | V |
| DC voltage on TXD, RXD | V_{DIG} | -0.3 to $V_{DD} + 0.3$ | V |
| DC Voltage at \overline{INT} | $V_{\overline{INT}}$ | -0.3 to 10 | V |
| DC Voltage at \overline{RST} | $V_{\overline{RST}}$ | -0.3 to $V_{DD} + 0.3$ | V |
| DC Voltage at MOSI, MSIO, SCLK and \overline{CS} | $V_{\overline{RST}}$ | -0.3 to $V_{DD} + 0.3$ | V |
| DC Voltage at MUXOUT | V_{MUX} | -0.3 to $V_{DD} + 0.3$ | V |
| DC Voltage at DBG | V_{DBG} | -0.3 to 10 | V |
| Continuous current on CANH and CANL | ILH | 200 | mA |

Table 3. Maximum Ratings (continued)

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Ratings | Symbol | Value | Unit |
|---|--------------|--------|------|
| ESD Capability | | | V |
| * AECQ100 ⁽¹⁾ | | | |
| Human Body Model - JESD22/A114 ($C_{ZAP} = 100 \text{ pF}$, $R_{ZAP} = 1500 \Omega$) | | | |
| CANH and CANL. LIN1 and LIN2, Pins versus all GND pins | V_{ESD1-1} | ±8000 | |
| all other Pins including CANH and CANL | V_{ESD1-2} | ±2000 | |
| Charge Device Model - JESD22/C101 ($C_{ZAP} = 4.0 \text{ pF}$) | | | |
| Corner Pins (Pins 1, 16, 17, and 32) | V_{ESD2-1} | ±750 | |
| All other Pins (Pins 2-15, 18-31) | V_{ESD2-2} | ±500 | |
| * According to IEC 61000-4-2 ($C_{ZAP} = 150 \text{ pF}$, $R_{ZAP} = 330 \Omega$) | | | |
| device unpowered, CANH and CANL pin without capacitor, versus GND | V_{ESD3-1} | ±15000 | |
| device unpowered, LIN pin, versus GND | V_{ESD3-2} | ±15000 | |
| device unpowered, VS1/VS2 (100 nF to GND), versus GND | V_{ESD3-3} | ±15000 | |
| * According to "OEM_HW_Requirements_For_CAN_LIN_FR-Interfaces_V10_20081210.pdf" | | | |
| CANH, CANL without bus filter | V_{ESD4-1} | ±9000 | |
| LIN with and without bus filter | V_{ESD4-2} | ±12000 | |
| I/O with external components (22k - 10nF) | V_{ESD4-3} | ±7000 | |

THERMAL RATINGS

| | | | |
|----------------------|----------|------------|----|
| Junction temperature | T_J | 150 | °C |
| Ambient temperature | T_A | -40 to 125 | °C |
| Storage temperature | T_{ST} | -55 to 165 | °C |

THERMAL RESISTANCE

| | | | |
|---|-----------------|-------------------|------|
| Thermal resistance junction to ambient | $R_{\theta JA}$ | 50 ⁽⁴⁾ | °C/W |
| Peak Package Reflow Temperature During Reflow ^{(2), (3)} | T_{PPRT} | Note 3 | °C |

Notes

- ESD testing is performed in accordance with the Human Body Model (HBM) ($C_{ZAP} = 100 \text{ pF}$, $R_{ZAP} = 1500 \Omega$) and the Charge Device Model (CDM), Robotic ($C_{ZAP} = 4.0 \text{ pF}$).
- The voltage on non- V_{sup} pins should never exceed the V_{sup} voltage at any time or permanent damage to the device may occur. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxx enter 33xxx)], and review parametrics.
- This parameter was measured according to [Figure 8](#) below:

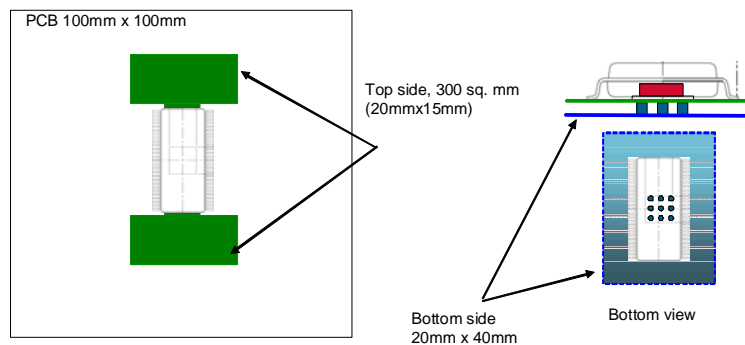


Figure 8. PCB with Top and Bottom Layer Dissipation Area (Dual Layer)

STATIC ELECTRICAL CHARACTERISTICS

Table 4. Static Electrical Characteristics

Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 27\text{ V}$, $-40^\circ\text{C} \leq T_{\text{A}} \leq 125^\circ\text{C}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_{\text{A}} = 25^\circ\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|-----------------------------------|------------------|--------------------|--------------------------|---------------|
| POWER INPUT | | | | | |
| Nominal DC Voltage Range ⁽⁵⁾ | $V_{\text{SUP1}}/V_{\text{SUP2}}$ | 5.5 | - | 27 | V |
| Extended DC Low Voltage Range ⁽⁶⁾ | $V_{\text{SUP1}}/V_{\text{SUP2}}$ | 4.0 | - | 5.5 | V |
| Under-voltage Detector Thresholds, at V_{SUP1} pin, Low threshold (V_{SUP1} ramp down) High threshold (V_{SUP1} ramp up) Hysteresis Note: function not active in Low Power modes | $V_{\text{S1_LOW}}$ | 5.5 - 0.22 | 6.0 - 0.35 | 6.5 6.6 0.5 | V |
| Under-voltage Detector Thresholds, at V_{SUP2} pin: Low threshold (V_{SUP2} ramp down) High threshold (V_{SUP2} ramp up) Hysteresis Note: function not active in Low Power modes | $V_{\text{S2_LOW}}$ | 5.5 - 0.22 | 6.0 - 0.35 | 6.5 6.6 0.5 | V |
| V_{SUP} Over-voltage Detector Thresholds, at V_{SUP1} pin: Not active in Low Power modes | $V_{\text{S_HIGH}}$ | 16.5 | 17 | 18.5 | V |
| Battery loss detection threshold, at V_{SUP1} pin. | BATFAIL | 2 | 2.8 | 4 | V |
| V_{sup} 1 to turn V_{dd} ON, V_{sup1} rising | $V_{\text{sup-th1}}$ | - | 4.1 | 4.5 | V |
| V_{sup} 1 to turn V_{dd} ON, hysteresis (guaranteed by design) | $V_{\text{sup-th1hyst}}$ | 150 | 180 | | mV |
| Supply current ⁽⁷⁾ - from V_{SUP1} - from V_{SUP2} , (5V-CAN V_{aux} , I/O OFF) | I_{SUP1} | - - | 2.0 0.05 | 4.0 0.85 | mA |
| Supply current, $I_{\text{SUP1}} + I_{\text{SUP2}}$, Normal Mode, V_{DD} ON - 5 V-CAN OFF, V_{AUX} OFF - 5 V-CAN ON, CAN interface in Low Power V_{DD} OFF Mode, V_{AUX} OFF - 5 V-CAN OFF, V_{aux} ON - 5 V-CAN ON, CAN interface in TxRx Mode, V_{AUX} OFF, I/O-x disable | $I_{\text{SUP1+2 N1}}$ | - - - - | 2.8 - - - | 4.5 5.0 5.5 8.0 | mA |
| Low Power Mode V_{DD} off. Wake-up from CAN, I/Ox inputs $V_{\text{SUP}} \leq 18\text{ V}$, -40 to 25°C $V_{\text{SUP}} = 18\text{ V}$, 125°C | $I_{\text{LPM_OFF}}$ | - - | 15 - | 35 50 | μA |
| Low Power Mode V_{DD} ON (5.0 V) with V_{DD} under-voltage and V_{DD} over-current monitoring, wake-up from CAN, I/Ox inputs $V_{\text{SUP}} \leq 18\text{ V}$, -40 to 25°C , $I_{\text{DD}} = 1.0\mu\text{A}$ $V_{\text{SUP}} \leq 18\text{ V}$, -40 to 25°C , $I_{\text{DD}} = 100\mu\text{A}$ (20% of I_{DD} load) $V_{\text{SUP}} = 18\text{ V}$, 125°C , $I_{\text{DD}} = 100\mu\text{A}$ | $I_{\text{LPM_ON}}$ | - - - | 20 40 - | - 65 85 | μA |
| Low Power Mode, additional current for oscillator (used for: cyclic sense, forced wake-up, and in Low Power V_{DD} ON Mode cyclic interruption and watchdog) $V_{\text{SUP}} \leq 18\text{ V}$, -40°C to 125°C | I_{OSC} | - | 5.0 | 9 | μA |

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 27\text{ V}$, $-40^\circ\text{C} \leq T_{\text{A}} \leq 125^\circ\text{C}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_{\text{A}} = 25^\circ\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

Notes

- All parameters in spec (ex: V_{DD} regulator tolerance).
- Device functional, some parameters could be out of spec. V_{DD} is active, device is not in Reset Mode if the lowest V_{DD} under-voltage reset threshold is selected (approx. 3.4 V). CAN and I/Os are not operational.
- In Run Mode, CAN interface in Sleep Mode, 5 V-CAN and VAUX turned off. I_{OUT} at $V_{\text{DD}} < 50\text{ mA}$. Ballast: turned off or not connected.

V_{DD} VOLTAGE REGULATOR, PIN VDD

| | | | | | |
|---|-----------------------|-----------------|-------------------|-----------------|------------------|
| Output Voltage $V_{\text{SUP}} 5.5$ to 27 V , $I_{\text{OUT}} 0$ to 100 mA $V_{\text{SUP}} 5.5$ to 27 V , $I_{\text{OUT}} 100$ to 150 mA $V_{\text{SUP}} 5.5$ to 27 V , $I_{\text{OUT}} 0$ to 150 mA | $V_{\text{OUT-5}}$ | 4.9 - 4.9 | 5.0 5.0 5.0 | 5.1 - 5.1 | V |
| Drop voltage without external PNP pass transistor $I_{\text{OUT}} = 100\text{ mA}$ $I_{\text{OUT}} = 150\text{ mA}$ | V_{DROP} | - - | 330 - | 450 500 | mV |
| Drop voltage with external transistor $I_{\text{OUT}} = 200\text{ mA}$ ($I_{\text{BALLAST}} + I_{\text{INTERNAL}}$) | $V_{\text{DROP-B}}$ | - | 350 | 500 | mV |
| External ballast versus internal current ratio ($I_{\text{BALLAST}} = K \times \text{Internal current}$) | K | 1.5 | 2.0 | 2.5 | |
| Output Current limitation, without external transistor | I_{LIM} | 150 | 350 | 550 | mA |
| Temperature prewarning (guaranteed by design) | T_{PW} | - | 140 | - | $^\circ\text{C}$ |
| Thermal shutdown (guaranteed by design) | T_{SD} | 160 | - | - | $^\circ\text{C}$ |
| Range of decoupling capacitor (guaranteed by design) | C_{EXT} | 4.7 | - | 100 | μF |
| Low Power Mode V_{DD} ON, output voltage -5.0 V , $I_{\text{OUT}} \leq 50\text{ mA}$ (time limited) $5.6\text{ V} \leq V_{\text{SUP}} \leq 27\text{ V}$ | $V_{\text{DDL P5}}$ | 4.75 | 5.0 | 5.25 | V |
| Low Power Mode V_{DD} ON, dynamic output current capability (Limited duration. Ref to device description). | $L_{\text{P-IOUTDC}}$ | - | - | 50 | mA |
| Low Power V_{DD} ON Mode: - Over-current wake-up threshold. - Hysteresis | $L_{\text{P-ITH}}$ | 1.0 0.1 | 3.0 1.0 | - - | mA |
| Low Power Mode V_{DD} ON, drop voltage, at $I_{\text{OUT}} = 30\text{ mA}$ (Limited duration. Ref to device description). | $L_{\text{P-VDROP}}$ | - | 200 | 400 | mV |
| Low Power Mode V_{DD} ON, min V_{SUP} operation (Below this value, a V_{DD} , under-voltage reset may occur) | $L_{\text{P-MINVS}}$ | 5.5 | - | - | V |
| VDD when $V_{\text{sup}} < V_{\text{sup-th1}}$, at $I_{\text{VDD}} \leq 10\mu\text{A}$ (guaranteed by design) | VDD_off | | | 0.3 | V |
| VDD when $V_{\text{sup}} \geq V_{\text{sup-th1}}$, at $I_{\text{VDD}} \leq 40\text{mA}$ (guaranteed with parameter $V_{\text{sup-th1}}$) | VDD_start up | 3.0 | | | V |

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 27\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25^\circ\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|------------------------------|--------------|------------|--------------|------------------|
| VOLTAGE REGULATOR FOR CAN INTERFACE SUPPLY, PIN 5 V-CAN⁽⁸⁾ | | | | | |
| Output voltage, $V_{\text{SUP}2} = 5.5$ to 40 V $I_{\text{OUT}} 0$ to 80 mA $I_{\text{OUT}} 80$ to 200 mA | $5V_{\text{-C}}\text{ OUT}$ | 4.75 4.75 | 5.0 5.0 | 5.25 5.25 | V |
| Output Current limitation ⁽¹⁰⁾ | $5V_{\text{-C}}\text{ ILIM}$ | 160 | 280 | - | mA |
| Under-voltage threshold | $5V_{\text{-C}}\text{ UV}$ | 4.1 | 4.5 | 4.7 | V |
| Thermal shutdown (guaranteed by design) | $5V_{\text{-C}}\text{ TS}$ | 160 | - | - | $^\circ\text{C}$ |
| External capacitance (guaranteed by design) | $C_{\text{EXT-CAN}}$ | 1.0 | - | 100 | μF |
| V AUXILIARY OUTPUT, 5 V AND 3.3 V SELECTABLE PIN VB-AUX, VC-AUX, VAUX⁽⁹⁾ | | | | | |
| VAUX output voltage, $V_{\text{SUP}} = V_{\text{SUP}2} 5.5$ to 40 V , $I_{\text{OUT}} 0$ to 150 mA | $V_{\text{AUX}5}$ | 4.75 | 5.0 | 5.25 | V |
| VAUX output voltage, $V_{\text{SUP}} = V_{\text{SUP}2} 5.5$ to 40 V , $I_{\text{OUT}} 0$ to 150 mA | $V_{\text{AUX}3}$ | 3.2 | 3.3 | 3.4 | V |
| VAUX under-voltage detector (5.0 V) - Low Threshold - Hysteresis | $V_{\text{AUX-UVTH}5}$ | 4.2 0.06 | 4.5 - | 4.70 0.12 | V |
| VAUX under-voltage detector (5 and 3.3V versions) | $V_{\text{AUX-UVTH}3}$ | 2.75 | 3.0 | 3.2 | V |
| VAUX over-current threshold detector V_{aux} set to 3.3 V V_{aux} set to 5.0 V | $V_{\text{AUX-ILIM}}$ | 250 230 | 360 330 | 450 430 | mA |
| External capacitance (guaranteed by design) | $V_{\text{aux cap}}$ | 2.2 | - | 100 | μF |
| UNDERVOLTAGE RESET AND RESET FUNCTION, RST PIN | | | | | |
| V_{DD} under-voltage threshold down - $90\% V_{\text{DD}}$ ($V_{\text{DD}} 5.0\text{ V}$) ^{(11), (13)} V_{DD} under-voltage threshold up - $90\% V_{\text{DD}}$ ($V_{\text{DD}} 5.0\text{ V}$) | $R_{\text{ST-TH}1-5}$ | 4.5 - | 4.65 - | 4.85 4.90 | V |
| V_{DD} under-voltage reset threshold down - $70\% V_{\text{DD}}$ ($V_{\text{DD}} 5.0\text{ V}$) ^{(12), (13)} | $R_{\text{ST-TH}2-5}$ | 2.95 | 3.2 | 3.45 | V |
| Hysteresis for threshold $90\% V_{\text{DD}}$, 5.0 V device for threshold $70\% V_{\text{DD}}$, 5.0 V device | $R_{\text{ST-HYST}}$ | 20 10 | - - | 150 150 | mV |
| V_{DD} under-voltage reset threshold down - Low Power V_{DD} ON Mode (note: device change to Normal Request Mode). | $R_{\text{ST-LP}}$ | 4.0 | 4.5 | 4.85 | V |
| Reset V_{OL} @ 1.5 mA , $V_{\text{SUP}} 2.5$ to 40 V | V_{OL} | - | 300 | 500 | mV |
| Current limitation, Reset activated, $V_{\text{RESET}} = 0.9 \times V_{\text{DD}}$ | $I_{\text{RESET LOW}}$ | 2.5 | 7.0 | 10 | mA |
| Pull-up resistor (to V_{DD} pin) | $I_{\text{PULL-UP}}$ | 8.0 | 11 | 15 | $\text{k}\Omega$ |
| V_{SUP} to guaranteed reset low level ⁽¹⁴⁾ | $V_{\text{SUP-RSTL}}$ | 2.5 | - | - | V |

Notes

8. The regulator is stable without external capacitor. Usage of external capacitor recommended for AC performance.
9. No external capacitor required for stability. External capacitor might be used to improve AC transient response.
10. Current limitation will report into a flag.
11. Generate a reset or an $\overline{\text{INT}}$. SPI programmable
12. Generate a reset
13. In Run Mode
14. Reset must be maintained low

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 27\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25^\circ\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|----------------------------|-------|------|-----------------------|----------------------------|
| UNDERVOLTAGE RESET AND RESET FUNCTION, RST PIN (CONTINUED) | | | | | |
| Reset input threshold | $R_{\text{ST-VTH}}$ | | | | V |
| Low threshold | | 1.5 | 1.9 | 2.2 | |
| High threshold | | 2.5 | 3.0 | 3.5 | |
| Reset input hysteresis | H_{YST} | 0.5 | 1.0 | 1.5 | V |
| I/O PINS WHEN FUNCTION SELECTED IS OUTPUT | | | | | |
| I/O-0 high side switch drop @ $I = -12\text{ mA}$, $V_{\text{SUP}} = 10.5\text{ V}$ | I/O-0 HSDRP | - | 0.5 | 1.4 | V |
| I/O-2 and I/O-3 high side switch drop @ $I = -20\text{ mA}$, $V_{\text{SUP}} = 10.5\text{ V}$ | I/O-2-3 HSDRP | - | 0.5 | 1.4 | V |
| I/O-1, high side switch drop @ $I = -400\text{ }\mu\text{A}$, $V_{\text{SUP}} = 10.5\text{ V}$ | I/O-1 HSDRP | - | 0.4 | 1.4 | V |
| I/O-0, I/O-1 low side switch drop @ $I = 400\text{ }\mu\text{A}$, $V_{\text{SUP}} = 10.5\text{ V}$ | I/O-0-1 LSDRP | - | 0.4 | 1.4 | V |
| Leakage current | I/O-LEAK | - | 0.1 | 3.0 | μA |
| I/O PINS WHEN FUNCTION SELECTED IS INPUT | | | | | |
| Negative threshold | I/O-NTH | 1.4 | 2.0 | 2.9 | V |
| Positive threshold | I/O-PTH | 2.1 | 3.0 | 3.8 | V |
| Hysteresis | I/O-HYST | 0.2 | 1.0 | 1.4 | V |
| Input current | I/O-IN | -5.0 | 1.0 | 5.0 | μA |
| I/O-0 and I/O-1 input resistor. /O_0 (or I/O-1) selected in MUX register, $2.0\text{ V} < V_{\text{i/o}_x} < 16\text{ V}$ (guaranteed by design). | $R_{\text{I/O-X}}$ | - | 100 | - | $\text{k}\Omega$ |
| VSENSE INPUT | | | | | |
| VSENSE under-voltage threshold (Not active in Low Power Modes) | $V_{\text{SENSE_TH}}$ | | | | V |
| - Low Threshold | | 8.1 | 8.6 | 9.0 | |
| - High threshold | | - | - | 9.1 | |
| - Hysteresis | | 0.1 | 0.25 | 0.5 | |
| Input resistor to GND. In all modes except in Low Power modes. (guaranteed by design). | $V_{\text{SENSE_R}}$ | - | 125 | - | $\text{k}\Omega$ |
| ANALOG MUX OUTPUT | | | | | |
| Output Voltage Range, with external resistor to GND $>2.0\text{ k}\Omega$ | $V_{\text{OUT_MAX}}$ | 0.0 | - | $V_{\text{DD}} - 0.5$ | V |
| Internal pull-down resistor for regulator output current sense | R_{MI} | 0.8 | 1.9 | 2.8 | $\text{k}\Omega$ |
| External capacitor at MUX OUTPUT ⁽¹⁵⁾ (guaranteed by design) | C_{MUX} | - | - | 1.0 | nF |
| Chip temperature sensor coeff (guaranteed by design and device characterization) | TEMP-COEFF | 20 | 21 | 22 | $\text{mV}/^\circ\text{C}$ |
| Chip temperature: MUX-OUT voltage at $T_A = 25^\circ\text{C}$, guaranteed by design and characterization. | V_{TEMP} | 1.5 | 1.65 | 1.8 | V |
| Chip temperature: MUX-OUT voltage at $T_A = 125^\circ\text{C}$ | V_{TEMP} | 3.6 | 3.75 | 3.9 | V |
| Gain for V_{SENSE} , with external $1.0\text{ k } 1\%$ resistor | $V_{\text{SENSE_GAIN}}$ | 5.13 | 5.48 | 5.67 | |
| Offset for V_{SENSE} , with external $1.0\text{ k } 1\%$ resistor | $V_{\text{SENSE_OFFSET}}$ | -20 | - | 20 | mV |
| Divider ratio for V_{SUP1} | $V_{\text{SUP1_RATIO}}$ | 5.335 | 5.5 | 5.665 | |
| Divider ratio for I/O-0 and I/O-1 actual voltage | $V_{\text{I/O_RATIO}}$ | | | | |
| - with attenuation selected (MUX-OUT register bit 3 set to 1); VSUP= 16V | | 3.8 | 4.0 | 4.2 | |
| VSUP= 27V | | 3.75 | 3.95 | 4.15 | |
| - with gain selected (MUX-OUT register bit 3 set to 0) | | - | 2.0 | - | |

Notes

- When C is higher than C_{MUX} , a serial resistor must be inserted

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 27\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25^\circ\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|-------------------------|----------------------------|----------|----------------------------|------------------|
| ANALOG MUX OUTPUT (CONTINUED) | | | | | |
| Internal reference voltage | V_{REF} | 2.425 | 2.5 | 2.575 | V |
| Current ratio between VDD output & I_{OUT} at MUX-OUT (I_{OUT} at MUX-OUT = I_{DD} out / $I_{\text{DD_RATIO}}$) - At $I_{\text{OUT}} = 50\text{ mA}$ - I_{OUT} from 25 mA to 150 mA | $I_{\text{DD_RATIO}}$ | 80 62.5 | 97 97 | 115 117 | |
| SAFE OUTPUT | | | | | |
| SAFE low level, at $I = 500\ \mu\text{A}$ | V_{OL} | 0.0 | 0.2 | 1.0 | V |
| Safe leakage current (V_{DD} low, or device unpowered). V_{SAFE} 0 to 27 V. | $V_{\text{SAFE-IN}}$ | - | 0.0 | 1.0 | μA |
| INTERRUPT | | | | | |
| Output low voltage, $I_{\text{OUT}} = 1.5\text{ mA}$ | V_{OL} | - | 0.2 | 1.0 | V |
| Pull-up resistor | R_{PU} | 6.5 | 10 | 14 | $\text{k}\Omega$ |
| Output high level in Low Power V_{DD} ON Mode (guaranteed by design) | $V_{\text{OH-LPVddon}}$ | 3.9 | 4.3 | | V |
| Leakage current $\overline{\text{INT}}$ voltage = 10 V (to allow high-voltage on MCU $\overline{\text{INT}}$ pin) | V_{MAX} | - | 35 | 100 | μA |
| Sink current, $V_{\overline{\text{INT}}} > 5.0\text{ V}$, $\overline{\text{INT}}$ low state | I_{SINK} | 2.5 | 6.0 | 10 | mA |
| MISO, MOSI, SCLK, CS PINS | | | | | |
| Output low-voltage, $I_{\text{OUT}} = 1.5\text{ mA}$ (MISO) | V_{OL} | - | - | 1.0 | V |
| Output high-voltage, $I_{\text{OUT}} = -0.25\text{ mA}$ (MISO) | V_{OH} | $V_{\text{DD}} - 0.9$ | - | | V |
| Input low voltage (MOSI, SCLK, CS) | V_{IL} | - | - | $0.3 \times V_{\text{DD}}$ | V |
| Input high-voltage (MOSI, SCLK, CS) | V_{IH} | $0.7 \times V_{\text{DD}}$ | - | - | V |
| Tri-state leakage current (MISO) | I_{HZ} | -2.0 | - | 2.0 | μA |
| Pull-up current (CS) | I_{PU} | 200 | 370 | 500 | μA |
| CAN LOGIC INPUT PINS (TXD) | | | | | |
| High Level Input Voltage | V_{IH} | $0.7 \times V_{\text{DD}}$ | - | $V_{\text{DD}} + 0.3$ | V |
| Low Level Input Voltage | V_{IL} | -0.3 | - | $0.3 \times V_{\text{DD}}$ | V |
| Pull-up Current, TXD, $V_{\text{IN}} = 0\text{ V}$ | I_{PDWN} | -850 | -650 | -200 | μA |
| CAN DATA OUTPUT PINS (RXD) | | | | | |
| Low Level Output Voltage $I_{\text{RXD}} = 5.0\text{ mA}$ | $V_{\text{OUT_LOW}}$ | 0.0 | - | $0.3 \times V_{\text{DD}}$ | V |
| High Level Output Voltage $I_{\text{RXD}} = -3.0\text{ mA}$ | $V_{\text{OUT_HIGH}}$ | $0.7 \times V_{\text{DD}}$ | - | V_{DD} | V |
| High Level Output Current $V_{\text{RXD}} = V_{\text{DD}} - 0.4\text{ V}$ | $I_{\text{OUT_HIGH}}$ | 2.5 | 5.0 | 9.0 | mA |
| Low Level Input Current $V_{\text{RXD}} = 0.4\text{ V}$ | $I_{\text{OUT_LOW}}$ | 2.5 | 5.0 | 9.0 | mA |

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 27\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25^\circ\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|---------------------------|------|------------------------|------|---------------|
| CAN OUTPUT PINS (CANH, CANL) | | | | | |
| Bus pins common mode voltage for full functionality | V_{COM} | -12 | - | 12 | V |
| Differential input voltage threshold | $V_{\text{CANH-VCANL}}$ | 500 | - | 900 | mV |
| Differential input hysteresis | $V_{\text{DIFF-HYST}}$ | 50 | - | - | mV |
| Input resistance | R_{IN} | 5.0 | - | 50 | k Ω |
| Differential input resistance | $R_{\text{IN-DIFF}}$ | 10 | - | 100 | k Ω |
| Input resistance matching | $R_{\text{IN-MATCH}}$ | -3.0 | 0.0 | 3.0 | % |
| CANH output voltage ($45\ \Omega < R_{\text{BUS}} < 65\ \Omega$) | V_{CANH} | | | | V |
| TX dominant state | | 2.75 | 3.5 | 4.5 | |
| TX recessive state | | 2.0 | 2.5 | 3.0 | |
| CANL output voltage ($45\ \Omega < R_{\text{BUS}} < 65\ \Omega$) | V_{CANL} | | | | V |
| TX dominant state | | 0.5 | 1.5 | 2.25 | |
| TX recessive state | | 2.0 | 2.5 | 3.0 | |
| Differential output voltage ($45\ \Omega < R_{\text{BUS}} < 65\ \Omega$) | $V_{\text{OH-VOL}}$ | | | | V |
| TX dominant state | | 1.5 | 2.0 | 3.0 | |
| TX recessive state | | -0.5 | 0.0 | 0.05 | |
| CAN H output current capability - Dominant state | I_{CANH} | - | - | -30 | mA |
| CAN L output current capability - Dominant state | I_{CANL} | 30 | - | - | mA |
| CANL over-current detection - Error reported in register | $I_{\text{CANL-OC}}$ | 75 | 120 | 195 | mA |
| CANH over-current detection - Error reported in register | $I_{\text{CANH-OC}}$ | -195 | -120 | -75 | mA |
| CANH, CANL input resistance to gnd, device supplied, CAN in Sleep Mode, V_{CANH} , V_{CANL} from 0 to 5.0 V | R_{INSLEEP} | 5.0 | - | 50 | k Ω |
| CANL, CANH output voltage in Low Power V_{DD} OFF and Low Power V_{DD} ON Modes | V_{CANLP} | -0.1 | 0.0 | 0.1 | V |
| CANH, CANL input current, V_{CANH} , $V_{\text{CANL}} = 0$ to 5V, device not supplied (V_{sup} , V_{dd} , 5V-CAN: open, direct connection to gnd, connect to gnd via 47k resistor). | $I_{\text{CAN-UN_SUP1}}$ | - | 3.0 | 10 | μA |
| CANH, CANL input current, V_{CANH} , $V_{\text{CANL}} = -2$ to 7V, device not supplied (V_{sup} , V_{dd} , 5V-CAN: open, direct connection to gnd, connect to gnd via 47k resistor). | $I_{\text{CAN-UN_SUP2}}$ | - | - | 250 | μA |
| Differential voltage for recessive bit detection in LP mode ⁽¹⁶⁾ | $V_{\text{DIFF-R-LP}}$ | - | - | 0.4 | V |
| Differential voltage for dominant bit detection in LP mode ⁽¹⁶⁾ | $V_{\text{DIFF-D-LP}}$ | 1.15 | - | - | V |
| CANH AND CANL DIAGNOSTIC INFORMATION | | | | | |
| CANL to GND detection threshold | V_{LG} | 1.6 | 1.75 | 2.0 | V |
| CANH to GND detection threshold | V_{HG} | 1.6 | 1.75 | 2.0 | V |
| CANL to VBAT detection threshold, V_{SUP1} and $V_{\text{SUP2}} > 8.0\text{ V}$ | V_{LVB} | - | $V_{\text{SUP}} - 2.0$ | - | V |
| CANH to VBAT detection threshold, V_{SUP1} and $V_{\text{SUP2}} > 8.0\text{ V}$ | V_{HVB} | - | $V_{\text{SUP}} - 2.0$ | - | V |
| CANL to VDD detection threshold | V_{L5} | 4.0 | $V_{\text{DD}} - 0.43$ | - | V |
| CANH to VDD detection threshold | V_{H5} | 4.0 | $V_{\text{DD}} - 0.43$ | - | V |

Notes

16. Guaranteed by design and device characterization.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 27\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25^\circ\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|----------------------------|---|--|---|------------------|
| SPLIT | | | | | |
| Output voltage Loaded condition $I_{\text{SPLIT}} = \pm 500\ \mu\text{A}$ Unloaded condition $R_{\text{measure}} > 1.0\ \text{M}\Omega$ | V_{SPLIT} | $0.3 \times V_{\text{DD}}$ $0.45 \times V_{\text{DD}}$ | $0.5 \times V_{\text{DD}}$ $0.5 \times V_{\text{DD}}$ | $0.7 \times V_{\text{DD}}$ $0.55 \times V_{\text{DD}}$ | V |
| Leakage current $-12\text{ V} < V_{\text{SPLIT}} < +12\text{ V}$ $-22\text{ to }-12\text{ V} < V_{\text{SPLIT}} < +12\text{ to }+35\text{ V}$ | I_{LSPLIT} | - - | 0.0 - | 5.0 200 | μA |
| LIN TERM1, LIN TERM2 | | | | | |
| LIN-T1, LIN-T2, high side switch drop @ $I = -20\ \text{mA}$, $V_{\text{SUP}} > 10.5\text{ V}$ | LT_{HSDRP} | - | 1.0 | 1.4 | V |
| LIN1 AND LIN 2 MC33905D PIN - LIN1 MC33905S PIN (Parameters guaranteed for V_{SUP1}, $V_{\text{SUP2}} 7\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$) | | | | | |
| Operating Voltage Range | V_{BAT} | 8.0 | - | 18 | V |
| Supply Voltage Range | V_{SUP} | 7.0 | - | 18 | V |
| Current Limitation for Driver Dominant State Driver ON, $V_{\text{BUS}} = 18\text{ V}$ | $I_{\text{BUS_LIM}}$ | 40 | 90 | 200 | mA |
| Input Leakage Current at the receiver Driver off; $V_{\text{BUS}} = 0\text{V}$; $V_{\text{BAT}} = 12\text{ V}$ | $I_{\text{BUS_PAS_DOM}}$ | -1.0 | - | - | mA |
| Leakage Output Current to GND Driver Off; $8.0\text{ V} < V_{\text{BAT}} < 18\text{ V}$; $8.0\text{ V} < V_{\text{BUS}} < 18\text{ V}$; $V_{\text{BUS}} \geq V_{\text{BAT}}$ | $I_{\text{BUS_PAS_REC}}$ | - | - | 20 | μA |
| Control unit disconnected from ground (Loss of local ground must not affect communication in the residual network) $GND_{\text{DEVICE}} = V_{\text{SUP}}$; $V_{\text{BAT}} = 12\text{ V}$; $0 < V_{\text{BUS}} < 18\text{ V}$ (guaranteed by design) | $I_{\text{BUS_NO_GND}}$ | -1.0 | - | 1.0 | mA |
| V_{BAT} Disconnected; $V_{\text{SUP_DEVICE}} = GND$; $0 < V_{\text{BUS}} < 18\text{ V}$ (Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition) | $I_{\text{BUSNO_BAT}}$ | - | - | 100 | μA |
| Receiver Dominant State | V_{BUSDOM} | - | - | 0.4 | V_{SUP} |
| Receiver Recessive State | V_{BUSREC} | 0.6 | - | - | V_{SUP} |
| Receiver Threshold Center $(V_{\text{TH_DOM}} + V_{\text{TH_REC}})/2$ | $V_{\text{BUS_CNT}}$ | 0.475 | 0.5 | 0.525 | V_{SUP} |
| Receiver Threshold Hysteresis $(V_{\text{TH_REC}} - V_{\text{TH_DOM}})$ | V_{HYS} | - | - | 0.175 | V_{SUP} |
| LIN Wake-up threshold from Low Power V_{DD} ON or Low Power V_{DD} OFF Mode | V_{BUSWU} | - | 5.3 | 5.8 | V |
| LIN Pull-up Resistor to V_{SUP} | R_{SLAVE} | 20 | 30 | 60 | $\text{k}\Omega$ |
| Over-temperature Shutdown (guaranteed by design) | $T_{\text{LINS D}}$ | 140 | 160 | 180 | $^\circ\text{C}$ |
| Over-temperature Shutdown Hysteresis (guaranteed by design) | $T_{\text{LINS D_HYS}}$ | - | 10 | - | $^\circ\text{C}$ |

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 5. Dynamic Electrical Characteristics

Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 27\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$, $\text{GND} = 0\text{ V}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25^\circ\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|--------------------------------------|-------------------------|------------------------|----------------------|---------------|
| SPI TIMING | | | | | |
| SPI operation frequency (MISO cap = 50 pF) | FREQ | 0.25 | - | 4.0 | MHz |
| SCLK Clock Period | t_{PCLK} | 250 | - | N/A | ns |
| SCLK Clock High Time | t_{WSCLKH} | 125 | - | N/A | ns |
| SCLK Clock Low Time | t_{WSCLKL} | 125 | - | N/A | ns |
| Falling Edge of $\overline{\text{CS}}$ to Rising Edge of SCLK | t_{LEAD} | 30 | - | N/A | ns |
| Falling Edge of SCLK to Rising Edge of $\overline{\text{CS}}$ | t_{LAG} | 30 | - | N/A | ns |
| MOSI to Falling Edge of SCLK | t_{SISU} | 30 | - | N/A | ns |
| Falling Edge of SCLK to MOSI | t_{SIH} | 30 | - | N/A | ns |
| MISO Rise Time (CL = 50 pF) | t_{RSO} | - | - | 30 | ns |
| MISO Fall Time (CL = 50 pF) | t_{FSO} | - | - | 30 | ns |
| Time from Falling to MISO Low-impedance | t_{SOEN} | - | - | 30 | ns |
| Time from Rising to MISO High-impedance | t_{SODIS} | - | - | 30 | ns |
| Time from Rising Edge of SCLK to MISO Data Valid | t_{VALID} | - | - | 30 | ns |
| Delay between rising and falling edge on $\overline{\text{CS}}$ | D2 $\overline{\text{CS}}$ | 1.0 | - | - | μs |
| $\overline{\text{CS}}$ low timeout detection | $\overline{\text{CS}}\text{-TO}$ | 2.5 | - | - | ms |
| SUPPLY, VOLTAGE REGULATOR, RESET | | | | | |
| VSUP under-voltage detector threshold deglitcher | $V_{\text{S_LOW1/2_DGLT}}$ | 30 | 50 | 100 | μs |
| Rise time at turn ON. V_{DD} from 1.0 to 4.5 μV . 2.2 μF at V_{DD} pin. | $t_{\text{RISE-ON}}$ | 50 | 250 | 800 | μs |
| Deglitcher time to set reset pin low | R ST-DGLT | 20 | 30 | 40 | μs |
| RESET PULSE DURATION | | | | | |
| V_{DD} under-voltage (SPI selectable) short, default at power on when BATFAIL bit set medium medium long long | R ST-PULSE | 0.9 4.0 8.5 17 | 1.0 5.0 10 20 | 1.4 6 12 24 | ms |
| Watchdog reset | R ST-WD | 0.9 | 1.0 | 1.4 | ms |
| VSENSE INPUT | | | | | |
| Under-voltage deglitcher time | B FT | 30 | - | 100 | μs |
| INTERRUPT | | | | | |
| $\overline{\text{INT}}$ pulse duration (refer to SPI for selection. Guaranteed by design) short long | $\overline{\text{INT}}\text{-PULSE}$ | 20 90 | 25 100 | 35 130 | μs |

Table 5. Dynamic Electrical Characteristics

Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 27\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$, $\text{GND} = 0\text{ V}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25^\circ\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|-------------------------|-----|-----|-----|---------------|
| STATE DIGRAM TIMINGS | | | | | |
| Delay for SPI Timer A, Timer B or Timer C write command after entering Normal Mode (No command should occur within $T_{\text{D_NM}}$. $T_{\text{D_NM}}$ delay definition: from $\overline{\text{CS}}$ rising edge of "Go to Normal Mode" command to CS falling edge of "Timer write" command) | $t_{\text{D_NM}}$ | 60 | - | - | μs |
| Tolerance for: W/D period in all modes, FWU delay, Cyclic sense period and active time, Cyclic Interrupt period, LP mode over current (unless otherwise noted) ⁽²⁰⁾ | $t_{\text{TIMING-ACC}}$ | -10 | - | 10 | % |

CAN DYNAMIC CHARACTERISTICS

| | | | | | |
|--|-------------------------|--------|------------|--------|---------------|
| TXD Dominant State Timeout | t_{DOUT} | 300 | 600 | 1000 | μs |
| Bus dominant clamping detection | t_{DOM} | 300 | 600 | 1000 | μs |
| Propagation loop delay TXD to RXD, recessive to dominant (Fast slew rate) | t_{LRD} | 60 | 120 | 210 | ns |
| Propagation delay TXD to CAN, recessive to dominant | t_{TRD} | - | 70 | 110 | ns |
| Propagation delay CAN to RXD, recessive to dominant | t_{RRD} | - | 45 | 140 | ns |
| Propagation loop delay TXD to RXD, dominant to recessive (Fast slew rate) | t_{LDR} | 100 | 120 | 200 | ns |
| Propagation delay TXD to CAN, dominant to recessive | t_{TDR} | - | 75 | 150 | ns |
| Propagation delay CAN to RXD, dominant to recessive | t_{RDR} | - | 50 | 140 | ns |
| Loop time TXD to RXD, Medium Slew rate (Selected by SPI) Rec to Dom Dom to Rec | $t_{\text{LOOP-MSL}}$ | - - | 200 200 | - - | ns |
| Loop time TXD to RXD, Slow Slew rate (Selected by SPI) Rec to Dom Dom to Rec | $t_{\text{LOOP-SSL}}$ | - - | 300 300 | - - | ns |
| CAN wake up filter time, single dominant pulse detection ⁽¹⁷⁾ (See Figure 29) | $t_{\text{CAN-WU1}}$ | 0.5 | 2.0 | 5.0 | μs |
| CAN wake up filter time, 3 dominant pulses detection ⁽¹⁸⁾ | $t_{\text{CAN-WU3-F}}$ | 300 | - | - | ns |
| CAN wake up filter time, 3 dominant pulses detection time out ⁽¹⁹⁾ (See Figure 30) | $t_{\text{CAN-WU3-TO}}$ | - | - | 120 | μs |

Notes

17. No wake up for single pulse shorter than $t_{\text{CAN-WU1}}$ min. Wake up for single pulse longer than $t_{\text{CAN-WU1}}$ max.
18. Each pulse should be greater than $t_{\text{CAN-WU3-F}}$ min. Guaranteed by design, and device characterization.
19. The 3 pulses should occur within $t_{\text{CAN-WU3-TO}}$. Guaranteed by design, and device characterization.
20. Guaranteed by design.

Table 5. Dynamic Electrical Characteristics

Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 27\text{ V}$, $-40^\circ\text{C} \leq T_{\text{A}} \leq 125^\circ\text{C}$, $\text{GND} = 0\text{ V}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_{\text{A}} = 25^\circ\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

LIN 1 AND LIN 2 PHYSICAL LAYER: DRIVER CHARACTERISTICS FOR NORMAL SLEW RATE - 20.0 KBIT/SEC ACCORDING TO LIN PHYSICAL LAYER SPECIFICATION

Bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 k Ω , 6.8 nF / 660 Ω , 10 nF / 500 Ω . See [Figure 13](#), page 25.

| | | | | | |
|---|----|-------|---|-------|--|
| Duty Cycle 1: $TH_{\text{REC}(\text{max})} = 0.744 * V_{\text{SUP}}$ $TH_{\text{DOM}(\text{max})} = 0.581 * V_{\text{SUP}}$ $D1 = t_{\text{BUS_REC}(\text{MIN})} / (2 * t_{\text{BIT}})$, $t_{\text{BIT}} = 50\ \mu\text{s}$, $7.0\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$ | D1 | 0.396 | - | - | |
| Duty Cycle 2: $TH_{\text{REC}(\text{MIN})} = 0.422 * V_{\text{SUP}}$ $TH_{\text{DOM}(\text{MIN})} = 0.284 * V_{\text{SUP}}$ $D2 = t_{\text{BUS_REC}(\text{MAX})} / (2 * t_{\text{BIT}})$, $t_{\text{BIT}} = 50\ \mu\text{s}$, $7.6\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$ | D2 | - | - | 0.581 | |

LIN PHYSICAL LAYER: DRIVER CHARACTERISTICS FOR SLOW SLEW RATE - 10.4 KBIT/SEC ACCORDING TO LIN PHYSICAL LAYER SPECIFICATION

Bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 k Ω , 6.8 nF / 660 Ω , 10 nF / 500 Ω . Measurement thresholds. See [Figure 14](#), page 26.

| | | | | | |
|---|----|-------|---|-------|--|
| Duty Cycle 3: $TH_{\text{REC}(\text{MAX})} = 0.778 * V_{\text{SUP}}$ $TH_{\text{DOM}(\text{MAX})} = 0.616 * V_{\text{SUP}}$ $D3 = t_{\text{BUS_REC}(\text{MIN})} / (2 * t_{\text{BIT}})$, $t_{\text{BIT}} = 96\ \mu\text{s}$, $7.0\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$ | D3 | 0.417 | - | - | |
| Duty Cycle 4: $TH_{\text{REC}(\text{MIN})} = 0.389 * V_{\text{SUP}}$ $TH_{\text{DOM}(\text{MIN})} = 0.251 * V_{\text{SUP}}$ $D4 = t_{\text{BUS_REC}(\text{MAX})} / (2 * t_{\text{BIT}})$, $t_{\text{BIT}} = 96\ \mu\text{s}$, $7.6\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$ | D4 | - | - | 0.590 | |

LIN PHYSICAL LAYER: DRIVER CHARACTERISTICS FOR FAST SLEW RATE

| | | | | | |
|---------------------------------------|--------------------|---|----|---|------------------|
| LIN Fast Slew Rate (Programming Mode) | SR _{FAST} | - | 20 | - | V/ μs |
|---------------------------------------|--------------------|---|----|---|------------------|

LIN PHYSICAL LAYER: CHARACTERISTICS AND WAKE-UP TIMINGS

V_{SUP} from 7.0 to 18 V, bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 k Ω , 6.8 nF / 660 Ω , 10 nF / 500 Ω . See [Figure 13](#), page 25.

| | | | | | |
|---|---|-----------|----------|------------|---------------|
| Propagation Delay and Symmetry (See Figure 13 , page 25 and Figure 14 , page 26) Propagation Delay of Receiver, $t_{\text{REC_PD}} = \text{MAX}(t_{\text{REC_PDR}}, t_{\text{REC_PDF}})$ Symmetry of Receiver Propagation Delay, $t_{\text{REC_PDF}} - t_{\text{REC_PDR}}$ | $t_{\text{REC_PD}}$ $t_{\text{REC_SYM}}$ | - -2.0 | 4.2 - | 6.0 2.0 | μs |
| Bus Wake-Up Deglitcher (Low Power V_{DD} OFF and Low Power V_{DD} ON Modes) (See Figure 15 , page 25 for Low Power V_{DD} OFF Mode and Figure 16 , page 26 for Low Power Mode) | t_{PROPWL} | 42 | 70 | 95 | μs |
| Bus Wake-up Event Reported From Low Power V_{DD} OFF Mode From Low Power V_{DD} ON Mode | $t_{\text{WAKE_LPVDD}}$ OFF $t_{\text{WAKE_LPVDD}}$ ON | - 1.0 | - - | 1500 12 | μs |
| TXD Permanent Dominant State Delay (guaranteed by design) | t_{TXDDOM} | 0.65 | 1.0 | 1.35 | s |

TIMING DIAGRAMS

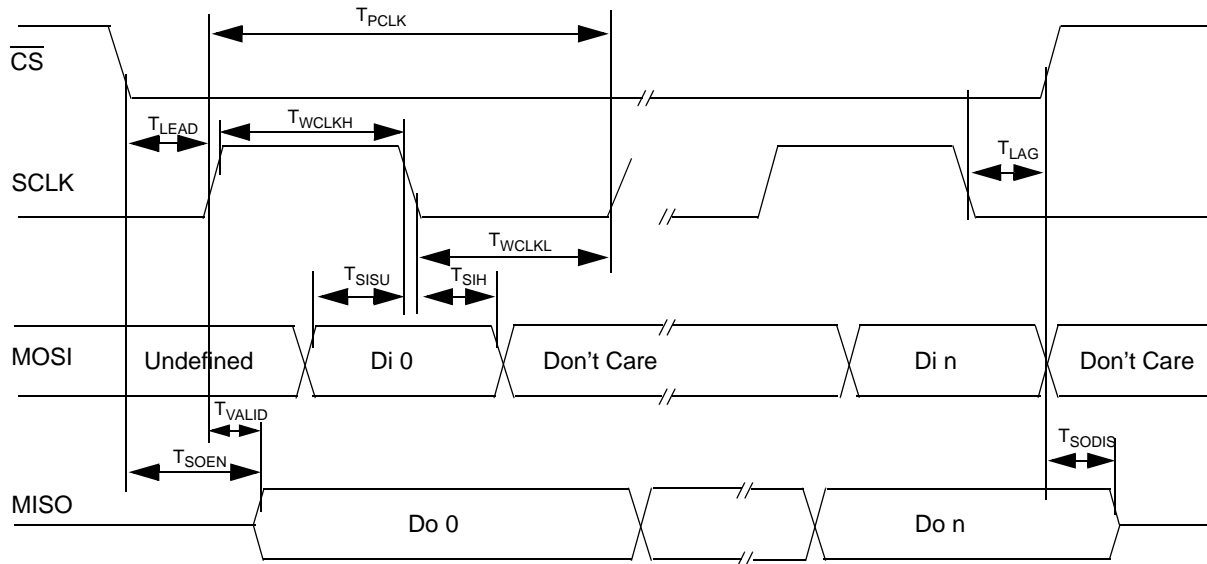


Figure 9. SPI Timings

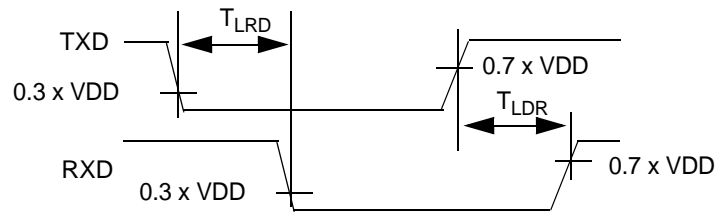


Figure 10. CAN Signal Propagation Loop Delay TXD to RXD

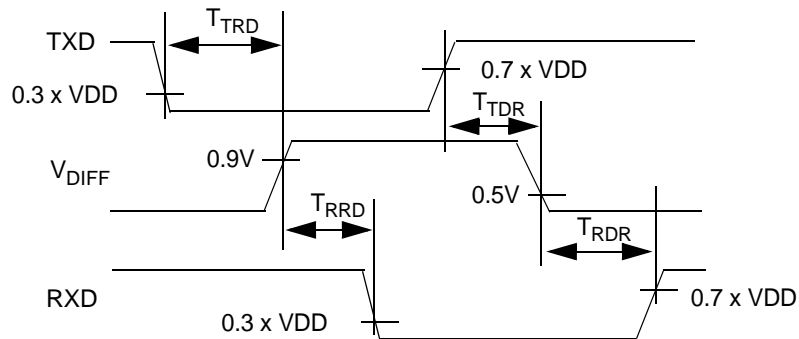


Figure 11. CAN Signal Propagation Delays TXD to CAN and CAN to RXD

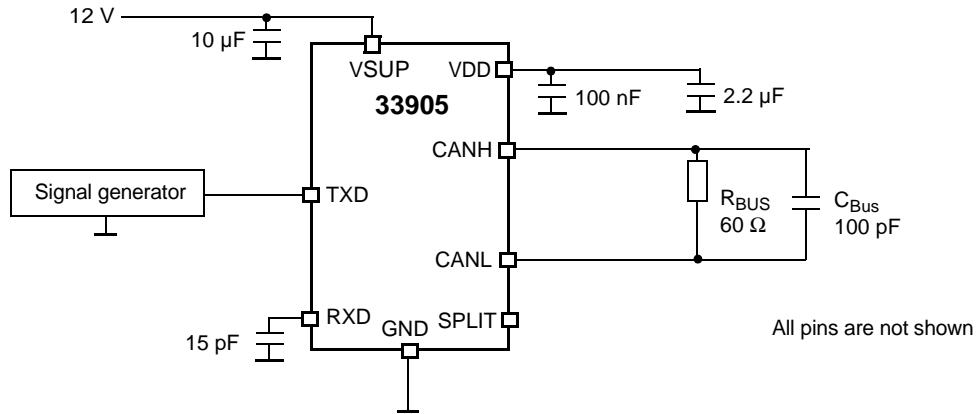


Figure 12. Test Circuit for CAN Timing Characteristics

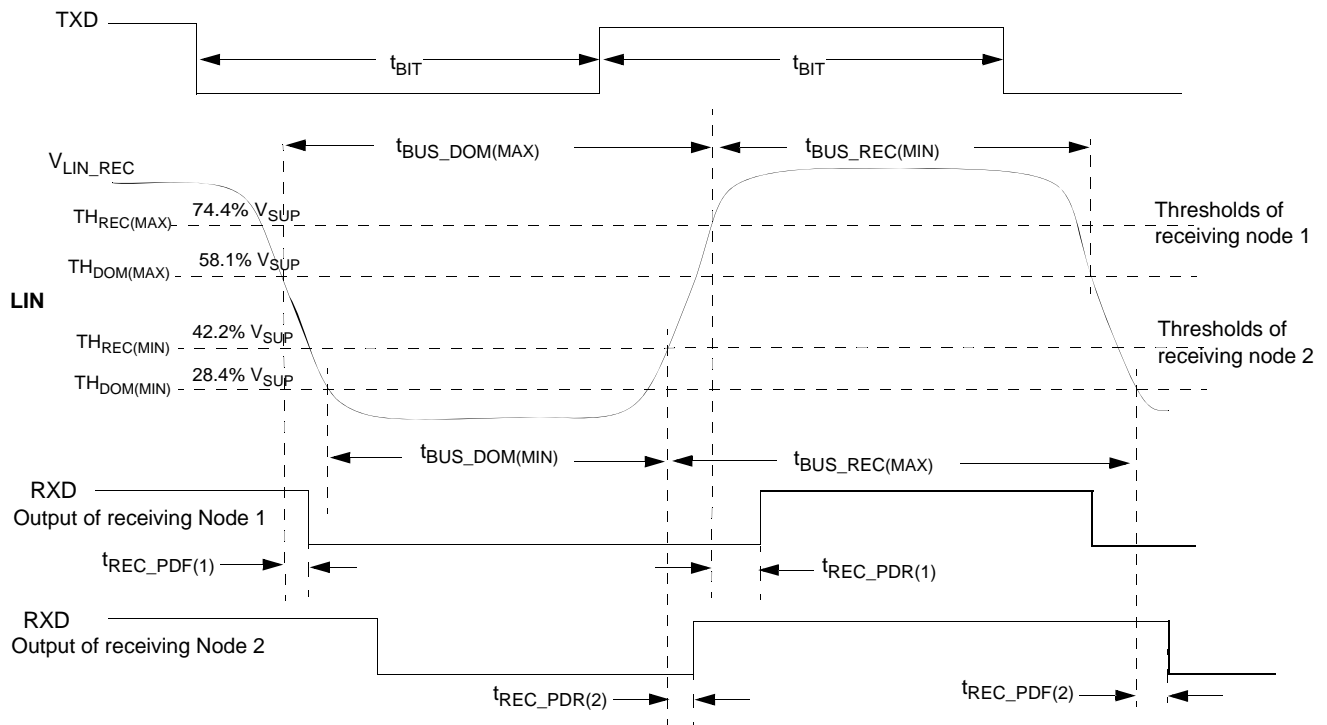


Figure 13. LIN Timing Measurements for Normal Slew Rate

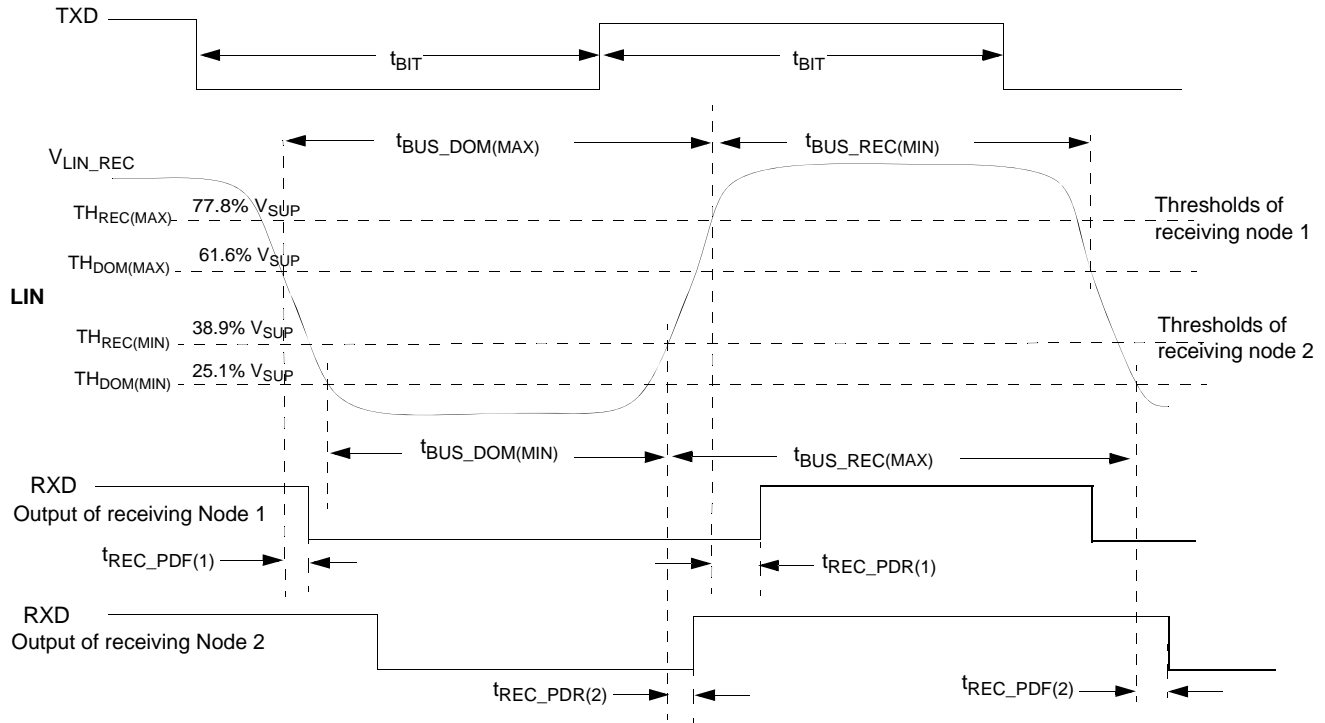


Figure 14. LIN Timing Measurements for Slow Slew Rate

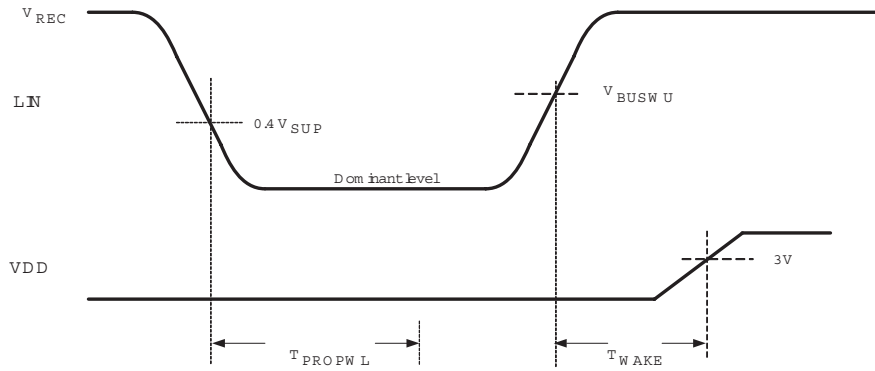


Figure 15. LIN Wake-up Low Power V_{DD} OFF Mode Timing

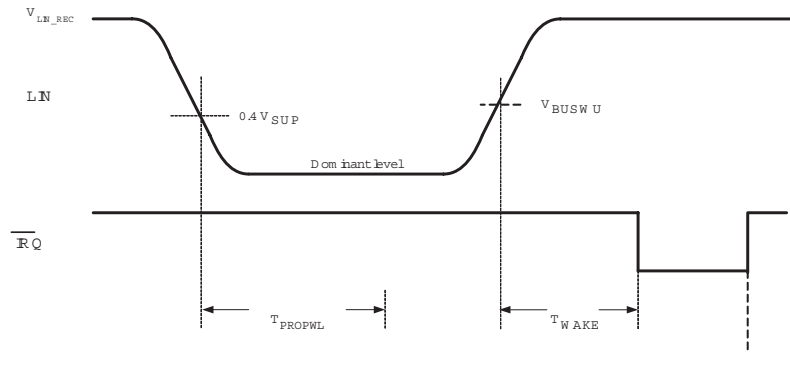


Figure 16. LIN Wake-up Low Power V_{DD} ON Mode Timing

FUNCTIONAL DESCRIPTION

INTRODUCTION

The MC33904_5 is the second generation of System Basis Chip, combining:

- Advanced power management unit for the MCU, the integrated CAN interface and for additional ICs such as sensors, CAN transceiver.

- Built in enhanced high speed CAN interface (ISO11898-2 and -5), with local and bus failure diagnostic, protection and fail safe operation mode.

- Built in LIN interface, compliant to LIN 2.1 and J2602-2 specification, with local and bus failure diagnostic and protection.

- Innovative and hardware configurable fail safe state machine solution.

- Multiple low power modes, with low current consumption.

- Family concept; with and without LIN interface devices with pin compatibility.

FUNCTIONAL PIN DESCRIPTION

POWER SUPPLY (VSUP1 AND VSUP2)

VSUP1 pin is the input pin for the device internal supply and the VDD regulator. VSUP2 is the input pin for the 5V-CAN regulator, LINs interfaces and I/O functions. The VSUP block includes over and under-voltage detections which can generate interrupt. The device includes a loss of battery detector connected to VSUP1.

Loss of battery is reported through a bit (called BATFAIL). This generates a POR (Power On Reset).

VDD VOLTAGE REGULATOR (VDD)

The regulator has two main modes of operation (Normal Mode and Low Power Mode). It can operate with or without an external PNP transistor.

In Normal Mode, without external PNP, the max DC capability is 150mA. Current limitation, temperature pre warning flag and over temperature shutdown features are included. When VDD is turned ON, rise time from 0 to 5.0V is controlled. Output voltage is 5.0V. A 3.3V option is available via dedicated part number.

If current higher than 150mA is required, an external PNP transistor must be connected to VEM (PNP emitter) and VB (PNP base) terminals, in order to increase total current capability and share the power dissipation between internal VDD transistor and the external transistor. See [External Transistor Q1 \(VE and VB\)](#). The PNP can be used even if current is less than 150mA, depending upon ambient temperature, maximum supply and thermal resistance. Typically, above 100-200mA, an external ballast transistor is recommended.

VDD REGULATOR IN LOW POWER MODE

When the device is set in Low Power V_{DD} ON Mode, the VDD regulator is able to supply the MCU with a DC current below typ 1.5mA (L_{P-ITH}). Transient current can also be supplied up to tenth of mA. Current in excess of 1.5mA is detected, and this event is managed by the device logic (wake-up detection, timer start for over current duration monitoring or watchdog refresh).

EXTERNAL TRANSISTOR Q1 (VE AND VB)

The device has a dedicated circuit to allow usage of an external P type transistor, with the objective to share the power dissipation between the internal transistor of the V_{DD} regulator and the external transistor. The bipolar PNP recommended transistor are MJD42C or BCP52-16.

When the external PNP is connected, the current is shared between the internal path transistor and the external PNP, with the following typical ratio: 1/3 in the internal transistor and 2/3 in the external PNP. The PNP activation and control is done by SPI.

The device is able to operate without an external transistor. In this case the V_{EM} and VB pins must remain open.

VOLTAGE REGULATOR FOR CAN INTERFACE SUPPLY (5V-CAN)

This regulator is supplied from the VSUP2 pin. A capacitor is required at 5V-CAN terminal. Analog MUX and part of the LIN interfaces are supplied from 5V-CAN.

5V-CAN regulator is OFF by default and must be turned ON by SPI. In Debug mode 5V-CAN is ON by default.

V AUXILIARY OUTPUT, 5V AND 3.3V SELECTABLE (VB-AUX, VC-AUX, AND VCAUX) - Q2

The VAUX block is used to provide an auxiliary voltage output, 5 or 3.3V, selectable by the SPI. It uses an external PNP pass transistor for flexibility and power dissipation constraints. The external recommended bipolar transistors are MJD42C or BCP52-16.

An over-current and under voltage detectors are provided.

V_{AUX} is controlled via the SPI, and can be turned ON or OFF. V_{AUX} low threshold detection and over-current information will disable \overline{Vaux} , and flags are reported in the SPI and can generate \overline{INT} .

Vaux is OFF by default and must be turned ON by SPI.

UNDER-VOLTAGE RESET AND RESET FUNCTION (RST)

The RESET pin is an open drain structure with an internal pull-up current source. The low side driver has limited current capability when asserted low, in order to tolerate a short to 5.0V. The Reset terminal voltage is monitored in order to detect failure (e.g. RESET pin shorted to 5.0V or GND).

The RESET pin reports to the MCU under-voltage condition at the VDD pin, as well as failure in watchdog refresh operation. VDD under-voltage reset operate also in Low Power V_{DD} ON Mode.

Two VDD under-voltage threshold are included. The upper one (typ 4.65V, R_{ST-TH1-5}) can lead to a Reset or an Interrupt. This is selected by the SPI. When "R_{ST-TH2-5}" is selected, in Normal Mode, an INT is asserted when VDD falls below "R_{ST-TH1-5}". This will allow the MCU to operate in a degraded mode, for example, with 4.0V V_{DD}.

I/O PINS (I/O-1: I/O-3)

I/Os are configurable input output pins. They can be used for small load or to drive external transistors. When used as output drivers, the I/Os are high side or low side type. They can also be set to high-impedance. I/Os are controlled by SPI and at power on, the I/Os are set as inputs. They include over load protection by temperature or excess of drop voltage.

In Low Power Mode, state of the I/O can be turned on or off, with extremely low extra consumption (except load). Protection is disabled in low power mode.

When cyclic sense is used, I/O-0 is the high side/low side switch, I/O-1, 2 and 3 and the wake inputs.

I/O-2 and I/O-3 terminals share also the LIN Master terminal function.

VSENSE INPUT (VSENSE)

This pin can be connected to the battery line (before the reverse battery protection diode), via a serial resistor and a

capacitor to gnd. It incorporates a threshold detector to sense the battery voltage and provide a battery early warning. It also includes a resistor divider to measure the VSENSE voltage via the MUX OUT pin.

MUX OUTPUT (MUXOUT)

The MUX-OUT terminal (Figures 17) delivers an analog voltage to the MCU A/D input. The voltage to be delivered to MUX-OUT is selected via the SPI, from one of the following functions: V_{sup1}, V_{sense}, I/O-0, I/O-1, Internal 2.5V reference, die temperature sensor, VDD current copy.

Voltage divider or amplifier are inserted in the chain, as shown in Figures 17.

For the VDD current copy, a resistor must be added to the MUX-OUT pin, to convert current into voltage. Device includes an internal 2k resistor selectable by SPI.

Voltage range at MUX_OUT is from gnd to VDD. It is automatically limited to VDD (max 3.3V for 3.3V part numbers).

The MUX-OUT buffer is supplied from 5V-CAN regulator, so the 5V-CAN regulator must be ON in order to have:

- 1) MUX-OUT functionality and
- 2) SPI selection of the analog function.

If 5V-CAN is OFF, MUX-OUT voltage is near gnd and the SPI command that selects one of the analog input is ignored.

Delay must be respected between SPI commands for 5V-CAN turn ON and SPI to select MUX-OUT function. The delay depends mainly upon the 5V-CAN capacitor and load on 5V-CAN.

The delay can be estimated using the following formula:

$$\text{delay} = C_{(5V-CAN)} \times U_{(5V)} / I_{\text{lim } 5V-CAN}$$

C = cap at 5V-CAN regulator, U = 5V,

I_{lim 5V-CAN} = min current limit of 5V-CAN regulator (parameter 5V-C_ILIM).

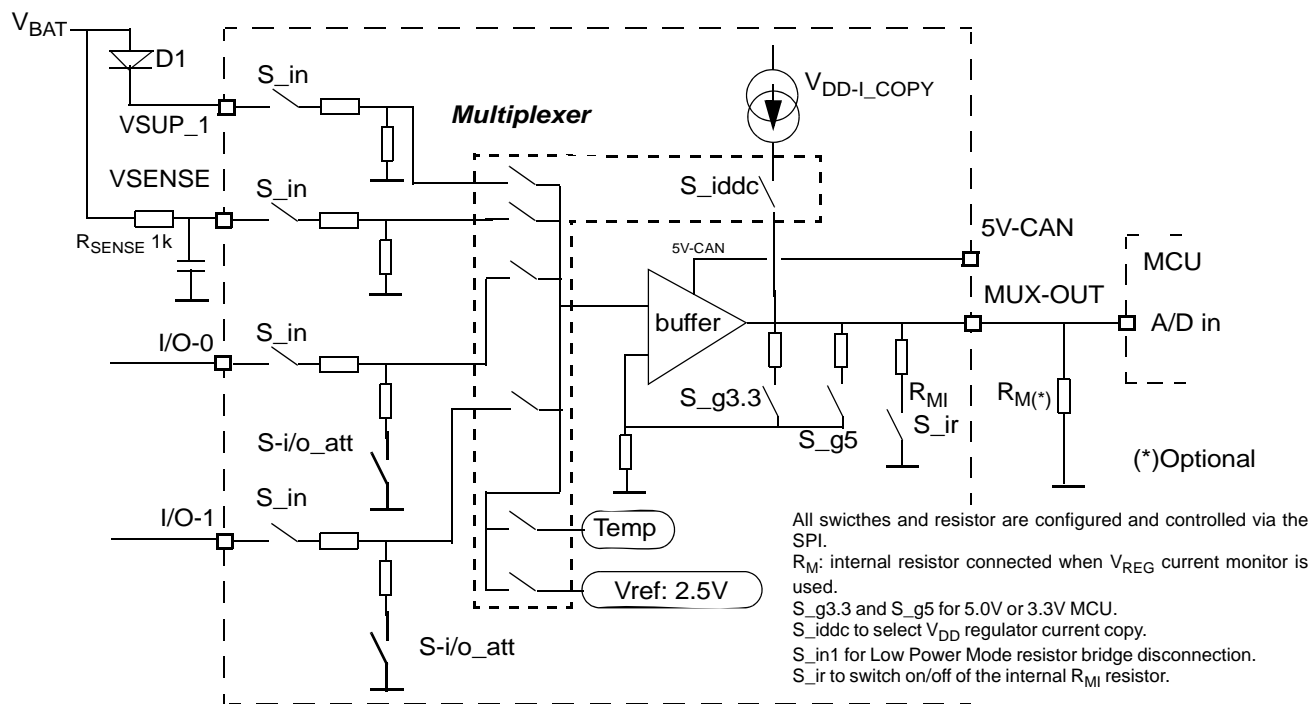


Figure 17. Analog Multiplexer Block Diagram

DGB (DGB) AND DEBUG MODE

The DBG pin has 2 functions:

Primary function:

It is an output used to set the device in Debug Mode. This is achieved by applying a voltage between 8V and 10V, at the debug terminal, and then powering up the device (ref to state diagram). When device leaves the INIT reset mode and enter in INIT mode, device detects that voltage at debug terminal is within the 8-10V range, and activate the debug mode.

When debug mode is detected, no watchdog SPI refresh commands is necessary. This allow easy debug of the hardware and software routines (i.e SPI commands).

Device is in debug mode is reported by SPI flag. While in de bug mode, when voltage at DBG terminal falls below the 8-10V range, the debug mode is left, and device start W/D operation, and expect proper W/D refresh. Debug mode can be left by SPI. Such command is recommended to avoid staying in debug mode in case of unwanted debug mode selection (pin FMEA). SPI command to leave debug has higher priority than providing 8-10V at debug pin.

Secondary function:

The resistor connected between DBG pin and gnd selects the Fail Safe Mode operation. DBG pin can also be connected directly to gnd (this prevent usage of debug mode).

Flexibility is provided to the user to select SAFE output operation via a resistor at the DBG pin or via SPI command. The SPI command has higher priority than the hardware selection via Debug resistor.

When the Debug mode is selected, the SAFE modes can not be configured via the resistor connected at DBG pin.

SAFE

Safe output terminal

This pin is an output which is asserted low in case a fault event occurs. The objective is to drive electrical safe circuitry and set the ECU in a know sate independent of the MCU and SBC, once a failure has been detected.

The SAFE output structure is an open drain, without a pull-up. No current flow is allowed when SAFE is forced externally to a high-voltage (< 40V).

INTERRUPT ($\overline{\text{INT}}$)

The $\overline{\text{INT}}$ output is asserted low or generate a low pulse when an interrupt condition occurs. The INT condition is enabled in the INT register. The selection of low level or pulse as well as pulse duration are selected by SPI.

No current will flow inside the INT structure when VDD is low, in Low Power V_{DD} OFF Mode. This allows the connection of an external pull resistor, and connection of an INT pin from other ICs without extra consumption in unpowered mode.

INT has internal pull up structure to V_{DD} . In Low Power V_{DD} ON Mode, a diode is inserted in series with the pull up, so the high level is slightly lower than in other modes.

CANH, CANL, SPLIT, RXD, TXD

These are the terminals of the high speed CAN physical interface, between the CAN bus and the micro controller. A detail description is provided in the document.

LIN, TXDL, RXDL AND LINTERM

These are the terminals of the Local Interconnect Network physical interface. Device contains zero, one or two LIN interfaces.

MC33904 has no LIN interface. MC33905S (S as Single) and MC33905D (D as Dual) contain respectively 1 and 2 LIN interfaces.

LIN 1 and LIN 2 terminals are the connection to the LIN sub buses.

LIN interfaces are connected to the MCU via the TxDL1 (TxDL2) and RxDL1 (RxDL2) terminals.

The device also include one or two high side switches to V_{sup2} terminal which can be used as a LIN master termination switch. Pins LINT-1 and LINT-2 are the same as I/O-2 and I/O-3.

A detail description is provided in the document

FUNCTIONAL DEVICE OPERATION

MODE AND STATE DESCRIPTION

The device has several operation modes. The transitions and conditions to enter or leave each modes are illustrated in the state diagram.

INIT RESET

This mode is automatically entered after device “power on”. In this mode, the RSTb pin is asserted low, for a duration of typ 1ms. Control bits and flags are “set” to their default reset condition. The BATFAIL is set to indicated that the device is coming from an unpowered condition, and that all previous device configuration are lost and “reset” the default value. The duration of the INIT reset is typ 1ms.

INIT reset mode is also entered from INIT mode in case the expected SPI command does not occur in due time (ref. INIT mode), and if device is not in debug mode.

INIT

This mode is automatically entered from “INIT reset” mode. In this mode, the device must be configured via SPI within a time of 256ms max.

Four registers called INIT Wdog, INIT REG, INIT LIN I/O and INIT MISC must be and can only be configured during INIT mode.

Other registers can be written in this mode, however they can be also written in other modes.

Once the INIT registers configuration is done, a SPI Watchdog Refresh command must be send in order to set the device into Normal mode. If the SPI W/D refresh does not occur within the 256ms period, the device will return into INIT reset mode for typ 1ms, and then re enter into INIT mode.

Register read operation is allowed in INIT mode to collect device status or to read back the INIT register configuration

When INIT mode is left by a SPI W/D refresh command, it is only possible to re enter the INIT mode using a secured SPI command.

RESET

In this mode, the RSTb pin is asserted low. Reset mode is entered from Normal mode, Normal Request mode, LP V_{DD} on mode and from Flash mode, when the W/D is not triggered, or if a VDD low condition is detected.

The duration of reset is typ 1ms by default. The user can defined a longer Reset pulse activation only for the case the reset mode is entered following a VDD low condition. Reset pulse is always 1ms, in case Reset mode in entered due to wrong W/D refresh command.

Reset mode can be entered via secured SPI command.

NORMAL REQUEST

This mode is automatically entered after RESET mode, or after a wake up from Low Power V_{DD} ON Mode.

A W/D refresh SPI command is necessary to transition to NORMAL mode. The duration of the Normal request mode is

256ms when Normal Request mode is entered after RESET mode. Different duration can be selected by SPI for the case when normal request is entered from LP V_{DD} ON mode.

If the W/D refresh SPI command does not occur within the 256ms (or the shorter user defined time out), then the device will enter into RESET mode, for a duration of typ 1ms.

note: in init reset, init, reset and normal request modes as well as in low power modes, the VDD external PNP is disabled.

NORMAL

In this mode, all device functions are available. This mode is entered by a SPI W/D refresh command from Normal Request mode, or from INIT mode.

During Normal mode, the device Watchdog function is operating, and a periodic W/D refresh must occurs. In case of incorrect or missing W/D refresh command device will enter into Reset mode.

From Normal mode, the device can be set by SPI command into Low Power modes (Low Power V_{DD} ON or Low Power V_{DD} OFF Modes). Dedicated secured SPI commands must be used to enter from Normal mode in RESET mode, INIT mode or FLASH mode.

FLASH

In this mode, the software watchdog period is extended up to typ 32 seconds. This allow programming of the MCU flash memory while minimizing the software overhead to refresh the W/D. The flash mode is entered by Secured SPI command and is left by SPI command. Device will enter into RESET mode. In case of incorrect or missing W/D refresh command device will enter into Reset mode. An INT can be generated at 50% of the W/D period.

CAN interface operates in Flash mode to allow flash via CAN bus, inside the vehicle.

DEBUG

Debug is a special operation mode of the device which allows system easy software and hardware debugging. The debug operation is detected after power up if the DBG pin is set in the 8.0-10V range.

When debug is detected, all the software watchdog operations are disabled: 256ms of INIT mode, W/D refresh of Normal mode and Flash mode, Normal Request time out (256ms or user defined value) are not operating and will not lead to transition into INIT reset or Reset mode.

When device is in Debug, SPI command can be send without any time constraints with respect to W/D operation, MCU program can be “halted” or “paused” to verify proper operation.

Debug can be left by removing 8-10V from debug pin, or by SPI command (ref to MODE register).

5V-CAN regulator is ON by default in debug mode.

LOW POWER MODES

The device has two main Low Power Modes: Low Power Mode with VDD off, and Low Power Mode with VDD on.

note: Prior to enter in Low Power mode, I/O and CAN wake up flags must be cleared (ref to Mode register).

LOW POWER - V_{DD} OFF

In this mode, VDD is turned off and the MCU connected to VDD is unsupplied. This mode is entered by the SPI. It can also be entered by automatic transition due to fail safe management. 5V-CAN and Vaux regulators are also turned OFF.

When the device is in Low Power V_{DD} OFF Mode, it monitors external events to wake up and leave the LP mode. The wake up events can occurs from:

- CAN
- LIN interface, depending upon device part number
- Expiration of an internal timer
- I/O-0, and I/O-inputs, and depending upon device part number and configuration, I/O-2 and/or 3 input
- Cyclic sense of I/O-1 input, associated by I/O-0 activation, and depending upon device part number and configuration, cyclic sense of I/O-2 and 3 input, associated by I/O-0 activation

When a wake up event is detected, the device enters into reset mode and then into Normal Request mode. The wake up source are reported into the device SPI registers. In summary, a wake up event from LP Vdd off, lead to Vdd regulator turn ON, and MCU operation restart.

LOW POWER - V_{DD} ON

In this mode, the voltage at the VDD terminal remains at 5.0V (or 3.3V, depending upon device part number). The objective is to maintain the MCU powered, with reduced consumption. In such mode, the DC output current is expected to be limited to few 100uA or few mA, as the ECU is in reduced power operation mode.

During this mode, the 5V-CAN and V_{AUX} regulators are OFF.

The same wake-up events as in LP Vdd off mode (CAN, LIN, I/O, timer, cyclic sense) are available in LP Vdd on mode.

In addition, two additional wake up conditions are available.

- Dedicated SPI command. When device is in LP Vdd ON mode, the wake up by SPI command uses a write to "Normal Request Mode", 0x5C10.
- Output current from Vdd exceeding typ 1.5mA threshold.

In Low Power V_{DD} ON Mode, the device is able to source several tenth of mA DC. The current source capability can be time limited, by a selectable internal timer. Timer duration is up to 32ms, and is triggered when the output current exceed the output current threshold typ 1.5mA.

This allow for instance a periodic activation of the MCU, while the device remains in LP V_{DD} on mode. If the duration exceed the selected time (ex 32ms), the device will detect a wake up.

Wake up event are reported to the MCU via a low level pulse at INT pulse. The MCU will detect the INT pulse and resume operation.

Watchdog function in LP V_{DD} ON mode

It is possible to enable the W/D function in Low Power V_{DD} ON Mode. In this case, the principle is time out.

Refresh of the W/D is done either by:

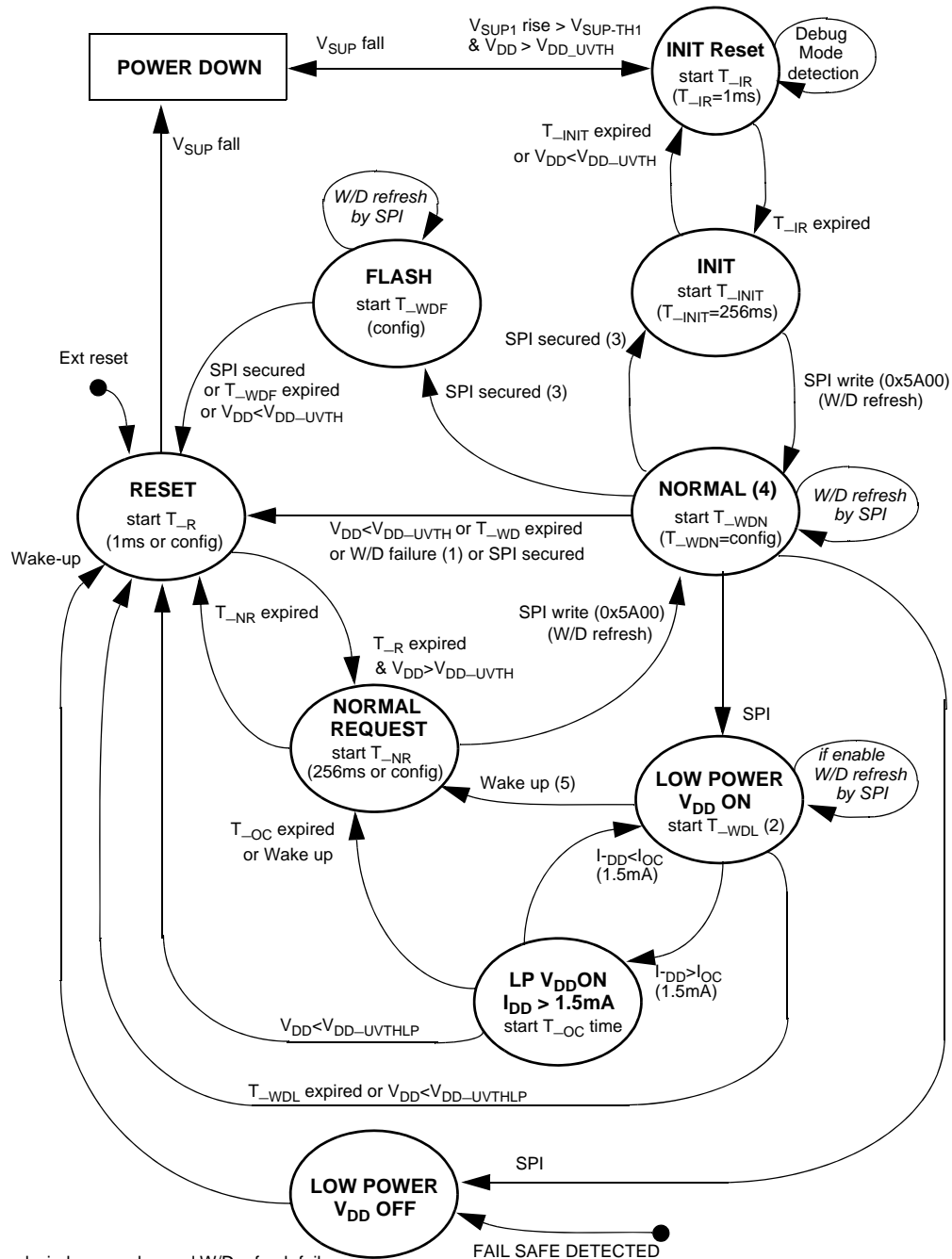
- a dedicated SPI command (different from any other SPI command or simple CSb activation which would wake up - ref to above paragraph)
- or by a temporary (less than 32ms max) Vdd over current wake-up (I_{dd} > 1.5mA typ).

As long as the W/D refresh occurs, the device remains in LP Vdd on mode.

MODE transition

mode transition are either done automatically (i.e after time out expired or voltage conditions), or via SPI command, or by external event such as wake up. Some mode change are performed via "secured" SPI commands.

STATE DIAGRAM



- (1) W/D refresh in closed window or enhanced W/D refresh failure
- (2) If enable by SPI, prior to enter LP V_{DD} ON mode
- (3) Ref to "SPI secure" description
- (4) V_{dd} external PNP is disable in all mode except Normal and Flash modes.
- (5) Wake up from LP V_{dd} ON mode by SPI command is done by a SPI mode change: 0X5C10

Figure 18. State Diagram

MODE CHANGE

“SECURED SPI” DESCRIPTION:

A request is done by a SPI command, the device provide on MISO an unpredictable “random code”. Software must perform a logical change on the code and return it to the device with the new SPI command to perform the desired action.

The “random code” is different at every exercise of the secured procedure and can be read back at any time.

The secured SPI uses the Special MODE register for the following transitions:

- from Normal mode to INT mode

- from Normal mode to FLASH mode

- from Normal mode to RESET mode (reset request).

“Random code” is also used when the “advance watchdog” is selected.

CHANGING OF DEVICE CRITICAL PARAMETERS

Some critical parameters are configured one time at device power on only, while the batfail flag is set in the INIT Mode. If a change is required while device is no longer in INIT mode, device must be set back in INIT mode using the “SPI secure” procedure.

WATCHDOG OPERATION

IN NORMAL REQUEST MODE

In Normal Request Mode, the device expects to receive a watchdog configuration before the end of the normal request time out period. This period is reset to a long (256ms) after power on and when BATFAIL is set.

The device can be configured to a different (shorter) time out period which can be used after wake-up from LP V_{DD} on mode.

After a software watchdog reset, the value is restored to 256ms, in order to allow for a complete software initialization, similar to a device power up.

In Normal Request Mode the watchdog operation is “timeout” only and can be triggered/served any time within the period.

WATCHDOG TYPE SELECTION

Two different watchdog modes are implemented: Window or Advance.

The selection of “Window” or “Advance” is done in INIT Mode, after device power up when the Batfail flag is set. Configuration is done via the SPI. Then the watchdog mode selection content is locked and can be changed only via a secured SPI procedure.

Window Watchdog Operation

The window watchdog is available in Normal Mode only. The watchdog period selection can be kept (SPI is selectable in INIT Mode), while the device enters into Low Power V_{DD} ON Mode. The watchdog period is reset to the default long period after BATFAIL.

The period and the refresh of watchdog is done by the SPI. A refresh must be done in the open window of the period, which starts at 50% of the selected period and ends at the end of the period.

If the watchdog is triggered before 50%, or not triggered before end of period, a reset has occurred. The device enters into Reset Mode.

Watchdog in Debug Mode

When the device is in Debug Mode (entered via the DBG pin), the watchdog continues to operate but does not affect the device operation by asserting a reset. For the user, operation appears without the watchdog.

When debug is left by software (SPI mode reg) the watchdog period starts at the end of the SPI command.

When debug mode is left by hardware (DBG pin below 8-10V), the device enters into Reset Mode.

Watchdog in Flash Mode

During flash mode operation, the watchdog can be set to a long time out period. Watchdog is timeout only and an INT pulse can be generated at 50% of the time window.

Advance Watchdog Operation

When the Advance watchdog is selected (at INIT Mode), the refresh of the watchdog must be done using a random number and with 1, 2, or 4 SPI commands. The number for the SPI command is selected in INIT mode.

The software must read a random byte from the device, and then must return the random byte inverted to clear the watchdog. The random byte write can be performed in 1, 2, or 4 different SPI commands.

If 1 command is selected, all 8 bits are written at once.

If 2 commands are selected, first write command must include 4 of the 8 bits of the inverted random byte. The second command must include the next 4 bits. This complete the watchdog refresh.

If 4 commands are selected, the first write command must include 2 of the 8 bits of the inverted random byte. The second command must include the next 2 bits, the 3rd command the next 2, and the last command, the last 2. This complete the watchdog refresh.

When multiple writes are used, the most significant bits are send first. The latest SPI command needs to be done inside the open window time frame, if window watchdog is selected.

DETAIL SPI OPERATION AND SPI COMMANDS FOR ALL WATCHDOG TYPES.

In INIT mode, the W/D type (window, time out, advance and number of SPI commands) is selected using register Init W/D, bits 1, 2 and 3. The W/D period is selected via TIM_A register. The W/D period selection can also be done in Normal mode or in Normal Request mode.

Transition from INIT mode to Normal Mode or from Normal Request mode to Normal mode is done via a single W/D refresh command (SPI 0x 5A00).

While in Normal mode, the W/D refresh command depends upon the W/D type selected in INIT mode. They are detailed in the paragraph below:

Simple W/D:

refresh commands is 0x5A00. It can be send any time within the W/D period if the time out W/D operation is selected (INIT-W/D register, bit 1 WD N/Win =0).

It must be send in the open window (second half of the period) if the Window Watchdog operation was selected (INIT-W/D register, bit 1 WD N/Win =1).

Advance Watchdog:

The first time device enters in Normal mode (entry on Normal mode using the 0x5A00 command), RND code must be read using SPI command 0x1B00. Device returns on MISO second byte the RND code. The full 16 bits MISO is called 0x XXRD. RD is the complement of the RD byte.

Advance Watchdog, refresh by 1 SPI command:

The refresh command is 0x5ARD. During each refresh command device returns on MISO a new Random Code. This new random code must be inverted and send along with the next refresh command and so on.

It must be done in the open window if the Window operation was selected.

Advance Watchdog, refresh by 2 SPI commands:

The refresh command is splitted in 2 SPI commands.

The first partial refresh command is 0x5Aw1, and the second is 0x5Aw2. Byte w1 contains the first 4 inverted bits of the RD byte plus the last 4 bits equal to zero. Byte w2 contains 4 bits equal to zero plus the last 4 inverted bits of the RD byte.

During this second refresh command device return on MISO a new Random Code. This new random code must be inverted and send along with the next 2 refresh commands and so on.

The second command must be done in the open window if the Window operation was selected.

Advance Watchdog, refresh by 4SPI commands:

The refresh command is splitted in 4 SPI commands.

The first partial refresh command is 0x5Aw1, the second is 0x5Aw2, the third is 0x5Aw3 and the last is 0x5Aw4.

Byte w1 contains the first 2inverted bits of the RD byte plus the last 6 bits equal to zero.

Byte w2 contains 2 bits equal to zero plus the next 2 inverted bits of the RD byte plus 4 bits equal to zero.

Byte w3 contains 4bits equal to zero plus the next 2 inverted bits of the RD byte plus 2 bits equal to zero.

Byte w4 contains 6bits equal to zero plus the next 2 inverted bits of the RD byte.

During this fourth refresh command device return on MISO a new Random Code. This new random code must be inverted and send along with the next 4 refresh commands.

The fourth command must be done in the open window if the Window operation was selected.

PROPER RESPONSE TO $\overline{\text{INT}}$

A device detect, that upon an $\overline{\text{INT}}$, the software handles the $\overline{\text{INT}}$ in a timely manner: Access of the $\overline{\text{INT}}$ register is done within 2 watchdog periods. Such feature must be enabled by SPI via the INIT WD register bit 7

FUNCTIONAL BLOCK OPERATION VERSUS MODE

Table 6. Device Block Operation for Each State

| State | VDD | 5V-CAN | I/Ox / WU | VAUX | CAN | LIN1/2 |
|---------------------------------|--|-------------------------------|---|------------|--|---|
| Power down | OFF | OFF | OFF | OFF | High-impedance | High-impedance |
| Init Reset | ON | OFF | HS/LS off Wake up disable | OFF | OFF: CAN termination 25k to gnd Transmitter / receiver /wake-up OFF | OFF: internal 30k pull up active. Transmitter: receiver / wake up OFF. LIN term OFF |
| INIT | ON | OFF | SPI config WU disable | OFF | OFF | OFF |
| Reset | ON | Keep SPI config | HS/LS off WU disable | OFF | OFF | OFF |
| Normal Request | ON | Keep SPI config | HS/LS off WU disable | OFF | OFF | OFF |
| Normal | ON | SPI config | SPI config WU SPI config | SPI config | SPI config | SPI config |
| Low power V _{DD} OFF | OFF | OFF | user defined WU SPI config | OFF | OFF + wake-up en/dis | OFF + wake-up en/dis |
| Low power V _{DD} ON | ON ⁽²¹⁾ | OFF | user defined WU SPI config | OFF | OFF + wake-up en/dis | OFF + wake-up en/dis |
| SAFE output low: Safe case A | safe case A:ON safe case B: OFF | A: Keep SPI config, B: OFF | HS/LS off wake-up by change state | OFF | OFF + wake-up enable | OFF + wake-up enable |
| FLASH | ON | SPI config | SPI config | SPI config | SPI config | OFF |

Notes

- 21. With limited current capability
- 22. 5V-CAN is ON in Debug mode.

The 5V-CAN default is ON when the device is powered-up and set in Debug Mode. It is fully controllable via the SPI command.

ILLUSTRATION OF DEVICE MODE TRANSITIONS.

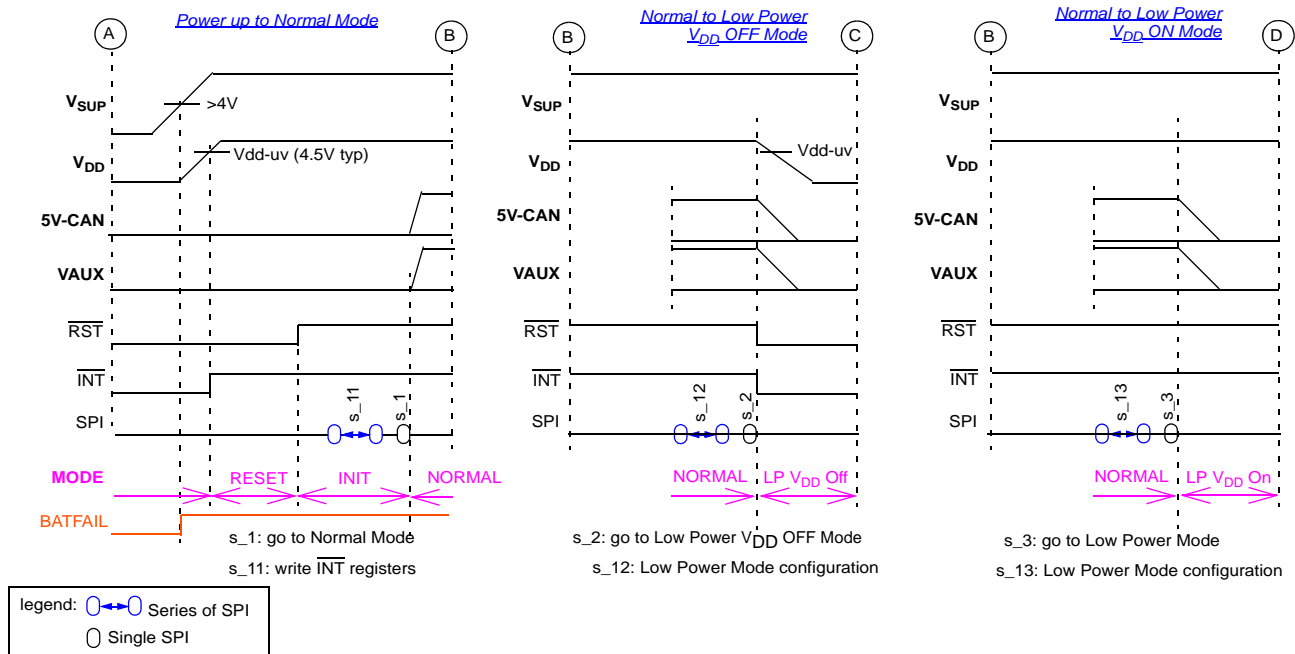


Figure 19. Power Up Normal and Low Power Modes

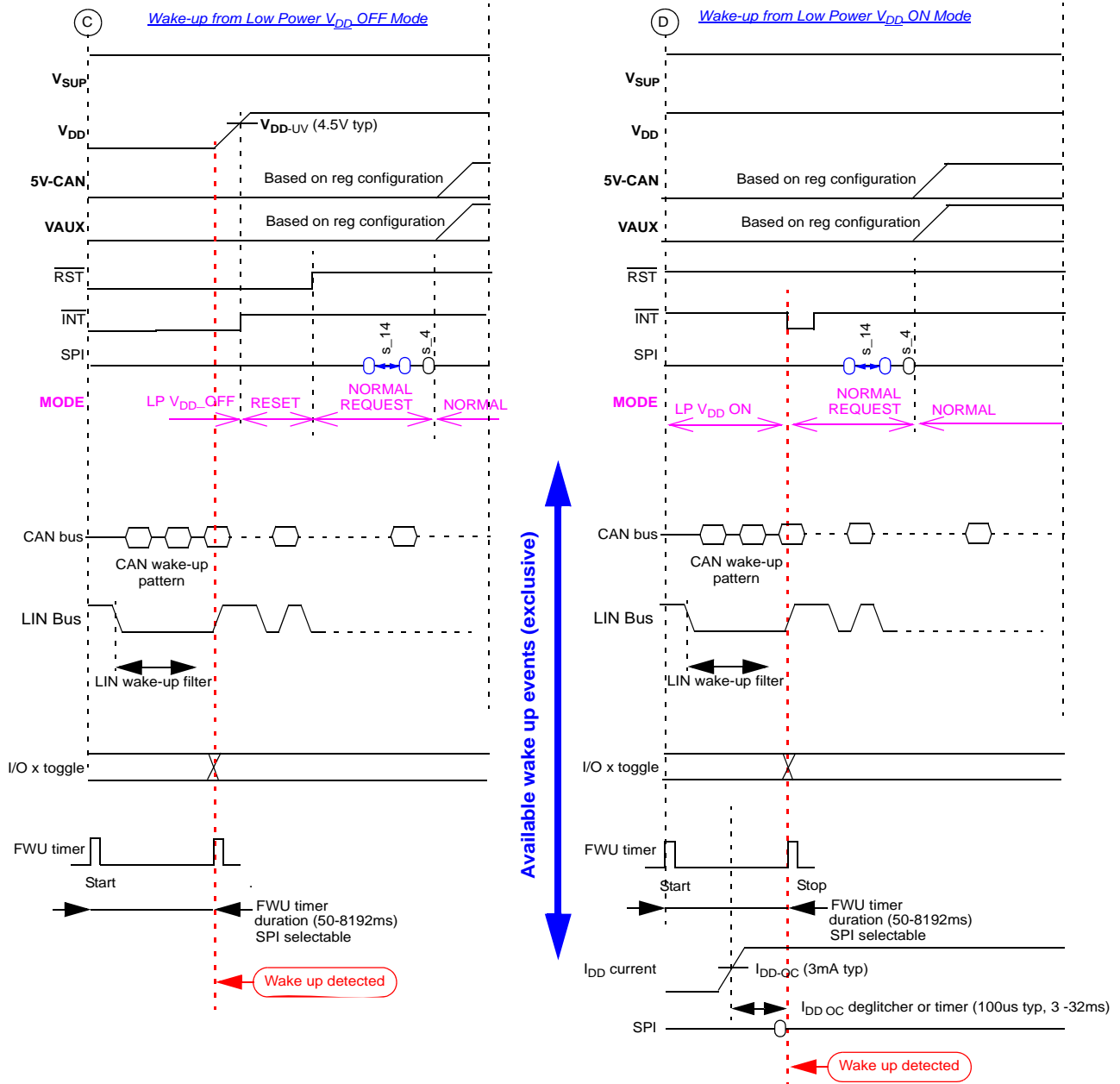


Figure 20. Wake-up from Low Power Modes

CYCLIC SENSE OPERATION DURING LP MODES

This function can be used in both Low Power modes (LP Vdd off and LP Vdd on).

Cyclic sense is the periodic activation of I/O-0, to allow biasing of external contact switches. The contact switch state can be detected via I/O-1, 2 and 3, and device can wake up from LP mode.

Cyclic sense is optimized and designed primarily for closed contact switch, in order to minimize consumption via the contact pull up resistor.

Principle:

A dedicated timer allows to select a cyclic sense period from 3 to 512ms (selection in timer B).

At end of the period, the I/O-0 will be activated for a duration of T_{cson} (SPI selectable in INIT register, to 200us,

400us, 800us or 1.6ms). The I/O-0 high side transistor or low side transistor can be activated. The selection is done by the state of I/O-0 prior to enter in low power mode.

During the T_{cson} duration, the I/O-x are monitored. If one of them is high, the device will detect a wake up. (Figure 21).

Cyclic sense period is selected by SPI configuration prior to enter in device low power mode. Upon entering LP mode, I/O-0 should be activated.

The level of I/O-1 is sense during the I/O-0 active time, and is deglitched for a duration of typ 30us. This mean that I/O-1 should be in the expected state for a duration longer than the deglitcher time.

The diagram below (Figure 21) illustrates the cyclic sense operation, with I/O-0 high side active and I/O-1 wake up in case of high level.

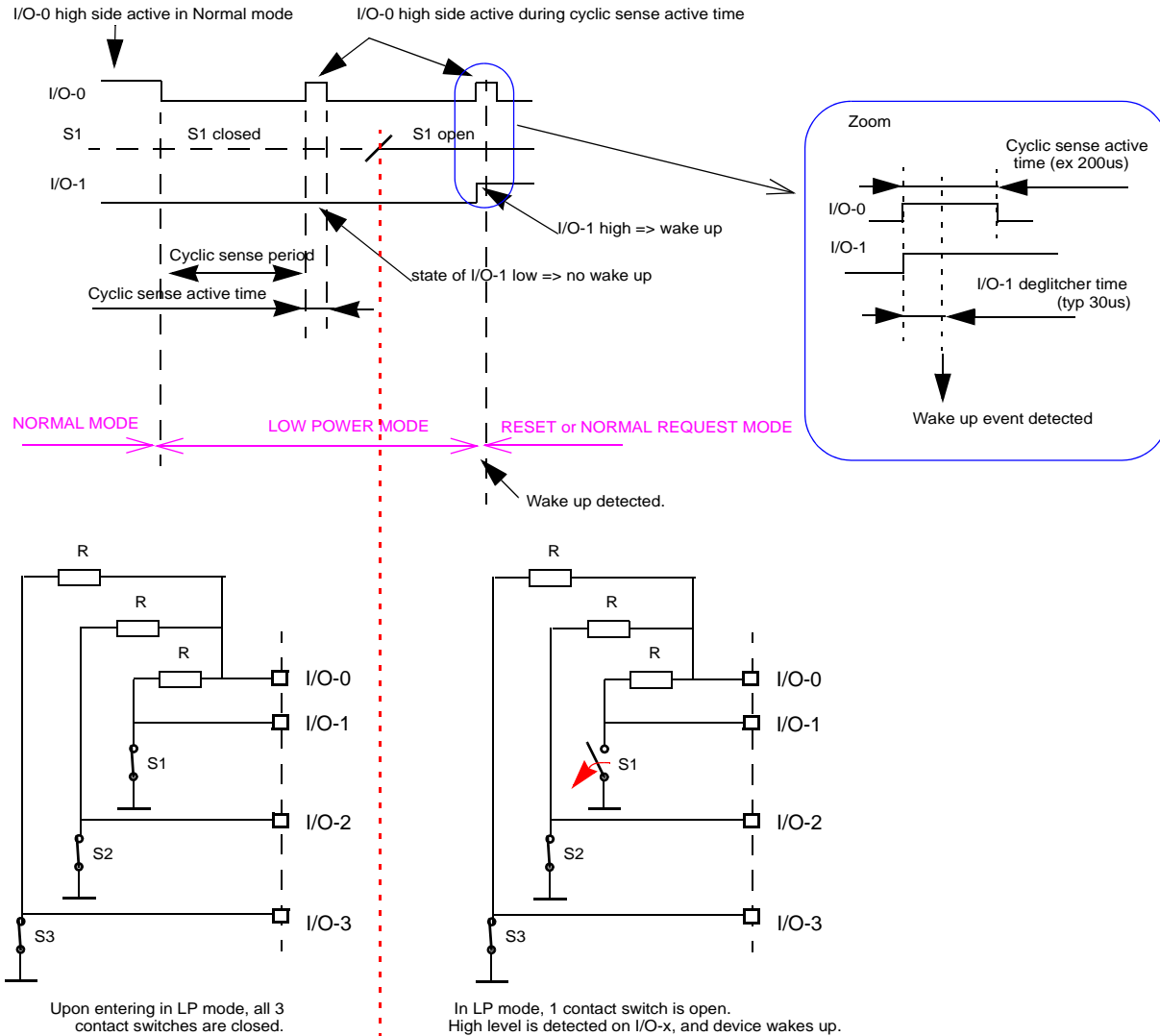


Figure 21. Cyclic Sense operation - switch to gnd, wake up by open switch

BEHAVIOR AT POWER UP AND POWER DOWN

DEVICE POWER UP:

This section describe the device behavior during ramp up, and ramp down of Vsup1, and the flexibility offered mainly by the Crank bit and the 2 Vdd undervoltage reset thresholds.

The figures below illustrate the device behavior during Vsup1 ramp up. As the Crank bit is by default set to 0, Vdd is enable when Vsup1 is above Vsup th 1 parameters.

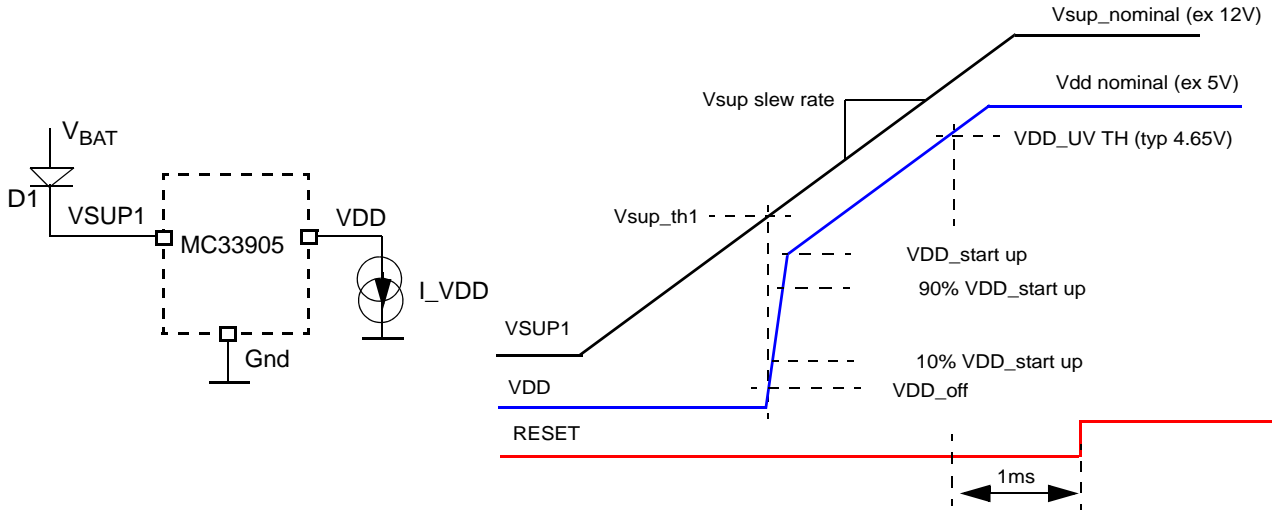


Figure 22. Vdd start up versus Vsup1 ramp

DEVICE POWER DOWN

The figures below illustrate the device behavior during Vsup1 ramp down, based on Crank bit configuration, and Vdd undervoltage reset selection.

(Vdd < 4.6V or Vdd < 3.2V typ, threshold selected by SPI). When device is in Reset, if Vsup is below “Vsup_th1”, Vdd is turned OFF.

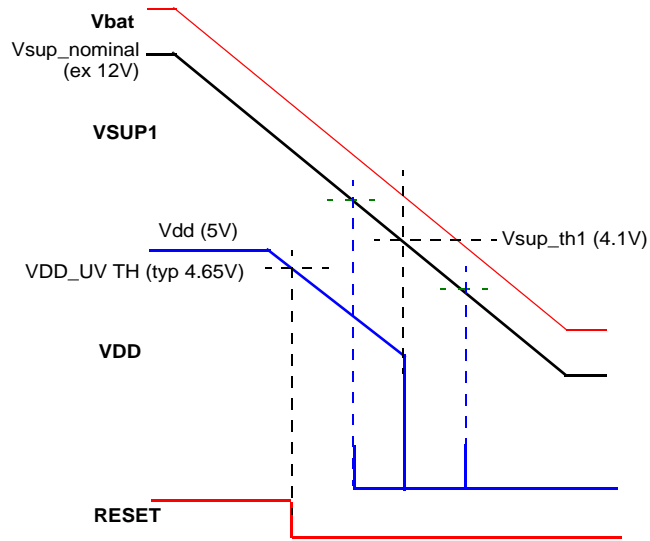
Crank bit reset (INIT W/D register, bit 0 =0):

Bit 0 = 0 is the default state for this bit.

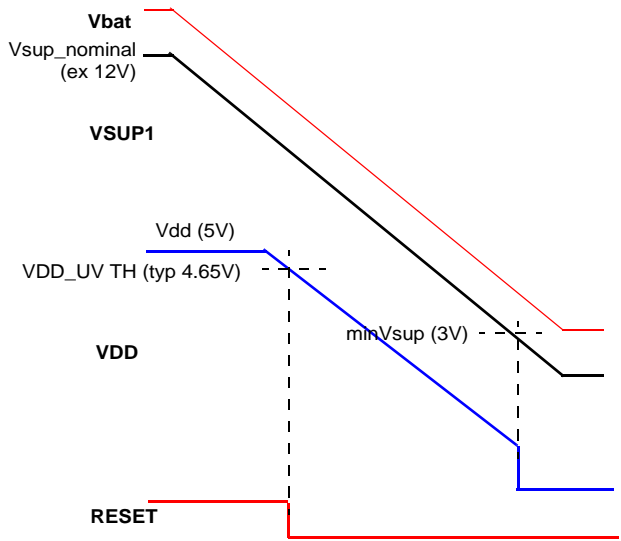
During Vsup ramp down, Vdd remain ON until device enters in Reset mode due to Vdd Under Voltage condition

Crank bit set (INIT W/D register, bit 0 =1):

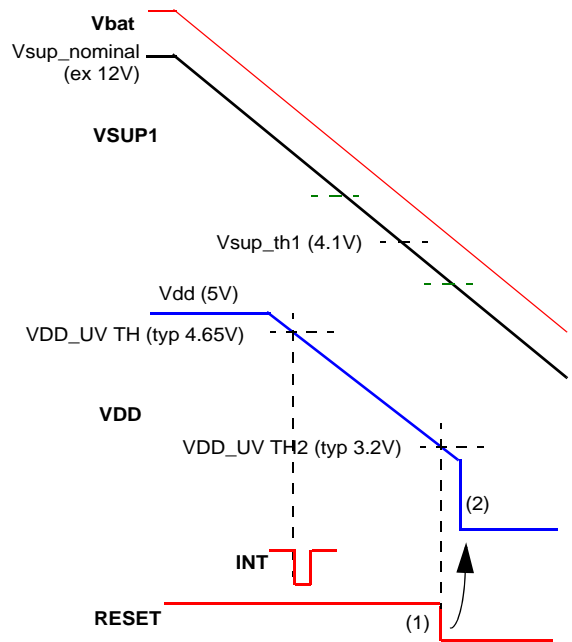
The bit 0 is set by SPI write. During Vsup ramp down, Vdd remains ON until device detects a POR and set BATfail. This occurs for a Vsup approx 3V.



Case 1: "Vdd UV th 4.6V", with bit Crank =0 (default value)

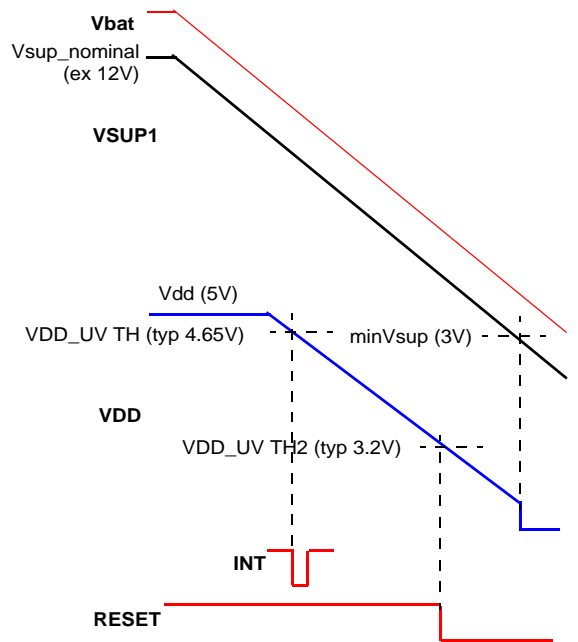


Case 2: "Vdd UV 4.6V", with bit Crank =1



(1) reset then (2) Vdd turn OFF

Case 3: "Vdd UV th 3.2V", with bit Crank =0 (default value)



Case 2: "Vdd UV th 3.2V", with bit Crank =1

Figure 23. Vdd Behavior During Vsup1 Ramp Down

FAIL SAFE OPERATION

OVERVIEW

Fail safe mode is entered when specific fail conditions occur. The “Safe state” condition is defined by the resistor connected at the DGB pin. Safe Mode is entered after additional event or conditions are met: time out for CAN communication and state at I/O-1 pin.

Exit of the safe state is always possible by a wake-up event: in the safe state the device is automatically wakeable CAN and I/O (if configured as inputs). Upon wake-up, the device operation is resumed: enter in Reset Mode.

FAIL SAFE FUNCTIONALITY

Upon dedicated event or issue detected at a device pin (i.e RESET), the Safe mode can be entered. In this mode, the SAFE terminal is active low.

Description

Upon activation of the SAFE terminal, and if the failure condition that make the SAFE pin activated have not recovered, the device can help to reduce ECU consumption, assuming that the MCU is not able to set the whole ECU in low power mode. Two main cases are available:

mode A:

Upon SAFE activation, the MCU remains powered (Vdd stays ON), until the failure condition recovers (i.e S/W is able to properly control the device and properly refresh the W/D).

modes B1, B2 and B3:

Upon SAFE activation, the system continues to monitor external event, and disable the MCU supply (turn Vdd off). The external events monitored are: CAN traffic, I/O-1 low level or both of them. 3 sub cases exist, B1, B2 and B3.

Note: no CAN traffic indicates that the ECU of the vehicle are no longer active, thus that the car is being parked and stopped. The I/O low level detection can also indicate that the vehicle is being shutdown, if the I/O-1 terminal is connected for instance to a switched battery signal (ignition key on/off signal).

The selection of the monitored events is done by hardware, via the resistor connected at DBG pin, but can be over write by software, via a specific SPI command.

By default, after power up the device detect the resistor value at DBG pin (upon transition from INIT to Normal mode), and, if no specific SPI command related to Debug resistor change is send, operates according to the detected resistor.

The INIT MISC register allow to verify and change the device behaviour, to either confirm or change the hardware selected behaviour. Device will then operate according to the SAFE mode configured by SPI.

Table below (Table 7) illustrates the complete options available:

Table 7. Fail Safe Options

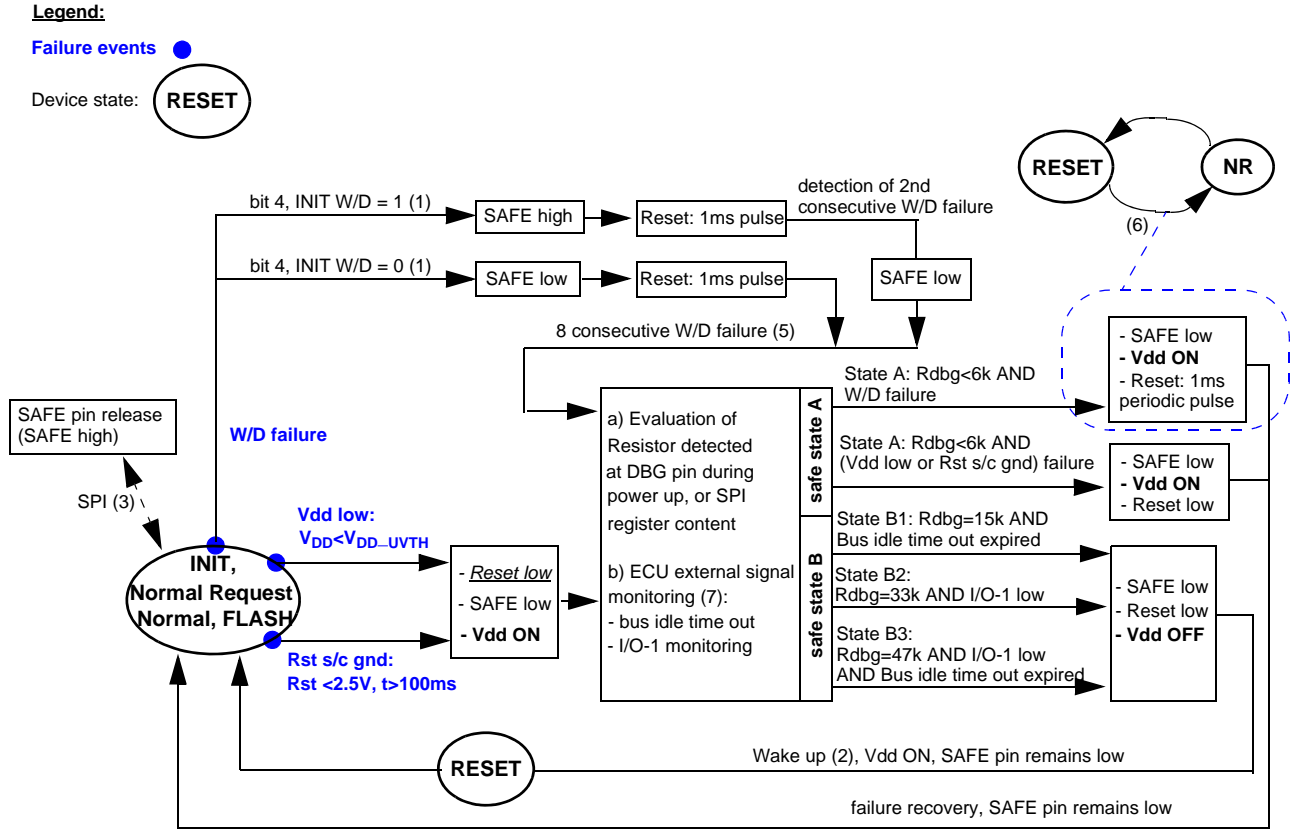
| Resistor at DBG pin | SPI coding - register INIT MISC bits [2,1,0] (higher priority that Resistor coding) | Safe mode code | Vdd status |
|---------------------|--|----------------|---|
| <6k | bits [2,1,0] = [111]: verification enable: resistor at DBG terminal is typ 0kohms (RA) - Selection of SAFE mode A | A | remains ON |
| typ 15k | bits [2,1,0] = [110]: verification enable: resistor at DBG terminal is typ 15kohms (RB1) - Selection of SAFE mode B1 | B1 | Turn OFF 8s after CAN traffic bus idle detection. |
| typ 33k | bits [2,1,0] = [101]: verification enable: resistor at DBG terminal is typ 33kohms (RB2) - Selection of SAFE mode B2 | B2 | Turn OFF when I/O-1 low level detected. |
| typ 68k | bits [2,1,0] = [100]: verification enable: resistor at DBG terminal is typ 68kohms (RB3) - Selection of SAFE mode B3 | B3 | Turn OFF 8s after CAN traffic bus idle detection AND when I/O-1 low level detected. |

Exit of Safe Mode

Exit of the safe state with Vdd off is always possible by a wake-up event: in this safe state the device is automatically wakeable by CAN and I/O (if I/O wake up was enable by SPI

prior to enter in SAFE mode). Upon wake-up, the device operation is resumed, and device enters in reset mode. The SAFE terminal remains active, until a proper read and clear of the SPI flags reporting the SAFE conditions.

SAFE operation flow chart



- 1) bit 4 of INIT Watchdog register
- 2) Wake up event: CAN, LIN or I/O-1 high level (if I/O-1 wake up previously enabled)
- 3) SPI commands: 0xDD00 or 0xDD80 to release SAFE pin
- 4) Recovery: reset low condition released, Vdd low condition released, correct SPI W/D refresh
- 5) detection of 8 consecutive W/D failures: no correct SPI W/D refresh command occurred for duration of 8 x 256ms.
- 6) Dynamic behavior: 1ms reset pulse every 256ms, due to no W/D refresh SPI command, and device state transition between RESET and NORMAL REQUEST mode, or INIT RESET and INIT modes.
- 7) 8 second timer for bus idle time out. I/O-1 high to low transition.

Figure 24. Safe Operation Flow Chart

Conditions to set SAFE pin active low:

Watchdog refresh issue: SAFE activated at 1st reset pulse or at the second consecutive reset pulse (selected by bit 4, INIT W/D register).

Vdd low: $V_{DD} < R_{ST-TH}$. SAFE pin is set low at same time as Reset pin is set low.

The RESET pin is monitored to verify that reset is not clamped to a low level preventing the MCU to operate. If this is the case, the Safe Mode is entered.

SAFE Mode A Illustration:

The figure below illustrate the event, and consequences when SAFE Mode A is selected via the appropriate debug resistor or SPI configuration.

Behavior illustration for safe state A (Rdg <6kOhms), or selection by SPI

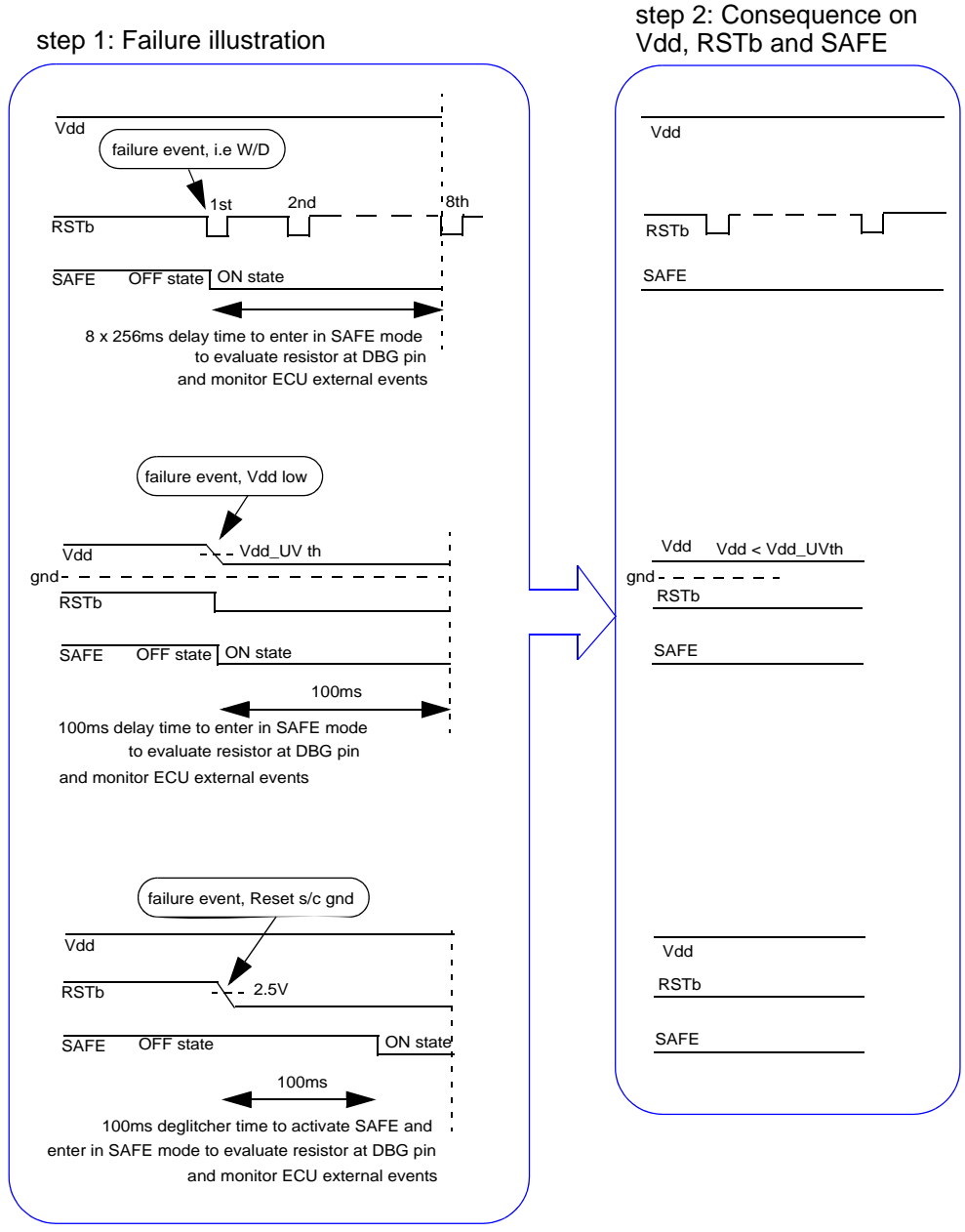


Figure 25. SAFE Mode A Behavior Illustration

SAFE mode B1, B2 and B3 illustration:

The figure below illustrates the event, and consequences when SAFE Mode B1, B2 or B3 is selected via the appropriate debug resistor or SPI configuration.

Behavior illustration for safe state B ($R_{dg} > 10k\Omega$)

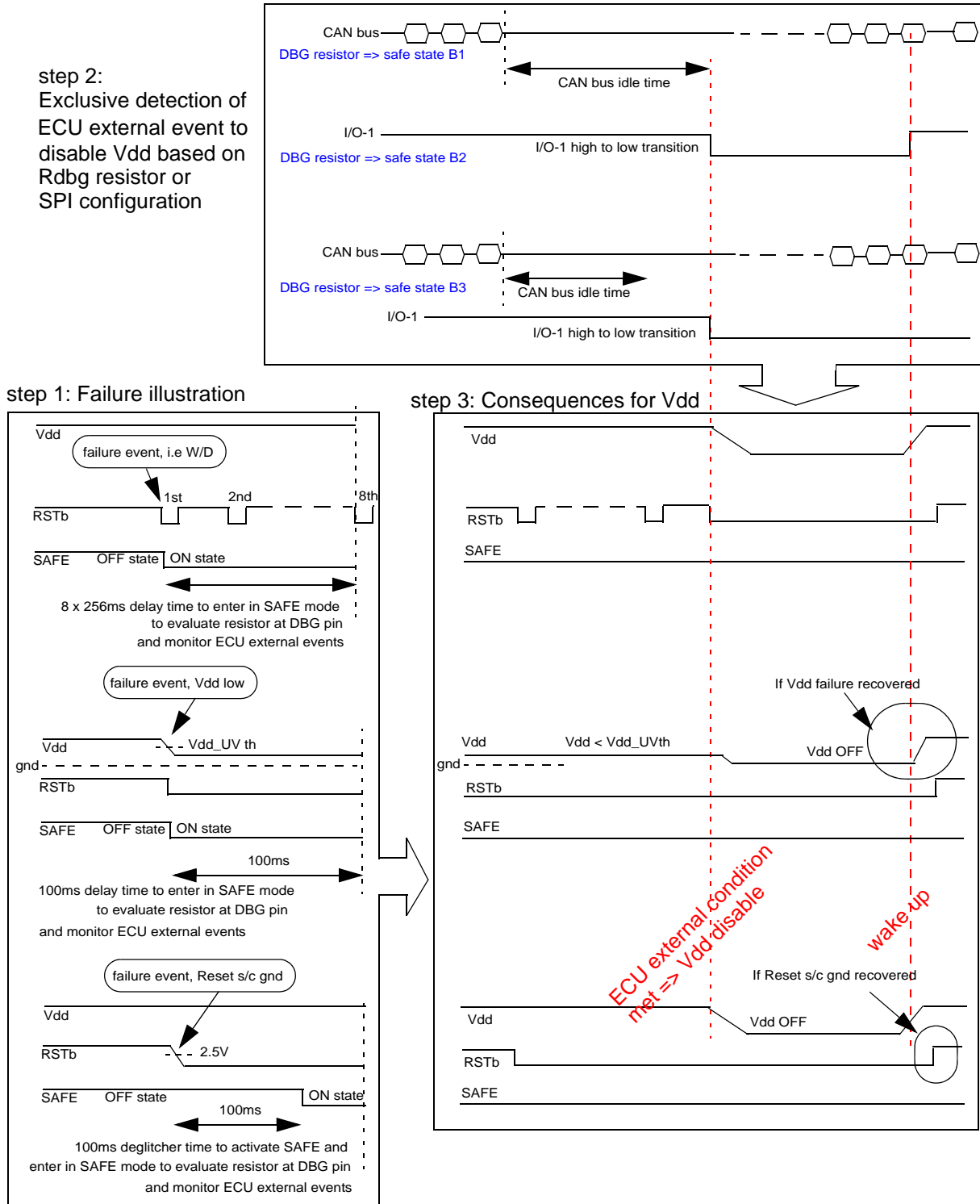


Figure 26. SAFE Modes B1, B2 or B3 Behavior Illustration

CAN INTERFACE

CAN INTERFACE DESCRIPTION

The figure below is a high level schematic of the CAN interface. It consist in a low side driver between CANL and gnd, and high side driver from CANH to 5V-CAN. Two differential receivers are connected between CANH and CANL, to detect bus state and to wake up from CAN Sleep

Mode. An internal 2.5V reference provide the 2.5V recessive level via the matched Rin resistors. The resistors can be switched to gnd in CAN Sleep Mode. A dedicated split buffer provide a low impedance 2.5V to the Split terminal, for recessive level stabilization.

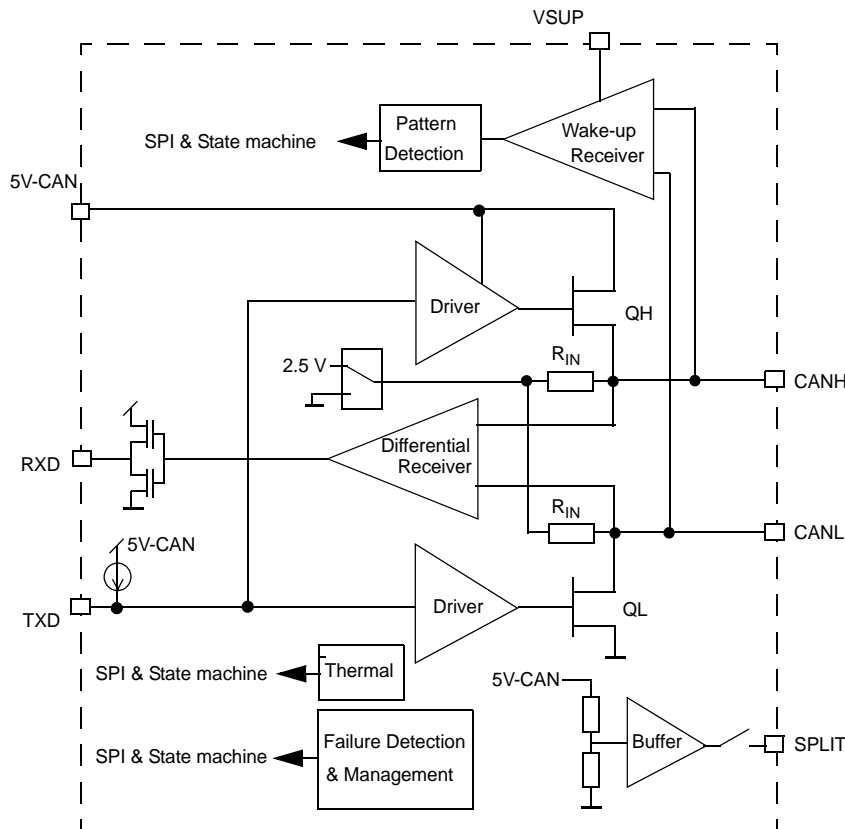


Figure 27. CAN Interface Block Diagram

CAN INTERFACE SUPPLY

The supply voltage for the CAN driver is the 5V-CAN pin. The CAN interface also has a supply pass from the battery line, through the VSUP pin. This pass is used in CAN Sleep Mode to allow wake-up detection.

During CAN communication (transmission and reception), the CAN interface current is sourced from the 5V-CAN pin. During CAN Low Power Mode, the current is sourced from the Vsup2 pin.

TX RX MODE

In Tx/Rx Mode, both the CAN driver and the receiver are ON. In this mode, the CAN lines are controlled by the TXD pin level, and the CAN bus state is reported on the RXD pin.

The 5V-CAN regulator must be ON. It supplies the CAN driver and receiver. The SPLIT pin is active and a 2.5V biasing is provided on the SPLIT output pin.

RECEIVE ONLY MODE

This mode is used to disable the CAN driver, but leave the CAN receiver active. In this mode, the device is only able to report the CAN state on the RXD pin. The TXD pin has no effect on CAN bus lines. The 5V-CAN regulator must be ON. The SPLIT pin is active and a 2.5V biasing is provided on the SPLIT output pin.

OPERATION in TX/RX Mode

The CAN driver will be enable as soon as the device is in Normal Mode and the TXD pin is recessive.

When the CAN interface is in Normal Mode, the driver has two states: recessive or dominant. The driver state is controlled by the TXD pin. The bus state is reported through the RXD pin.

When TXD is high, the driver is set in the recessive state, and CANH and CANL lines are biased to the voltage set with $5V-CAN$ divided by 2, or approx. 2.5V.

When TXD is low, the bus is set into the dominant state, and CANL and CANH drivers are active. CANL is pulled low and CANH is pulled high.

The RXD pin reports the bus state: CANH minus the CANL voltage is compared versus an internal threshold (a few hundred mV).

If "CANH minus CANL" is below the threshold, the bus is recessive and RXD is set high.

If "CANH minus CANL" is above the threshold, the bus is dominant and RXD is set low.

The SPLIT pin is active and provide a 2.5V biasing to the SPLIT output.

Tx/Rx Mode and Slew Rate Selection

The CAN signal slew rate selection is done via the SPI. By default and if no SPI is used, the device is in the fastest slew rate. Three slew rates are available. The slew rate controls the recessive to dominant, and dominant to recessive transitions. This also affects the delay time from the TXD pin

to the bus, and from the bus to the RXD. The loop time is thus affected by the slew rate selection.

Minimum Baud rate

The minimum baud is determined by the shortest TXD permanent dominant timing detection. The maximum number of consecutive dominant bits in a frame is 12 (6 bits of active error flag and its echo error flag).

The shortest TXD dominant detection time of $300\mu s$ lead to a single bit time of: $300\mu s / 12 = 25\mu s$.

So the minimum Baud rate is $1 / 25\mu s = 40k\text{Baud}$.

SLEEP MODE

Sleep Mode is a reduced current consumption mode. CANH and CANL driver are disabled and CANH and CANL lines are terminated to GND via the Rin resistor, the SPLIT pin is high-impedance. In order to monitor bus activities, the CAN wake-up receiver can be enabled. It is supplied internally from Vsup2.

Wake-up events occurring on the CAN bus pin are reporting by dedicated flags in SPI and by INT pulse, and results in a device wake up if device was in Low Power Mode.

When the device is set back into Normal Mode, CANH and CANL are set back into the recessive level. This is illustrated in Figure 28.

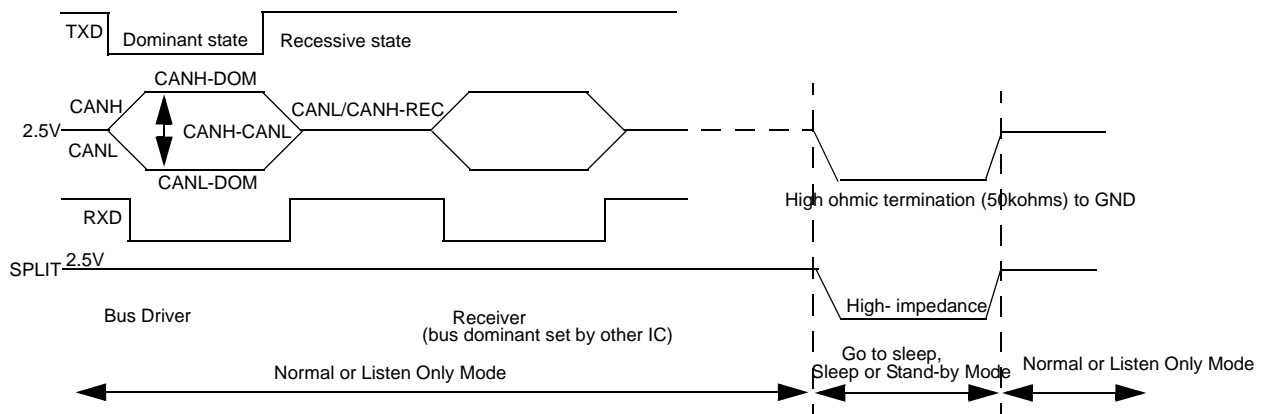


Figure 28. Bus Signal in Tx/Rx and Low Power Mode

Wake-up

When the CAN interface is in Sleep Mode with wake-up enabled, the CAN bus traffic is detected. The CAN bus wake-

up is a pattern wake-up. The wake-up by the CAN is enabled or disabled via the SPI.

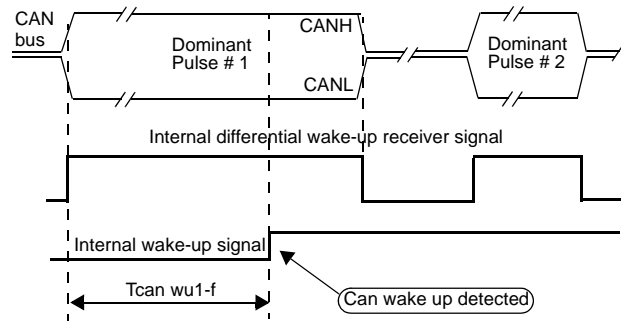
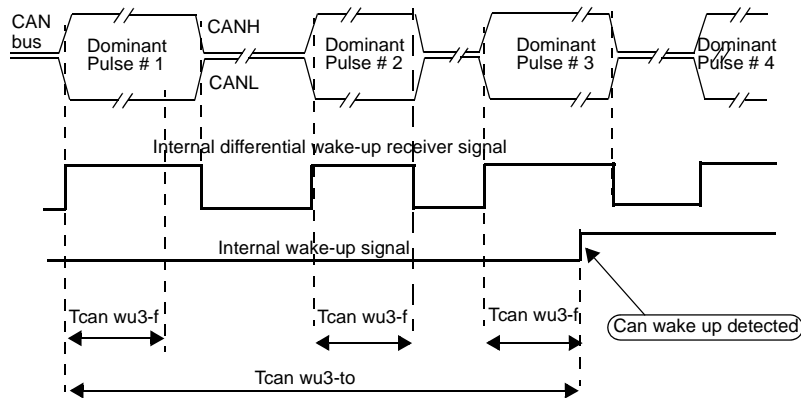


Figure 29. Single Dominant Pulse Wake-up

Pattern Wake-up

In order to wake-up the CAN interface, the wake-up receiver must receive a series of 3 consecutive valid dominant pulses, by default when the CANWU bit is low. CANWU bit can be set high by SPI and the wake-up will occur after a single pulse duration of 2µs (typ).

A valid dominant pulse should be longer than 500ns. The 3 pulses should occur in a time frame of 120µs, to be considered valid. When 3 pulses meet these conditions, the wake signal is detected. This is illustrated by the following figure.



Dominant Pulse # n: duration 1 or multiple dominant bits

Figure 30. Pattern Wake-up - Multiple Dominant Detection

BUS TERMINATION

The device supports the two main types of bus terminations:

- Differential termination resistors between CANH and CANL lines.

- SPLIT termination concept, with the mid point of the differential termination connected to GND through a capacitor and to the SPLIT pin.
- In application, device can also be used without termination.

- The figure below illustrate some of the most common terminations.

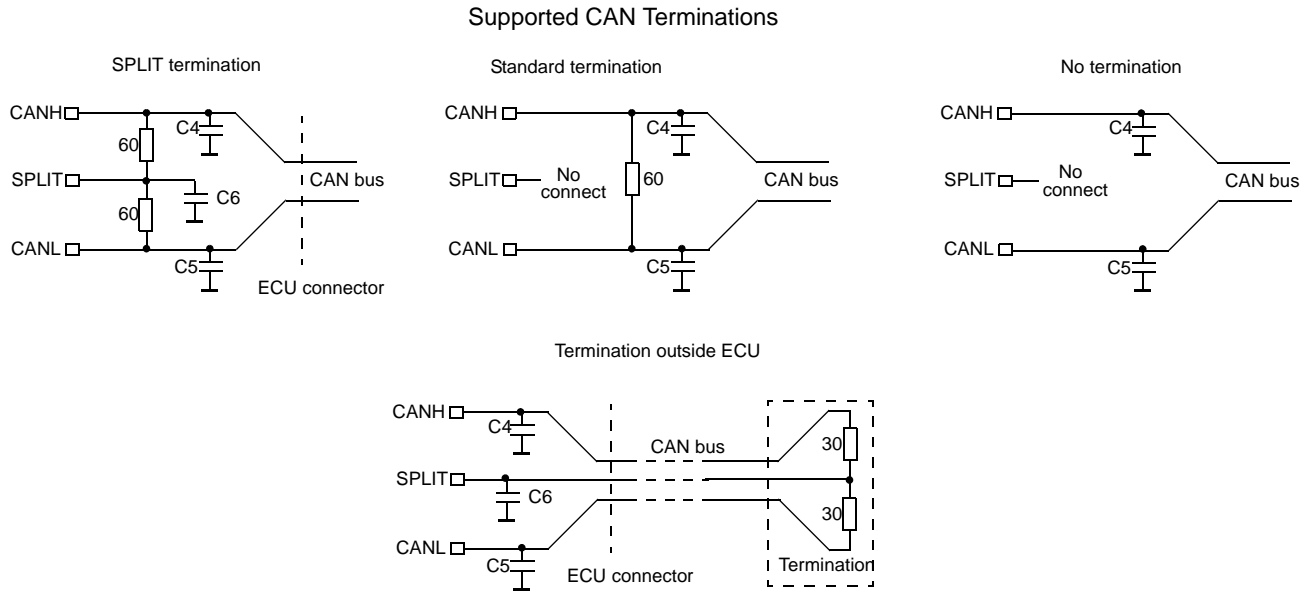


Figure 31. Typical Application and Bus Termination Options

CAN BUS FAULT DIAGNOSTIC

The device includes diagnostic of bus short-circuit to GND, VBAT, and internal ECU 5.0 V. Several comparators are implemented on CANH and CANL lines. These comparators

monitor the bus level in the recessive and dominant states. The information is then managed by a logic circuitry to properly determine the failure and report it.

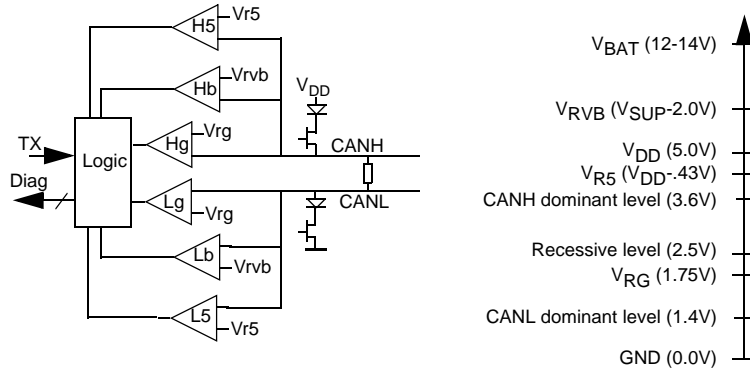


Figure 32. CAN Bus Simplified Structure Truth Table for Failure Detection

The following table indicates the state of the comparators in case of a bus failure, and depending upon the driver state.

Table 8. Failure Detection Truth Table

| Failure Description | Driver Recessive State | | Driver Dominant State | |
|---------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| | Lg (threshold 1.75V) | Hg (threshold 1.75V) | Lg (threshold 1.75V) | Hg (threshold 1.75V) |
| No failure | 1 | 1 | 0 | 1 |
| CANL to GND | 0 | 0 | 0 | 1 |
| CANH to GND | 0 | 0 | 0 | 0 |
| | Lb (threshold $V_{SUP} - 2.0V$) | Hb (threshold $V_{SUP} - 2.0V$) | Lb (threshold $V_{SUP} - 2.0V$) | Hb (threshold $V_{SUP} - 2.0V$) |
| No failure | 0 | 0 | 0 | 0 |
| CANL to VBAT | 1 | 1 | 1 | 1 |
| CANH to VBAT | 1 | 1 | 0 | 1 |
| | L5 (threshold $V_{DD} - 0.43V$) | H5 (threshold $V_{DD} - 0.43V$) | L5 (threshold $V_{DD} - 0.43V$) | H5 (threshold $V_{DD} - 0.43V$) |
| No failure | 0 | 0 | 0 | 0 |
| CANL to 5.0V | 1 | 1 | 1 | 1 |
| CANH to 5.0V | 1 | 1 | 0 | 1 |

DETECTION PRINCIPLE

In the recessive state, if one of the two bus lines are shorted to GND, VDD (5V), or VBAT, the voltage at the other line follows the shorted line, due to the bus termination resistance. For example: if CANL is shorted to GND, the CANL voltage is zero, the CANH voltage measured by the Hg comparator is also close to zero.

In the recessive state, the failure detection to GND or VBAT is possible. However, it is not possible with the above implementation to distinguish which of the CANL or CANH lines are shorted to GND or VBAT. A complete diagnostic is possible once the driver is turned on, and in the dominant state.

Number of Samples for Proper Failure Detection

The failure detector requires at least one cycle of the recessive and dominant states to properly recognize the bus failure. The error will be fully detected after 5 cycles of the recessive-dominant states. As long as the failure detection

circuitry has not detected the same error for 5 recessive-dominant cycles, the error is not reported.

BUS CLAMPING DETECTION

If the bus is detected to be in dominant for a time longer than (T_{DOM}), the bus failure flag is set and the error is reported in the SPI.

Such condition could occur in case the CANH line is shorted to a high-voltage. In this case current will flow from the high-voltage short circuit through the bus termination resistors (60Ω) and then in the SPLIT pin (if used) and in the device CANH and CANL input resistors, which are terminated to internal 2.5V biasing or to GND (Sleep Mode).

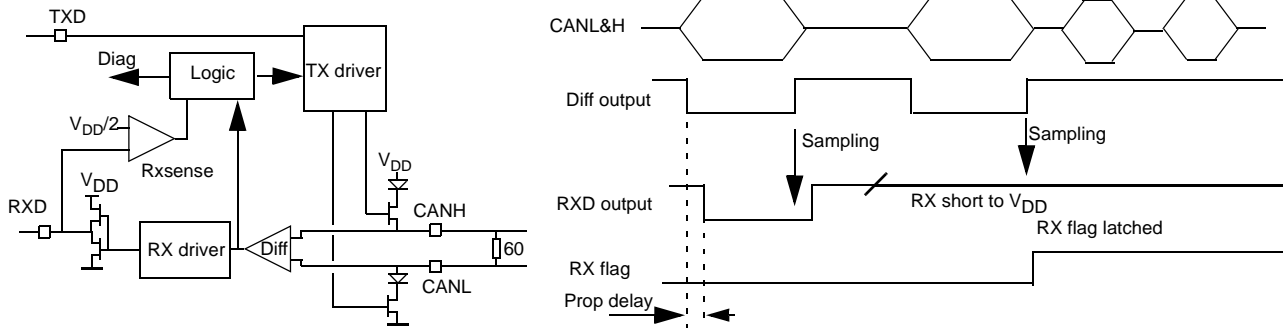
Depending upon the high-voltage short-circuit, the number of nodes, usage of the SPLIT pin, R_{IN} actual resistor and Mode state (Sleep or Active) the voltage across the bus termination can be sufficient to create a positive dominant voltage between CANH and CANL, and RXD pin will be low. This would prevent start of any CAN communication, and

thus a proper failure identification (requires 5 pulses on TXD). The bus dominant clamp circuit will help to determine such failure situation.

RX PERMANENT RECESSIVE FAILURE

The aim of this detection, is to diagnose an external hardware failure at the RX output pin and ensure that a

permanent failure at RX does not disturb the network communication. If RX is shorted to a logic high signal, the CAN protocol module within the MCU will not recognize any incoming message. In addition it will not be able to easily distinguish the bus idle state and can start communication at any time. In order to prevent this, an RX failure detection is necessary.



The RX flag is not the RXPR bit in the LPC register, and neither is the CANF in the INTR register.

Figure 33. RX Path Simplified Schematic, RX Short to V_{DD} Detection

Implementation for Detection

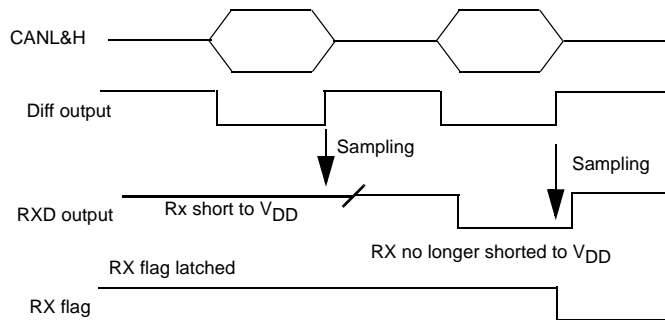
The implementation sense the RXD output voltage at each low to high transition of the differential receiver. Excluding the internal propagation delay, the RXD output should be low when the differential receiver is low. In case of an external short to V_{DD} at the RXD output, RXD will be tied to a high level and can be detected at the next low to high transition of the differential receiver.

As soon as the RXD permanent recessive is detected, the RXD driver is deactivated.

Once the error is detected the driver is disabled and the error is reported via SPI in CAN register.

Recovery Condition

The internal recovery is done by sampling a correct low level at TXD as shown in the following illustration.



The RX flag is not the RXPR bit in the LPC register, and neither is the CANF in the INTR register.

Figure 34. RX Path Simplified Schematic, Rx Short to V_{DD} Detection

TXD PERMANENT DOMINANT

Principle

If the TXD is set to a permanent low level, the CAN bus is set into dominant level, and no communication is possible. The device has a TXD permanent time out detector. After the timeout, the bus driver is disabled and the bus is released into a recessive state. The TXD permanent flag is set.

Recovery

The TXD permanent dominant is used and activated also in case of a TXD short to RXD. The recovery condition for a TXD permanent dominant (recovery means the re-activation of the CAN drivers) is done by entering into a Normal Mode controlled by the MCU or when TXD is recessive while RXD change from recessive to dominant.

TXD TO RXD SHORT CIRCUIT:

Principle

In case TXD is shorted to RXD during incoming dominant information, RXD is set low. Consequently, the TXD pin is low and drives CANH and CANL into a dominant state. Thus the bus is stuck in dominant. No further communication is possible.

Detection and Recovery

The TXD permanent dominant timeout will be activated and release the CANL and CANH drivers. However, at the next

incoming dominant bit, the bus will then be stuck in dominant again. The recovery condition is same as the TXD dominant failure

IMPORTANT INFORMATION FOR BUS DRIVER REACTIVATION

The driver stays disabled until the failure is/are removed (Tx and/or RX is no longer permanent dominant or recessive state or shorted) and the failure flags cleared (read). The CAN driver must be set by SPI in TxRx mode in order to re enable the CAN bus driver.

LIN BLOCK

LIN INTERFACE DESCRIPTION

The physical interface is dedicated to automotive LIN sub-bus applications.

The interface has 20kbps and 10kbps baud rates, and includes as well as a fast baud rate for test and programming modes. It has excellent ESD robustness and immunity against disturbance, and radiated emission performance. It has safe behavior in case of a LIN bus short-to-ground, or a LIN bus leakage during low power mode.

Digital inputs are related to device Vdd terminal.

POWER SUPPLY PIN (VSUP)

The VSUP-2 terminal is the supply pin for the LIN interface. To avoid a false bus message, an under-voltage on V_{SUP} disables the transmission path (from TXD to LIN) when V_{SUP} falls below 6.1 V.

GROUND PIN (GND)

In case of a ground disconnection at the module level, the LIN interface do not have significant current consumption on the LIN bus pin when in the recessive state.

LIN BUS PIN (LIN1, LIN2)

The LIN terminal represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems, and is compliant to the LIN bus specification 2.1 and SAEJ2602-2.

The LIN interface is only active during Normal mode.

Driver Characteristics

The LIN driver is a low side MOSFET with internal over-current thermal shutdown. An internal pull-up resistor with a serial diode structure is integrated so no external pull-up components are required for the application in a slave node. An additional pull-up resistor of 1.0 k Ω must be added when the device is used in the master node. The 1.0 k Ω pull resistor can connected to LIN term or to ECU battery supply.

The LIN pin exhibits no reverse current from the LIN bus line to V_{SUP} , even in the event of a GND shift or V_{SUP} disconnection.

The transmitter has a 20 kbps, 10 kbps and fast baud rate, which are selected by SPI.

Receiver Characteristics

The receiver thresholds are ratiometric with the device V_{sup2} voltage.

If the V_{sup2} voltage goes below typ 6.1V, the LIN bus enters into a recessive state even if communication is sent on TXD.

If LIN driver temperature reached over temperature threshold, the transceiver and receiver are disabled. When the temperature falls below the over temperature threshold, LIN driver and receiver will be automatically enabled.

DATA INPUT PIN (TXDL1, TXDL2)

The TXDI1 (TXDL2) input pin is the MCU interface to control the state of the LIN output. When TXDL is LOW (dominant), LIN output is LOW. When TXDL is HIGH (recessive), the LIN output transistor is turned OFF.

This pin has an internal pull-up current source to Vdd to force the recessive state if the input pin is left floating.

If the pin stays low (dominant sate) more than t_{TXDDOM} , the LIN transmitter goes automatically in recessive state. This is reported by flag in LIN register.

DATA OUTPUT PIN (RXDL1, RXDL2)

The RXDI output pin is the MCU interface, which reports the state of the LIN bus voltage.

LIN HIGH (recessive) is reported by a high voltage on RXD, LIN LOW (dominant) is reported by a low voltage on RXD.

LIN OPERATIONAL MODES

The LIN interface have two operational modes, Transmit receiver and LIN disable modes.

TRANSMIT RECEIVE

In the TxRx mode, the LIN bus can transmit and receive information.

When the 20kbps baud rate is selected, the slew rate and timing are compatible with LIN protocol specification 2.1.

When the 10kbps baud rate is selected, the slew rate and timing are compatible with J2602-2.

When the fast baud rate is selected, the slew rate and timing are much faster than the above specification and allow fast data transition.

SLEEP MODE

This mode is selected by SPI, and the transmission path is disabled. Supply current for LIN block from V_{SUP2} is very low (typ 3 μ A). LIN bus is monitor to detect wake-up event. In the Sleep Mode, the internal 725 k Ω m pull-up resistor is connected and the 30 k Ω m disconnected.

The LIN block can be awakened from Sleep Mode by detection of LIN bus activity.

LIN Bus Activity Detection

The LIN bus wake-up is recognized by a recessive to dominant transition, followed by a dominant level with a duration greater than 70 μ s, followed by a dominant to recessive transition. This is illustrated in [Figures 15](#) on page [26](#) and [Figures 16](#) on page [27](#). Once the wake-up is

detected, the event is reported to the device state machine. An INT is generated if device is in LP Vdd ON mode, or Vdd will restart if device was in LP Vdd off mode.

The wake up can be enable or disable by SPI.

Fail-Safe Features

The table below describes the LIN block behavior in case of failure.

Table 9. LIN Block Failure

| FAULT | FUNCTIONNAL MODE | CONDITION | CONSEQUENCE | RECOVERY |
|----------------------------|------------------|--|---|----------------|
| LIN supply undervoltage | Tx Rx | LIN supply voltage < 6V (typ) | LIN transmitter in recessive State | Condition gone |
| TXD Pin Permanent Dominant | | TXD pin low for more than t_{TXDDOM} | LIN transmitter in recessive State | Condition gone |
| LIN Thermal Shutdown | Tx Rx | LIN driver temperature > 160°C (typ) | LIN transmitter and receiver disabled High Side turned off | Condition gone |

SERIAL PERIPHERAL INTERFACE

HIGH LEVEL OVERVIEW

The device is using a 16 bits SPI, with the following arrangement:

MOSI, Master Out Slave In bits:

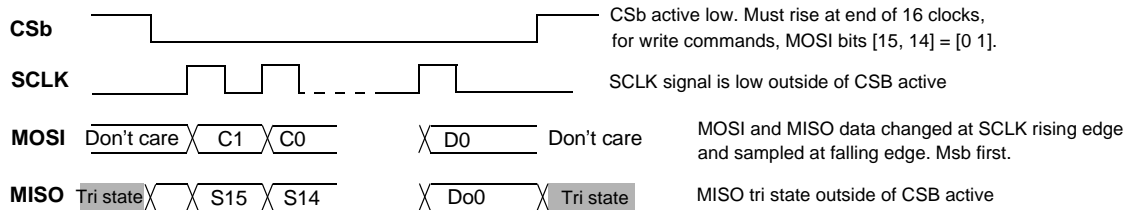
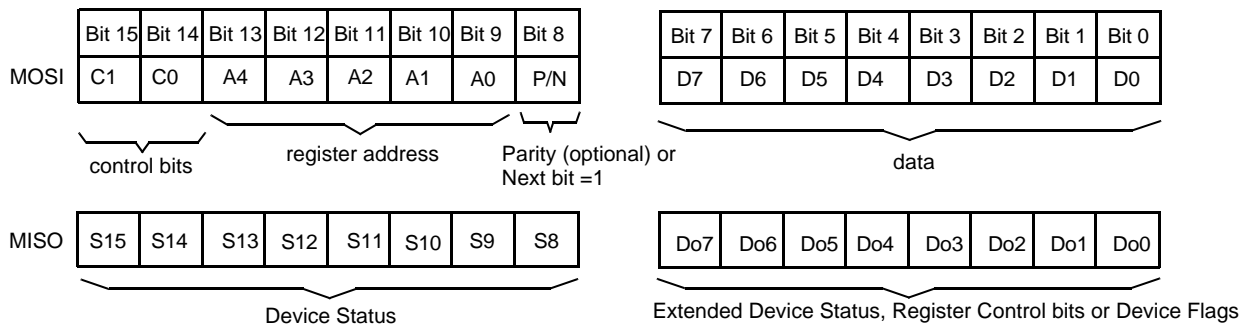
- bits 15 and 14 (called C1 and C0) are control bits to select the SPI operation mode (write control bit to device register, read back of the control bits, read of device flag).
- bit 13 to 9 (A4 to A0) to select the register address.

- bit 8 (P/N) has two functions: parity bit in write mode (optional, = 0 if not used), Next bit (=1) in read mode.
- bit7 to 0 (D7 to D0): control bits

MISO, Master IN Slave Out bits:

- bits 15 to 8 (S15 to S8) are device status bits
- bits 7 to 0 (Do7 to Do0) are either extended device status bits, device internal control register content or device flags.

Figure 35 is an overview of the SPI implementation.



SPI wave form, and signals polarity

Figure 35. Device SPI Overview

DETAIL OPERATION

BITS 15,14 AND 8 FUNCTIONS

[Table 10](#) summarizes the various SPI operation, depending upon bit 15, 14 and 8.

Table 10. SPI Operations (bits 8, 14 & 15)

| Control bits MOSI[15-14], C1-C0 | Type of Command | Parity/Next MOSI[8] P/N | Note for Bit 8 P/N |
|---------------------------------|--|-------------------------|--|
| 00 | Read back of register content | 1 | Bit 8 must be set to 1, independently of the parity function selected or not selected. |
| 01 | Write to register address, to control device operation | 0 | If bit 8 is set to "0": means parity not selected OR parity is selected AND parity = 0 |
| | | 1 | if bit 8 is set to "1": means parity is selected AND parity = 1 |
| 10 | Reserved | | |
| 11 | Read of device flags form a register address | 1 | Bit 8 must be set to 1, independently of the parity function selected or not selected. |

BITS 13-9 FUNCTIONS

The device contains several registers. Their address is coded on 5 bits (bits 13 to 9).

Each register controls or reports part of the device function. Data can be written to the register, to control the device operation or set default value or behavior.

Every register can also be read back in order to ensure that its content (default setting or value previously written) is correct.

In addition some of the registers are used to report device flags.

Device status on MISO

When a write operation is performed to store data or control bit into the device, MISO pin reports a 16 bits fixed device status composed of 2 bytes: Device Fixed Status (bits 15 to 8) + extended Device Status (bits 7 to 0). In a read operation, MISO will report the Fixed device status (bits 15 to 8) and the next 8 bits will be the content of the selected register.

REGISTER ADDRESS TABLE

Table 11 is the list of device registers and their associated address, coded with bits 13 to 9.

Table 11. Device Registers with Corresponding Address

| Address MOSI[13-9] A4...A0 | Description | Quick Ref. Name | Functionality |
|----------------------------------|--|--------------------|---|
| 0_0000 | Analog Multiplexer | MUX | 1) Write "device control bits" to register address. 2) Read back register "control bits" |
| 0_0001 | Memory byte A | RAM_A | 1) Write "data byte" to register address. 2) Read back "data byte" from register address |
| 0_0010 | Memory byte B | RAM_B | |
| 0_0011 | Memory byte C | RAM_C | |
| 0_0100 | Memory byte D | RAM_D | |
| 0_0101 | Initialization Regulators | Init REG | 1) Write "device initialization control bits" to register address. 2) Read back "initialization control bits" from register address |
| 0_0110 | Initialization Watchdog | Init W/D | |
| 0_0111 | Initialization LIN and I/O | Init LIN I/O | |
| 0_1000 | Initialization Miscellaneous functions | Init MISC | |
| 0_1001 | Specific Modes | SPE_MODE | 1) Write to register to select device Specific Mode, using "Inverted Random Code". 2) Read "Random Code" |
| 0_1010 | Timer_A: W/D & Low Power MCU consumption | TIM_A | 1) Write "timing values" to register address. 2) Read back register "timing values" |
| 0_1011 | Timer_B: Cyclic Sense & Cyclic Interrupt | TIM_B | |
| 0_1100 | Timer_C: W/D Low Power & Forced Wake-up | TIM_C | |
| 0_1101 | Watchdog Refresh | W/D | Watchdog Refresh Commands |
| 0_1110 | Mode register | MODE | 1) Write to register to select Low Power Mode, with optional "Inverted Random code" and select wake-up functionality 2) Read operations: Read back device "Current Mode" Read "Random Code", Leave "Debug Mode" |
| 0_1111 | Regulator Control | REG | 1) Write "device control bits" to register address, to select device operation. 2) Read back register "control bits". 3) Read device flags from each of the register addresses. |
| 1_0000 | CAN interface control | CAN | |
| 1_0001 | Input Output control | I/O | |
| 1_0010 | Interrupt Control | Interrupt | |

COMPLETE SPI OPERATION

Table 12 is a compiled view of all the SPI capabilities and options. Both MOSI and MISO information are described.

Table 12. SPI Capabilities with Options

| Type of Command | MOSI/ MISO | Control bits [15-14] | Address [13-9] | Parity/Next bits [8] | Bit 7 | Bits [6-0] |
|--|---------------|------------------------------|-------------------|-------------------------|---------------------------------|---|
| Read back of "device control bits" (MOSI bit 7 = 0) OR Read specific device information (MOSI bit 7 = 1) | MOSI | 00 | address | 1 | 0 | 000 0000 |
| | MISO | Device Fixed Status (8 bits) | | | Register control bits content | |
| | MOSI | 00 | address | 1 | 1 | 000 0000 |
| | MISO | Device Fixed Status (8 bits) | | | Device ID and I/Os state | |
| Write device control bit to address selected by bits (13-9). MISO return 16 bits device status | MOSI | 01 | address | (note) | Control bits | |
| | MISO | Device Fixed Status (8 bits) | | | Device Extended Status (8 bits) | |
| Reserved | MOSI | 10 | Reserved | | | |
| | MISO | Reserved | | | | |
| Read device flags and wake-up flags, from register address (bit 13-9), and sub address (bit 7). MISO return fixed device status (bit 15-8) + flags from the selected address and sub-address. | MISO | 11 | address | Reserved | 0 | Read of device flags form a register address, and sub address LOW (bit 7) |
| | MOSI | Device Fixed Status (8 bits) | | | Flags | |
| | MISO | 11 | address | 1 | 1 | Read of device flags form a register address, and sub address HIGH (bit 7) |
| | MOSI | Device Fixed Status (8 bits) | | | Flags | |

Note: P = 0 if parity bit is not selected or parity = 0. P = 1 if parity is selected and parity = 1.

Thus the Exact command will then be:
 MOSI [bit 15-0]= 01 00 011 0 01101001

PARITY BIT 8

Calculation

The parity is used for write to register command (bit 15,14 = 01). It is calculated based on the number of logic one contained in bits 15-9,7-0 sequence (this is the whole 16 bits of the write command except bit 8).

- Bit 8 must be set to 0 if the number of 1 is odd.
- Bit 8 must be set to 1 if the number of 1 is even.

Examples 1:

MOSI [bit 15-0]= 01 00 011 P 01101001, P should be 0, because the command contains 7 bits with logic 1.

Examples 2:

MOSI [bit 15-0]= 01 00 011 P 0100 0000, P should be 1, because the command contains 4 bits with logic 1.

Thus the Exact command will then be:
 MOSI [bit 15-0]= 01 00 011 1 0100 0000

Parity function selection:

The parity function is optional. It is selected by bit 6 in INIT MISC register.

If parity function is not selected (bit 6 of INIT MISC =0), then Parity bits in all SPI commands (bit 8) must be "0".

DETAIL OF CONTROL BITS AND REGISTER MAPPING

The following tables contain register bit meaning arranged by register address, from address 0_000 to address 1_0100

MUX AND RAM REGISTERS

Table 13. MUX Register

| MOSI First Byte [15-8] [b_15 b_14] 0_0000 [P/N] | MOSI Second Byte, bits 7-0 | | | | | | | |
|--|---|-------|-------|--------|---------|-------|-------|-------|
| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 01 00 _ 000 P | MUX_2 | MUX_1 | MUX_0 | Int 2K | I/O-att | X | X | X |
| Default state | 0 | 0 | 0 | N/A | 0 | | | |
| Condition for default | POR, 5V-CAN off, any mode different from Normal | | | | POR | | | |

| Bits | Description |
|-----------------|--|
| b7 b6 b5 | MUX_2, MUX_1, MUX_0 - Selection of external input signal or internal signal to be measured at MUX-OUT terminal |
| 000 | All functions disable. No output voltage at MUX-OUT terminal |
| 001 | V _{DD} regulator current recopy. Ratio is approx 1/97. Requires an external resistor or selection of Internal 2K (bit 3) |
| 010 | Device internal voltage reference (approx 2.5V) |
| 011 | Device internal temperature sensor voltage |
| 100 | Voltage at I/O-0. Attenuation or gain is selected by bit 3. |
| 101 | Voltage at I/O-1. Attenuation or gain is selected by bit 3. |
| 110 | Voltage at VSUP_1 terminal. Refer to electrical table for attenuation ratio (approx 5) |
| 111 | Voltage at VSENSE terminal. Refer to electrical table for attenuation ratio (approx 5) |
| b4 | INT 2k - Select device internal 2kohm resistor between AMUX and GND. This resistor allows the measurement of a voltage proportional to the V _{DD} output current. |
| 0 | Internal 2 kohm resistor disable. An external resistor must be connected between AMUX and GND. |
| 1 | Internal 2 kohm resistor enable. |
| b3 | I/O-att - When I/O-0 (or I/O-1) is selected with b7,b6,b5=100 (or 101), b3 selects attenuation or gain between I/O-0 (or I/O-1) and MUX-OUT terminal |
| 0 | Gain is approx 2 for device with V _{DD} =5V (Ref to electrical table for exact gain value) Gain is approx 1.3 for device with V _{DD} =3.3V (Ref to electrical table for exact gain value) |
| 1 | Attenuation is approx 6 for device with V _{DD} =5V (Ref to electrical table for exact attenuation value) Attenuation is approx 4 for device with V _{DD} =3.3V (Ref to electrical table for exact attenuation value) |

Table 14. Internal Memory Registers A, B, C and D, RAM_A, RAM_B, RAM_C and RAM_D

| MOSI First Byte [15-8] [b_15 b_14] 0_0xxx [P/N] | MOSI Second Byte, bits 7-0 | | | | | | | |
|--|----------------------------|--------|--------|--------|--------|--------|--------|--------|
| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 01 00 _ 001 P | Ram a7 | Ram a6 | Ram a5 | Ram a4 | Ram a3 | Ram a2 | Ram a1 | Ram a0 |
| Default state | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Condition for default | POR | | | | | | | |
| 01 00 _ 010 P | Ram b7 | Ram b6 | Ram b5 | Ram b4 | Ram b3 | Ram b2 | Ram b1 | Ram b0 |
| Default state | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Condition for default | POR | | | | | | | |
| 01 00 _ 011 P | Ram c7 | Ram c6 | Ram c5 | Ram c4 | Ram c3 | Ram c2 | Ram c1 | Ram c0 |
| Default state | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Condition for default | POR | | | | | | | |
| 01 00 _ 100 P | Ram d7 | Ram d6 | Ram d5 | Ram d4 | Ram d3 | Ram d2 | Ram d1 | Ram d0 |
| Default state | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Condition for default | POR | | | | | | | |

INIT REGISTERS

Note: these registers can be written only in INIT mode

Table 15. Initialization Regulator Registers, INIT REG (note: register can be written only in INIT mode)

| MOSI First Byte [15-8] [b_15 b_14] 0_0101 [P/N] | MOSI Second Byte, bits 7-0 | | | | | | | |
|--|----------------------------|-------------------------|-------------------------|-------------------------|-------------------------|---------------------|--------------|--------------|
| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 01 00 _ 101 P | I/Ox sync | V _{DDL} rst[1] | V _{DDL} rst[0] | V _{DD} rstD[1] | V _{DD} rstD[0] | V _{AUX5/3} | Cyclic on[1] | Cyclic on[0] |
| Default state | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Condition for default | POR | | | | | | | |

| Bit | Description |
|---------------|--|
| b7 | I/Ox sync - Determine if I/O-1 is sensed during I/O-0 activation, when cyclic sense function is selected |
| 0 | I/O-1 sense anytime |
| 1 | I/O-1 sense during I/O-0 activation |
| b6, b5 | V_{DDL} rst[1] V_{DDL} rst[0] - Select the V _{DD} Under-voltage threshold, to activate Reset terminal and/or INT |
| 00 | Reset at approx 0.9 V _{DD} . |
| 01 | INT at approx 0.9 V _{DD} , Reset at approx 0.7 V _{DD} |
| 10 | Reset at approx 0.7 V _{DD} |
| 11 | Reset at approx 0.9 V _{DD} . |
| b4, b3 | V_{DD} rstD[1] V_{DD} rstD[0] - Select the Reset terminal low lev duration, after V _{DD} rises above the V _{DD} under-voltage threshold |
| 00 | 1ms |
| 01 | 5ms |
| 10 | 10ms |
| 11 | 20ms |
| b2 | [V_{AUX} 5/3] - Select Vauxiliary output voltage |
| 0 | V _{AUX} = 3.3V |
| 1 | V _{AUX} = 5 |
| b1, b0 | Cyclic on[1] Cyclic on[0] - Determine if I/O-1 activation time, when cyclic sense function is selected |
| 00 | 200µs (typical value. ref to dynamic parameters for exact value) |
| 01 | 400µs (typical value. ref to dynamic parameters for exact value) |
| 10 | 800µs (typical value. ref to dynamic parameters for exact value) |
| 11 | 1600µs (typical value. ref to dynamic parameters for exact value) |

Table 16. Initialization Watchdog Registers, INIT W/D (note: register can be written only in INIT mode)

| MOSI First Byte [15-8] [b_15 b_14] 0_0110 [P/N] | MOSI Second Byte, bits 7-0 | | | | | | | |
|--|----------------------------|--------|--------|---------|-----------|-----------|----------|-------|
| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 01 00 _ 110 P | WD2INT | MCU_OC | OC-TIM | WD Safe | WD_spi[1] | WD_spi[0] | WD N/Win | Crank |
| Default state | 0 | 1 | 0 | | 0 | 0 | 1 | 0 |
| Condition for default | POR | | | | | | | |

| Bit | Description |
|---------------|---|
| b7 | WD2INT - Select the maximum time delay between INT occurrence and INT source read SPI command |
| 0 | Function disable. No constraint between INT occurrence and INT source read. |
| 1 | INT source read must occur before the remaining of the current W/D period plus 2 complete W/D periods. |
| b6, b5 | MCU_OC, OC-TIM - In Low Power V _{DD} ON, select watchdog refresh and V _{DD} current monitoring functionality. V _{DD_OC_LP} threshold is defined in device electrical parameters (approx 1.5mA) |
| | In low power mode, when W/D is not selected |
| no W/D + 00 | In Low Power V _{DD} ON Mode, V _{DD} over-current has no effect |
| no W/D + 01 | In Low Power V _{DD} ON Mode, V _{DD} over-current has no effect |
| no W/D + 10 | In Low Power V _{DD} ON Mode, V _{DD} current > V _{DD_OC_LP} threshold for a time > 100µs (typ) is a wakeup event |
| no W/D + 11 | In Low Power V _{DD} ON Mode, V _{DD} current > V _{DD_OC_LP} threshold for a time > I _{mcu_OC} is a wake-up event. I _{mcu_OC} time is selected in Timer register (selection range from 3 to 32ms) |
| | In low power mode when W/D is selected |
| W/D + 00 | In Low Power V _{DD} ON Mode, V _{DD} current > V _{DD_OC_LP} threshold has no effect. W/D refresh must occur by SPI command. |
| W/D + 01 | In Low Power V _{DD} ON Mode, V _{DD} current > V _{DD_OC_LP} threshold has no effect. W/D refresh must occur by SPI command. |
| W/D + 10 | In Low Power V _{DD} ON Mode, V _{DD} over-current for a time > 100µs (typ) is a wake-up event. |
| W/D + 11 | In Low Power V _{DD} ON Mode, V _{DD} current > V _{DD_OC_LP} threshold for a time < I _{mcu_OC} is a W/D refresh condition. V _{DD} current > V _{DD_OC_LP} threshold for a time > I _{mcu_OC} is wake-up event. I _{mcu_OC} time is selected in Timer register (selection range from 3 to 32ms) |
| b4 | WD Safe - Select the activation of the SAFE terminal low, at first or second consecutive RESET pulse |
| 0 | SAFE terminal is set low at the time of the RESET terminal low activation |
| 1 | SAFE terminal is set low at the second consecutive time RESET pulse |
| b3, b2 | WD_spi[1] WD_spi[0] - Select the Watchdog (W/D) Operation |
| 00 | Simple Watchdog selection: W/D refresh done by a 8bits or 16 bits SPI |
| 01 | Enhanced 1: Refresh is done using the Random Code, and by a single 16 bits. |
| 10 | Enhanced 2: Refresh is done using the Random Code, and by two 16 bits command. |
| 11 | Enhanced 4: Refresh is done using the Random Code, and by four 16 bits command. |
| b1 | WD N/Win - Select the Watchdog (W/D) Window or Time out operation |
| 0 | Watchdog operation is TIME OUT, W/D refresh can occur anytime in the period |
| 1 | Watchdog operation is WINDOW, W/D refresh must occur in the open window (second half of period) |
| b0 | Crank - Select the V _{sup1} threshold to disable V _{dd} , while V _{sup1} is falling toward gnd |
| 0 | V _{dd} disable when V _{sup1} is below typ 4V (parameter V _{sup-th1}), and device in Reset mode |
| 1 | V _{dd} kept ON when V _{sup1} is below typ4V (parameter V _{sup_th1}) |

Table 17. Initialization LIN and I/O registers, INIT LIN I/O (note: register can be written only in INIT mode)

| MOSI First Byte [15-8] [b_15 b_14] 0_0111 [P/N] | MOSI Second Byte, bits 7-0 | | | | | | | |
|--|----------------------------|-----------|-----------|-----------|-----------|--------------|--------------|---------|
| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 01 00 _ 111 P | I/O-1 ovsf | LIN_T1[1] | LIN_T1[0] | LIN_T0[1] | LIN_T0[0] | I/O-1 out-en | I/O-0 out-en | Cyc_Inv |
| Default state | 0 | 0 | 0 | | 0 | 0 | 0 | 0 |
| Condition for default | POR | | | | | | | |

| Bit | Description |
|---------------|---|
| b7 | I/O-1 ovsf - Select the deactivation of I/O-1 in case V_{DD} or V_{AUX} over voltage condition is detected |
| 0 | Disable I/O-1 turn off. |
| 1 | Enable I/O-1 turn off, in case V_{DD} or V_{AUX} over-voltage condition is detected. |
| b6, b5 | LIN_T1[1], LIN_T1[1] - Select Terminal operation as LIN Master Terminal switch or I/O |
| 00 | Terminal is OFF |
| 01 | Terminal operation as LIN Master Terminal switch |
| 10 | Terminal operation as I/O: high side switch and wake-up input |
| 11 | N/A |
| b4, b3 | LIN_T0[1], LIN_T0[1] - Select Terminal operation as LIN Master Terminal switch or I/O |
| 00 | Terminal is OFF |
| 01 | Terminal operation as LIN Master Terminal switch |
| 10 | Terminal operation as I/O: high side switch and wake-up input |
| 11 | N/A |
| b2 | I/O-1 out-en - Select the operation of the I/O-1 as output driver (high side, low side) |
| 0 | Disable high side and low side drivers of terminal I/O-1. I/O-1 can only be used as input. |
| 1 | Enable high side and low side drivers of terminal I/O-1. Terminal can be used as input and output driver. |
| b1 | I/O-0 out-en - Select the operation of the I/O-0 as output driver (high side, low side) |
| 0 | Disable high side and low side drivers of terminal I/O-0. I/O-0 can only be used as input. |
| 1 | Enable high side and low side drivers of terminal I/O-0. Terminal can be used as input and output driver. |
| b0 | Cyc_Inv - Select I/O-0 operation in device Low Power mode, when cyclic sense is selected |
| | During cyclic sense active time, I/O is set to the same state prior to enter in low power mode. During cyclic sense off time, I/O-0 is disable (high side and low side drivers OFF). |
| | During cyclic sense active time, I/O is set to the same state prior to enter in low power mode. During cyclic sense on time, I/O-0 is actively set to the opposite (High side or low side driver is turned on). |

Table 18. Initialization Miscellaneous Functions, INIT MISC (note: register can be written only in INIT mode)

| MOSI First Byte [15-8] [b_15 b_14] 0_1000 [P/N] | MOSI Second Byte, bits 7-0 | | | | | | | |
|--|----------------------------|------------|-----------|-----------|-----------|------------|------------|------------|
| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 01 01_000 P | LPM w RND | SPI parity | INT pulse | INT width | INT flash | Dbg Res[2] | Dbg Res[1] | Dbg Res[0] |
| Default state | 0 | 0 | 0 | | 0 | 0 | 0 | 0 |
| Condition for default | POR | | | | | | | |

| Bit | Description |
|-------------------|--|
| b7 | LPM w RND - Select the functionality to change mode (enter in Low Power) using the device Random Code |
| 0 | Function disable: the Low Power mode can be entered without usage of Random Code |
| 1 | Function enabled: the Low Power mode is entered using the Random Code |
| b6 | SPI parity - Select usage of the parity bit in SPI write operation |
| 0 | Function disable: the parity is not used. The parity bit must always set to logic 0. |
| 1 | Function enable: the parity is used, and parity must be calculated. |
| b5 | INT pulse -Select INT terminal operation: low level pulse or low level |
| 0 | INT terminal will assert a low level pulse, duration selected by bit [b4] |
| 1 | INT terminal assert a permanent low level (no pulse) |
| b4 | INT width - Select the INT pulse duration |
| 0 | INT pulse duration is typ 100µs. Ref to dynamic parameter table for exact value. |
| 1 | INT pulse duration is typ 25µs. Ref to dynamic parameter table for exact value. |
| b3 | INT flash - Select INT pulse generation at 50% of the Watchdog Period in Flash mode |
| | Function disable |
| | Function enable: an INT pulse will occur at 50% of the Watchdog Period when device in flash mode. |
| b2, b1, b0 | Dbg Res[2], Dbg Res[1], Dbg Res[0] - Allow verification of the external resistor connected at DBG terminal. Ref to parametric table for resistor range value. |
| 0xx | Function disable |
| 100 | 100 verification enable: resistor at DBG terminal is typ 68kohms (RB3) - Selection of SAFE mode B3 |
| 101 | 101 verification enable: resistor at DBG terminal is typ 33kohms (RB2) - Selection of SAFE mode B2 |
| 110 | 110 verification enable: resistor at DBG terminal is typ 15kohms (RB1) - Selection of SAFE mode B1 |
| 111 | 111 verification enable: resistor at DBG terminal is typ 0kohms (RA) - Selection of SAFE mode A |

Notes

23. Bits b2,1 and 0 allow the following operation:
First, check the resistor device has detected at the Debug pin. If the resistor is different, bit 5 (Debug resistor) is set in INTerrupt register (ref to device flag table).
Second, over write the resistor decoded by device, to set the SAFE mode operation by SPI. Once this function is selected by bit 2 =1, this selection has higher priority than “hardware”, and device will behave according to b2,b1 and b0 setting

.SPECIFIC MODE REGISTER

Table 19. Specific Mode Register, SPE_MODE

| MOSI First Byte [15-8] [b_15 b_14] 01_001 [P/N] | MOSI Second Byte, bits 7-0 | | | | | | | |
|--|----------------------------|------------|---------|---------|---------|---------|---------|---------|
| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 01 01_ 001 P | Sel_Mod[1] | Sel_Mod[0] | Rnd_C5b | Rnd_C4b | Rnd_C3b | Rnd_C2b | Rnd_C1b | Rnd_C0b |
| Default state | 0 | 0 | 0 | | 0 | 0 | 0 | 0 |
| Condition for default | POR | | | | | | | |

| Bit | Description |
|----------------|--|
| b7, b6 | Sel_Mod[1], Sel_Mod[0] - Mode selection: these 2 bits are used to select which mode the device will enter upon a SPI command. |
| 00 | RESET mode |
| 01 | INIT mode |
| 10 | FLASH mode |
| 11 | N/A |
| b5...b0 | [Rnd_C4b... Rnd_C0b] - Random Code inverted, these 6 bits are the inverted bits obtained from the SPE-MODE Register read command. |

The SPE MODE register is used for the following operation:

- Set the device in RESET mode, to exercise or test the RESET functions.
- Go to INIT mode, using the Secure SPi command.
- Go to FLASH mode (in this mode the watchdog timer can be extended up to 32s).
- Activate the SAFE terminal by S/W.

These mode (called Special Mode) are accessible via secured SPI command, which consist in 2 commands:

- 1) reading a random code and
- 2) then write the inverted random code plus mode selection or SAFE pin activation:

Return to INIT mode is done as follow (this is done from Normal mode only):

- 1) Read random code:
 MOSI : 0001 0011 0000 0000 [Hex:0x 13 00]
 MISO report 16 bits, random code are bits (5-0)
 miso = xxxx xxxx xxR5 R4 R3 R2 R1 R0 (Rx= 6 bits random code)

- 2) Write INIT mode + random code inverted
 MOSI : 0101 0010 01 Ri5 Ri4 Ri3 Ri2 Ri1 Ri0 [Hex 0x 52 HH] (Rix= random code inverted)

MISO : xxxx xxxx xxxx xxxx (don't care)
 SAFE pin activation: SAFE pin can be set low, only in INIT mode, with following commands:

- 1) Read random code:
 MOSI : 0001 0011 0000 0000 [Hex:0x 13 00]
 MISO report 16 bits, random code are bits (5-0)
 miso = xxxx xxxx xxR5 R4 R3 R2 R1 R0 (Rx= 6 bits random code)
- 2) Write INIT mode + random code bits 5:4 not inverted and random code bits 3:0 inverted
 MOSI : 0101 0010 01 R5 R4 Ri3 Ri2 Ri1 Ri0 [Hex 0x 52 HH] (Rix= random code inverted)
 MISO : xxxx xxxx xxxx xxxx (don't care)

Return to RESET or FLASH mode is done similarly to the go to INIT mode, except that the b7, b6 are set according to table above (b7, b6 = 00 - go to reset, b7, b6 = 10 - go to FLASH).

TIMER REGISTERS

Table 20. Timer Register A, Low Power Vdd over current & Watchdog Period Normal mode, TIM_A

| MOSI First Byte [15-8] [b_15 b_14] 01_010 [P/N] | MOSI Second Byte, bits 7-0 | | | | | | | |
|--|----------------------------|----------|----------|------------|----------|------------|----------|------------|
| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 01 01_ 010 P | I_mcu[2] | I_mcu[1] | I_mcu[1] | W/D Nor[4] | W/D_N[4] | W/D_Nor[3] | W/D_N[2] | W/D_Nor[0] |
| Default state | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| Condition for default | POR | | | | | | | |

| Low Power Vdd over current (ms) | | | | |
|---------------------------------|---------|----|----|----|
| b7 | b6, b5 | | | |
| | 00 | 01 | 10 | 11 |
| 0 | 3 (def) | 6 | 12 | 24 |
| 1 | 4 | 8 | 16 | 32 |

| Watchdog Period in Device Normal Mode (ms) | | | | | | | | |
|--|------------|-----|-----|-----|-----|-----|-----------|-----|
| b4, b3 | b2, b1, b0 | | | | | | | |
| | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
| 00 | 2.5 | 5 | 10 | 20 | 40 | 80 | 160 | 320 |
| 01 | 3 | 6 | 12 | 24 | 48 | 96 | 192 | 384 |
| 10 | 3.5 | 7 | 14 | 28 | 56 | 112 | 224 | 448 |
| 11 | 4 | 8 | 16 | 32 | 64 | 128 | 256 (def) | 512 |

Table 21. Timer Register B, Cyclic Sense and Cyclic INT, in Device Low Power Mode, TIM_B

| MOSI First Byte [15-8] [b_15 b_14] 01_011 [P/N] | MOSI Second Byte, bits 7-0 | | | | | | | |
|--|----------------------------|------------|------------|------------|------------|------------|------------|------------|
| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 01 01_ 011 P | Cyc-sen[3] | Cyc-sen[2] | Cyc-sen[1] | Cyc-sen[0] | Cyc-int[3] | Cyc-int[2] | Cyc-int[1] | Cyc-int[0] |
| Default state | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Condition for default | POR | | | | | | | |

| Cyclic sense (ms) | | | | | | | | |
|-------------------|------------|-----|-----|-----|-----|-----|-----|-----|
| b7 | b6, b5, b4 | | | | | | | |
| | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
| 0 | 3 | 6 | 12 | 24 | 48 | 96 | 192 | 384 |
| 1 | 4 | 8 | 16 | 32 | 64 | 128 | 256 | 512 |

| Cyclic Interrupt (ms) | | | | | | | | |
|-----------------------|------------|-----|-----|-----|-----|-----|-----|------|
| b3 | b2, b1, b0 | | | | | | | |
| | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
| 0 | 6 (def) | 12 | 24 | 48 | 96 | 192 | 384 | 768 |
| 1 | 8 | 16 | 32 | 64 | 128 | 258 | 512 | 1024 |

Table 22. Timer Register C, Watchdog LP Mode or Flash Mode and Forced Wake-up Timer, TIM_C

| MOSI First Byte [15-8] [b ₁₅ b ₁₄] 01_100 [P/N] | MOSI Second Byte, bits 7-0 | | | | | | | |
|---|----------------------------|------------|------------|------------|--------|--------|--------|--------|
| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 01 01_ 100 P | WD-LP-F[3] | WD-LP-F[2] | WD-LP-F[1] | WD-LP-F[0] | FWU[3] | FWU[2] | FWU[1] | FWU[0] |
| Default state | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Condition for default | POR | | | | | | | |

Table 23. Typical Timing Values

| Watchdog in Low Power V _{DD} ON Mode (in ms) | | | | | | | | |
|---|------------|-----|-----|-----|-----|-----|------|------|
| b7 | b6, b5, b4 | | | | | | | |
| | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
| 0 | 12 | 24 | 48 | 96 | 192 | 384 | 768 | 1536 |
| 1 | 16 | 32 | 64 | 128 | 256 | 512 | 1024 | 2048 |

| Watchdog in Flash Mode (in ms) | | | | | | | | |
|--------------------------------|------------|-----|------|------|------|------|-------|-------|
| b7 | b6, b5, b4 | | | | | | | |
| | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
| 0 | 48 (def) | 96 | 192 | 384 | 768 | 1536 | 3072 | 6144 |
| 1 | 256 | 512 | 1024 | 2048 | 4096 | 8192 | 16384 | 32768 |

| Forced Wake Up (in ms) | | | | | | | | |
|------------------------|------------|-----|-----|-----|------|------|------|------|
| b3 | b2, b1, b0 | | | | | | | |
| | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
| 0 | 48 (def) | 96 | 192 | 384 | 768 | 1536 | 3072 | 6144 |
| 1 | 64 | 128 | 258 | 512 | 1024 | 2048 | 4096 | 8192 |

WATCHDOG AND MODE REGISTERS

Table 24. Watchdog refresh register, W/D

| MOSI First Byte [15-8] [b_15 b_14] 01_101 [P/N] | MOSI Second Byte, bits 7-0 | | | | | | | |
|--|----------------------------|-------|-------|-------|-------|-------|-------|-------|
| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 01 01_ 101 P | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Default state | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Condition for default | POR | | | | | | | |

Notes

24. The Simple Watchdog Refresh command is in hexadecimal: 5A00. This command is used to refresh the W/D and also to transition from INIT mode to Normal Mode, and from Normal Request Mode to Normal mode (after a wake up of a reset)

Table 25. MODE Register, MODE

| MOSI First Byte [15-8] [b_15 b_14] 01_110 [P/N] | MOSI Second Byte, bits 7-0 | | | | | | | |
|--|----------------------------|---------|---------|---------|---------|----------|----------|----------|
| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 01 01_ 110 P | Mode[4] | Mode[3] | Mode[2] | Mode[1] | Mode[0] | Rnd_b[2] | Rnd_b[1] | Rnd_b[0] |
| Default state | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |

| Low Power Vdd OFF selection and FWU / Cyclic Sense selection | | |
|--|-----|--------------|
| b7, b6, b5, b4, b3 | FWU | Cyclic Sense |
| 0 1100 | off | off |
| 0 1101 | off | ON |
| 0 1110 | ON | off |
| 0 1111 | ON | ON |

Table 26.

| Low Power Vdd ON selection and operation mode | | | | |
|---|---|--------------|------------|----------|
| b7, b6, b5, b4, b3 | FWU | Cyclic Sense | Cyclic INT | Watchdog |
| 1 0000 | off | off | off | off |
| 1 0001 | off | off | off | ON |
| 1 0010 | off | off | ON | off |
| 1 0011 | off | off | ON | ON |
| 1 0100 | off | ON | off | off |
| 1 0101 | off | ON | off | ON |
| 1 0110 | off | ON | ON | off |
| 1 0111 | off | ON | ON | ON |
| 1 1000 | ON | off | off | off |
| 1 1001 | ON | off | off | ON |
| 1 1010 | ON | off | ON | off |
| 1 1011 | ON | off | ON | ON |
| 1 1100 | ON | ON | off | off |
| 1 1101 | ON | ON | off | ON |
| 1 1110 | ON | ON | ON | off |
| 1 1111 | ON | ON | ON | ON |
| b2, b1, b0 | Random Code inverted, these 3bits are the inverted bits obtained from the previous SPI command. | | | |

Prior to enter in LP Vdd ON or LP Vdd OFF, the wake up flags must be cleared or read.

This is done by the following SPI commands: 0xE100 and 0xE380 for CAN and I/O wake up respectively. Ref to table “Device Flag, I/O real time and Device Identification” for details.

If wake up flags are not cleared, device will enter in selected LP mode but will wake up immediately. When the device is in LP Vdd ON mode, the wake up by SPI command uses a write to “Normal Request Mode”, 0x5C10.

Mode Register Features

The mode register include specific function and “global SPI command” that allow the following:

- read device current mode
- read device Debug status
- read state of SAFE terminal
- leave Debug state
- release or turn off SAFE terminal

These global commands are built using the MODE register address bit [13-9], along with several combinations of bit [15-14] and bit [7]. Note that bit [8] is always set to 1.

The table below summarize these commands

Table 27. Device Modes

| Global commands and effects | | | | | | | | |
|--|------|------------|-----------|---------------------|-------|-------------|-------|-------|
| Read device current Mode, Leave debug mode. Keep SAFE terminal as is. MOSI in hexadecimal: 1D 00 | MOSI | bits 15-14 | bits 13-9 | bit 8 | bit 7 | bits 6-0 | | |
| | | 00 | 01 110 | 1 | 0 | 000 0000 | | |
| | MISO | bit 15-8 | | bit 7-3 | | bit 2-0 | | |
| | | Fix Status | | device current mode | | Random code | | |
| Read device current mode Release SAFE terminal (turn OFF). MOSI in hexadecimal: 1D 80 | MOSI | bits 15-14 | bits 13-9 | bit 8 | bit 7 | bits 6-0 | | |
| | | 00 | 01 110 | 1 | 1 | 000 0000 | | |
| | MISO | bit 15-8 | | bit 7-3 | | bit 2-0 | | |
| | | Fix Status | | device current mode | | Random code | | |
| Read device current Mode, Leave debug mode. Keep SAFE terminal as is. MOSI in hexadecimal: DD 00 MISO reports Debug and SAFE state (bits 1,0) | MOSI | bits 15-14 | bits 13-9 | bit 8 | bit 7 | bits 6-0 | | |
| | | 11 | 01 110 | 1 | 0 | 000 0000 | | |
| | MISO | bit 15-8 | | bit 7-3 | | bit 2 | bit 1 | bit 0 |
| | | Fix Status | | device current mode | | X | SAFE | DEBUG |
| Read device current mode, Keep DEBUG mode Release SAFE terminal (turn OFF). MOSI in hexadecimal: DD 80 MISO reports Debug and SAFE state (bits 1,0) | MOSI | bits 15-14 | bits 13-9 | bit 8 | bit 7 | bits 6-0 | | |
| | | 11 | 01 110 | 1 | 1 | 000 0000 | | |
| | MISO | bit 15-8 | | bit 7-3 | | bit 2 | bit 1 | bit 0 |
| | | Fix Status | | device current mode | | X | SAFE | DEBUG |

Tables below describe the meaning of MISO bits 7-0, that allow to decode the device current mode.

Table below describes the SAFE and DEBUG bit decoding.

Table 28. MISO bits 7-0

| Device current mode, any of the above command | |
|---|----------------|
| b7, b6, b5, b4, b3 | MODE |
| 0 0000 | INIT |
| 0 0001 | FLASH |
| 0 0010 | Normal Request |
| 0 0011 | Normal mode |

Table 29. SAFE and DEBUG status

| SAFE and DEBUG bits | |
|---------------------|----------------------------------|
| b1 | description |
| 0 | SAFE terminal OFF, not activated |
| 1 | FLASH |
| b0 | |
| 0 | DEBUG mode OFF |
| 1 | DEBUG mode Active |

.REGULATOR, CAN, I/O, INT AND LIN REGISTERS

Table 30. (25)REGULATOR register, REG

| MOSI First Byte [15-8] [b_15 b_14] 01_111 [P/N] | MOSI Second Byte, bits 7-0 | | | | | | | |
|--|----------------------------|----------------------|-------|-----------|-----------|------------------------|--------------------------|------------------------|
| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 01 01_ 111 P | V _{AUX} [1] | V _{AUX} [0] | - | 5V-can[1] | 5V-can[0] | V _{DD} bal en | V _{DD} bal auto | V _{DD} off en |
| Default state | 0 | 0 | N/A | 0 | 0 | N/A | N/A | N/A |
| Condition for default | POR | | | POR | | | | |

| Bits | Description |
|--------------|---|
| b7 b6 | V_{AUX}[1], V_{AUX}[0] - Vauxiliary regulator control |
| 00 | Regulator OFF |
| 01 | Regulator ON. Under-voltage (UV) and Over-current (OC) monitoring flags not reported. V _{AUX} disable in case UV or UV detected after 1.0ms blanking time. |
| 10 | Regulator ON. Under-voltage (UV) and Over-current (OC) monitoring flags active. V _{AUX} disable in case UV or UV detected after 1.0ms blanking time. |
| 11 | Regulator ON. Under-voltage (UV) and Over-current (OC) monitoring flags active. V _{AUX} disable in case UV or UV detected after 25µs blanking time. |
| b4 b3 | 5V-can[1], 5V-can[0] - 5V-CAN regulator control |
| 00 | Regulator OFF |
| 01 | Regulator ON. Thermal protection active. Under-voltage (UV) and Over-current (OC) monitoring flags not reported. |
| 10 | Regulator ON. Thermal protection active. Under-voltage (UV) and Over-current (OC) monitoring flags active. |
| 11 | Regulator ON. Thermal protection active. Under-voltage (UV) and Over-current (OC) monitoring flags active. 5V-CAN disable in case UV or UV detected after 25µs blanking time. |
| b2 | V_{DD} bal en - Control bit to Enable the V _{DD} external ballast transistor |
| 0 | External V _{DD} ballast disable |
| 1 | External V _{DD} ballast Enable |
| b1 | V_{DD} bal auto - Control bit to automatically Enable the V _{DD} external ballast transistor, if V _{DD} is > typ 60mA |
| 0 | Disable the automatic activation of the external ballast |
| 1 | Enable the automatic activation of the external ballast, if V _{DD} > typ 60mA |
| b0 | V_{DD} off en - Control bit to allow transition into Low Power V _{DD} OFF Mode (to prevent V _{DD} turn OFF) |
| 0 | Disable Usage of Low Power V _{DD} OFF Mode |
| 1 | Enable Usage of Low Power V _{DD} OFF Mode |

Notes

25. The first time the device is set in Normal mode, the CAN is in Sleep wake-up enable (10). The next time the device is set in Normal mode, the CAN state is controlled by the bit 7 and bit6 states.

Table 31. CAN Register, CAN

| MOSI First byte [15-8] [b_15 b_14] 10_000 [P/N] | MOSI Second Byte, bits 7-0 | | | | | | | |
|--|----------------------------|------------|---------|---------|-------------|-------|-------|---------|
| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 01 10_000P | CAN mod[1] | CAN mod[0] | Slew[1] | Slew[0] | Wake up 1/3 | - | - | CAN int |
| Default state | 1 | 0 | 0 | 0 | 0 | - | - | 0 |
| Condition for default | note | | POR | | POR | | | POR |

| Bits | Description |
|--------------|--|
| b7 b6 | CAN mod[1], CAN mod[0] - CAN interface mode control, wake-up enable / disable |
| 00 | CAN interface in Sleep Mode, CAN wake-up disable. |
| 01 | CAN interface in receive only mode, CAN driver disable. |
| 10 | CAN interface is in Sleep Mode, CAN wake-up enable. In device low power mode, CAN wake-up is reported by device wake-up. In device normal mode, CAN wake-up reported by INT. |
| 11 | CAN interface in transmit and receive mode. |
| b5 b4 | Slew[1] Slew[0] - CAN driver slew rate selection |
| 00 | FAST |
| 01 | MEDIUM |
| 10 | SLOW |
| 11 | SLOW |
| b3 | Wake-up 1/3 - Selection of CAN wake-up mechanism |
| 0 | 3 dominant pulses wake-up mechanism |
| 1 | Single dominant pulse wake-up mechanism |
| b0 | CAN INT - Select the CAN failure detection reporting |
| 0 | Select INT generation when a bus failure is fully identified and decoded (i.e after 5 dominant pulses on TxCAN) |
| 1 | Select INT generation as soon as a bus failure is detected, event if not fully identified |

Table 32. I/O Register, I/O

| MOSI First byte [15-8] [b_15 b_14] 10_001 [P/N] | MOSI Second Byte, bits 7-0 | | | | | | | |
|--|----------------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 01 10_001P | I/O-3 [1] | I/O-3 [0] | I/O-2 [1] | I/O-2 [0] | I/O-1 [1] | I/O-1 [0] | I/O-0 [1] | I/O-0 [0] |
| Default state | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Condition for default | POR | | | | | | | |

| Bits | Description |
|--------------|--|
| b7 b6 | I/O-3 [1], I/O-3 [0] - I/O-3 terminal operation |
| 00 | I/O-3 driver disable, Wake-up capability disable |
| 01 | I/O-3 driver disable, Wake-up capability enable. |
| 10 | I/O-3 High Side driver enable. |
| 11 | I/O-3 High Side driver enable. |
| b5 b4 | I/O-2 [1], I/O-2 [0] - I/O-2 terminal operation |
| 00 | I/O-2 driver disable, Wake-up capability disable |
| 01 | I/O-2 driver disable, Wake-up capability enable. |
| 10 | I/O-2 High Side driver enable. |
| 11 | I/O-2 High Side driver enable. |
| b3 b2 | I/O-1 [1], I/O-1 [0] - I/O-1 terminal operation |
| 00 | I/O-1 driver disable, Wake-up capability disable |
| 01 | I/O-1 driver disable, Wake-up capability enable. |
| 10 | I/O-1 Low Side driver enable. |
| 11 | I/O-1 High Side driver enable. |
| b1 b0 | I/O-0 [1], I/O-0 [0] - I/O-0 terminal operation |
| 00 | I/O-0 driver disable, Wake-up capability disable |
| 01 | I/O-0 driver disable, Wake-up capability enable. |
| 10 | I/O-0 Low Side driver enable. |
| 11 | I/O-0 High Side driver enable. |

Table 33. INT Register, INT

| MOSI First byte [15-8] [b_15 b_14] 10_010 [P/N] | MOSI Second Byte, bits 7-0 | | | | | | | |
|--|----------------------------|---------|-----------|----------|-------|-------|-------|-------|
| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 01 10_010P | CAN failure | MCU req | LIN1 fail | LIN0fail | I/O | SAFE | - | Vmon |
| Default state | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Condition for default | POR | | | | | | | |

| Bits | Description |
|-----------|---|
| b7 | CAN failure - control bit for CAN failure INT (CANH/L to GND, VDD or VSUP, CAN over-current, Driver Over Temp, TX-PD, RX-PR, RX2HIGH, and CANBUS Dominate clamp) |
| 0 | INT disable |
| 1 | INT enable. |
| b6 | MCU req - Control bit to request an INT. INT will occur once when the bit is enable |
| 0 | INT disable |
| 1 | INT enable. |
| b5 | not implemented in MC33904 |
| 0 | INT disable |
| 1 | INT enable. |
| b4 | not implemented in MC33904 |
| 0 | INT disable |
| 1 | INT enable. |
| b3 | I/O - Bit to control I/O interruption: I/O Wake-up |
| 0 | INT disable |
| 1 | INT enable. |
| b2 | SAFE - description to be done |
| 0 | INT disable |
| 1 | INT enable. |
| b0 | Vmon - enable interruption by voltage monitoring of one of the voltage regulator: V_{AUX} , 5V-CAN, V_{DD} (IDD Over-current, VDD_Temp_prewarning), VSUV, VSOV, VSENSElow, 5V-CAN low or thermal shutdown, V_{AUX} low or V_{AUX} over-current |
| 0 | INT disable |
| 1 | INT enable. |

Table 34. LIN 1 Register, LIN1

| MOSI First byte [15-8] [b_15 b_14] 10_010 [P/N] | MOSI Second Byte, bits 7-0 | | | | | | | |
|--|----------------------------|-------------|--------------|--------------|-------|-----------|-------|----------|
| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 01 10_ 011P | LIN mode[1] | LIN mode[0] | Slew rate[1] | Slew rate[0] | - | LIN T1 on | - | Vsup ext |
| Default state | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Condition for default | POR | | | | | | | |

| Bits | Description |
|--------------|---|
| b7 b6 | LIN mode [1], LIN mode [0] - LIN 1 interface mode control, wake-up enable / disable |
| 00 | LIN1 disable, wake-up capability disable |
| 01 | not used |
| 10 | LIN1 disable, wake-up capability enable |
| 11 | LIN1 Transmit Receive mode |
| b5 b4 | Slew rate[1], Slew rate[0] LIN 1 slew rate selection |
| 00 | Slew rate for 20kbit/s baud rate |
| 01 | Slew rate for 10kbit/s baud rate |
| 10 | Slew rate for fast baud rate |
| 11 | Slew rate for fast baud rate |
| b2 | LIN T1 on |
| 0 | LIN 1 termination OFF |
| 1 | LIN 1 termination ON |
| b0 | Vsup ext |
| 0 | LIN goes recessive when device Vsup2 is below typ 6V. This is to meet J2602 specification |
| 1 | LIN continues operation below Vsup2 6V, until 5V-CAN is disabled. |

Table 35. LIN 2 Register, LIN2

| MOSI First byte [15-8] [b_15 b_14] 10_010 [P/N] | MOSI Second Byte, bits 7-0 | | | | | | | |
|--|----------------------------|-------------|--------------|--------------|-------|-----------|-------|----------|
| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 01 10_ 100P | LIN mode[1] | LIN mode[0] | Slew rate[1] | Slew rate[0] | - | LIN T2 on | - | Vsup ext |
| Default state | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Condition for default | POR | | | | | | | |

| Bits | Description |
|--------------|---|
| b7 b6 | LIN mode [1], LIN mode [0] - LIN 2 interface mode control, wake-up enable / disable |
| 00 | LIN2 disable, wake-up capability disable |
| 01 | not used |
| 10 | LIN2 disable, wake-up capability enable |
| 11 | LIN2 Transmit Receive mode |
| b5 b4 | Slew rate[1], Slew rate[0] LIN 2slew rate selection |
| 00 | Slew rate for 20kbit/s baud rate |
| 01 | Slew rate for 10kbit/s baud rate |
| 10 | Slew rate for fast baud rate |
| 11 | Slew rate for fast baud rate |
| b2 | LIN T2 on |
| 0 | LIN 2 termination OFF |
| 1 | LIN 2 termination ON |
| b0 | Vsup ext |
| 0 | LIN goes recessive when device Vsup2 is below typ 6V. This is to meet J2602 specification |
| 1 | LIN continues operation below Vsup2 6V, until 5V-CAN is disabled. |

FLAGS

DESCRIPTION

The table below is the summary of the device flags, I/O real time level and device Identification. They are obtained using the following commands.

This command is composed of the following:

bits 15 and 14: [1 1] for failure flags, or [0 0] for I/O real time status or device identification.

- bit 13 to 9 are the register address from which the flags is to be read.
- bit 8 = 1 (this is not parity bit function, as this is a read command).

Table 36. Device Flag, I/O real time and Device Identification

| Bits | 15-14 | 13-9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|--|------------------|-------|-------|---|-------------------------------|--------------------------|-----------------------------------|-------------------------|---------------------------------|---------------------------------|---|
| MOSI | MOSI bits 15-7 | | | | Next 6 MOSI bits (bits 6.0) should be "000_0000" | | | | | | | |
| | bits [15, 14] | Address [13-9] | bit 8 | bit 7 | | | | | | | | |
| MISO | 8 Bits Device Fixed Status (bits 15...8) | | | | MISO bits [7-0], device response on MISO terminal | | | | | | | |
| | | | | | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| REG | 11 | 0_1111 REG | 1 | 0 | V _{AUX_low} | V _{AUX_over-current} | 5V-can_ Thermal shutdown | 5V-can_ UV | 5V-can_ over-current | V _{SENSE_low} | V _{SUP_ Under-voltage} | I _{DD-OC-NORMAL mode} |
| | 11 | | | 1 | - | - | - | V _{DD_ Thermal shutdown} | | R _{ST_low (<100ms)} | V _{SUP_ batfail} | I _{DD-OC-LP V_{DDon mode}} |
| Hexa SPI commands to get Vreg Flags: MOSI Ox DF 00, and MOSI Ox DF 80 | | | | | | | | | | | | |
| CAN | 11 | 1_0000 CAN | 1 | 0 | CAN wake-up | - | CAN Over-temp | RxD low | RxD high | TxD dom | Bus Dom clamp | CAN Over-current |
| | | | | 1 | CAN_UF | CAN_F | CANL to V _{BAT} | CANL to V _{DD} | CANL to GND | CANH to V _{BAT} | CANH to V _{DD} | CANH to GND |
| Hexa SPI commands to get CAN Flags: MOSI Ox E1 00, and MOSI Ox E1 80 | | | | | | | | | | | | |
| I/O | 11 | 1_0001 I/O | 1 | 0 | HS3 short to GND | HS2 short to GND | SPI parity error | CSB low >2ms | V _{SUP2-UV} | V _{SUP1-OV} | I/O-O thermal | W/D flash mode 50% |
| | | | | 1 | I/O-1-3 wake-up | I/O-0-2 wake-up | SPI wake-up | FWU | INT service Timeout | Low Power V _{DD OFF} | Reset request | Hardware Leave Debug |
| Hexa SPI commands to get I/O Flags and I/O wake up: MOSI Ox E3 00, and MOSI Ox E3 80 | | | | | | | | | | | | |
| | 00 | 1_0001 I/O | 1 | 1 | | I/O-3 state | | I/O-2 state | | I/O-1 state | | I/O-0 state |
| Hexa SPI commands to get I/O real time level: MOSI Ox 23 00 | | | | | | | | | | | | |
| INT | 11 | 1_0010 Interrupt | 1 | 0 | INT request | RST high | DBG resistor | V _{DD temp Prewarning} | V _{DD UV} | V _{DD Over-voltage} | V _{AUX_over-voltage} | - |
| | | | | 1 | - | - | - | V _{DD low >100ms} | V _{DD low RST} | RST low >100ms | multiple Resets | W/D refresh failure |
| Hexa SPI commands to get INT Flags: MOSI Ox E5 00, and MOSI Ox E5 80 | | | | | | | | | | | | |
| | 00 | 1_0010 Interrupt | 1 | 1 | V _{dd (5V or 3.3V)} | device p/n 1 | device p/n 0 | id4 | id3 | id2 | id1 | id0 |
| Hexa SPI commands to get device Identification: MOSI Ox 25 10 MISO bit [7-0] = 1011 0001: MC33904, 5V version, silicon pass 3.0 MISO bit [7-0] = 1011 0010: MC33904, 5V version, silicon pass 3.1 | | | | | | | | | | | | |
| LIN1 | 11 | 1_0011 LIN 1 | 1 | 0 | - | LIN1 wake up | LIN1 Term short to gnd | LIN 1 Over-temp | RxD1 low | RxD1 high | TxD1 dom | LIN1 bus dom clamp |
| | | | | | Hexa SPI commands to get LIN 2 Flags: MOSI Ox E7 00 | | | | | | | |
| LIN2 | 11 | 1_0100 LIN 2 | 1 | 0 | - | LIN2 wake up | LIN2 Term short to gnd | LIN 2 Over-temp | RxD2 low | RxD2 high | TxD2 dom | LIN2 bus dom clamp |
| | | | | | Hexa SPI commands to get LIN 2 Flags: MOSI Ox E9 00 | | | | | | | |

Table 37. Flag Descriptions

| Flag | | Description |
|---|-----------------------|--|
| Vaux_low | Description | Reports that V _{AUX} regulator output voltage is lower than the V _{AUX-UV} threshold. |
| | Set / Reset condition | Set: V _{AUX} below threshold for t > 100µs typ. Reset: V _{AUX} above threshold and flag read (SPI) |
| Vaux_over-current | Description | Report that current out of V _{AUX} regulator is above V _{AUX-OC} threshold. |
| | Set / Reset condition | Set: Current above threshold for t > 100µs. Reset: Current below threshold and flag read by SPI. |
| 5V-can_Thermal shutdown | Description | Report that the 5V-can regulator has reached over temperature threshold. |
| | Set / Reset condition | Set: 5V-can thermal sensor above threshold. Reset: thermal sensor below threshold and flag read (SPI) |
| 5V-can_UV | Description | Reports that 5V-can regulator output voltage is lower than the 5V-can UV threshold. |
| | Set / Reset condition | Set: 5V-can below 5V-can UV for t > 100µs typ. Reset: 5V-can > threshold and flag read (SPI) |
| 5V-can_over-current | Description | Report that the CAN driver output current is above threshold. |
| | Set / Reset condition | Set: 5V-can current above threshold for t > 100µs. Reset: 5V-can current below threshold and flag read (SPI) |
| V _{SENSE-low} | Description | Reports that V _{sense} terminal is lower than the V _{sense low} threshold. |
| | Set / Reset condition | Set: V _{sense} below threshold for t > 100µs typ. Reset: V _{sense} above threshold and flag read (SPI) |
| V _{SUP-Under-voltage} | Description | Reports that V _{sup1} terminal is lower than the V _{sup1 low} resoled. |
| | Set / Reset condition | Set: V _{sup1} below threshold for t > 100µs typ. Reset: V _{sup1} above threshold and flag read (SPI) |
| I _{DD-OC-NORMAL mode} | Description | Report that current out of V _{dd} pin is higher that I _{dd-oc} threshold, while device is in Normal mode. |
| | Set / Reset condition | Set: current above threshold for t > 100µs typ. Reset; current below threshold and flag read (SPI) |
| V _{DD-Thermal shutdown} | Description | Report that the V _{dd} has reached over temperature threshold, and was turned off. |
| | Set / Reset condition | Set: V _{dd} off due to thermal condition. Reset: V _{dd} recover and flag read (SPI) |
| R _{ST-low (<100ms)} | Description | Report that the Reset pin has detected a low level, shorter than 100ms |
| | Set / Reset condition | Set: after detection of reset low pulse. Reset: Reset pulse terminated and flag read (SPI) |
| V _{SUP-batfail} | Description | Report that the device voltage at V _{sup1} pin was below BATFAIL threshold. |
| | Set / Reset condition | Set: V _{sup1} below BATFAIL. Reset: V _{sup1} above threshold, and flag read (SPI) |
| I _{DD-OC-LP V_{dd}on mode} | Description | Report that current out of V _{dd} pin is higher that I _{dd-oc} threshold LP, while device is in Low Power V _{DD} ON Mode. |
| | Set / Reset condition | Set: current above threshold for t > 100µs typ. Reset; current below threshold and flag read (SPI) |
| CAN wake-up | Description | Report that wake up source is CAN |
| | Set / Reset condition | Set: after CAN wake detected. Reset: Flag read (SPI) |
| CAN Over-temp | Description | Report that the CAN interface has reach over temperature threshold. |
| | Set / Reset condition | Set: CAN thermal sensor above threshold. Reset: thermal sensor below threshold and flag read (SPI) |
| RxD low | Description | Report that Rx pin is shorted to gnd. |
| | Set / Reset condition | Set: Rx low failure detected. Reset: failure recovered and flag read (SPI) |
| RxD high | Description | Report that Rx pin is shorted to recessive voltage. |
| | Set / Reset condition | Set: Rx high failure detected. Reset: failure recovered and flag read (SPI) |
| TxD dom | Description | Report that Tx pin is shorted to gnd. |
| | Set / Reset condition | Set: Tx low failure detected. Reset: failure recovered and flag read (SPI) |
| Bus Dom clamp | Description | Report that the CAN bus is dominant for a time longer than t _{DOM} |
| | Set / Reset condition | Set: Bus dominant clamp failure detected. Reset: failure recovered and flag read (SPI) |

Table 37. Flag Descriptions

| Flag | | Description |
|--------------------------|-----------------------|--|
| CAN Over-current | Description | Report that the CAN current is above CAN over current threshold. |
| | Set / Reset condition | Set: CAN current above threshold. Reset: current below threshold and flag read (SPI) |
| CAN_UF | Description | Report that the CAN failure detection has not yet identified the bus failure |
| | Set / Reset condition | Set: bus failure pre detection. Reset: CAN bus failure recovered and flag read |
| CAN_F | Description | Report that the CAN failure detection has identified the bus failure |
| | Set / Reset condition | Set: bus failure complete detection. Reset: CAN bus failure recovered and flag read |
| CANL to V _{BAT} | Description | Report CAN L short to Vbat failure |
| | Set / Reset condition | Set: failure detected. Reset failure recovered and flag read (SPI) |
| CANL to GND | Description | Report CAN L short to gnd failure |
| | Set / Reset condition | Set: failure detected. Reset failure recovered and flag read (SPI) |
| CANL to GND | Description | Report CAN L short to Vbat failure |
| | Set / Reset condition | Set: failure detected. Reset failure recovered and flag read (SPI) |
| CANH to V _{BAT} | Description | Report CAN H short to Vbat failure |
| | Set / Reset condition | Set: failure detected. Reset failure recovered and flag read (SPI) |
| CANH to GND | Description | Report CAN H short to gnd failure |
| | Set / Reset condition | Set: failure detected. Reset failure recovered and flag read (SPI) |
| CANH to GND | Description | Report CAN H short to Vbat failure |
| | Set / Reset condition | Set: failure detected. Reset failure recovered and flag read (SPI) |
| HS3 short to GND | Description | Report I/O-3 high side switch short to gnd failure |
| | Set / Reset condition | Set: failure detected. Reset failure recovered and flag read (SPI) |
| HS2 short to GND | Description | Report I/O-2 high side switch short to gnd failure |
| | Set / Reset condition | Set: failure detected. Reset failure recovered and flag read (SPI) |
| SPI parity error | Description | Report SPI parity error was detected. |
| | Set / Reset condition | Set: failure detected. Reset: flag read (SPI) |
| CSB low >2ms | Description | Report SPI CSB was low for a time longer than typ 2ms |
| | Set / Reset condition | Set: failure detected. Reset: flag read (SPI) |
| V _{SUP2-UV} | Description | Report that V _{SUP2} is below V _{SUP2-UV} threshold. |
| | Set / Reset condition | Set V _{SUP2} below V _{SUP2-UV} thresh. Reset V _{SUP2} > V _{SUPUV} thresh and flag read (SPI) |
| V _{SUP1-OV} | Description | Report that V _{SUP1} is above V _{SUP1-OV} threshold. |
| | Set / Reset condition | Set V _{SUP1} above V _{SUP1-OV} thresh. Reset V _{SUP1} < V _{SUPOV} thresh and flag read (SPI) |
| I/O-0 thermal | Description | Report that the I/O-0 high side switch has reach over temperature threshold. |
| | Set / Reset condition | Set: I/O-0 high side switch thermal sensor above threshold. Reset: thermal sensor below threshold and flag read (SPI) |
| W/D flash mode 50% | Description | Report that the W/D period has reach 50% of its value, while device is in Flash mode. |
| | Set / Reset condition | Set: W/D period > 50%. Reset: flag read |
| I/O-1-3 wake-up | Description | Report that wake up source is I/O-1 or I/O-3 |
| | Set / Reset condition | Set: after I/O-1 or I/O-3 wake detected. Reset: Flag read (SPI) |
| I/O-0-2 wake-up | Description | Report that wake up source is I/O-0 or I/O-2 |
| | Set / Reset condition | Set: after I/O-0 or I/O-2 wake detected. Reset: Flag read (SPI) |
| SPI wake-up | Description | Report that wake up source is SPI command, in Low Power V _{DD} ON Mode. |
| | Set / Reset condition | Set: after SPI Wake Up detected. Reset: Flag read (SPI) |

Table 37. Flag Descriptions

| Flag | | Description |
|---------------------------------|-----------------------|---|
| FWU | Description | Report that wake up source is Forced Wake Up |
| | Set / Reset condition | Set: after Forced Wake Up detected. Reset: Flag read (SPI) |
| INT service Timeout | Description | Report that INT time out error detected. |
| | Set / Reset condition | Set: INT service time out expired. Reset: flag read. |
| Low Power V _{DD} OFF | Description | Report that Low Power V _{DD} OFF Mode was selected, prior wake up occurred. |
| | Set / Reset condition | Set: Low Power V _{DD} OFF selected. Reset: Flag read (SPI) |
| Reset request | Description | Report that RST source is an request from a SPI command (go to RST mode). |
| | Set / Reset condition | Set: After reset occurred due to SPI request. Reset: flag read (SPI) |
| Hardware Leave Debug | Description | Report that the device left the Debug mode due to Hardware cause (voltage at DBG pin lower than typ 8V). |
| | Set / Reset condition | Set: device leave debug mode due to Hardware cause. Reset: flag read. |
| INT request | Description | Report that INT source is an INT request from a SPI command. |
| | Set / Reset condition | Set: INT occurred. Reset: flag read (SPI) |
| RST high | Description | Report that RST pin is shorted to high voltage. |
| | Set / Reset condition | Set: RST failure detection. Reset: flag read. |
| DBG resistor | Description | Report that the resistor at DBG pin is different from expected (different from SPI register content). |
| | Set / Reset condition | Set: failure detected. Reset: correct resistor and flag read (SPI). |
| V _{DD} temp Prewarning | Description | Report that the V _{DD} has reached over temperature pre warning threshold. |
| | Set / Reset condition | Set: V _{DD} thermal sensor above threshold. Reset: V _{DD} thermal sensor below threshold and flag read (SPI) |
| V _{DD} UV | Description | Reports that V _{DD} terminal is lower than the V _{DD} UV threshold. |
| | Set / Reset condition | Set: V _{DD} below threshold for t >100μs typ. Reset: V _{DD} above threshold and flag read (SPI) |
| V _{DD} Over-voltage | Description | Reports that V _{DD} terminal is higher than the typ V _{DD} + 0.6V threshold. I/O-1 can be turned OFF if this function is selected in INIT register. |
| | Set / Reset condition | Set: V _{DD} above threshold for t >100μs typ. Reset: V _{DD} below threshold and flag read (SPI) |
| V _{AUX} _over-voltage | Description | Reports that V _{AUX} terminal is higher than the typ V _{AUX} + 0.6V threshold. I/O-1 can be turned OFF if this function is selected in INIT register. |
| | Set / Reset condition | Set: V _{AUX} above threshold for t >100μs typ. Reset: V _{AUX} below threshold and flag read (SPI) |
| V _{DD} low >100ms | Description | Reports that V _{DD} terminal is lower than the V _{DD} UV threshold for a time longer than 100ms |
| | Set / Reset condition | Set: V _{DD} below threshold for t >100ms typ. Reset: V _{DD} above threshold and flag read (SPI) |
| V _{DD} low | Description | Report that V _{DD} is below V _{DD} undervoltage threshold. |
| | Set / Reset condition | Set: V _{DD} below threshold. Reset: flag read (SPI) |
| RST low >100ms | Description | Report that the Reset pin has detected a low level, longer than 100ms (Reset permanent low) |
| | Set / Reset condition | Set: after detection of reset low pulse. Reset: Reset pulse terminated and flag read (SPI) |
| multiple Resets | Description | Report that the more than 8 consecutive reset pulses occurred, due to missing or wrong W/D refresh. |
| | Set / Reset condition | Set: after detection of multiple reset pulses. Reset: flag read (SPI) |
| W/D refresh failure | Description | Report that a wrong or missing W/D failure occurred. |
| | Set / Reset condition | Set: failure detected. reset: flag read (SPI) |
| LIN1/2 wake up | Description | Report that wake up source is LIN1 or LIN2 |
| | Set / Reset condition | Set: after LIN1 or LIN 2 wake detected. Reset: Flag read (SPI) |
| LIN1/2 Term short to gnd | Description | Report LIN term 1 or LIN term 2 short to gnd failure |
| | Set / Reset condition | Set: failure detected. Reset failure recovered and flag read (SPI) |

Table 37. Flag Descriptions

| Flag | | Description |
|-----------------------|-----------------------|---|
| LIN 1 Over-temp | Description | Report that the LIN1 or LIN 2 interface has reach over temperature threshold. |
| | Set / Reset condition | Set: LIN1 /LIN2 thermal sensor above threshold. Reset: sensor below threshold and flag read (SPI) |
| RxD1 low | Description | Report that RxD1 / RxD2 pin is shorted to gnd. |
| | Set / Reset condition | Set: Rx low failure detected. Reset: failure recovered and flag read (SPI) |
| RxD1 high | Description | Report that RxD1 / RxD2 pin is shorted to recessive voltage. |
| | Set / Reset condition | Set: Rx high failure detected. Reset: failure recovered and flag read (SPI) |
| TxD1 dom | Description | Report that TxD1 / RxD2 pin is shorted to gnd. |
| | Set / Reset condition | Set: Tx low failure detected. Reset: failure recovered and flag read (SPI) |
| LIN1 bus dom clamp | Description | Report that the LIN1 / LIN2 bus is dominant for a time longer than t_{DOM} |
| | Set / Reset condition | Set: Bus dominant clamp failure detected. Reset: failure recovered and flag read (SPI) |

FIX AND EXTENDED DEVICE STATUS

For every SPI command the device response on MISO is a fix status information. This information is either:

one byte

Fix Status: when a device read operation is performed (MOSI bits 15-14, bits C1 C0 = 00 or 11).

two bytes

Fix Status + Extended Status: when a device write command is used (MOSI bits 15-14, bits C1 C0 = 01)

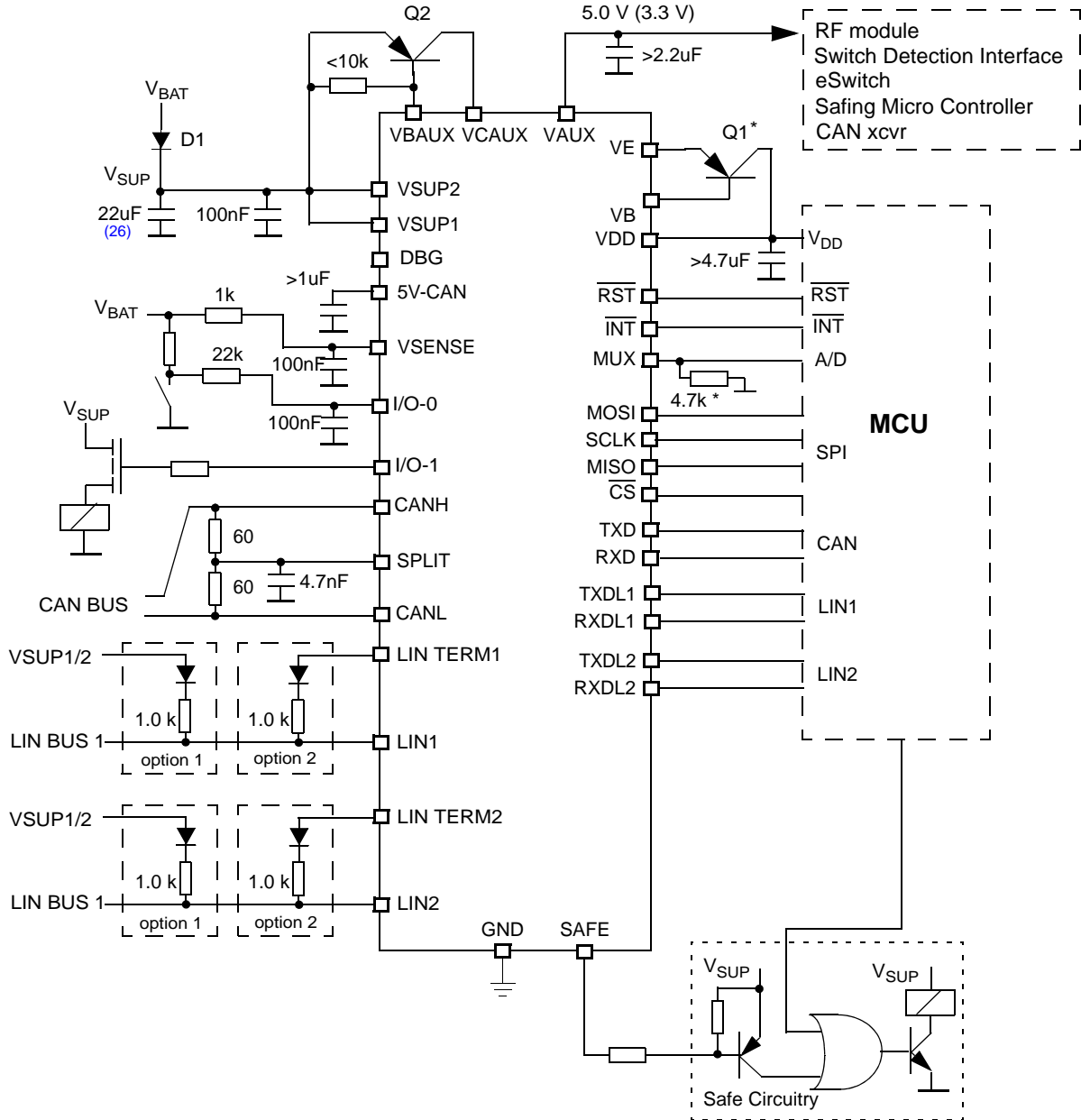
Table 38. status bits description

| Bits | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----|----|-----|-------|-------|-------|--------|--------|---------|---------|------|------|-------|-------|--------|--------|
| MOSI | INT | WU | RST | CAN-G | LIN-G | I/O-G | SAFE-G | VREG-G | CAN-BUS | CAN-LOC | LIN1 | LIN0 | I/O-1 | I/O-0 | VREG-1 | VREG-0 |

| Bits | Description |
|---------|---|
| INT | Indicate that an INT has occurred and that INT flags are pending to be read. |
| WU | Indicate that an Wake Up has occurred and that Wake Up flags are pending to be read. |
| RST | Indicate that an Reset has occurred and that the flags that report the Reset source are pending to be read. |
| CAN-G | The INT, or WU or RST source is CAN interface. CAN local or CAN bus source. |
| I/O-G | The INT, or WU or RST source is I/O interfaces. |
| SAFE-G | The INT, or WU or RST source is from a SAFE condition |
| VREG-G | The INT, or WU or RST source is from a Regulator event, or voltage monitoring event |
| CAN-LOC | The INT, or WU or RST source is CAN interface. CAN local source. |
| CAN-BUS | The INT, or WU or RST source is CAN interface. CAN bus source. |
| I/O-1 | The INT, or WU or RST source is I/O interface, flag from I/O sub adress Low (bit 7 =0) |
| I/O-0 | The INT, or WU or RST source is I/O interface, flag from I/O sub adress High (bit 7 =1) |
| VREG-1 | The INT, or WU or RST source is from a Regulator event, flag from REG register sub adress high (bit 7 =1) |
| VREG-0 | The INT, or WU or RST source is from a Regulator event, flag from REG register sub adress low (bit 7 =0) |

TYPICAL APPLICATIONS

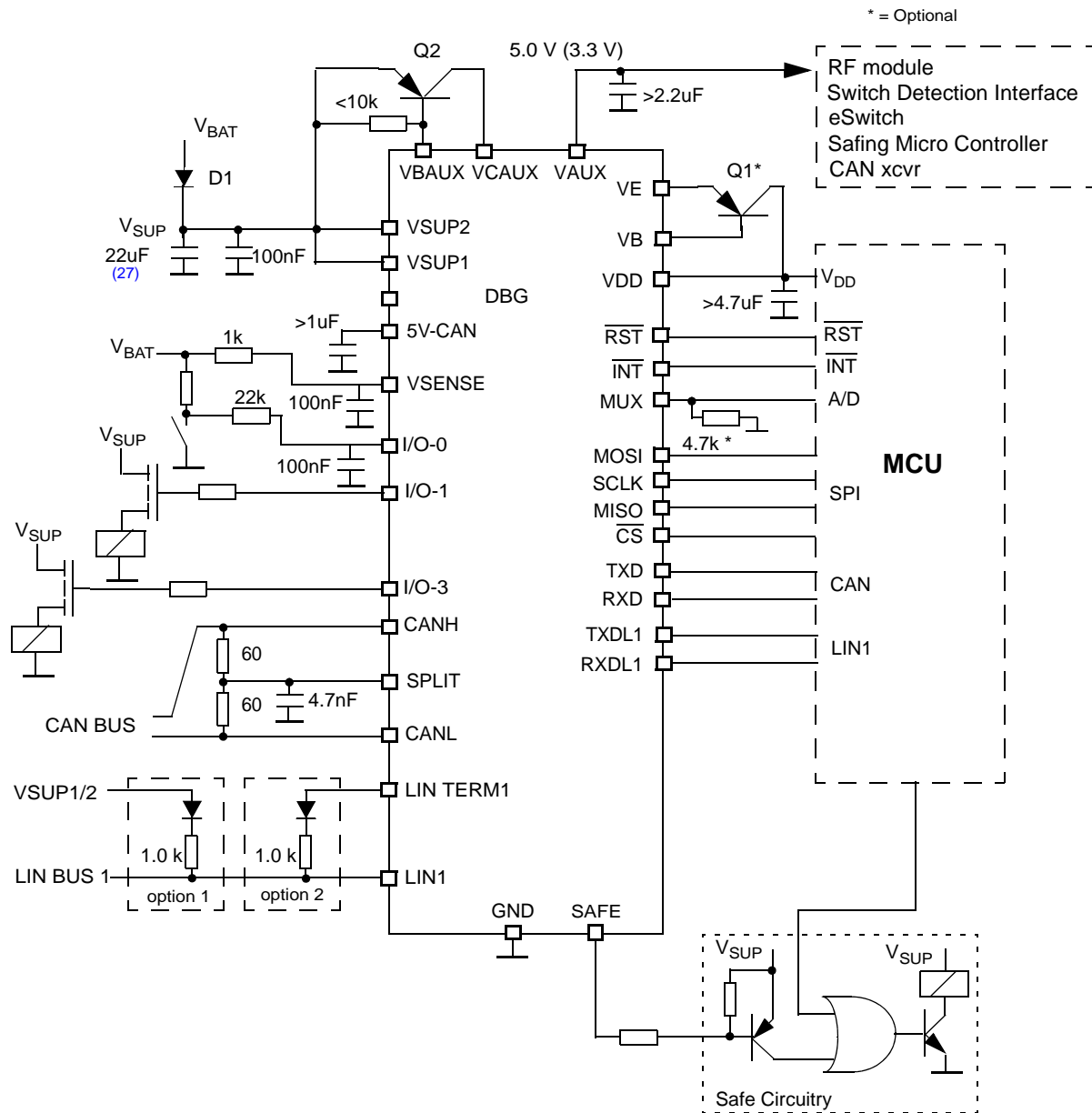
* = Optional



Notes

- 26. Cap > 10uF required to pass EMC requirement according to "OEM_HW_Requirement-For CAN_LIN_FR-interface_V10_20081210" or newer

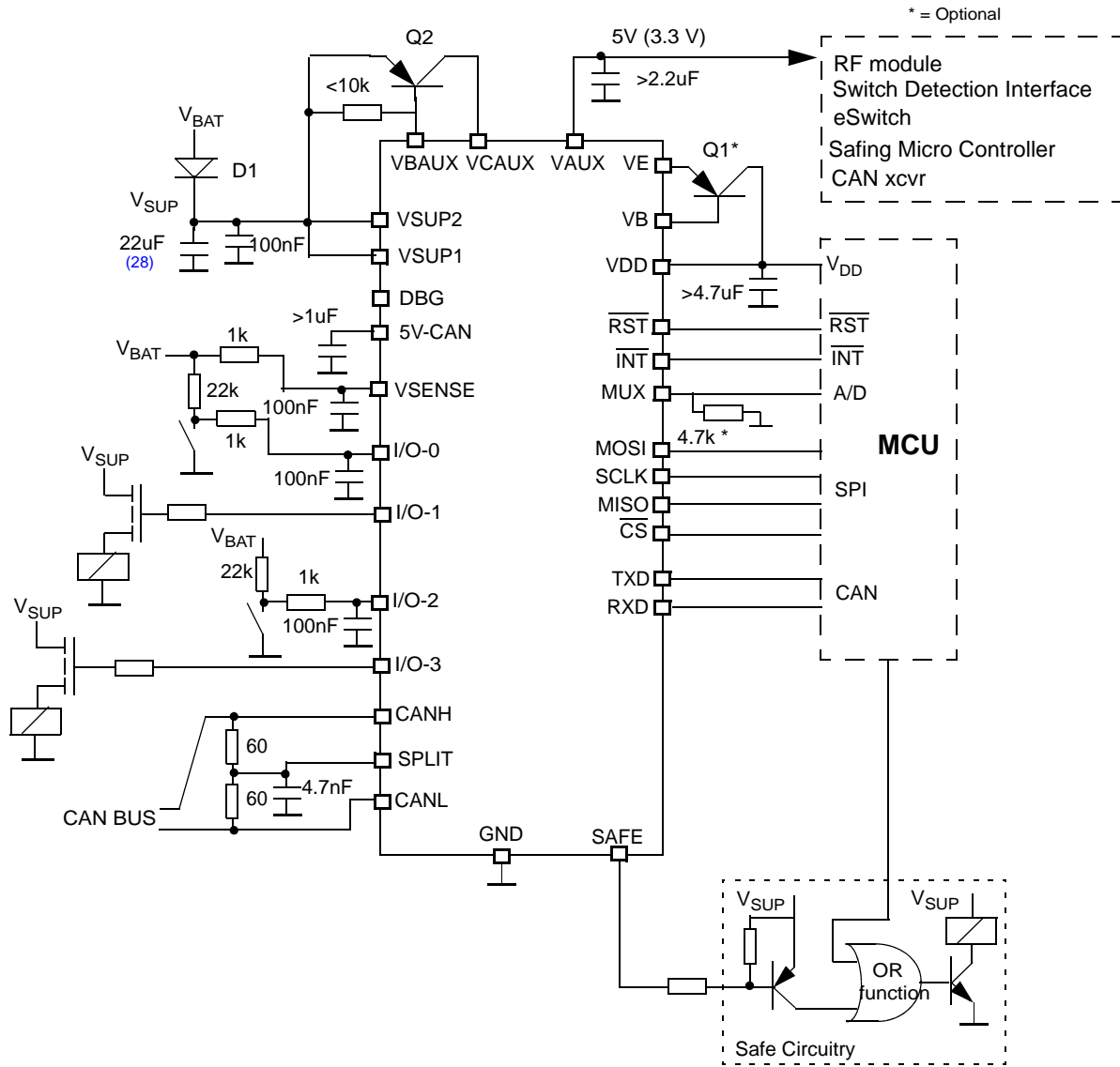
Figure 36. 33905D Typical Application Schematic



Notes

- 27. Cap > 10uF required to pass EMC requirement according to "OEM_HW_Requirement-For CAN_LIN_FR-interface_V10_20081210" or newer

Figure 37. 33905S Typical Application Schematic



Notes

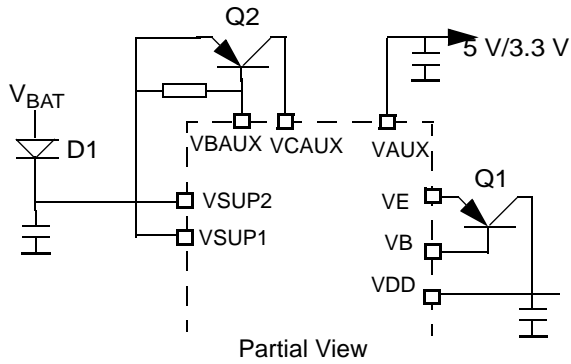
- 28. Cap > 10uF required to pass EMC requirement according to "OEM_HW_Requirement-For CAN_LIN_FR-interface_V10_20081210" or newer

Figure 38. 33904A Typical Application Schematic

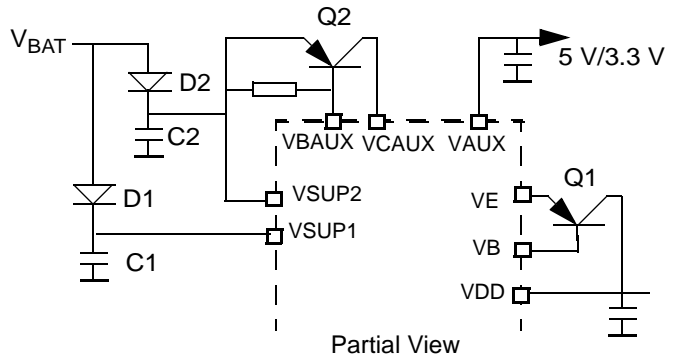
The following figure illustrates the application case where 2 reverse battery diodes can be used for optimization of the filtering and buffering capacitor at the V_{DD} pin. This allows using a minimum value capacitor at the V_{DD} pin to guarantee reset free operation of the MCU during the

cranking pulse, and temporary (50 ms) loss of the V_{BAT} supply.

Applications without an external ballast on V_{DD} and without using the VAUX regulator are illustrated as well.

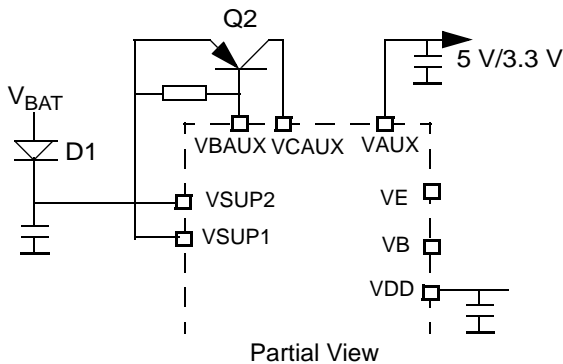


ex1: Single V_{SUP} Supply

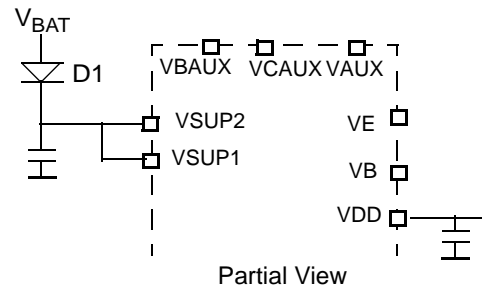


ex2: Split V_{SUP} Supply

Optimized solution for cranking pulses. C1 is sized for MCU power supply buffer only.



ex 3: No External Transistor, V_{DD} ~100 mA Capability delivered by internal path transistor.



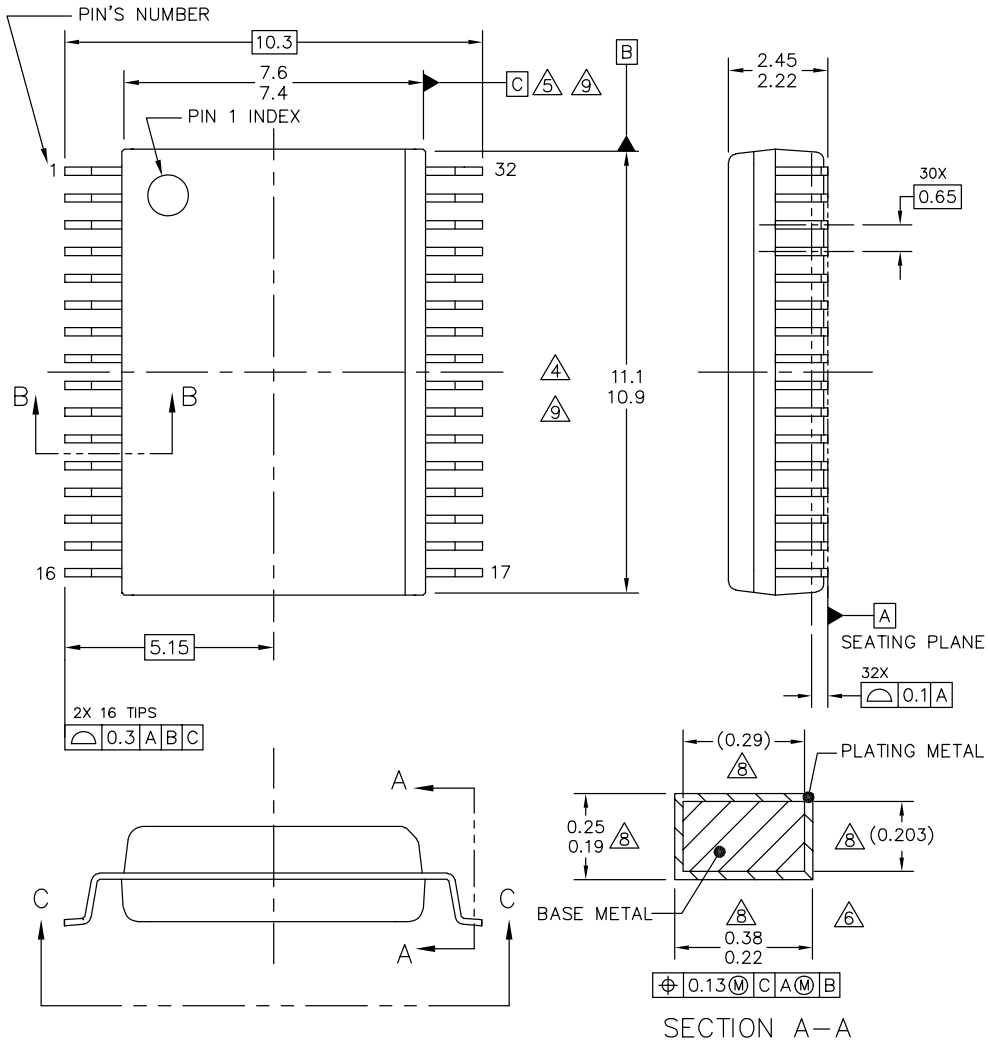
ex 4: No External Transistor - No VAUX

Figure 39. Application Options

PACKAGING

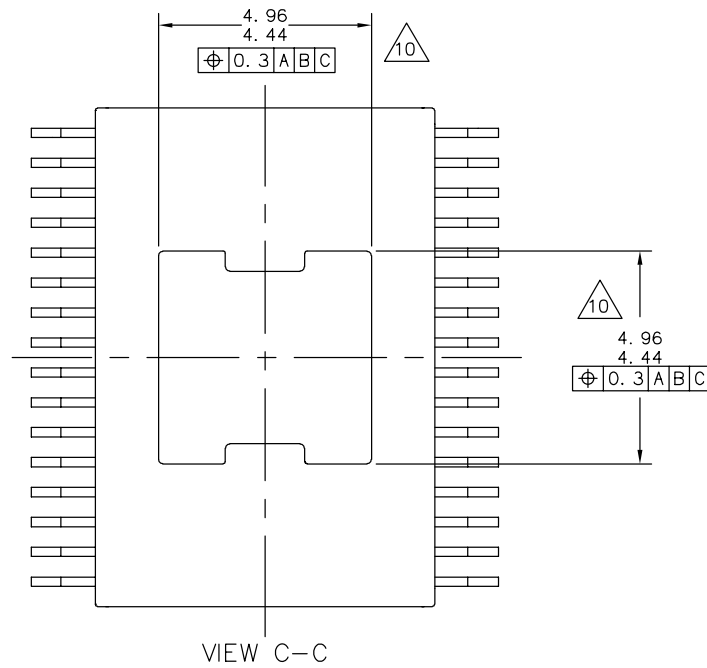
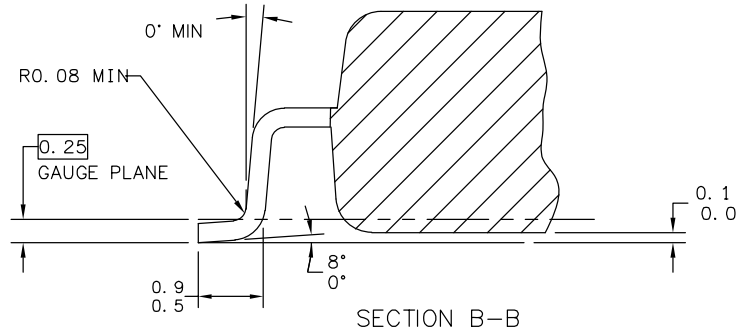
SOIC 32 PACKAGE DIMENSIONS

For the most current package revision, visit www.freescale.com and perform a keyword search using the "98A" listed below.



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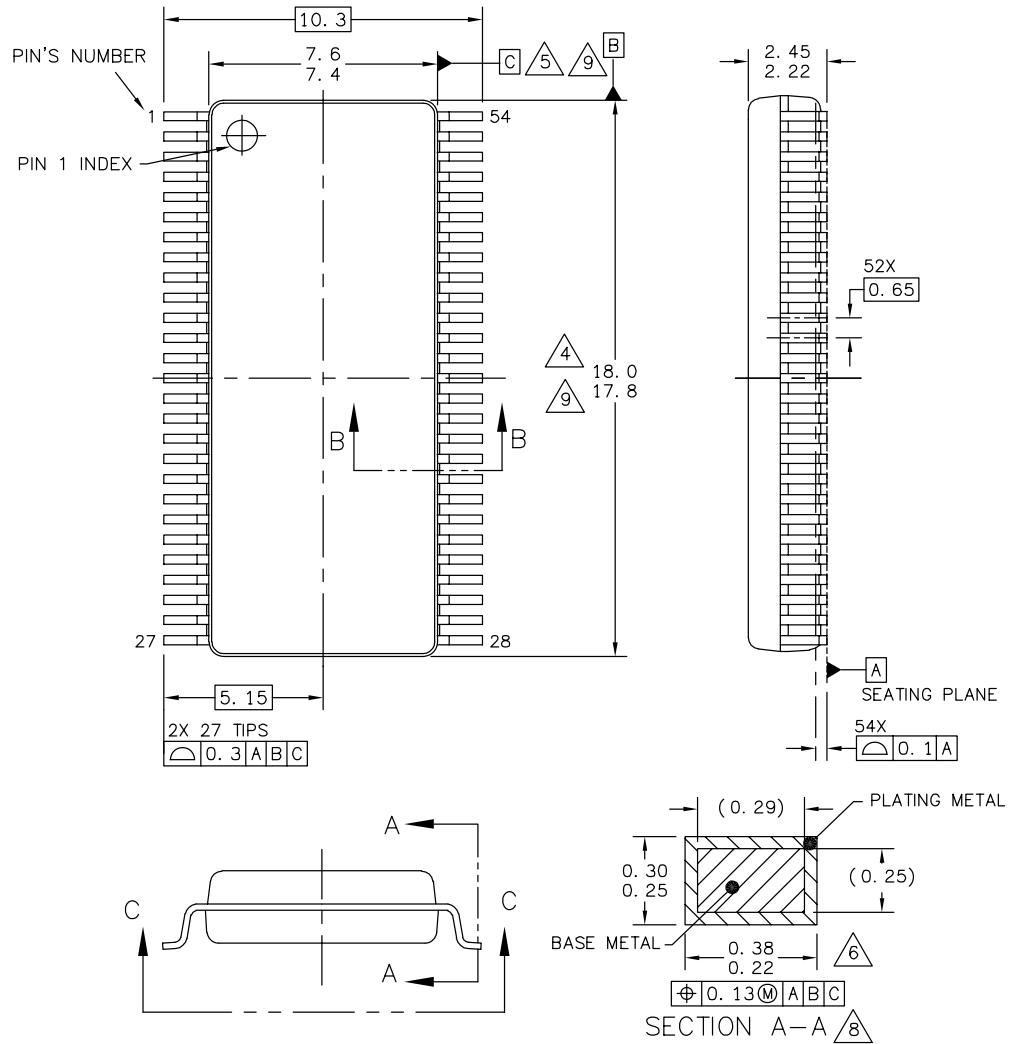
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3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 mm.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.3 mm FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER-LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
10. THESE DIMENSION RANGES DEFINE THE PRIMARY KEEP-OUT AREA. MOLD LOCKING AND RESIN BLEED CONTROL FEATURES MAY BE VISIBLE AND THEY MAY EXTEND TO 0.34mm FROM MAXIMUM EXPOSED PAD SIZE

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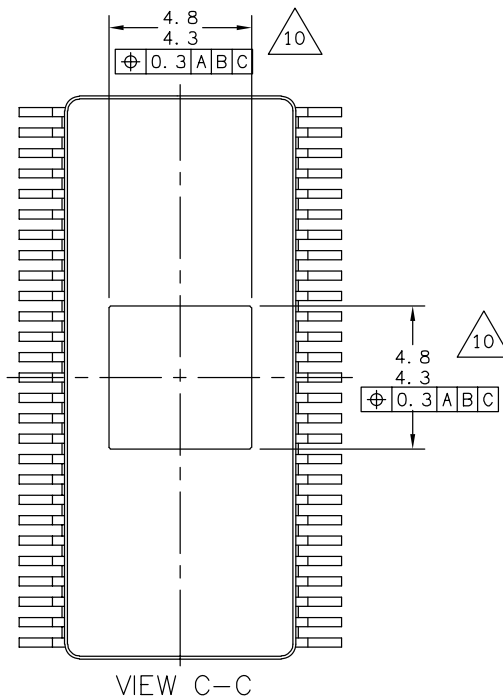
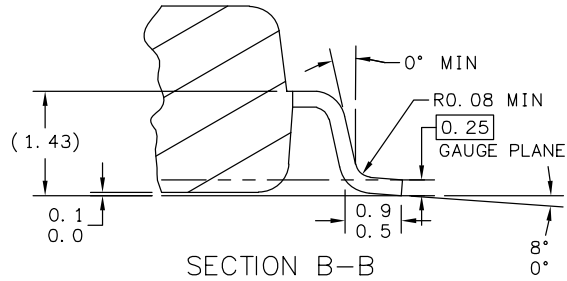
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SOIC 54 PACKAGE DIMENSIONS



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5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
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8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.3 mm FROM THE LEAD TIP.
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10. THESE DIMENSIONS RANGES DEFINE THE PRIMARY KEEP-OUT AREA. MOLD LOCKING AND RESIN BLEED CONTROL FEATURES MAY BE VISIBLE AND THEY MAY EXTEND TO 1.5mm FROM MAXIMUM EXPOSED PAD SIZE

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REVISION HISTORY

| REVISION | DATE | DESCRIPTION OF CHANGES |
|----------|---------|--|
| 1.0 | 11/2009 | <ul style="list-style-type: none">Initial Release |
| 2.0 | 1/2010 | <ul style="list-style-type: none">Updated LIN 2.0 to LIN 2.1 throughout documentChanged Pin VC to VEChanged Pin VBASE to VBAdded note to Simplified Application and Typical Application drawings for Q1 to be optional.Updated Parameters Tables.; Timing accuracy added, CAN wake and CANL/CANH input current.Changed default setting of: INIT Reg register, bit7, I/Ox sync - INIT W/D register, bit 6 MCU_OC and bit 1 W/D N/Win |
| 3.0 | 2/2010 | <ul style="list-style-type: none">Re-arranged the order of the devices. |

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