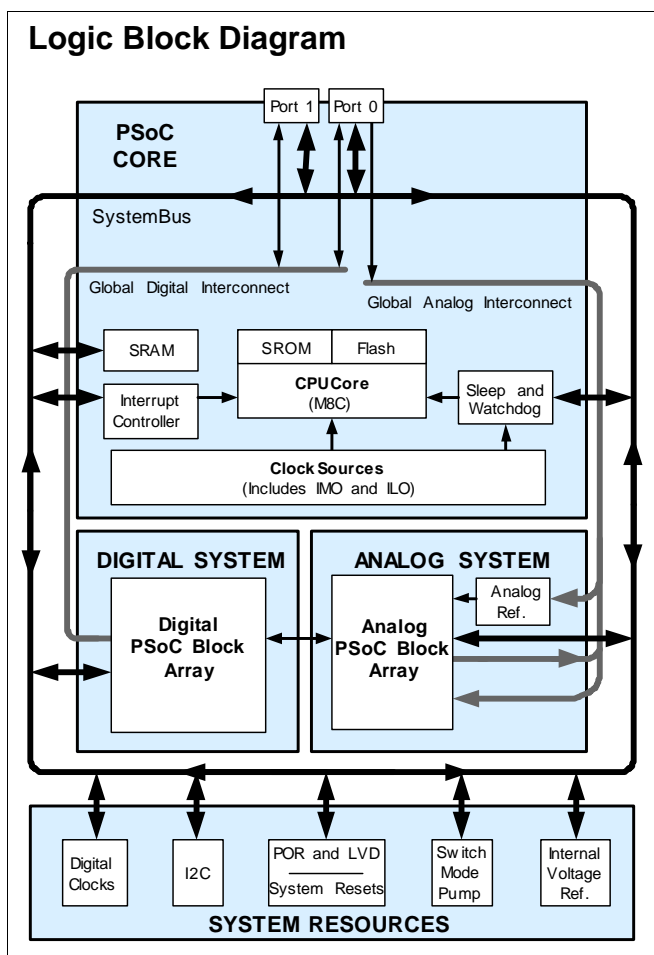


## Features

- **Powerful Harvard Architecture Processor:**
  - M8C Processor Speeds to 24 MHz
  - Low Power at High Speed
  - 2.4V to 5.25V Operating Voltage
  - Operating Voltages down to 1.0V using On-Chip Switch Mode Pump (SMP)
  - Industrial Temperature Range: -40°C to +85°C
- **Advanced Peripherals (PSoC<sup>®</sup> Blocks):**
  - Four Analog Type "E" PSoC Blocks Provide:
    - Two Comparators with DAC Refs
    - Single or Dual 8-Bit 8:1 ADC
  - Four Digital PSoC Blocks Provide:
    - 8 to 32-Bit Timers, Counters, and PWMs
    - CRC and PRS Modules
  - Full Duplex UART, SPI<sup>™</sup> Master or Slave: Connectable to All GPIO Pins
  - Complex Peripherals by Combining Blocks
- **Flexible On-Chip Memory:**
  - 4K Flash Program Storage 50,000 Erase/Write Cycles
  - 256 Bytes SRAM Data Storage
  - In-System Serial Programming (ISSP)
  - Partial Flash Updates
  - Flexible Protection Modes
  - EEPROM Emulation in Flash
- **Complete Development Tools:**
  - Free Development Software (PSoC Designer<sup>™</sup>)
  - Full Featured, In-Circuit Emulator and Programmer
  - Full Speed Emulation
  - Complex Breakpoint Structure
  - 128 Bytes Trace Memory
- **Precision, Programmable Clocking:**
  - Internal ±2.5% 24/48 MHz Oscillator
  - Internal Oscillator for Watchdog and Sleep
- **Programmable Pin Configurations:**
  - 25 mA Sink, 10 mA Drive on All GPIO
  - Pull Up, Pull Down, High Z, Strong, or Open Drain Drive Modes on All GPIO
  - Up to Eight Analog Inputs on GPIO
  - Configurable Interrupt on all GPIO

- **Additional System Resources:**
  - I<sup>2</sup>C<sup>™</sup> Master, Slave and MultiMaster to 400 kHz
  - Watchdog and Sleep Timers
  - User Configurable Low Voltage Detection
  - Integrated Supervisory Circuit
  - On-Chip Precision Voltage Reference



## PSoC Functional Overview

The PSoC family consists of many programmable system-on-chip controller devices. These devices are designed to replace multiple traditional MCU-based system components with a low cost single-chip programmable component. A PSoC device includes configurable blocks of analog and digital logic, and programmable interconnect. This architecture allows the user to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable IO are included in a range of convenient pinouts.

The PSoC architecture, as shown in Figure 1, consists of four main areas: the Core, the System Resources, the Digital System, and the Analog System. Configurable global bus resources allow the combining of all device resources into a complete custom system. Each PSoC device includes four digital blocks. Depending on the PSoC package, up to two analog comparators and up to 16 General Purpose IO (GPIO) are also included. The GPIO provide access to the global digital and analog interconnects.

### PSoC Core

The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO (internal main oscillator) and ILO (internal low speed oscillator). The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a four MIPS 8-bit Harvard architecture microprocessor.

System Resources provide additional capability, such as digital clocks to increase the flexibility of the PSoC Programmable System-on-Chips, I2C functionality for implementing an I2C master, slave, MultiMaster, an internal voltage reference that provides an absolute value of 1.3V to a number of PSoC subsystems, a switch mode pump (SMP) that generates normal operating voltages off a single battery cell, and various system resets supported by the M8C.

The Digital System consists of an array of digital PSoC blocks, which can be configured into any number of digital peripherals. The digital blocks can be connected to the GPIO through a series of global bus that can route any signal to any pin. This frees designs from the constraints of a fixed peripheral controller.

The Analog System consists of four analog PSoC blocks, supporting comparators and analog-to-digital conversion up to 8 bits in precision.

## Digital System

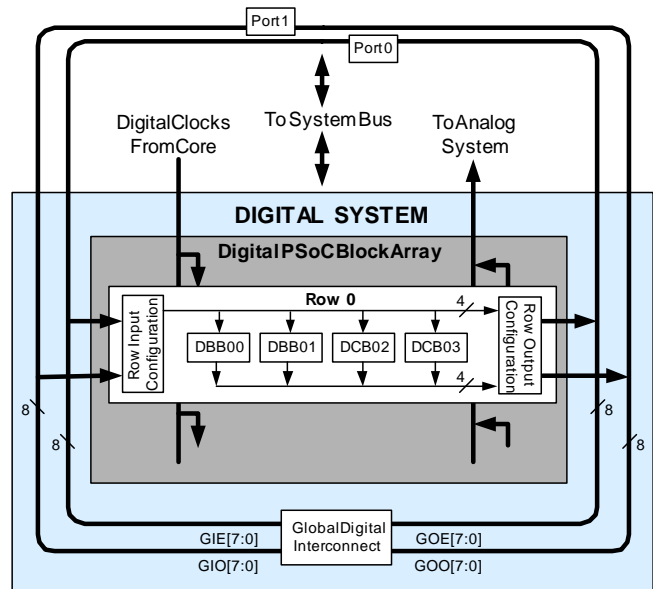
The Digital System consists of four digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references. Digital peripheral configurations include:

- PWMs (8 to 32 bit)
- PWMs with Dead band (8 to 32 bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8 bit with selectable parity (up to four)
- SPI master and slave
- I2C slave, master, MultiMaster (one available as a System Resource)
- Cyclical Redundancy Checker/Generator (8 to 32 bit)
- IrDA (up to four)
- Pseudo Random Sequence Generators (8 to 32 bit)

The digital blocks can be connected to any GPIO through a series of global bus that can route any signal to any pin. The busses also allow for signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This provides an optimum choice of system resources for your application. Family resources are shown in Table 1 on page 3.

Figure 1. Digital System Block Diagram



## Analog System

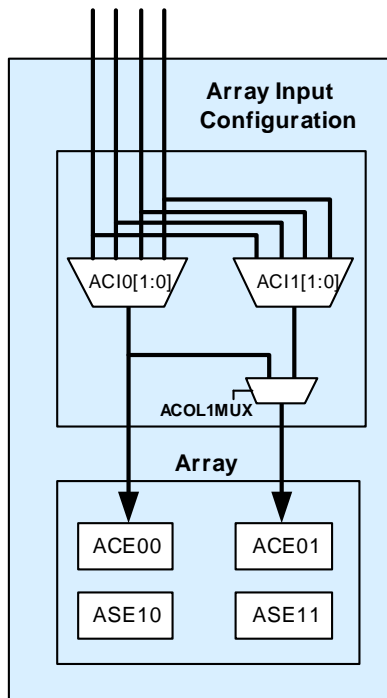
The Analog System consists of four configurable blocks to allow creation of complex analog signal flows. Analog peripherals are very flexible and may be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- Analog-to-digital converters (single or dual, with 8-bit or 10-bit resolution)
- Pin-to-pin comparators (one)
- Single-ended comparators (up to 2) with absolute (1.3V) reference or 8-bit DAC reference
- 1.3V reference (as a System Resource)

In most PSoC devices, analog blocks are provided in columns of three, which includes one CT (Continuous Time) and two SC (Switched Capacitor) blocks. The CY8C21x23 devices provide limited functionality Type “E” analog blocks. Each column contains one CT block and one SC block.

The number of blocks on the device family is listed in [Table 1](#).

**Figure 2. CY8C21x23 Analog System Block Diagram**



## Additional System Resources

System Resources, some of which listed in the previous sections, provide additional capability useful to complete systems. Additional resources include a switch mode pump, low voltage detection, and power on reset. The merits of each system resource are.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3 voltage reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch mode pump (SMP) generates normal operating voltages from a single 1.2V battery cell, providing a low cost boost converter.

## PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks, and 12, 6, or 4 analog blocks. [Table 1](#) lists the resources available for specific PSoC device groups. The PSoC device covered by this data sheet is highlighted.

**Table 1. PSoC Device Characteristics**

| PSoC Part Number | Digital IO | Digital Rows | Digital Blocks | Analog Inputs | Analog Outputs | Analog Columns | Analog Blocks          | SRAM Size        | Flash     |
|------------------|------------|--------------|----------------|---------------|----------------|----------------|------------------------|------------------|-----------|
| CY8C29x66        | up to 64   | 4            | 16             | 12            | 4              | 4              | 12                     | 2K               | 32 K      |
| CY8C27x43        | up to 44   | 2            | 8              | 12            | 4              | 4              | 12                     | 256 Bytes        | 16 K      |
| CY8C24x94        | 56         | 1            | 4              | 48            | 2              | 2              | 6                      | 1K               | 16 K      |
| CY8C24x23A       | up to 24   | 1            | 4              | 12            | 2              | 2              | 6                      | 256 Bytes        | 4K        |
| CY8C21x34        | up to 28   | 1            | 4              | 28            | 0              | 2              | 4 <sup>[1]</sup>       | 512 Bytes        | 8K        |
| <b>CY8C21x23</b> | <b>16</b>  | <b>1</b>     | <b>4</b>       | <b>8</b>      | <b>0</b>       | <b>2</b>       | <b>4<sup>[1]</sup></b> | <b>256 Bytes</b> | <b>4K</b> |
| CY8C20x34        | up to 28   | 0            | 0              | 28            | 0              | 0              | 3 <sup>[2]</sup>       | 512 Bytes        | 8K        |

### Notes

1. Limited analog functionality
2. Two analog blocks and one CapSense™

## Getting Started

The quickest way to understand PSoC silicon is to read this data sheet and then use the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the PSoC<sup>®</sup> Programmable System-on-Chip™ Technical Reference Manual for CY8C28xxx PSoC devices.

For up to date ordering, packaging, and electrical specification information, see the latest PSoC device data sheets on the web at [www.cypress.com/psoc](http://www.cypress.com/psoc).

## Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs. They are located here: [www.cypress.com/psoc](http://www.cypress.com/psoc). Select Application Notes under the Documentation tab.

## Development Kits

PSoC Development Kits are available online from Cypress at [www.cypress.com/shop](http://www.cypress.com/shop) and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

## Training

Free PSoC technical training (on demand, webinars, and workshops) is available online at [www.cypress.com/training](http://www.cypress.com/training). The training covers a wide variety of topics and skill levels to assist you in your designs.

## CYPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to [www.cypress.com/cypros](http://www.cypress.com/cypros).

## Solutions Library

Visit our growing library of solution focused designs at [www.cypress.com/solutions](http://www.cypress.com/solutions). Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

## Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at [www.cypress.com/support](http://www.cypress.com/support). If you cannot find an answer to your question, call technical support at 1-800-541-4736.

## Development Tools

PSoC Designer is a Microsoft<sup>®</sup> Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE runs on Windows XP or Windows Vista.

This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and built in support for third party assemblers and C compilers.

PSoC Designer also supports C language compilers developed specifically for the devices in the PSoC family.

## PSoC Designer Software Subsystems

### *System-Level View*

A drag-and-drop visual embedded system design environment based on PSoC Express. In the system level view you create a model of your system inputs, outputs, and communication interfaces. You define when and how an output device changes state based upon any or all other system devices. Based upon the design, PSoC Designer automatically selects one or more PSoC Programmable System-on-Chip Controllers that match your system requirements.

PSoC Designer generates all embedded code, then compiles and links it into a programming file for a specific PSoC device.

### *Chip-Level View*

The chip-level view is a more traditional integrated development environment (IDE) based on PSoC Designer 4.4. Choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

### *Hybrid Designs*

You can begin in the system-level view, allow it to choose and configure your user modules, routing, and generate code, then switch to the chip-level view to gain complete control over on-chip resources. All views of the project share a common code editor, builder, and common debug, emulation, and programming tools.

## Code Generation Tools

PSoC Designer supports multiple third party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

**Assemblers.** The assemblers allow assembly code to merge seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

**C Language Compilers.** C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices.

The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

## Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write IO registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

## Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

## In-Circuit Emulator

A low cost, high functionality In-Circuit Emulator (ICE) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

## Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select Components
2. Configure Components
3. Organize and Connect
4. Generate, Verify, and Debug

### Select Components

Both the system-level and chip-level views provide a library of prebuilt, pretested hardware peripheral components. In the system-level view, these components are called “drivers” and correspond to inputs (a thermistor, for example), outputs (a brushless DC fan, for example), communication interfaces (I<sup>2</sup>C-bus, for example), and the logic to control how they interact with one another (called valuator).

In the chip-level view, the components are called “user modules”. User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and programmable system-on-chip varieties.

### Configure Components

Each of the components you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a Pulse Width Modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus.

Both the system-level drivers and chip-level user modules are documented in data sheets that are viewed directly in the PSoC Designer. These data sheets explain the internal operation of the component and provide performance specifications. Each data sheet describes the use of each user module parameter or driver property, and other information you may need to successfully implement your design.

## Organize and Connect

You can build signal chains at the chip level by interconnecting user modules to each other and the IO pins, or connect system level inputs, outputs, and communication interfaces to each other with valuator functions.

In the system-level view, selecting a potentiometer driver to control a variable speed fan driver and setting up the valuator to control the fan speed based on input from the pot selects, places, routes, and configures a programmable gain amplifier (PGA) to buffer the input from the potentiometer, an analog to digital converter (ADC) to convert the potentiometer's output to a digital signal, and a PWM to control the fan.

In the chip-level view, perform the selection, configuration, and routing so that you have complete control over the use of all on-chip resources.

## Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the "Generate Application" step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system.

Both system-level and chip-level designs generate software based on your design. The chip-level design provides application programming interfaces (APIs) with high level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed. The system-level design also generates a C `main()` program that completely controls the chosen application and contains placeholders for custom code at strategic positions allowing you to further refine the software without disrupting the generated code.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside the PSoC Designer's Debugger subsystem. The Debugger downloads the HEX image to the ICE where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

## Document Conventions

### Acronyms Used

This table lists the acronyms used in this data sheet.

**Table 2. Acronyms**

| Acronym           | Description   |
|-------------------|---|
| AC                | alternating current                                 |
| ADC               | analog-to-digital converter                         |
| API               | application programming interface                   |
| CPU               | central processing unit                             |
| CT                | continuous time                                     |
| DAC               | digital-to-analog converter                         |
| DC                | direct current                                      |
| EEPROM            | electrically erasable programmable read-only memory |
| FSR               | full scale range                                    |
| GPIO              | general purpose IO                                  |
| ICE               | in-circuit emulator                                 |
| IDE               | integrated development environment                  |
| IO                | input/output  |
| ISSP              | in-system serial programming                        |
| IPOR              | imprecise power on reset                            |
| LSb               | least-significant bit                               |
| LVD               | low voltage detect                                  |
| MSb               | most-significant bit                                |
| PC                | program counter                                     |
| PGA               | programmable gain amplifier                         |
| POR               | power on reset                                      |
| PPOR              | precision power on reset                            |
| PSoC <sup>®</sup> | Programmable System-on-Chip <sup>™</sup>            |
| PWM               | pulse width modulator                               |
| ROM               | read only memory                                    |
| SC                | switched capacitor                                  |
| SMP               | switch mode pump                                    |
| SRAM              | static random access memory                         |

### Units of Measure

A units of measure table is located in the section [Electrical Specifications](#) on page 15. [Table 11](#) on page 15 lists all the abbreviations used to measure the PSoC devices.

### Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h', 'b', or 0x are decimal.

## Pin Information

This section describes, lists, and illustrates the CY8C21x23 PSoC device pins and pinout configurations. Every port pin (labeled with a "P") is capable of Digital IO. However, Vss, Vdd, SMP, and XRES are not capable of Digital IO.

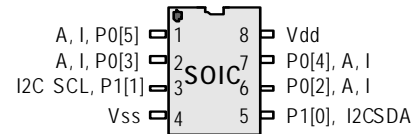
### 8-Pin Part Pinout

**Table 3. Pin Definitions - CY8C21123 8-Pin SOIC**

| Pin No. | Type    |        | Pin Name | Description                                      |
|---------|---------|--------|----------|--|
|         | Digital | Analog |          |  |
| 1       | IO      | I      | P0[5]    | Analog Column Mux Input                          |
| 2       | IO      | I      | P0[3]    | Analog Column Mux Input                          |
| 3       | IO      |        | P1[1]    | I2C Serial Clock (SCL), ISSP-SCLK <sup>[3]</sup> |
| 4       | Power   |        | Vss      | Ground Connection                                |
| 5       | IO      |        | P1[0]    | I2C Serial Data (SDA), ISSP-SDATA <sup>[3]</sup> |
| 6       | IO      | I      | P0[2]    | Analog Column Mux Input                          |
| 7       | IO      | I      | P0[4]    | Analog Column Mux Input                          |
| 8       | Power   |        | Vdd      | Supply Voltage                                   |

**LEGEND:** A = Analog, I = Input, and O = Output.

**Figure 3. CY8C21123 8-Pin SOIC**



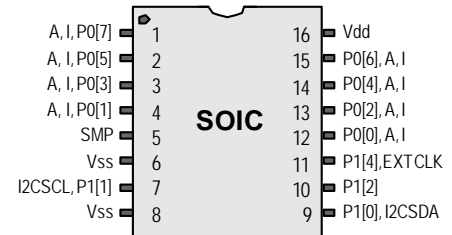
### 16-Pin Part Pinout

**Table 4. Pin Definitions - CY8C21223 16-Pin SOIC**

| Pin No. | Type    |        | Pin Name | Description   |
|---------|---------|--------|----------|---|
|         | Digital | Analog |          |   |
| 1       | IO      | I      | P0[7]    | Analog Column Mux Input   |
| 2       | IO      | I      | P0[5]    | Analog Column Mux Input   |
| 3       | IO      | I      | P0[3]    | Analog Column Mux Input   |
| 4       | IO      | I      | P0[1]    | Analog Column Mux Input   |
| 5       | Power   |        | SMP      | Switch Mode Pump (SMP) Connection to required External Components |
| 6       | Power   |        | Vss      | Ground Connection   |
| 7       | IO      |        | P1[1]    | I2C Serial Clock (SCL), ISSP-SCLK <sup>[3]</sup>                  |
| 8       | Power   |        | Vss      | Ground Connection   |
| 9       | IO      |        | P1[0]    | I2C Serial Data (SDA), ISSP-SDATA <sup>[3]</sup>                  |
| 10      | IO      |        | P1[2]    |   |
| 11      | IO      |        | P1[4]    | Optional External Clock Input (EXTCLK)                            |
| 12      | IO      | I      | P0[0]    | Analog Column Mux Input   |
| 13      | IO      | I      | P0[2]    | Analog Column Mux Input   |
| 14      | IO      | I      | P0[4]    | Analog Column Mux Input   |
| 15      | IO      | I      | P0[6]    | Analog Column Mux Input   |
| 16      | Power   |        | Vdd      | Supply Voltage  |

**LEGEND:** A = Analog, I = Input, and O = Output.

**Figure 4. CY8C21223 16-Pin SOIC**







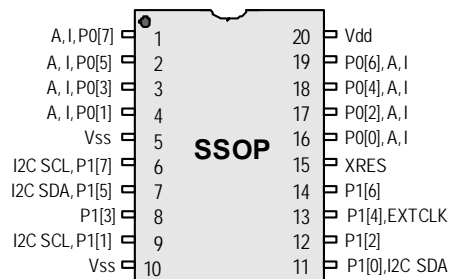
20-Pin Part Pinout

Table 6. Pin Definitions - CY8C21323 20-Pin SSOP

| Pin No. | Type    |        | Pin Name | Description  |
|---------|---------|--------|----------|--|
|         | Digital | Analog |          |  |
| 1       | IO      | I      | P0[7]    | Analog Column Mux Input                            |
| 2       | IO      | I      | P0[5]    | Analog Column Mux Input                            |
| 3       | IO      | I      | P0[3]    | Analog Column Mux Input                            |
| 4       | IO      | I      | P0[1]    | Analog Column Mux Input                            |
| 5       | Power   |        | Vss      | Ground Connection                                  |
| 6       | IO      |        | P1[7]    | I2C Serial Clock (SCL)                             |
| 7       | IO      |        | P1[5]    | I2C Serial Data (SDA)                              |
| 8       | IO      |        | P1[3]    |  |
| 9       | IO      |        | P1[1]    | I2C Serial Clock (SCL), ISSP-SCLK <sup>[3]</sup>   |
| 10      | Power   |        | Vss      | Ground connection                                  |
| 11      | IO      |        | P1[0]    | I2C Serial Data (SDA), ISSP-SDATA <sup>[3]</sup>   |
| 12      | IO      |        | P1[2]    |  |
| 13      | IO      |        | P1[4]    | Optional External Clock Input (EXTCLK)             |
| 14      | IO      |        | P1[6]    |  |
| 15      | Input   |        | XRES     | Active High External Reset with Internal Pull Down |
| 16      | IO      | I      | P0[0]    | Analog Column Mux Input                            |
| 17      | IO      | I      | P0[2]    | Analog Column Mux Input                            |
| 18      | IO      | I      | P0[4]    | Analog Column Mux Input                            |
| 19      | IO      | I      | P0[6]    | Analog Column Mux Input                            |
| 20      | Power   |        | Vdd      | Supply Voltage                                     |

LEGEND A = Analog, I = Input, and O = Output.

Figure 6. CY8C21323 20-Pin SSOP



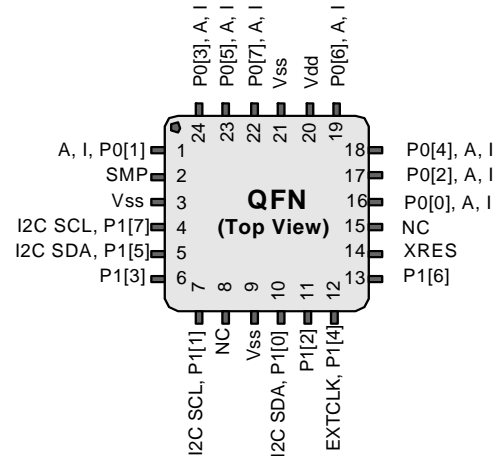
24-Pin Part Pinout

Table 7. Pin Definitions - CY8C21323 24-Pin QFN<sup>[5]</sup>

| Pin No. | Type    |        | Pin Name | Description   |
|---------|---------|--------|----------|---|
|         | Digital | Analog |          |   |
| 1       | IO      | I      | P0[1]    | Analog Column Mux Input   |
| 2       | Power   |        | SMP      | Switch Mode Pump (SMP) Connection to required External Components |
| 3       | Power   |        | Vss      | Ground connection   |
| 4       | IO      |        | P1[7]    | I2C Serial Clock (SCL)  |
| 5       | IO      |        | P1[5]    | I2C Serial Data (SDA)   |
| 6       | IO      |        | P1[3]    |   |
| 7       | IO      |        | P1[1]    | I2C Serial Clock (SCL), ISSP-SCLK <sup>[3]</sup>                  |
| 8       |         |        | NC       | No Connection   |
| 9       | Power   |        | Vss      | Ground Connection   |
| 10      | IO      |        | P1[0]    | I2C Serial Data (SDA), ISSP-SDATA <sup>[3]</sup>                  |
| 11      | IO      |        | P1[2]    |   |
| 12      | IO      |        | P1[4]    | Optional External Clock Input (EXTCLK)                            |
| 13      | IO      |        | P1[6]    |   |
| 14      | Input   |        | XRES     | Active High External Reset with Internal Pull Down                |
| 15      |         |        | NC       | No Connection   |
| 16      | IO      | I      | P0[0]    | Analog Column Mux Input   |
| 17      | IO      | I      | P0[2]    | Analog Column Mux Input   |
| 18      | IO      | I      | P0[4]    | Analog Column Mux Input   |
| 19      | IO      | I      | P0[6]    | Analog Column Mux Input   |
| 20      | Power   |        | Vdd      | Supply Voltage  |
| 21      | Power   |        | Vss      | Ground Connection   |
| 22      | IO      | I      | P0[7]    | Analog Column Mux Input   |
| 23      | IO      | I      | P0[5]    | Analog Column Mux Input   |
| 24      | IO      | I      | P0[3]    | Analog Column Mux Input   |

LEGEND A = Analog, I = Input, and O = Output.

Figure 7. CY8C21323 24-Pin QFN



Note

- The center pad on the QFN package must be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.

## Register Reference

This section lists the registers of the CY8C21x23 PSoC device. For detailed register information, refer the PSoC Programmable System-on-Chip Technical Reference Manual.

### Register Conventions

The register conventions specific to this section are listed in the following table.

**Table 8. Register Conventions**

| Convention | Description                  |
|------------|------------------------------|
| R          | Read register or bit(s)      |
| W          | Write register or bit(s)     |
| L          | Logical register or bit(s)   |
| C          | Clearable register or bit(s) |
| #          | Access is bit specific       |

## Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as IO space and is divided into two banks. The XO1 bit in the Flag register (CPU\_F) determines which bank the user is currently in. When the XO1 bit is set the user is in Bank 1.

**Note** In the following register mapping tables, blank fields are Reserved and must not be accessed.

Table 9. Register Map Bank 0 Table: User Space

| Name     | Addr (0,Hex) | Access | Name    | Addr (0,Hex) | Access | Name     | Addr (0,Hex) | Access | Name     | Addr (0,Hex) | Access |
|----------|--------------|--------|---------|--------------|--------|----------|--------------|--------|----------|--------------|--------|
| PRT0DR   | 00           | RW     |         | 40           |        | ASE10CR0 | 80           | RW     |          | C0           |        |
| PRT0IE   | 01           | RW     |         | 41           |        |          | 81           |        |          | C1           |        |
| PRT0GS   | 02           | RW     |         | 42           |        |          | 82           |        |          | C2           |        |
| PRT0DM2  | 03           | RW     |         | 43           |        |          | 83           |        |          | C3           |        |
| PRT1DR   | 04           | RW     |         | 44           |        | ASE11CR0 | 84           | RW     |          | C4           |        |
| PRT1IE   | 05           | RW     |         | 45           |        |          | 85           |        |          | C5           |        |
| PRT1GS   | 06           | RW     |         | 46           |        |          | 86           |        |          | C6           |        |
| PRT1DM2  | 07           | RW     |         | 47           |        |          | 87           |        |          | C7           |        |
|          | 08           |        |         | 48           |        |          | 88           |        |          | C8           |        |
|          | 09           |        |         | 49           |        |          | 89           |        |          | C9           |        |
|          | 0A           |        |         | 4A           |        |          | 8A           |        |          | CA           |        |
|          | 0B           |        |         | 4B           |        |          | 8B           |        |          | CB           |        |
|          | 0C           |        |         | 4C           |        |          | 8C           |        |          | CC           |        |
|          | 0D           |        |         | 4D           |        |          | 8D           |        |          | CD           |        |
|          | 0E           |        |         | 4E           |        |          | 8E           |        |          | CE           |        |
|          | 0F           |        |         | 4F           |        |          | 8F           |        |          | CF           |        |
|          | 10           |        |         | 50           |        |          | 90           |        |          | D0           |        |
|          | 11           |        |         | 51           |        |          | 91           |        |          | D1           |        |
|          | 12           |        |         | 52           |        |          | 92           |        |          | D2           |        |
|          | 13           |        |         | 53           |        |          | 93           |        |          | D3           |        |
|          | 14           |        |         | 54           |        |          | 94           |        |          | D4           |        |
|          | 15           |        |         | 55           |        |          | 95           |        |          | D5           |        |
|          | 16           |        |         | 56           |        |          | 96           |        | I2C_CFG  | D6           | RW     |
|          | 17           |        |         | 57           |        |          | 97           |        | I2C_SCR  | D7           | #      |
|          | 18           |        |         | 58           |        |          | 98           |        | I2C_DR   | D8           | RW     |
|          | 19           |        |         | 59           |        |          | 99           |        | I2C_MSCR | D9           | #      |
|          | 1A           |        |         | 5A           |        |          | 9A           |        | INT_CLR0 | DA           | RW     |
|          | 1B           |        |         | 5B           |        |          | 9B           |        | INT_CLR1 | DB           | RW     |
|          | 1C           |        |         | 5C           |        |          | 9C           |        |          | DC           |        |
|          | 1D           |        |         | 5D           |        |          | 9D           |        | INT_CLR3 | DD           | RW     |
|          | 1E           |        |         | 5E           |        |          | 9E           |        | INT_MSK3 | DE           | RW     |
|          | 1F           |        |         | 5F           |        |          | 9F           |        |          | DF           |        |
| DBB00DR0 | 20           | #      | AMX_IN  | 60           | RW     |          | A0           |        | INT_MSK0 | E0           | RW     |
| DBB00DR1 | 21           | W      |         | 61           |        |          | A1           |        | INT_MSK1 | E1           | RW     |
| DBB00DR2 | 22           | RW     | PWM_CR  | 62           | RW     |          | A2           |        | INT_VC   | E2           | RC     |
| DBB00CR0 | 23           | #      |         | 63           |        |          | A3           |        | RES_WDT  | E3           | W      |
| DBB01DR0 | 24           | #      | CMP_CR0 | 64           | #      |          | A4           |        |          | E4           |        |
| DBB01DR1 | 25           | W      |         | 65           |        |          | A5           |        |          | E5           |        |
| DBB01DR2 | 26           | RW     | CMP_CR1 | 66           | RW     |          | A6           |        | DEC_CR0  | E6           | RW     |
| DBB01CR0 | 27           | #      |         | 67           |        |          | A7           |        | DEC_CR1  | E7           | RW     |
| DCB02DR0 | 28           | #      | ADC0_CR | 68           | #      |          | A8           |        |          | E8           |        |
| DCB02DR1 | 29           | W      | ADC1_CR | 69           | #      |          | A9           |        |          | E9           |        |
| DCB02DR2 | 2A           | RW     |         | 6A           |        |          | AA           |        |          | EA           |        |
| DCB02CR0 | 2B           | #      |         | 6B           |        |          | AB           |        |          | EB           |        |
| DCB03DR0 | 2C           | #      | TMP_DR0 | 6C           | RW     |          | AC           |        |          | EC           |        |
| DCB03DR1 | 2D           | W      | TMP_DR1 | 6D           | RW     |          | AD           |        |          | ED           |        |
| DCB03DR2 | 2E           | RW     | TMP_DR2 | 6E           | RW     |          | AE           |        |          | EE           |        |
| DCB03CR0 | 2F           | #      | TMP_DR3 | 6F           | RW     |          | AF           |        |          | EF           |        |

Blank fields are Reserved and must not be accessed.

# Access is bit specific.

**Table 9. Register Map Bank 0 Table: User Space (continued)**

| Name | Addr (0,Hex) | Access | Name     | Addr (0,Hex) | Access | Name    | Addr (0,Hex) | Access | Name     | Addr (0,Hex) | Access |
|------|--------------|--------|----------|--------------|--------|---------|--------------|--------|----------|--------------|--------|
|      | 30           |        |          | 70           |        | RDI0RI  | B0           | RW     |          | F0           |        |
|      | 31           |        |          | 71           |        | RDI0SYN | B1           | RW     |          | F1           |        |
|      | 32           |        | ACE00CR1 | 72           | RW     | RDI0IS  | B2           | RW     |          | F2           |        |
|      | 33           |        | ACE00CR2 | 73           | RW     | RDI0LT0 | B3           | RW     |          | F3           |        |
|      | 34           |        |          | 74           |        | RDI0LT1 | B4           | RW     |          | F4           |        |
|      | 35           |        |          | 75           |        | RDI0RO0 | B5           | RW     |          | F5           |        |
|      | 36           |        | ACE01CR1 | 76           | RW     | RDI0RO1 | B6           | RW     |          | F6           |        |
|      | 37           |        | ACE01CR2 | 77           | RW     |         | B7           |        | CPU_F    | F7           | RL     |
|      | 38           |        |          | 78           |        |         | B8           |        |          | F8           |        |
|      | 39           |        |          | 79           |        |         | B9           |        |          | F9           |        |
|      | 3A           |        |          | 7A           |        |         | BA           |        |          | FA           |        |
|      | 3B           |        |          | 7B           |        |         | BB           |        |          | FB           |        |
|      | 3C           |        |          | 7C           |        |         | BC           |        |          | FC           |        |
|      | 3D           |        |          | 7D           |        |         | BD           |        |          | FD           |        |
|      | 3E           |        |          | 7E           |        |         | BE           |        | CPU_SCR1 | FE           | #      |
|      | 3F           |        |          | 7F           |        |         | BF           |        | CPU_SCR0 | FF           | #      |

Blank fields are Reserved and must not be accessed.

# Access is bit specific.

**Table 10. Register Map Bank 1 Table: Configuration Space**

| Name    | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name     | Addr (1,Hex) | Access | Name     | Addr (1,Hex) | Access |
|---------|--------------|--------|------|--------------|--------|----------|--------------|--------|----------|--------------|--------|
| PRT0DM0 | 00           | RW     |      | 40           |        | ASE10CR0 | 80           | RW     |          | C0           |        |
| PRT0DM1 | 01           | RW     |      | 41           |        |          | 81           |        |          | C1           |        |
| PRT0IC0 | 02           | RW     |      | 42           |        |          | 82           |        |          | C2           |        |
| PRT0IC1 | 03           | RW     |      | 43           |        |          | 83           |        |          | C3           |        |
| PRT1DM0 | 04           | RW     |      | 44           |        | ASE11CR0 | 84           | RW     |          | C4           |        |
| PRT1DM1 | 05           | RW     |      | 45           |        |          | 85           |        |          | C5           |        |
| PRT1IC0 | 06           | RW     |      | 46           |        |          | 86           |        |          | C6           |        |
| PRT1IC1 | 07           | RW     |      | 47           |        |          | 87           |        |          | C7           |        |
|         | 08           |        |      | 48           |        |          | 88           |        |          | C8           |        |
|         | 09           |        |      | 49           |        |          | 89           |        |          | C9           |        |
|         | 0A           |        |      | 4A           |        |          | 8A           |        |          | CA           |        |
|         | 0B           |        |      | 4B           |        |          | 8B           |        |          | CB           |        |
|         | 0C           |        |      | 4C           |        |          | 8C           |        |          | CC           |        |
|         | 0D           |        |      | 4D           |        |          | 8D           |        |          | CD           |        |
|         | 0E           |        |      | 4E           |        |          | 8E           |        |          | CE           |        |
|         | 0F           |        |      | 4F           |        |          | 8F           |        |          | CF           |        |
|         | 10           |        |      | 50           |        |          | 90           |        | GDI_O_IN | D0           | RW     |
|         | 11           |        |      | 51           |        |          | 91           |        | GDI_E_IN | D1           | RW     |
|         | 12           |        |      | 52           |        |          | 92           |        | GDI_O_OU | D2           | RW     |
|         | 13           |        |      | 53           |        |          | 93           |        | GDI_E_OU | D3           | RW     |
|         | 14           |        |      | 54           |        |          | 94           |        |          | D4           |        |
|         | 15           |        |      | 55           |        |          | 95           |        |          | D5           |        |
|         | 16           |        |      | 56           |        |          | 96           |        |          | D6           |        |
|         | 17           |        |      | 57           |        |          | 97           |        |          | D7           |        |
|         | 18           |        |      | 58           |        |          | 98           |        |          | D8           |        |
|         | 19           |        |      | 59           |        |          | 99           |        |          | D9           |        |
|         | 1A           |        |      | 5A           |        |          | 9A           |        |          | DA           |        |
|         | 1B           |        |      | 5B           |        |          | 9B           |        |          | DB           |        |

Blank fields are Reserved and must not be accessed.

# Access is bit specific.

Table 10. Register Map Bank 1 Table: Configuration Space (continued)

| Name    | Addr (1,Hex) | Access | Name      | Addr (1,Hex) | Access | Name    | Addr (1,Hex) | Access | Name      | Addr (1,Hex) | Access |
|---------|--------------|--------|-----------|--------------|--------|---------|--------------|--------|-----------|--------------|--------|
|         | 1C           |        |           | 5C           |        |         | 9C           |        |           | DC           |        |
|         | 1D           |        |           | 5D           |        |         | 9D           |        | OSC_GO_EN | DD           | RW     |
|         | 1E           |        |           | 5E           |        |         | 9E           |        | OSC_CR4   | DE           | RW     |
|         | 1F           |        |           | 5F           |        |         | 9F           |        | OSC_CR3   | DF           | RW     |
| DBB00FN | 20           | RW     | CLK_CR0   | 60           | RW     |         | A0           |        | OSC_CR0   | E0           | RW     |
| DBB00IN | 21           | RW     | CLK_CR1   | 61           | RW     |         | A1           |        | OSC_CR1   | E1           | RW     |
| DBB00OU | 22           | RW     | ABF_CR0   | 62           | RW     |         | A2           |        | OSC_CR2   | E2           | RW     |
|         | 23           |        | AMD_CR0   | 63           | RW     |         | A3           |        | VLT_CR    | E3           | RW     |
| DBB01FN | 24           | RW     | CMP_GO_EN | 64           | RW     |         | A4           |        | VLT_CMP   | E4           | R      |
| DBB01IN | 25           | RW     |           | 65           |        |         | A5           |        | ADC0_TR   | E5           | RW     |
| DBB01OU | 26           | RW     | AMD_CR1   | 66           | RW     |         | A6           |        | ADC1_TR   | E6           | RW     |
|         | 27           |        | ALT_CR0   | 67           | RW     |         | A7           |        |           | E7           |        |
| DCB02FN | 28           | RW     |           | 68           |        |         | A8           |        | IMO_TR    | E8           | W      |
| DCB02IN | 29           | RW     |           | 69           |        |         | A9           |        | ILO_TR    | E9           | W      |
| DCB02OU | 2A           | RW     |           | 6A           |        |         | AA           |        | BDG_TR    | EA           | RW     |
|         | 2B           |        | CLK_CR3   | 6B           | RW     |         | AB           |        | ECO_TR    | EB           | W      |
| DCB03FN | 2C           | RW     | TMP_DR0   | 6C           | RW     |         | AC           |        |           | EC           |        |
| DCB03IN | 2D           | RW     | TMP_DR1   | 6D           | RW     |         | AD           |        |           | ED           |        |
| DCB03OU | 2E           | RW     | TMP_DR2   | 6E           | RW     |         | AE           |        |           | EE           |        |
|         | 2F           |        | TMP_DR3   | 6F           | RW     |         | AF           |        |           | EF           |        |
|         | 30           |        |           | 70           |        | RDI0RI  | B0           | RW     |           | F0           |        |
|         | 31           |        |           | 71           |        | RDI0SYN | B1           | RW     |           | F1           |        |
|         | 32           |        | ACE00CR1  | 72           | RW     | RDI0IS  | B2           | RW     |           | F2           |        |
|         | 33           |        | ACE00CR2  | 73           | RW     | RDI0LT0 | B3           | RW     |           | F3           |        |
|         | 34           |        |           | 74           |        | RDI0LT1 | B4           | RW     |           | F4           |        |
|         | 35           |        |           | 75           |        | RDI0RO0 | B5           | RW     |           | F5           |        |
|         | 36           |        | ACE01CR1  | 76           | RW     | RDI0RO1 | B6           | RW     |           | F6           |        |
|         | 37           |        | ACE01CR2  | 77           | RW     |         | B7           |        | CPU_F     | F7           | RL     |
|         | 38           |        |           | 78           |        |         | B8           |        |           | F8           |        |
|         | 39           |        |           | 79           |        |         | B9           |        |           | F9           |        |
|         | 3A           |        |           | 7A           |        |         | BA           |        | FLS_PR1   | FA           | RW     |
|         | 3B           |        |           | 7B           |        |         | BB           |        |           | FB           |        |
|         | 3C           |        |           | 7C           |        |         | BC           |        |           | FC           |        |
|         | 3D           |        |           | 7D           |        |         | BD           |        |           | FD           |        |
|         | 3E           |        |           | 7E           |        |         | BE           |        | CPU_SCR1  | FE           | #      |
|         | 3F           |        |           | 7F           |        |         | BF           |        | CPU_SCR0  | FF           | #      |

Blank fields are Reserved and must not be accessed.

# Access is bit specific.

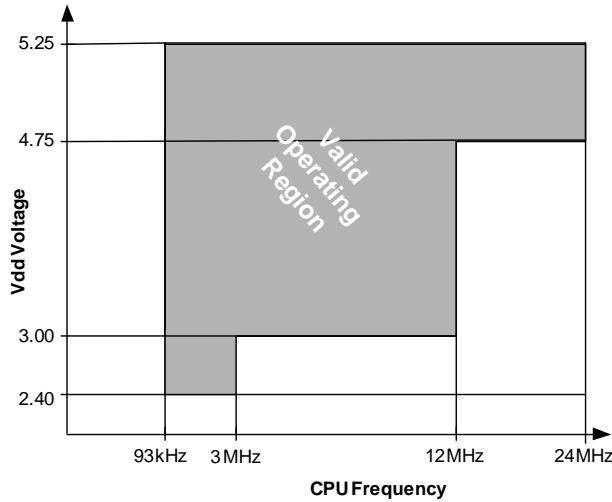
## Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C21x23 PSoC device. For up to date electrical specifications, check if you have the latest data sheet by visiting the web at <http://www.cypress.com/psoc>.

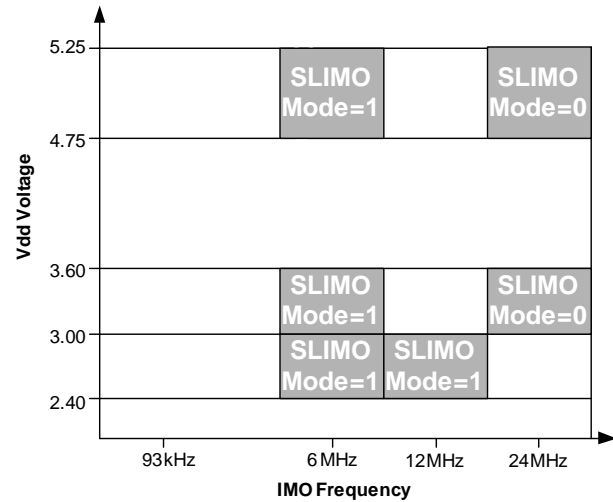
Specifications are valid for  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  and  $T_J \leq 100^{\circ}\text{C}$ , except where noted.

Refer to [Table 25](#) on page 25 for the electrical specifications on the internal main oscillator (IMO) using SLIMO mode.

**Figure 10. Voltage versus CPU Frequency**



**Figure 11. Voltage versus IMO Frequency**



The following table lists the units of measure that are used in this section.

**Table 11. Units of Measure**

| Symbol                     | Unit of Measure             | Symbol        | Unit of Measure               |
|----------------------------|-----------------------------|---------------|-------------------------------|
| $^{\circ}\text{C}$         | degree Celsius              | $\mu\text{W}$ | microwatts                    |
| dB                         | decibels                    | mA            | milli-ampere                  |
| fF                         | femto farad                 | ms            | milli-second                  |
| Hz                         | hertz                       | mV            | milli-volts                   |
| KB                         | 1024 bytes                  | nA            | nanoampere                    |
| Kbit                       | 1024 bits                   | ns            | nanosecond                    |
| kHz                        | kilohertz                   | nV            | nanovolts                     |
| k $\Omega$                 | kilohm                      | W             | ohm                           |
| MHz                        | megahertz                   | pA            | picoampere                    |
| M $\Omega$                 | megaohm                     | pF            | picofarad                     |
| $\mu\text{A}$              | microampere                 | pp            | peak-to-peak                  |
| $\mu\text{F}$              | microfarad                  | ppm           | parts per million             |
| $\mu\text{H}$              | microhenry                  | ps            | picosecond                    |
| $\mu\text{s}$              | microsecond                 | sps           | samples per second            |
| $\mu\text{V}$              | microvolts                  | s             | sigma: one standard deviation |
| $\mu\text{V}_{\text{rms}}$ | microvolts root-mean-square | V             | volts                         |

### Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

**Table 12. Absolute Maximum Ratings**

| Symbol           | Description   | Min                   | Typ | Max                   | Units | Notes   |
|------------------|---|-----------------------|-----|-----------------------|-------|---|
| T <sub>STG</sub> | Storage Temperature   | -55                   | –   | +100                  | °C    | Higher storage temperatures reduce data retention time. Recommended storage temperature is +25°C ± 25°C. Extended duration storage temperatures above 65°C degrade reliability. |
| T <sub>A</sub>   | Ambient Temperature with Power Applied                        | -40                   | –   | +85                   | °C    |   |
| V <sub>DD</sub>  | Supply Voltage on V <sub>DD</sub> Relative to V <sub>SS</sub> | -0.5                  | –   | +6.0                  | V     |   |
| V <sub>IO</sub>  | DC Input Voltage  | V <sub>SS</sub> - 0.5 | –   | V <sub>DD</sub> + 0.5 | V     |   |
| V <sub>IOZ</sub> | DC Voltage Applied to Tristate                                | V <sub>SS</sub> - 0.5 | –   | V <sub>DD</sub> + 0.5 | V     |   |
| I <sub>MIO</sub> | Maximum Current into any Port Pin                             | -25                   | –   | +50                   | mA    |   |
| ESD              | Electro Static Discharge Voltage                              | 2000                  | –   | –                     | V     | Human Body Model ESD  |
| LU               | Latch up Current  | –                     | –   | 200                   | mA    |   |

### Operating Temperature

**Table 13. Operating Temperature**

| Symbol         | Description          | Min | Typ | Max  | Units | Notes  |
|----------------|----------------------|-----|-----|------|-------|--|
| T <sub>A</sub> | Ambient Temperature  | -40 | –   | +85  | °C    |  |
| T <sub>J</sub> | Junction Temperature | -40 | –   | +100 | °C    | The temperature rise from ambient to junction is package specific. See <a href="#">Table 37</a> on page 34. The user must limit the power consumption to comply with this requirement. |



**DC Electrical Characteristics**
*DC Chip-Level Specifications*

Table 14 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 2.4V to 3.0V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

**Table 14. DC Chip-Level Specifications**

| Symbol             | Description   | Min                      | Typ              | Max                      | Units | Notes   |
|--------------------|---|--------------------------|------------------|--------------------------|-------|---|
| V <sub>DD</sub>    | Supply Voltage  | 2.40                     | –                | 5.25                     | V     | See DC POR and LVD specifications, Table 21 on page 21.   |
| I <sub>DD</sub>    | Supply Current, IMO = 24 MHz  | –                        | 3                | 4                        | mA    | Conditions are V <sub>DD</sub> = 5.0V, 25°C, CPU = 3 MHz, SYSCLK doubler disabled. VC1 = 1.5 MHz<br>VC2 = 93.75 kHz<br>VC3 = 0.366 kHz. |
| I <sub>DD3</sub>   | Supply Current, IMO = 6 MHz   | –                        | 1.2              | 2                        | mA    | Conditions are V <sub>DD</sub> = 3.3V, 25°C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz<br>VC2 = 23.4 kHz<br>VC3 = 0.091 kHz    |
| I <sub>DD27</sub>  | Supply Current, IMO = 6 MHz   | –                        | 1.1              | 1.5                      | mA    | Conditions are V <sub>DD</sub> = 2.55V, 25°C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz<br>VC2 = 23.4 kHz<br>VC3 = 0.091 kHz   |
| I <sub>SB27</sub>  | Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active. Mid temperature range. | –                        | 2.6              | 4                        | μA    | V <sub>DD</sub> = 2.55V, 0°C to 40°C  |
| I <sub>SB</sub>    | Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active.                        | –                        | 2.8              | 5                        | μA    | V <sub>DD</sub> = 3.3V, $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  |
| V <sub>REF</sub>   | Reference Voltage (Bandgap)   | 1.28                     | 1.30             | 1.32                     | V     | Trimmed for appropriate V <sub>DD</sub> . V <sub>DD</sub> = 3.0V to 5.25V   |
| V <sub>REF27</sub> | Reference Voltage (Bandgap)   | 1.16                     | 1.30             | 1.330                    | V     | Trimmed for appropriate V <sub>DD</sub> . V <sub>DD</sub> = 2.4V to 3.0V  |
| AGND               | Analog Ground   | V <sub>REF</sub> - 0.003 | V <sub>REF</sub> | V <sub>REF</sub> + 0.003 | V     |   |

**DC General Purpose IO Specifications**

Table 15 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at  $25^{\circ}\text{C}$  and are for design guidance only.

**Table 15. 5V and 3.3V DC GPIO Specifications**

| Symbol           | Description                       | Min                   | Typ | Max  | Units      | Notes  |
|------------------|-----------------------------------|-----------------------|-----|------|------------|--|
| R <sub>PU</sub>  | Pull up Resistor                  | 4                     | 5.6 | 8    | k $\Omega$ |  |
| R <sub>PD</sub>  | Pull down Resistor                | 4                     | 5.6 | 8    | k $\Omega$ |  |
| V <sub>OH</sub>  | High Output Level                 | V <sub>DD</sub> - 1.0 | –   | –    | V          | I <sub>OH</sub> = 10 mA, V <sub>DD</sub> = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined I <sub>OH</sub> budget.  |
| V <sub>OL</sub>  | Low Output Level                  | –                     | –   | 0.75 | V          | I <sub>OL</sub> = 25 mA, V <sub>DD</sub> = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined I <sub>OL</sub> budget. |
| V <sub>IL</sub>  | Input Low Level                   | –                     | –   | 0.8  | V          | V <sub>DD</sub> = 3.0 to 5.25  |
| V <sub>IH</sub>  | Input High Level                  | 2.1                   | –   | –    | V          | V <sub>DD</sub> = 3.0 to 5.25  |
| V <sub>H</sub>   | Input Hysteresis                  | –                     | 60  | –    | mV         |  |
| I <sub>IL</sub>  | Input Leakage (Absolute Value)    | –                     | 1   | –    | nA         | Gross tested to 1 $\mu\text{A}$  |
| C <sub>IN</sub>  | Capacitive Load on Pins as Input  | –                     | 3.5 | 10   | pF         | Package and pin dependent. Temp = $25^{\circ}\text{C}$   |
| C <sub>OUT</sub> | Capacitive Load on Pins as Output | –                     | 3.5 | 10   | pF         | Package and pin dependent. Temp = $25^{\circ}\text{C}$   |

Table 16 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 2.4V to 3.0V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ . Typical parameters apply to 2.7V at  $25^{\circ}\text{C}$  and are for design guidance only.

**Table 16. 2.7V DC GPIO Specifications**

| Symbol           | Description                       | Min                   | Typ | Max  | Units      | Notes  |
|------------------|-----------------------------------|-----------------------|-----|------|------------|--|
| R <sub>PU</sub>  | Pull up Resistor                  | 4                     | 5.6 | 8    | k $\Omega$ |  |
| R <sub>PD</sub>  | Pull down Resistor                | 4                     | 5.6 | 8    | k $\Omega$ |  |
| V <sub>OH</sub>  | High Output Level                 | V <sub>DD</sub> - 0.4 | –   | –    | V          | I <sub>OH</sub> = 2.5 mA (6.25 Typ), V <sub>DD</sub> = 2.4 to 3.0V (16 mA maximum, 50 mA Typ combined I <sub>OH</sub> budget). |
| V <sub>OL</sub>  | Low Output Level                  | –                     | –   | 0.75 | V          | I <sub>OL</sub> = 10 mA, V <sub>DD</sub> = 2.4 to 3.0V (90 mA maximum combined I <sub>OL</sub> budget).                        |
| V <sub>IL</sub>  | Input Low Level                   | –                     | –   | 0.75 | V          | V <sub>DD</sub> = 2.4 to 3.0   |
| V <sub>IH</sub>  | Input High Level                  | 2.0                   | –   | –    | V          | V <sub>DD</sub> = 2.4 to 3.0   |
| V <sub>H</sub>   | Input Hysteresis                  | –                     | 60  | –    | mV         |  |
| I <sub>IL</sub>  | Input Leakage (Absolute Value)    | –                     | 1   | –    | nA         | Gross tested to 1 $\mu\text{A}$  |
| C <sub>IN</sub>  | Capacitive Load on Pins as Input  | –                     | 3.5 | 10   | pF         | Package and pin dependent. Temp = $25^{\circ}\text{C}$   |
| C <sub>OUT</sub> | Capacitive Load on Pins as Output | –                     | 3.5 | 10   | pF         | Package and pin dependent. Temp = $25^{\circ}\text{C}$   |

**DC Amplifier Specifications**

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 2.4V to 3.0V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

**Table 17. 5V DC Amplifier Specifications**

| Symbol                     | Description                                | Min | Typ | Max     | Units                          | Notes                                     |
|----------------------------|--|-----|-----|---------|--------------------------------|---|
| $V_{\text{OSOA}}$          | Input Offset Voltage (absolute value)      | –   | 2.5 | 15      | mV                             |   |
| $\text{TCV}_{\text{OSOA}}$ | Average Input Offset Voltage Drift         | –   | 10  | –       | $\mu\text{V}/^{\circ}\text{C}$ |   |
| $I_{\text{EBOA}}$          | Input Leakage Current (Port 0 Analog Pins) | –   | 200 | –       | pA                             | Gross tested to 1 $\mu\text{A}$           |
| $C_{\text{INOA}}$          | Input Capacitance (Port 0 Analog Pins)     | –   | 4.5 | 9.5     | pF                             | Package and pin dependent.<br>Temp = 25°C |
| $V_{\text{CMOA}}$          | Common Mode Voltage Range                  | 0.0 | –   | Vdd - 1 | V                              |   |
| $G_{\text{OLOA}}$          | Open Loop Gain                             | 80  | –   | –       | dB                             |   |
| $I_{\text{SOA}}$           | Amplifier Supply Current                   | –   | 10  | 30      | $\mu\text{A}$                  |   |

**Table 18. 3.3V DC Amplifier Specifications**

| Symbol                     | Description                                | Min | Typ | Max     | Units                          | Notes                                     |
|----------------------------|--|-----|-----|---------|--------------------------------|---|
| $V_{\text{OSOA}}$          | Input Offset Voltage (absolute value)      | –   | 2.5 | 15      | mV                             |   |
| $\text{TCV}_{\text{OSOA}}$ | Average Input Offset Voltage Drift         | –   | 10  | –       | $\mu\text{V}/^{\circ}\text{C}$ |   |
| $I_{\text{EBOA}}$          | Input Leakage Current (Port 0 Analog Pins) | –   | 200 | –       | pA                             | Gross tested to 1 $\mu\text{A}$           |
| $C_{\text{INOA}}$          | Input Capacitance (Port 0 Analog Pins)     | –   | 4.5 | 9.5     | pF                             | Package and pin dependent.<br>Temp = 25°C |
| $V_{\text{CMOA}}$          | Common Mode Voltage Range                  | 0   | –   | Vdd - 1 | V                              |   |
| $G_{\text{OLOA}}$          | Open Loop Gain                             | 80  | –   | –       | dB                             |   |
| $I_{\text{SOA}}$           | Amplifier Supply Current                   | –   | 10  | 30      | $\mu\text{A}$                  |   |

**Table 19. 2.7V DC Amplifier Specifications**

| Symbol                     | Description                                | Min | Typ | Max     | Units                          | Notes                                     |
|----------------------------|--|-----|-----|---------|--------------------------------|---|
| $V_{\text{OSOA}}$          | Input Offset Voltage (absolute value)      | –   | 2.5 | 15      | mV                             |   |
| $\text{TCV}_{\text{OSOA}}$ | Average Input Offset Voltage Drift         | –   | 10  | –       | $\mu\text{V}/^{\circ}\text{C}$ |   |
| $I_{\text{EBOA}}$          | Input Leakage Current (Port 0 Analog Pins) | –   | 200 | –       | pA                             | Gross tested to 1 $\mu\text{A}$           |
| $C_{\text{INOA}}$          | Input Capacitance (Port 0 Analog Pins)     | –   | 4.5 | 9.5     | pF                             | Package and pin dependent.<br>Temp = 25°C |
| $V_{\text{CMOA}}$          | Common Mode Voltage Range                  | 0   | –   | Vdd - 1 | V                              |   |
| $G_{\text{OLOA}}$          | Open Loop Gain                             | 80  | –   | –       | dB                             |   |
| $I_{\text{SOA}}$           | Amplifier Supply Current                   | –   | 10  | 30      | $\mu\text{A}$                  |   |

### DC Switch Mode Pump Specifications

Table 20 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 2.4V to 3.0V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at  $25^{\circ}\text{C}$  and are for design guidance only.

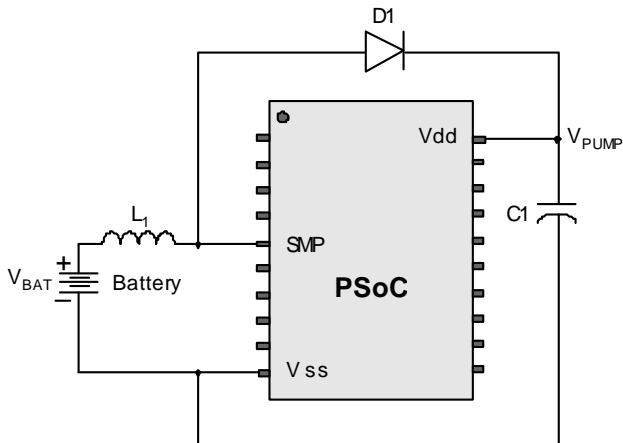
**Table 20. DC Switch Mode Pump (SMP) Specifications**

| Symbol                           | Description  | Min         | Typ         | Max         | Units          | Notes  |
|----------------------------------|--|-------------|-------------|-------------|----------------|--|
| $V_{\text{PUMP5V}}$              | 5V Output Voltage from Pump  | 4.75        | 5.0         | 5.25        | V              | Configuration of footnote. <sup>[6]</sup> Average, neglecting ripple. SMP trip voltage is set to 5.0V.   |
| $V_{\text{PUMP3V}}$              | 3.3V Output Voltage from Pump  | 3.00        | 3.25        | 3.60        | V              | Configuration of footnote. <sup>[6]</sup> Average, neglecting ripple. SMP trip voltage is set to 3.25V.  |
| $V_{\text{PUMP2V}}$              | 2.6V Output Voltage from Pump  | 2.45        | 2.55        | 2.80        | V              | Configuration of footnote. <sup>[6]</sup> Average, neglecting ripple. SMP trip voltage is set to 2.55V.  |
| $I_{\text{PUMP}}$                | Available Output Current<br>$V_{\text{BAT}} = 1.8\text{V}$ , $V_{\text{PUMP}} = 5.0\text{V}$<br>$V_{\text{BAT}} = 1.5\text{V}$ , $V_{\text{PUMP}} = 3.25\text{V}$<br>$V_{\text{BAT}} = 1.3\text{V}$ , $V_{\text{PUMP}} = 2.55\text{V}$ | 5<br>8<br>8 | –<br>–<br>– | –<br>–<br>– | mA<br>mA<br>mA | Configuration of footnote. <sup>[6]</sup><br>SMP trip voltage is set to 5.0V.<br>SMP trip voltage is set to 3.25V.<br>SMP trip voltage is set to 2.55V.                            |
| $V_{\text{BAT5V}}$               | Input Voltage Range from Battery   | 1.8         | –           | 5.0         | V              | Configuration of footnote. <sup>[6]</sup> SMP trip voltage is set to 5.0V.   |
| $V_{\text{BAT3V}}$               | Input Voltage Range from Battery   | 1.0         | –           | 3.3         | V              | Configuration of footnote. <sup>[6]</sup> SMP trip voltage is set to 3.25V.  |
| $V_{\text{BAT2V}}$               | Input Voltage Range from Battery   | 1.0         | –           | 2.8         | V              | Configuration of footnote. <sup>[6]</sup> SMP trip voltage is set to 2.55V.  |
| $V_{\text{BATSTART}}$            | Minimum Input Voltage from Battery to Start Pump   | 1.2         | –           | –           | V              | Configuration of footnote. <sup>[6]</sup> $0^{\circ}\text{C} \leq T_A \leq 100$ . 1.25V at $T_A = -40^{\circ}\text{C}$ .   |
| $\Delta V_{\text{PUMP\_Line}}$   | Line Regulation (over $V_i$ range)   | –           | 5           | –           | % $V_O$        | Configuration of footnote. <sup>[6]</sup> $V_O$ is the “Vdd Value for PUMP Trip” specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 21 on page 21.        |
| $\Delta V_{\text{PUMP\_Load}}$   | Load Regulation  | –           | 5           | –           | % $V_O$        | Configuration of footnote. <sup>[6]</sup> $V_O$ is the “Vdd Value for PUMP Trip” specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 21 on page 21.        |
| $\Delta V_{\text{PUMP\_Ripple}}$ | Output Voltage Ripple (depends on cap/load)  | –           | 100         | –           | mVpp           | Configuration of footnote. <sup>[6]</sup> Load is 5 mA.  |
| $E_3$                            | Efficiency   | 35          | 50          | –           | %              | Configuration of footnote. <sup>[6]</sup> Load is 5 mA. SMP trip voltage is set to 3.25V.  |
| $E_2$                            | Efficiency   | 35          | 80          | –           | %              | For $I_{\text{load}} = 1\text{mA}$ , $V_{\text{PUMP}} = 2.55\text{V}$ , $V_{\text{BAT}} = 1.3\text{V}$ , 10 $\mu\text{H}$ inductor, 1 $\mu\text{F}$ capacitor, and Schottky diode. |
| $F_{\text{PUMP}}$                | Switching Frequency  | –           | 1.3         | –           | MHz            |  |
| $\text{DC}_{\text{PUMP}}$        | Switching Duty Cycle   | –           | 50          | –           | %              |  |

**Note**

6.  $L_1 = 2\text{mH}$  inductor,  $C_1 = 10\text{mF}$  capacitor,  $D_1 = \text{Schottky diode}$ . See Figure 12 on page 21.

Figure 12. Basic Switch Mode Pump Circuit



DC POR and LVD Specifications

Table 21 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T<sub>A</sub> ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T<sub>A</sub> ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T<sub>A</sub> ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 21. DC POR and LVD Specifications

| Symbol             | Description                                  | Min  | Typ  | Max                  | Units | Notes  |
|--------------------|--|------|------|----------------------|-------|--|
| V <sub>PPOR0</sub> | Vdd Value for PPOR Trip<br>PORLEV[1:0] = 00b |      | 2.36 | 2.40                 | V     | Vdd must be greater than or equal to 2.5V during startup, reset from the XRES pin, or reset from Watchdog. |
| V <sub>PPOR1</sub> | PORLEV[1:0] = 01b                            | –    | 2.82 | 2.95                 | V     |  |
| V <sub>PPOR2</sub> | PORLEV[1:0] = 10b                            |      | 4.55 | 4.70                 | V     |  |
| V <sub>LVD0</sub>  | Vdd Value for LVD Trip<br>VM[2:0] = 000b     | 2.40 | 2.45 | 2.51 <sup>[7]</sup>  | V     |  |
| V <sub>LVD1</sub>  | VM[2:0] = 001b                               | 2.85 | 2.92 | 2.99 <sup>[8]</sup>  | V     |  |
| V <sub>LVD2</sub>  | VM[2:0] = 010b                               | 2.95 | 3.02 | 3.09                 | V     |  |
| V <sub>LVD3</sub>  | VM[2:0] = 011b                               | 3.06 | 3.13 | 3.20                 | V     |  |
| V <sub>LVD4</sub>  | VM[2:0] = 100b                               | 4.37 | 4.48 | 4.55                 | V     |  |
| V <sub>LVD5</sub>  | VM[2:0] = 101b                               | 4.50 | 4.64 | 4.75                 | V     |  |
| V <sub>LVD6</sub>  | VM[2:0] = 110b                               | 4.62 | 4.73 | 4.83                 | V     |  |
| V <sub>LVD7</sub>  | VM[2:0] = 111b                               | 4.71 | 4.81 | 4.95                 | V     |  |
| V <sub>PUMP0</sub> | Vdd Value for PUMP Trip<br>VM[2:0] = 000b    | 2.45 | 2.55 | 2.62 <sup>[9]</sup>  | V     |  |
| V <sub>PUMP1</sub> | VM[2:0] = 001b                               | 2.96 | 3.02 | 3.09                 | V     |  |
| V <sub>PUMP2</sub> | VM[2:0] = 010b                               | 3.03 | 3.10 | 3.16                 | V     |  |
| V <sub>PUMP3</sub> | VM[2:0] = 011b                               | 3.18 | 3.25 | 3.32 <sup>[10]</sup> | V     |  |
| V <sub>PUMP4</sub> | VM[2:0] = 100b                               | 4.54 | 4.64 | 4.74                 | V     |  |
| V <sub>PUMP5</sub> | VM[2:0] = 101b                               | 4.62 | 4.73 | 4.83                 | V     |  |
| V <sub>PUMP6</sub> | VM[2:0] = 110b                               | 4.71 | 4.82 | 4.92                 | V     |  |
| V <sub>PUMP7</sub> | VM[2:0] = 111b                               | 4.89 | 5.00 | 5.12                 | V     |  |

Notes

7. Always greater than 50 mV above V<sub>PPOR</sub> (PORLEV = 00) for falling supply.
8. Always greater than 50 mV above V<sub>PPOR</sub> (PORLEV = 01) for falling supply.
9. Always greater than 50 mV above V<sub>LVD0</sub>.
10. Always greater than 50 mV above V<sub>LVD3</sub>.

### DC Programming Specifications

Table 22 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 2.4V to 3.0V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at  $25^{\circ}\text{C}$  and are for design guidance only.

**Table 22. DC Programming Specifications**

| Symbol                | Description   | Min                   | Typ | Max                    | Units | Notes                               |
|-----------------------|---|-----------------------|-----|------------------------|-------|-------------------------------------|
| Vdd <sub>IWRITE</sub> | Supply Voltage for Flash Write Operations   | 2.70                  | –   | –                      | V     |                                     |
| I <sub>DDP</sub>      | Supply Current During Programming or Verify   | –                     | 5   | 25                     | mA    |                                     |
| V <sub>ILP</sub>      | Input Low Voltage During Programming or Verify  | –                     | –   | 0.8                    | V     |                                     |
| V <sub>IHP</sub>      | Input High Voltage During Programming or Verify   | 2.2                   | –   | –                      | V     |                                     |
| I <sub>ILP</sub>      | Input Current when Applying V <sub>ilp</sub> to P1[0] or P1[1] During Programming or Verify | –                     | –   | 0.2                    | mA    | Driving internal pull down resistor |
| I <sub>IHP</sub>      | Input Current when Applying V <sub>ihp</sub> to P1[0] or P1[1] During Programming or Verify | –                     | –   | 1.5                    | mA    | Driving internal pull down resistor |
| V <sub>OLV</sub>      | Output Low Voltage During Programming or Verify   | –                     | –   | V <sub>ss</sub> + 0.75 | V     |                                     |
| V <sub>OHV</sub>      | Output High Voltage During Programming or Verify  | V <sub>dd</sub> - 1.0 | –   | V <sub>dd</sub>        | V     |                                     |
| Flash <sub>ENPB</sub> | Flash Endurance (per block)   | 50,000                | –   | –                      | –     | Erase/write cycles per block        |
| Flash <sub>ENT</sub>  | Flash Endurance (total) <sup>[11]</sup>   | 1,800,000             | –   | –                      | –     | Erase/write cycles                  |
| Flash <sub>DR</sub>   | Flash Data Retention  | 10                    | –   | –                      | Years |                                     |

**Note**

11. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (and so forth to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles). For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at <http://www.cypress.com> under Application Notes for more information.

**AC Electrical Characteristics**
*AC Chip-Level Specifications*

Table 23 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 2.4V to 3.0V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

**Table 23. 5V and 3.3V AC Chip-Level Specifications**

| Symbol              | Description   | Min  | Typ  | Max                        | Units | Notes   |
|---------------------|---|------|------|----------------------------|-------|---|
| F <sub>IMO24</sub>  | Internal Main Oscillator Frequency for 24 MHz           | 23.4 | 24   | 24.6 <sup>[12,13,14]</sup> | MHz   | Trimmed for 5V or 3.3V operation using factory trim values. See Figure 11 on page 15. SLIMO mode = 0. |
| F <sub>IMO6</sub>   | Internal Main Oscillator Frequency for 6 MHz            | 5.75 | 6    | 6.35 <sup>[12,13,14]</sup> | MHz   | Trimmed for 3.3V operation using factory trim values. See Figure 11 on page 15. SLIMO mode = 1.       |
| F <sub>CPU1</sub>   | CPU Frequency (5V Nominal)                              | 0.93 | 24   | 24.6 <sup>[12,13]</sup>    | MHz   | 24 MHz only for SLIMO mode = 0.   |
| F <sub>CPU2</sub>   | CPU Frequency (3.3V Nominal)                            | 0.93 | 12   | 12.3 <sup>[13,14]</sup>    | MHz   |   |
| F <sub>BLK5</sub>   | Digital PSoC Block Frequency (5V Nominal)               | 0    | 48   | 49.2 <sup>[12,13,15]</sup> | MHz   | Refer to the AC Digital Block Specifications.   |
| F <sub>BLK33</sub>  | Digital PSoC Block Frequency (3.3V Nominal)             | 0    | 24   | 24.6 <sup>[13,15]</sup>    | MHz   |   |
| F <sub>32K1</sub>   | Internal Low Speed Oscillator Frequency                 | 15   | 32   | 64                         | kHz   |   |
| Jitter32k           | 32 kHz RMS Period Jitter                                | –    | 100  | 200                        | ns    |   |
| Jitter32k           | 32 kHz Peak-to-Peak Period Jitter                       | –    | 1400 | –                          | ns    |   |
| T <sub>XRST</sub>   | External Reset Pulse Width                              | 10   | –    | –                          | μs    |   |
| DC24M               | 24 MHz Duty Cycle                                       | 40   | 50   | 60                         | %     |   |
| Step24M             | 24 MHz Trim Step Size                                   | –    | 50   | –                          | kHz   |   |
| F <sub>out48M</sub> | 48 MHz Output Frequency                                 | 46.8 | 48.0 | 49.2 <sup>[12,14]</sup>    | MHz   | Trimmed. Using factory trim values.   |
| Jitter24M1          | 24 MHz Peak-to-Peak Period Jitter (IMO)                 | –    | 300  | –                          | ps    |   |
| F <sub>MAX</sub>    | Maximum frequency of signal on row input or row output. | –    | –    | 12.3                       | MHz   |   |
| T <sub>RAMP</sub>   | Supply Ramp Time  | 0    | –    | –                          | μs    |   |

**Notes**

12. 4.75V < V<sub>dd</sub> < 5.25V.

13. Accuracy derived from Internal Main Oscillator with appropriate trim for V<sub>dd</sub> range.

14. 3.0V < V<sub>dd</sub> < 3.6V. See application note AN2012 "Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation" for information on trimming for operation at 3.3V.

15. See the individual user module data sheets for information on maximum frequencies for user modules.

Table 24. 2.7V AC Chip-Level Specifications

| Symbol             | Description  | Min   | Typ  | Max                        | Units | Notes   |
|--------------------|--|-------|------|----------------------------|-------|---|
| F <sub>IMO12</sub> | Internal Main Oscillator Frequency for 12 MHz          | 11.5  | 12   | 12.7 <sup>[16,17,18]</sup> | MHz   | Trimmed for 2.7V operation using factory trim values. See Figure 11 on page 15. SLIMO mode = 1. |
| F <sub>IMO6</sub>  | Internal Main Oscillator Frequency for 6 MHz           | 5.5   | 6    | 6.35 <sup>[16,17,18]</sup> | MHz   | Trimmed for 2.7V operation using factory trim values. See Figure 11 on page 15. SLIMO mode = 1. |
| F <sub>CPU1</sub>  | CPU Frequency (2.7V Nominal)                           | 0.093 | 3    | 3.15 <sup>[16,17]</sup>    | MHz   | 24 MHz only for SLIMO mode = 0.   |
| F <sub>BLK27</sub> | Digital PSoC Block Frequency (2.7V Nominal)            | 0     | 12   | 12.5 <sup>[16,17,18]</sup> | MHz   | Refer to the AC Digital Block Specifications.   |
| F <sub>32K1</sub>  | Internal Low Speed Oscillator Frequency                | 8     | 32   | 96                         | kHz   |   |
| Jitter32k          | 32 kHz RMS Period Jitter                               | –     | 150  | 200                        | ns    |   |
| Jitter32k          | 32 kHz Peak-to-Peak Period Jitter                      | –     | 1400 | –                          | ns    |   |
| T <sub>XRST</sub>  | External Reset Pulse Width                             | 10    | –    | –                          | μs    |   |
| F <sub>MAX</sub>   | Maximum frequency of signal on row input or row output | –     | –    | 12.3                       | MHz   |   |
| T <sub>RAMP</sub>  | Supply Ramp Time                                       | 0     | –    | –                          | μs    |   |

Figure 13. 24 MHz Period Jitter (IMO) Timing Diagram



Figure 14. 32 kHz Period Jitter (ILO) Timing Diagram



Notes

16. 2.4V < V<sub>dd</sub> < 3.0V.

17. Accuracy derived from Internal Main Oscillator with appropriate trim for V<sub>dd</sub> range.

18. See application note AN2012 "Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation" for information on maximum frequency for user modules.



*AC General Purpose IO Specifications*

Table 25 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 2.4V to 3.0V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

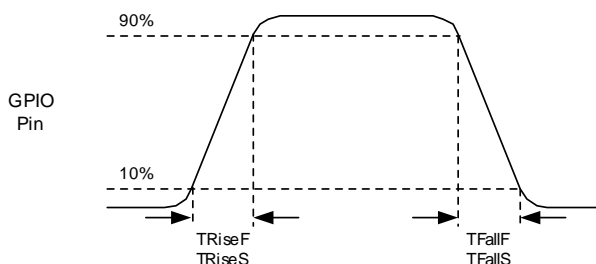
**Table 25. 5V and 3.3V AC GPIO Specifications**

| Symbol            | Description                                 | Min | Typ | Max | Units | Notes                         |
|-------------------|---|-----|-----|-----|-------|-------------------------------|
| F <sub>GPIO</sub> | GPIO Operating Frequency                    | 0   | –   | 12  | MHz   | Normal Strong Mode            |
| TRiseF            | Rise Time, Normal Strong Mode, Load = 50 pF | 3   | –   | 18  | ns    | Vdd = 4.5 to 5.25V, 10% - 90% |
| TFallF            | Fall Time, Normal Strong Mode, Load = 50 pF | 2   | –   | 18  | ns    | Vdd = 4.5 to 5.25V, 10% - 90% |
| TRiseS            | Rise Time, Slow Strong Mode, Load = 50 pF   | 10  | 27  | –   | ns    | Vdd = 3 to 5.25V, 10% - 90%   |
| TFallS            | Fall Time, Slow Strong Mode, Load = 50 pF   | 10  | 22  | –   | ns    | Vdd = 3 to 5.25V, 10% - 90%   |

**Table 26. 2.7V AC GPIO Specifications**

| Symbol            | Description                                 | Min | Typ | Max | Units | Notes                        |
|-------------------|---|-----|-----|-----|-------|------------------------------|
| F <sub>GPIO</sub> | GPIO Operating Frequency                    | 0   | –   | 3   | MHz   | Normal Strong Mode           |
| TRiseF            | Rise Time, Normal Strong Mode, Load = 50 pF | 6   | –   | 50  | ns    | Vdd = 2.4 to 3.0V, 10% - 90% |
| TFallF            | Fall Time, Normal Strong Mode, Load = 50 pF | 6   | –   | 50  | ns    | Vdd = 2.4 to 3.0V, 10% - 90% |
| TRiseS            | Rise Time, Slow Strong Mode, Load = 50 pF   | 18  | 40  | 120 | ns    | Vdd = 2.4 to 3.0V, 10% - 90% |
| TFallS            | Fall Time, Slow Strong Mode, Load = 50 pF   | 18  | 40  | 120 | ns    | Vdd = 2.4 to 3.0V, 10% - 90% |

**Figure 15. GPIO Timing Diagram**



*AC Amplifier Specifications*

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 2.4V to 3.0V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

**Table 27. 5V and 3.3V AC Amplifier Specifications**

| Symbol             | Description   | Min | Typ | Max | Units |
|--------------------|---|-----|-----|-----|-------|
| T <sub>COMP1</sub> | Comparator Mode Response Time, 50 mVpp Signal Centered on Ref |     |     | 100 | ns    |
| T <sub>COMP2</sub> | Comparator Mode Response Time, 2.5V Input, 0.5V Overdrive     |     |     | 300 | ns    |

**Table 28. 2.7V AC Amplifier Specifications**

| Symbol             | Description   | Min | Typ | Max | Units |
|--------------------|---|-----|-----|-----|-------|
| T <sub>COMP1</sub> | Comparator Mode Response Time, 50 mVpp Signal Centered on Ref |     |     | 600 | ns    |
| T <sub>COMP2</sub> | Comparator Mode Response Time, 1.5V Input, 0.5V Overdrive     |     |     | 300 | ns    |

## AC Digital Block Specifications

Table 29 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 2.4V to 3.0V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at  $25^{\circ}\text{C}$  and are for design guidance only.

**Table 29. 5V and 3.3V AC Digital Block Specifications**

| Function          | Description                                | Min                | Typ | Max  | Units | Notes  |
|-------------------|--|--------------------|-----|------|-------|--|
| All Functions     | Maximum Block Clocking Frequency (> 4.75V) |                    |     | 49.2 | MHz   | 4.75V < Vdd < 5.25V                                    |
|                   | Maximum Block Clocking Frequency (< 4.75V) |                    |     | 24.6 | MHz   | 3.0V < Vdd < 4.75V                                     |
| Timer             | Capture Pulse Width                        | 50 <sup>[19]</sup> | –   | –    | ns    |  |
|                   | Maximum Frequency, No Capture              | –                  | –   | 49.2 | MHz   | 4.75V < Vdd < 5.25V                                    |
|                   | Maximum Frequency, With or Without Capture | –                  | –   | 24.6 | MHz   |  |
| Counter           | Enable Pulse Width                         | 50                 | –   | –    | ns    |  |
|                   | Maximum Frequency, No Enable Input         | –                  | –   | 49.2 | MHz   | 4.75V < Vdd < 5.25V                                    |
|                   | Maximum Frequency, Enable Input            | –                  | –   | 24.6 | MHz   |  |
| Dead Band         | Kill Pulse Width:                          |                    |     |      |       |  |
|                   | Asynchronous Restart Mode                  | 20                 | –   | –    | ns    |  |
|                   | Synchronous Restart Mode                   | 50                 | –   | –    | ns    |  |
|                   | Disable Mode                               | 50                 | –   | –    | ns    |  |
|                   | Maximum Frequency                          | –                  | –   | 49.2 | MHz   | 4.75V < Vdd < 5.25V                                    |
| CRCPRS (PRS Mode) | Maximum Input Clock Frequency              | –                  | –   | 49.2 | MHz   | 4.75V < Vdd < 5.25V                                    |
| CRCPRS (CRC Mode) | Maximum Input Clock Frequency              | –                  | –   | 24.6 | MHz   |  |
| SPIM              | Maximum Input Clock Frequency              | –                  | –   | 8.2  | MHz   | Maximum data rate at 4.1 MHz due to 2 x over clocking  |
| SPIS              | Maximum Input Clock Frequency              | –                  | –   | 4.1  | MHz   |  |
|                   | Width of SS_ Negated Between Transmissions | 50                 | –   | –    | ns    |  |
| Transmitter       | Maximum Input Clock Frequency              | –                  | –   | 24.6 | MHz   | Maximum data rate at 3.08 MHz due to 8 x over clocking |
| Receiver          | Maximum Input Clock Frequency              | –                  | –   | 24.6 | MHz   | Maximum data rate at 3.08 MHz due to 8 x over clocking |

**Note**

19. 50 ns minimum input pulse width is based on the input synchronizers running at 12 MHz (84 ns nominal period).

**Table 30. 2.7V AC Digital Block Specifications**

| Function          | Description                                | Min                 | Typ | Max  | Units | Notes  |
|-------------------|--|---------------------|-----|------|-------|--|
| All Functions     | Maximum Block Clocking Frequency           |                     |     | 12.7 | MHz   | 2.4V < Vdd < 3.0V                                      |
| Timer             | Capture Pulse Width                        | 100 <sup>[20]</sup> | –   | –    | ns    |  |
|                   | Maximum Frequency, With or Without Capture | –                   | –   | 12.7 | MHz   |  |
| Counter           | Enable Pulse Width                         | 100                 | –   | –    | ns    |  |
|                   | Maximum Frequency, No Enable Input         | –                   | –   | 12.7 | MHz   |  |
|                   | Maximum Frequency, Enable Input            | –                   | –   | 12.7 | MHz   |  |
| Dead Band         | Kill Pulse Width:                          |                     |     |      |       |  |
|                   | Asynchronous Restart Mode                  | 20                  | –   | –    | ns    |  |
|                   | Synchronous Restart Mode                   | 100                 | –   | –    | ns    |  |
|                   | Disable Mode                               | 100                 | –   | –    | ns    |  |
| CRCPRS (PRS Mode) | Maximum Input Clock Frequency              | –                   | –   | 12.7 | MHz   |  |
|                   | Maximum Input Clock Frequency              | –                   | –   | 12.7 | MHz   |  |
| SPIM              | Maximum Input Clock Frequency              | –                   | –   | 6.35 | MHz   | Maximum data rate at 3.17 MHz due to 2 x over clocking |
| SPIS              | Maximum Input Clock Frequency              | –                   | –   | 4.1  | MHz   |  |
|                   | Width of SS_ Negated Between Transmissions | 100                 | –   | –    | ns    |  |
| Transmitter       | Maximum Input Clock Frequency              | –                   | –   | 12.7 | MHz   | Maximum data rate at 1.59 MHz due to 8 x over clocking |
| Receiver          | Maximum Input Clock Frequency              | –                   | –   | 12.7 | MHz   | Maximum data rate at 1.59 MHz due to 8 x over clocking |

**Note**

20. 100 ns minimum input pulse width is based on the input synchronizers running at 12 MHz (84 ns nominal period).

**AC External Clock Specifications**

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at  $25^{\circ}\text{C}$  and are for design guidance only.

**Table 31. 5V AC External Clock Specifications**

| Symbol              | Description            | Min   | Typ | Max  | Units | Notes |
|---------------------|------------------------|-------|-----|------|-------|-------|
| F <sub>OSCEXT</sub> | Frequency              | 0.093 | –   | 24.6 | MHz   |       |
| –                   | High Period            | 20.6  | –   | 5300 | ns    |       |
| –                   | Low Period             | 20.6  | –   | –    | ns    |       |
| –                   | Power Up IMO to Switch | 150   | –   | –    | μs    |       |

**Table 32. 3.3V AC External Clock Specifications**

| Symbol              | Description                                     | Min   | Typ | Max  | Units | Notes   |
|---------------------|---|-------|-----|------|-------|---|
| F <sub>OSCEXT</sub> | Frequency with CPU Clock divide by 1            | 0.093 | –   | 12.3 | MHz   | Maximum CPU frequency is 12 MHz at 3.3V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.  |
| F <sub>OSCEXT</sub> | Frequency with CPU Clock divide by 2 or greater | 0.186 | –   | 24.6 | MHz   | If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met. |
| –                   | High Period with CPU Clock divide by 1          | 41.7  | –   | 5300 | ns    |   |
| –                   | Low Period with CPU Clock divide by 1           | 41.7  | –   | –    | ns    |   |
| –                   | Power Up IMO to Switch                          | 150   | –   | –    | μs    |   |

**Table 33. 2.7V AC External Clock Specifications**

| Symbol              | Description                                     | Min   | Typ | Max   | Units | Notes  |
|---------------------|---|-------|-----|-------|-------|--|
| F <sub>OSCEXT</sub> | Frequency with CPU Clock divide by 1            | 0.093 | –   | 6.06  | MHz   | Maximum CPU frequency is 3 MHz at 2.7V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.  |
| F <sub>OSCEXT</sub> | Frequency with CPU Clock divide by 2 or greater | 0.186 | –   | 12.12 | MHz   | If the frequency of the external clock is greater than 3 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met. |
| –                   | High Period with CPU Clock divide by 1          | 83.4  | –   | 5300  | ns    |  |
| –                   | Low Period with CPU Clock divide by 1           | 83.4  | –   | –     | ns    |  |
| –                   | Power Up IMO to Switch                          | 150   | –   | –     | μs    |  |

### AC Programming Specifications

Table 34 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at  $25^{\circ}\text{C}$  and are for design guidance only.

**Table 34. AC Programming Specifications**

| Symbol       | Description                              | Min | Typ | Max | Units | Notes                      |
|--------------|--|-----|-----|-----|-------|----------------------------|
| $T_{RSCLK}$  | Rise Time of SCLK                        | 1   | –   | 20  | ns    |                            |
| $T_{FSCLK}$  | Fall Time of SCLK                        | 1   | –   | 20  | ns    |                            |
| $T_{SSCLK}$  | Data Set up Time to Falling Edge of SCLK | 40  | –   | –   | ns    |                            |
| $T_{HSCLK}$  | Data Hold Time from Falling Edge of SCLK | 40  | –   | –   | ns    |                            |
| $F_{SCLK}$   | Frequency of SCLK                        | 0   | –   | 8   | MHz   |                            |
| $T_{ERASEB}$ | Flash Erase Time (Block)                 | –   | 15  | –   | ms    |                            |
| $T_{WRITE}$  | Flash Block Write Time                   | –   | 30  | –   | ms    |                            |
| $T_{DSCLK3}$ | Data Out Delay from Falling Edge of SCLK | –   | –   | 50  | ns    | $3.0 \leq V_{dd} \leq 3.6$ |
| $T_{DSCLK2}$ | Data Out Delay from Falling Edge of SCLK | –   | –   | 70  | ns    | $2.4 \leq V_{dd} \leq 3.0$ |

### AC I<sup>2</sup>C Specifications

Table 35 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , 3.0V to 3.6V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 2.4V to 3.0V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at  $25^{\circ}\text{C}$  and are for design guidance only.

**Table 35. AC Characteristics of the I<sup>2</sup>C SDA and SCL Pins for  $V_{cc} \geq 3.0\text{V}$**

| Symbol         | Description  | Standard Mode |     | Fast Mode           |     | Units         |
|----------------|--|---------------|-----|---------------------|-----|---------------|
|                |  | Min           | Max | Min                 | Max |               |
| $F_{SCLi2C}$   | SCL Clock Frequency  | 0             | 100 | 0                   | 400 | kHz           |
| $T_{HDSTAI2C}$ | Hold Time (repeated) START Condition. After this period, the first clock pulse is generated. | 4.0           | –   | 0.6                 | –   | $\mu\text{s}$ |
| $T_{LOWI2C}$   | LOW Period of the SCL Clock  | 4.7           | –   | 1.3                 | –   | $\mu\text{s}$ |
| $T_{HIGHI2C}$  | HIGH Period of the SCL Clock   | 4.0           | –   | 0.6                 | –   | $\mu\text{s}$ |
| $T_{SUSTAI2C}$ | Setup Time for a Repeated START Condition  | 4.7           | –   | 0.6                 | –   | $\mu\text{s}$ |
| $T_{HDDATI2C}$ | Data Hold Time   | 0             | –   | 0                   | –   | $\mu\text{s}$ |
| $T_{SUDATI2C}$ | Data Setup Time  | 250           | –   | 100 <sup>[20]</sup> | –   | ns            |
| $T_{SUSTOI2C}$ | Setup Time for STOP Condition  | 4.0           | –   | 0.6                 | –   | $\mu\text{s}$ |
| $T_{BUFI2C}$   | Bus Free Time Between a STOP and START Condition   | 4.7           | –   | 1.3                 | –   | $\mu\text{s}$ |
| $T_{SPI2C}$    | Pulse Width of spikes are suppressed by the input filter.                                    | –             | –   | 0                   | 50  | ns            |

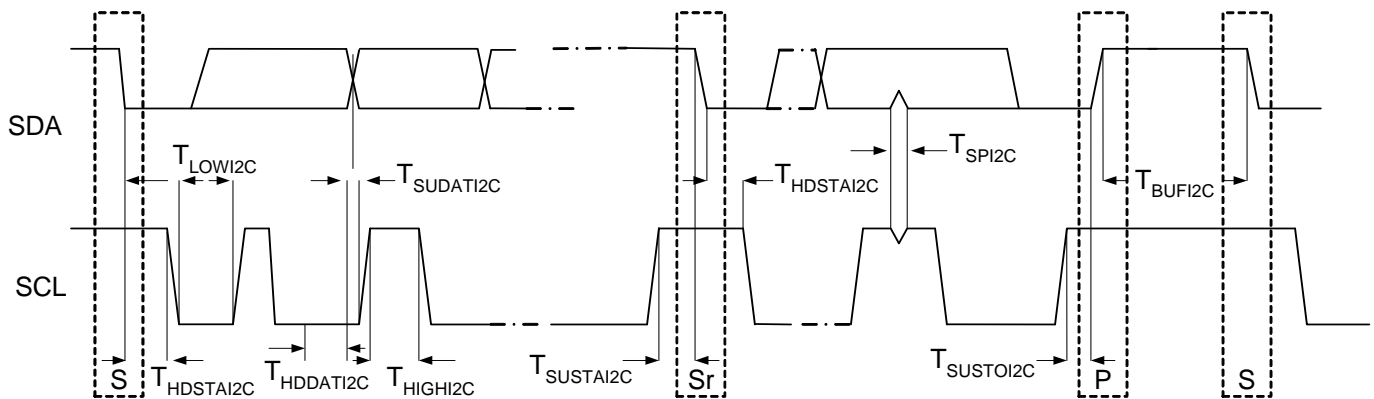
**Note**

20. A Fast-Mode I<sup>2</sup>C-bus device can be used in a Standard-Mode I<sup>2</sup>C-bus system, but the requirement  $t_{SU,DAT} \geq 250$  ns must then be met. This automatically becomes the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line  $t_{max} + t_{SU,DAT} = 1000 + 250 = 1250$  ns (according to the Standard-Mode I<sup>2</sup>C-bus specification) before the SCL line is released.

Table 36. 2.7V AC Characteristics of the I<sup>2</sup>C SDA and SCL Pins (Fast Mode Not Supported)

| Symbol                 | Description  | Standard Mode |     | Fast Mode |     | Units |
|------------------------|--|---------------|-----|-----------|-----|-------|
|                        |  | Min           | Max | Min       | Max |       |
| F <sub>SCL I2C</sub>   | SCL Clock Frequency  | 0             | 100 | –         | –   | kHz   |
| T <sub>HDSTAI2C</sub>  | Hold Time (repeated) START Condition. After this period, the first clock pulse is generated. | 4.0           | –   | –         | –   | μs    |
| T <sub>LOWI2C</sub>    | LOW Period of the SCL Clock  | 4.7           | –   | –         | –   | μs    |
| T <sub>HIGHI2C</sub>   | HIGH Period of the SCL Clock   | 4.0           | –   | –         | –   | μs    |
| T <sub>SUSTA I2C</sub> | Setup Time for a Repeated START Condition  | 4.7           | –   | –         | –   | μs    |
| T <sub>HDDAT I2C</sub> | Data Hold Time   | 0             | –   | –         | –   | μs    |
| T <sub>SUDAT I2C</sub> | Data Setup Time  | 250           | –   | –         | –   | ns    |
| T <sub>SUSTO I2C</sub> | Setup Time for STOP Condition  | 4.0           | –   | –         | –   | μs    |
| T <sub>BUFI2C</sub>    | Bus Free Time Between a STOP and START Condition   | 4.7           | –   | –         | –   | μs    |
| T <sub>SPI2C</sub>     | Pulse Width of spikes are suppressed by the input filter.                                    | –             | –   | –         | –   | ns    |

Figure 16. Definition for Timing for Fast/Standard Mode on the I<sup>2</sup>C Bus



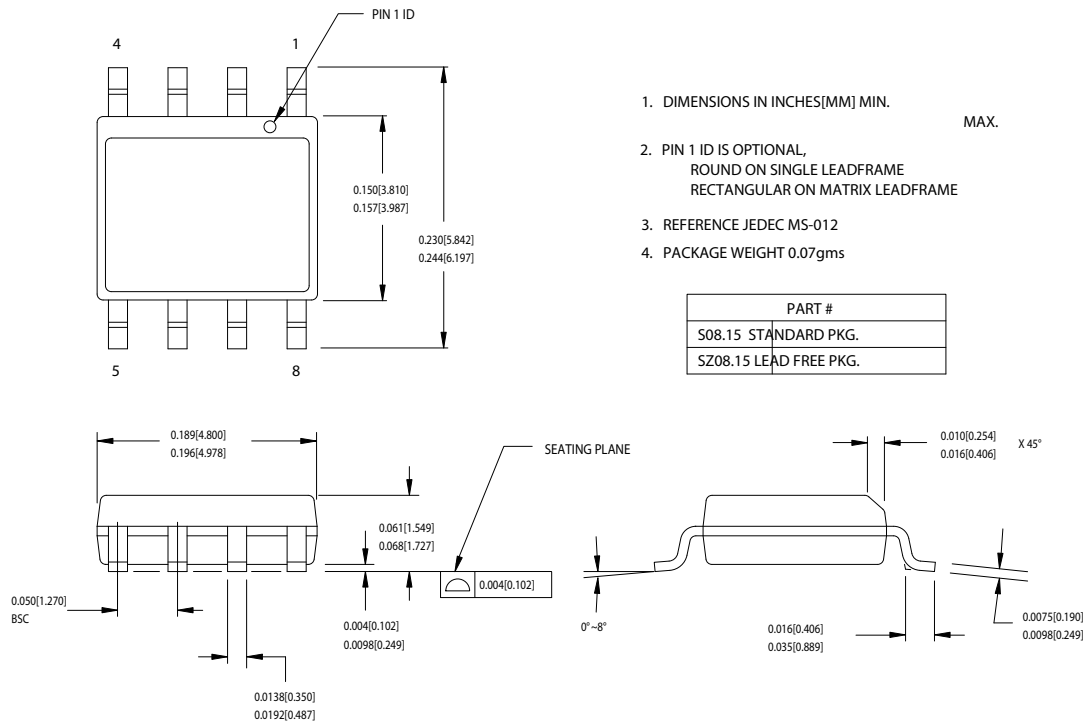
## Packaging Information

This section illustrates the packaging specifications for the CY8C21x23 PSoC device, along with the thermal impedances for each package and minimum solder reflow peak temperature.

**Important Note** Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at <http://www.cypress.com/design/MR10161>.

## Packaging Dimensions

Figure 17. 8-Pin (150-Mil) SOIC



51-85066 \*C

Figure 18. 16-Pin (150-Mil) SOIC

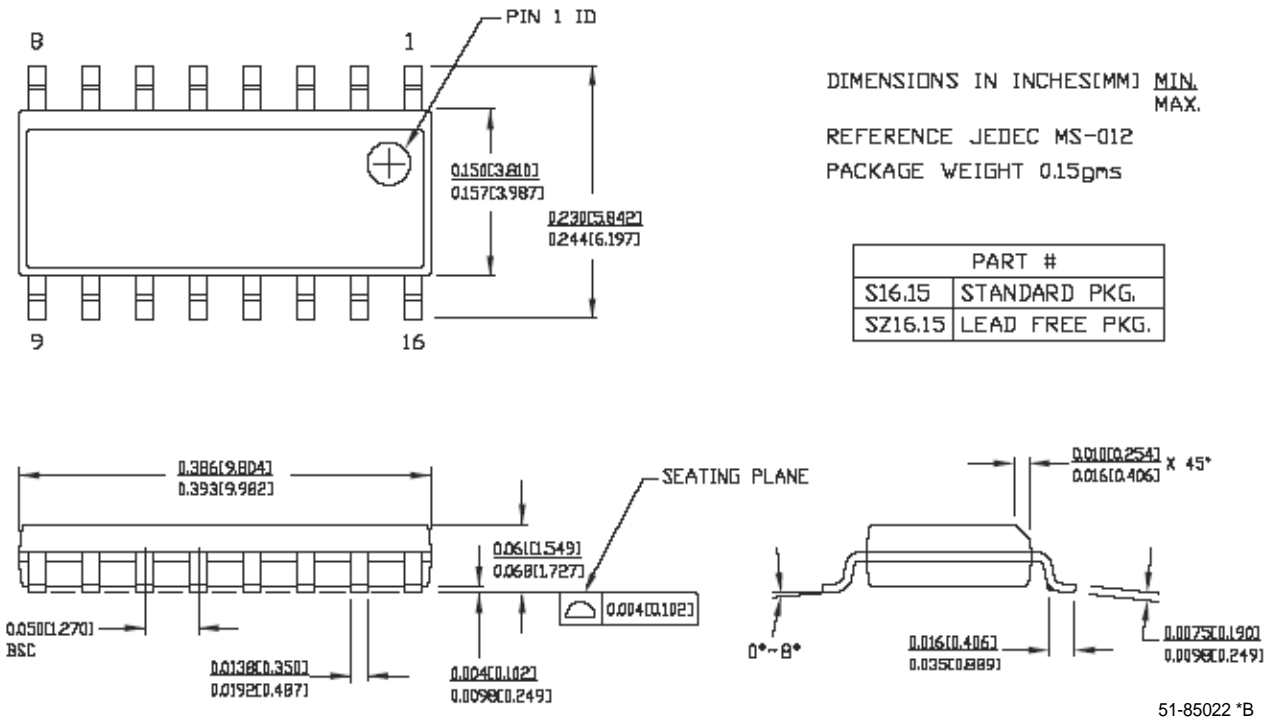
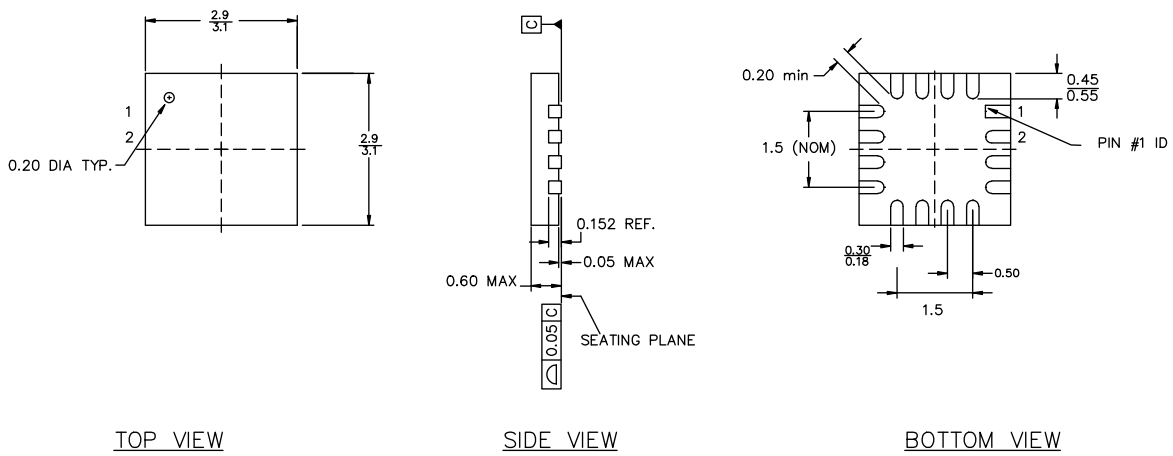


Figure 19. 16-Pin COL



| PART NO. | DESCRIPTION |
|----------|-------------|
| LG16A    | LEAD-FREE   |
| LD16A    | STANDARD    |

NOTES:

1. JEDEC # MO-220
2. Package Weight: 0.014g
3. DIMENSIONS IN MM, MIN MAX

001-09116 \*D



Figure 20. 20-Pin (210-MIL) SSOP

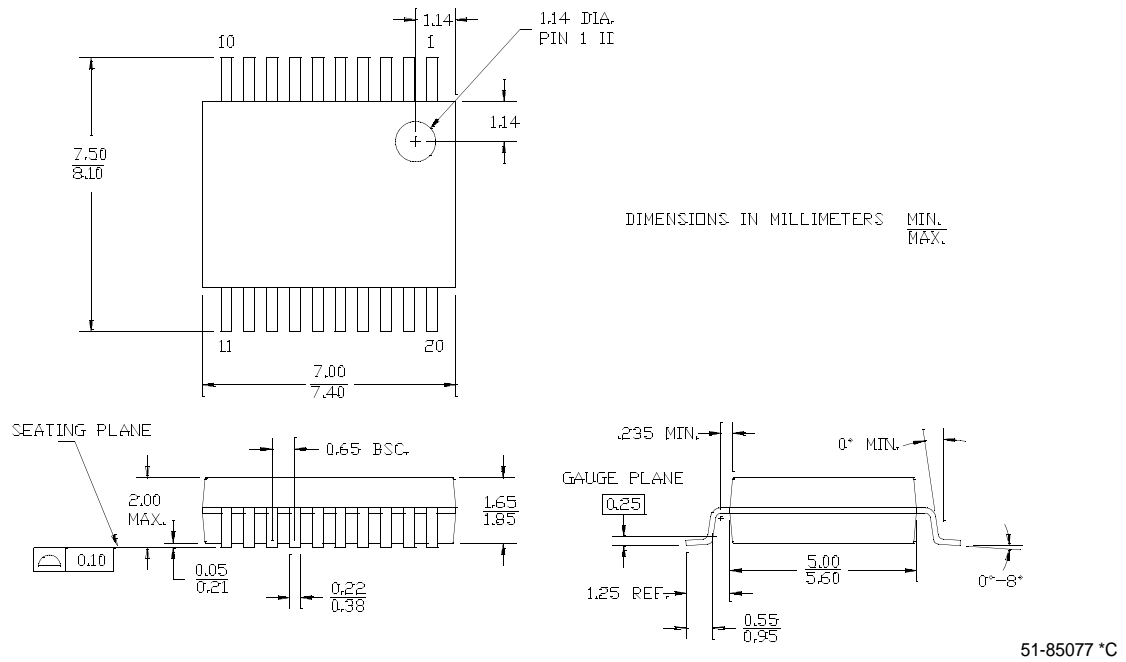
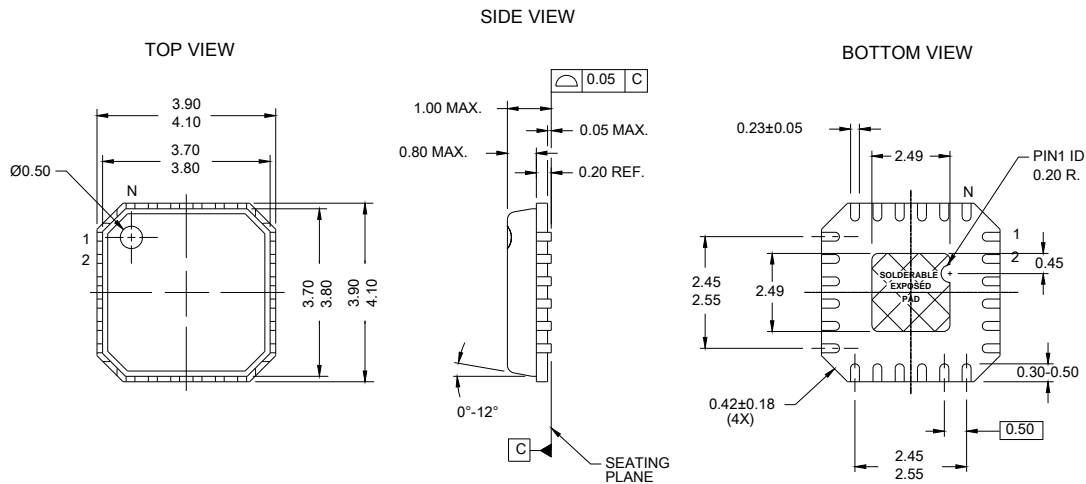



Figure 21. 24-Pin (4x4) QFN



NOTES:

1.  HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.042g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

| PART # | DESCRIPTION |
|--------|-------------|
| LF24A  | STANDARD    |
| LY24A  | LEAD FREE   |

51-85203 \*A

**Important Note** For information on the preferred dimensions for mounting QFN packages, see the following Application Note at [http://www.amkor.com/products/notes\\_papers/MLFAppNote.pdf](http://www.amkor.com/products/notes_papers/MLFAppNote.pdf).

Note that pinned vias for thermal conduction are not required for the low power 24, 32, and 48-pin QFN PSoC devices.

## Thermal Impedances

**Table 37. Thermal Impedances per Package**

| Package                | Typical $\theta_{JA}$ [21] |
|------------------------|----------------------------|
| 8 SOIC                 | 186°C/W                    |
| 16 SOIC                | 125°C/W                    |
| 16 COL                 | 46°C/W                     |
| 20 SSOP                | 117°C/W                    |
| 24 QFN <sup>[22]</sup> | 40°C/W                     |

## Solder Reflow Peak Temperature

Table 38 lists the minimum solder reflow peak temperature to achieve good solderability.

**Table 38. Solder Reflow Peak Temperature**

| Package | Minimum Peak Temperature <sup>[23]</sup> | Maximum Peak Temperature |
|---------|--|--------------------------|
| 8 SOIC  | 240°C                                    | 260°C                    |
| 16 SOIC | 240°C                                    | 260°C                    |
| 16 COL  | 240°C                                    | 260°C                    |
| 20 SSOP | 240°C                                    | 260°C                    |
| 24 QFN  | 240°C                                    | 260°C                    |

### Notes

21.  $T_J = T_A + \text{POWER} \times \theta_{JA}$

22. To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane.

23. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220+/-5°C with Sn-Pb or 245+/-5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

## Ordering Information

The following table lists the CY8C21x23 PSoC device's key package features and ordering codes.

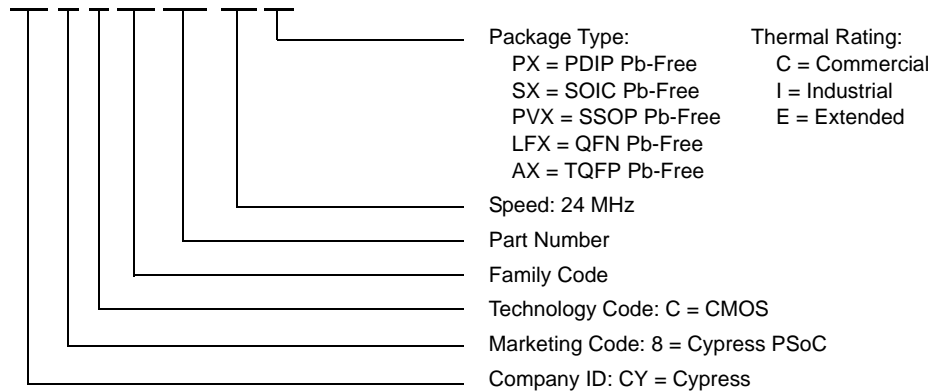
**Table 39. CY8C21x23 PSoC Device Key Features and Ordering Information**

| Package                               | Ordering Code     | Flash (Bytes) | RAM (Bytes) | Switch Mode Pump | Temperature Range | Digital PSoC Blocks | Analog Blocks | Digital IO Pins | Analog Inputs | Analog Outputs | XRES Pin |
|---------------------------------------|-------------------|---------------|-------------|------------------|-------------------|---------------------|---------------|-----------------|---------------|----------------|----------|
| 8-Pin (150-Mil) SOIC                  | CY8C21123-24SXI   | 4K            | 256         | No               | -40°C to +85°C    | 4                   | 4             | 6               | 4             | 0              | No       |
| 8-Pin (150-Mil) SOIC (Tape and Reel)  | CY8C21123-24SXIT  | 4K            | 256         | No               | -40°C to +85°C    | 4                   | 4             | 6               | 4             | 0              | No       |
| 16-Pin (150-Mil) SOIC                 | CY8C21223-24SXI   | 4K            | 256         | Yes              | -40°C to +85°C    | 4                   | 4             | 12              | 8             | 0              | No       |
| 16-Pin (150-Mil) SOIC (Tape and Reel) | CY8C21223-24SXIT  | 4K            | 256         | Yes              | -40°C to +85°C    | 4                   | 4             | 12              | 8             | 0              | No       |
| 16-Pin (3x3) COL                      | CY8C21223-24LGXI  | 4K            | 256         | Yes              | -40°C to +85°C    | 4                   | 4             | 12              | 8             | 0              | No       |
| 20-Pin (210-Mil) SSOP                 | CY8C21323-24PVXI  | 4K            | 256         | No               | -40°C to +85°C    | 4                   | 4             | 16              | 8             | 0              | Yes      |
| 20-Pin (210-Mil) SSOP (Tape and Reel) | CY8C21323-24PVXIT | 4K            | 256         | No               | -40°C to +85°C    | 4                   | 4             | 16              | 8             | 0              | Yes      |
| 24-Pin (4x4) QFN                      | CY8C21323-24LFXI  | 4K            | 256         | Yes              | -40°C to +85°C    | 4                   | 4             | 16              | 8             | 0              | Yes      |
| 24-Pin (4x4) QFN (Tape and Reel)      | CY8C21323-24LFXIT | 4K            | 256         | Yes              | -40°C to +85°C    | 4                   | 4             | 16              | 8             | 0              | Yes      |

**Note** For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

## Ordering Code Definitions

CY 8 C 21 xxx-24xx



**Document History Page**

| Document Title: CY8C21123, CY8C21223, CY8C21323 PSoC® Programmable System-on-Chip™<br>Document Number:38-12022 |         |                 |                 |   |
|--|---------|-----------------|-----------------|---|
| Rev.   | ECN No. | Orig. of Change | Submission Date | Description of Change   |
| **   | 133248  | NWJ             | See ECN         | New silicon and document (Revision **).   |
| *A   | 208900  | NWJ             | See ECN         | Add new part, new package and update all ordering codes to Pb-free.   |
| *B   | 212081  | NWJ             | See ECN         | Expand and prepare Preliminary version.   |
| *C   | 227321  | CMS Team        | See ECN         | Update specs., data, format.  |
| *D   | 235973  | SFV             | See ECN         | Updated Overview and Electrical Spec. chapters, along with 24-pin pinout. Added CMP_GO_EN register (1,64h) to mapping table.  |
| *E   | 290991  | HMT             | See ECN         | Update data sheet standards per SFV memo. Fix device table. Add part numbers to pinouts and fine tune. Change 20-pin SSOP to CY8C21323. Add Reflow Temp. table. Update diagrams and specs.  |
| *F   | 301636  | HMT             | See ECN         | DC Chip-Level Specification changes. Update links to new CY.com Portal.   |
| *G   | 324073  | HMT             | See ECN         | Obtained clearer 16 SOIC package. Update Thermal Impedances and Solder Reflow tables. Re-add pinout ISSP notation. Fix ADC type-o. Fix TMP register names. Update Electrical Specifications. Add CY logo. Update CY copyright. Make data sheet Final. |
| *H   | 2588457 | KET/HMI/AESA    | 10/22/2008      | New package information on page 9. Converted data sheet to new template. Added 16-Pin OFN package diagram.  |
| *I   | 2618175 | OGNE/PYRS       | 12/09/08        | Added Note in Ordering Information Section. Changed title from PSoC Mixed-Signal Array to PSoC Programmable System-on-Chip. Updated 'Development Tools' and 'Designing with PSoC Designer' sections on pages 5 and 6                                  |
| *J   | 2682782 | MAXK/AESA       | 04/03/2009      | Corrected 16 COL pinout.  |
| *K   | 2699713 | MAXK            | 04/29/09        | Minor ECN to correct paragraph style of 16 COL Pinout. No change in content.  |

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