0.5 OHM, DUAL SPDT ANALOG SWITCH

IDTAS4684A

Description

The IDTAS4684A low on-resistance (RON), low voltage, dual single-pole/double-throw (SPDT) analog switch operates from a single +1.8 V to +5.5 V supply. The IDTAS4684A features a 0.5Ω (max) RON for its NC switch and a 0.8Ω (max) RON for its NO switch at a +2.7 V supply. It also features break-before-make switching action (2 ns) with t_{ON} = 50 ns and t_{OFF} = 40 ns at +3 V. The digital logic inputs are 1.8 V logic-compatible with a +2.7 V to +3.3 V supply. Comes in a 12-bump CSP package.

Applications

- Speaker headset switching
- MP3 players
- Battery-operated equipment
- Audio and video signal routing
- PCMCIA cards
- Cellular phones
- Modems

Features

- +1.8 V to +5.5 V single-supply operation
- Rail-to-rail signal handling
- 1.8 V logic compatibility
- RON match between channels: 0.06Ω (max)
- RON flatness over signal range: 0.15Ω (max)
- NCx Switch RON: 0.5Ω max (+2.7 V Supply)
- NOx Switch RON: 0.8Ω max (+2.7 V Supply)
- Low crosstalk: -68dB (100 kHz)
- High Off-isolation: -64dB (100 kHz)
- THD: 0.03%
- 50 nA (max) supply current
- Low leakage currents: 1 nA (max) at T_A = +25°C
- 12-bump, 0.5 mm-Pitch UCSP package

Block Diagram
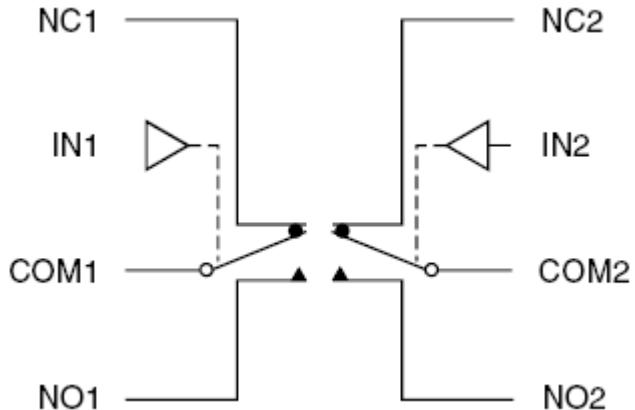
Pin Assignment (CSP)

	A	B	C
1	NC1	GND	NC2
2	IN1	NC	IN2
3	COM1	NC	COM2
4	NO1	V+	NO2

Truth Table

IN	NO	NC
0	OFF	ON
1	ON	OFF

Note: Switches shown for logic "0" input.

Pin Descriptions

Pin Numbers	Pin Name	Pin Description
A1	NC1	Analog switch. Normally closed terminal 1.
A2	IN1	Digital control input 1.
A3	COM1	Analog switch. Common terminal 1.
A4	NO1	Analog switch. Normally open terminal 1.
B1	GND	Ground.
B2	NC	No connect.
B3	NC	No connect.
B4	V+	Positive supply voltage input.
C1	NC2	Analog switch. Normally closed terminal 2.
C2	IN2	Digital control input 2.
C3	COM2	Analog switch. Common terminal 2.
C4	NO2	Analog switch. Normally open terminal 2.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDTAS4684A. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range. All voltages referenced to ground.

Symbol	Rating	Min	Max	Unit
V+, IN		-0.3	+6	V
COM, NO, NC		-0.3	(V+ + 0.3)	V
NO, NC, COM	Continuous current		±300	mA
	Peak current (pulsed at 1ms, 50% duty cycle)		±400	
	Peak current (pulsed at 1ms, 10% duty cycle)		±500	
	Continuous power dissipation (TA = +70°C) and 12-bump UCSP (derate 11.4mW/°C above +70°C)		+909	mW
	Operating temperature range	0	+70	°C
TSTG	Storage temperature range	-65	+150	°C
	Lead temperature (soldering, 10s)		+300	°C
	Bump temperature (soldering, infrared, 15s)		+200	°C
	Vapor phase (60s)		+215	°C

Electrical Characteristics

Unless stated otherwise, **V+ = 2.7 V to 3.3 V, V_{IH} = 1.4 V, V_{IL} = 0.5 V, T_A = T_{MIN} to T_{MAX}.** Typical values are at +3 V and 25°C

Parameter	Symbol	Conditions	T_A	Min.	Typ.	Max.	Units
Analog Switch							
Analog Signal Range	V_{NO}, V_{NC}, V_{COM}		$T_{MIN\ to\ TMAX}$	0		V+	V
NC On-Resistance	$R_{ON(NC)}$	V+ = 2.7 V, I_{COM} = 100 mA, V_{NC} = 0 to V+; Note 3	+25°C		3.0	0.5	Ω
			$T_{MIN\ to\ TMAX}$			0.5	
NO On-Resistance	$R_{ON(NO)}$	V+ = 2.7 V, I_{COM} = 100 mA, V_{NO} = 0 to V+; Note 3	+25°C		0.45	0.8	Ω
			$T_{MIN\ to\ TMAX}$			0.8	
On-Resistance Match between channels	$\triangle R_{ON}$	V+ = 2.7 V, I_{COM} = 100 mA, V_{NO} or V_{NC} = 1.5 V; Notes 3, 4	+25°C		0	0.6	Ω
			$T_{MIN\ to\ TMAX}$			0.6	
NC On-Resistance Flatness	$R_{FLAT(NC)}$	V+ = 2.7 V, I_{COM} = 100 mA, V_{NC} = 0 to V+; Note 5	$T_{MIN\ to\ TMAX}$			0.15	Ω
NO On-Resistance Flatness	$R_{FLAT(NO)}$	V+ = 2.7 V, I_{COM} = 100 mA, V_{NO} = 0 to V+; Note 5	$T_{MIN\ to\ TMAX}$			0.35	Ω
NO or NC Off-leakage Current	I_{NO}(OFF) or I_{NC}(OFF)	V+ = 3.3 V, V_{NO} or V_{NC} = 3 V, 0.3 V V_{COM} = 0.3 V, 3 V	+25°C	-1		+1	nA
			$T_{MIN\ to\ TMAX}$	-10		+10	
COM On-leakage Current	I_{COM}(ON)	V+ = 3.3 V, V_{NO} or V_{NC} = 3 V, 0.3 V, or floating V_{COM} = 0.3 V, 3 V, or floating	+25°C	-2		+2	nA
			$T_{MIN\ to\ TMAX}$	-20		+20	
Dynamic Characteristics							
Turn-on Time	t_{ON}	V+ = 2.7 V, V_{NO} or V_{NC} = 1.5 V, R_L = 50Ω, C_L = 35 pF	+25°C		30	50	ns
			$T_{MIN\ to\ TMAX}$			60	ns
Turn-off Time	t_{OFF}	V+ = 2.7 V, V_{NO} or V_{NC} = 1.5 V, R_L = 50Ω, C_L = 35 pF	+25°C		25	30	ns
			$T_{MIN\ to\ TMAX}$			40	ns
Break-Before-Make-Delay	t_{BBM}	V+ = 2.7 V, V_{NO} or V_{NC} = 1.5 V, R_L = 50Ω, C_L = 35 pF	$T_{MIN\ to\ TMAX}$	2	15		ns
Charge Injection	Q	COM = 0, RS = 0, C_L = 1 nF	+25°C		200		pC
Off-Isolation	V_{ISO}	C_L = 5 pF; R_L = 50Ω, f = 100 kHz, V_{COM} = 1 V_{RMS}, Note 6	+25°C		-64		dB
Crosstalk	V_{CT}	f = 100 kHz, R_L = 50Ω, C_L = 5 pF, V_{COM} = 1 V_{RMS}	+25°C		-68		dB
Total Harmonic Distortion	THD	R_L = 600Ω, IN = 2 V p-p, f = 20Hz to 20 kHz	+25°C		0.03		%
NC Off-Capacitance	C_{NC}(OFF)	f = 1 MHz	+25°C		84		pF
NC Off-Capacitance	C_{NO}(OFF)	f = 1 MHz	+25°C		37		pF
NC On-Capacitance	C_{NC}(ON)	f = 1 MHz	+25°C		190		pF
NC On-Capacitance	C_{NO}(ON)	f = 1 MHz	+25°C		150		pF

| Parameter	Symbol	Conditions	T_A	Min.	Typ.	Max.	Units
Digital I/O							
Input Logic HIGH	V_{IH}		T_{MIN} to T_{MAX}	1.4			V
Input Logic LOW	V_{IL}		T_{MIN} to T_{MAX}			0.5	V
IN Input Leakage Current	I_{IN}	V_{IN} = 0 or V+	T_{MIN} to T_{MAX}	-1		1	µA
Power Supply							
Power Supply Range	V+		T_{MIN} to T_{MAX}	1.8		5.5	V
Supply Current	I+	V+ = 5.5 V, V_{IN} = 0 or V+, Note 3	+25°C	-50	+0.04	+50	nA
			T_{MIN} to T_{MAX}	-200		+200	

Notes:

1. The algebraic convention used in this data sheet is where the most negative value is a minimum and the most positive value a maximum.

2. UCSP parts are 100% tested at +25°C only and guaranteed by design and correlation at the full hot-rated temperature.

3. Guaranteed by design.

4. $\triangle R_{ON}$ = $R_{ON(MAX)}$ - $R_{ON(MIN)}$, between NC1 and NC2 or between NO1 and NO2.

5. Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal ranges.

6. Off-isolation = 20log10 (V_{COM} / V_{CO}), V_{COM} = output, V_{CO} = input to off switch.

Test Circuits and Timing Diagrams
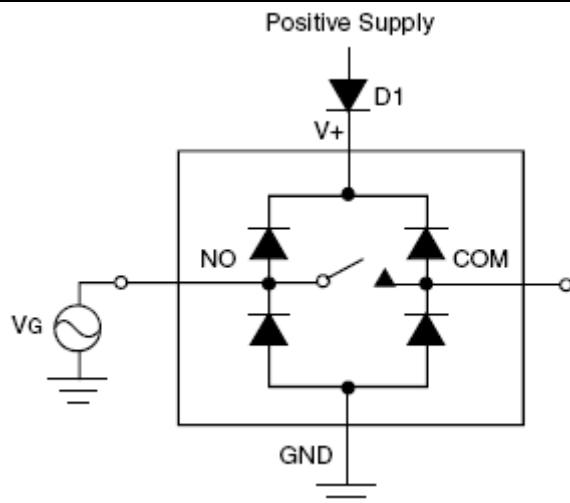
**Overvoltage Protection Using Two External Blocking Diodes**
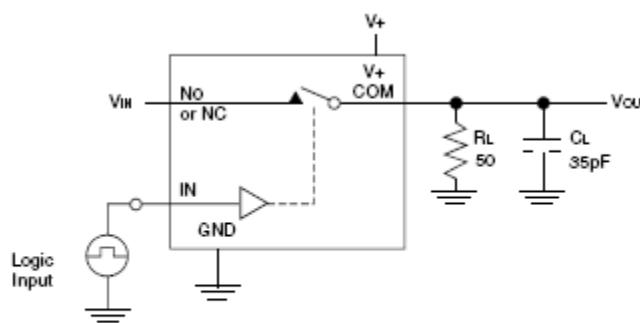
DEFINITIONS:
CL = Includes fixture and stray capacitance.

$$V_{OUT} = V_{IN} \left(\frac{R_L}{R_L + R_{ON}} \right)$$
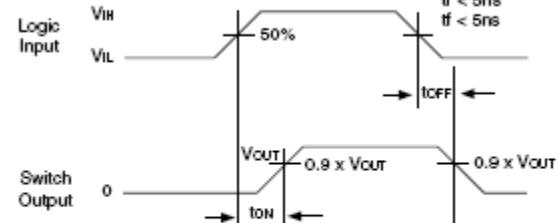
NOTE:
1. Logic input waveforms inverted for switches that have the opposite logic sense

Switching Time
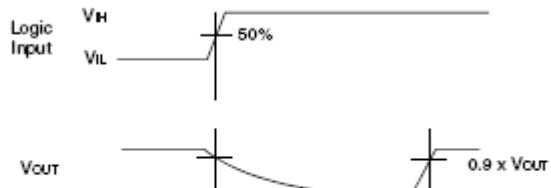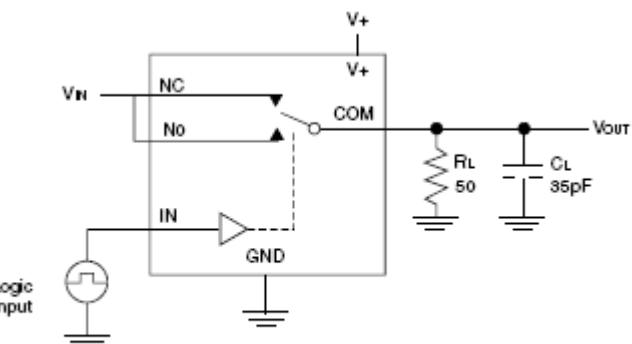
DEFINITIONS:
CL = Includes fixture and stray capacitance.

Break-Before-Make Interval
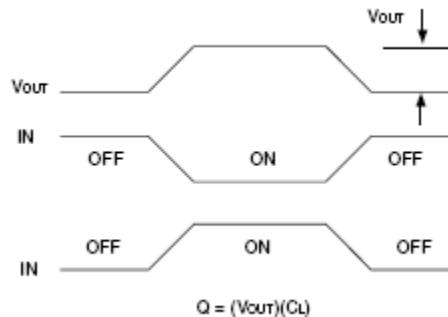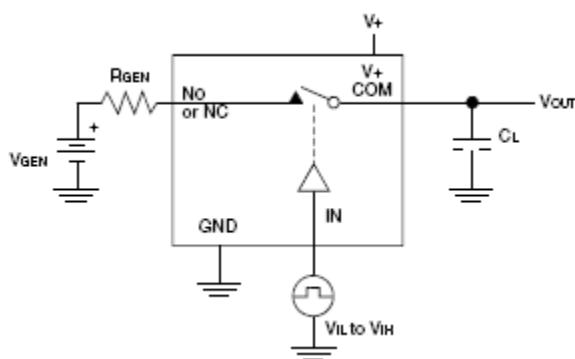
Charge Injection
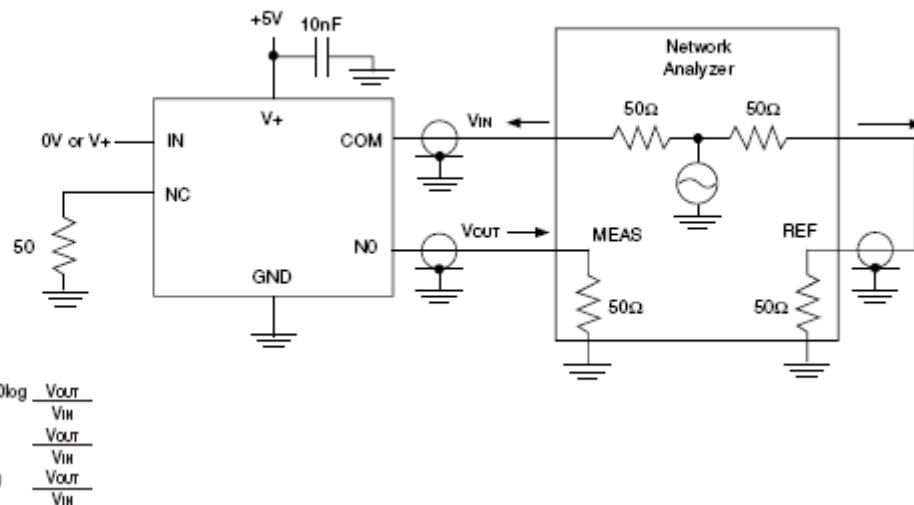
On-Loss, Off-Isolation, and Crosstalk

NOTE:

$$\text{OFF-ISOLATION} = 20\log \frac{V_{OUT}}{V_{IN}}$$

$$\text{ON-LOSS} = 20\log \frac{V_{OUT}}{V_{IN}}$$

$$\text{CROSSTALK} = 20\log \frac{V_{OUT}}{V_{IN}}$$
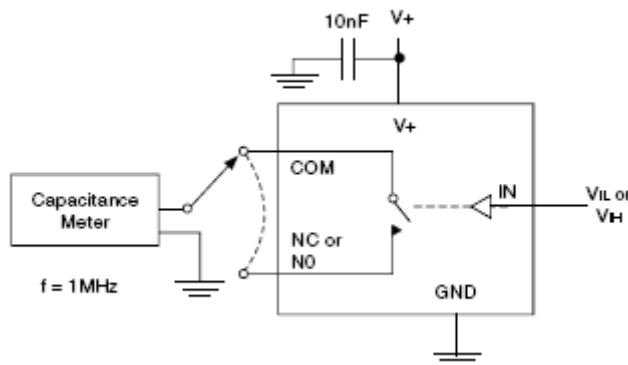
Channel Off/On Capacitance

Marking Diagram (CSP)

IDTAS4
684AHG
0633AAH
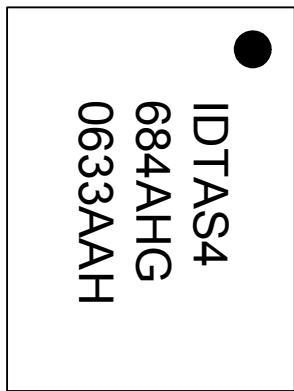
Notes:

1. "Z" is the device step (1 to 2 characters).

2. YYWW is the last two digits of the year and week that the part was assembled.

3. "$" is the assembly mark code.

4. "G" after the two-letter package code designates RoHS compliant package.

5. "I" at the end of part number indicates industrial temperature range.

6. Bottom marking: country of origin if not USA.

Package Outline and Package Dimensions (12-bump CSP)

Package dimensions are kept current with JESD Publication No. 95-1,
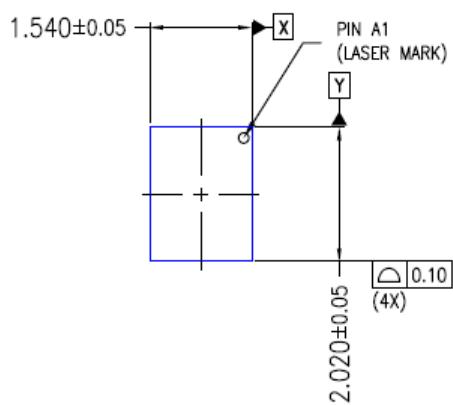

WAFER BACK SIDE
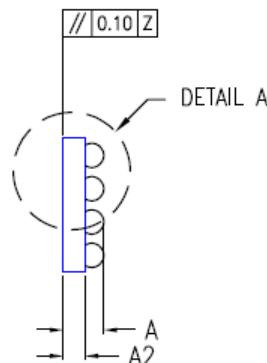
SIDE VIEW
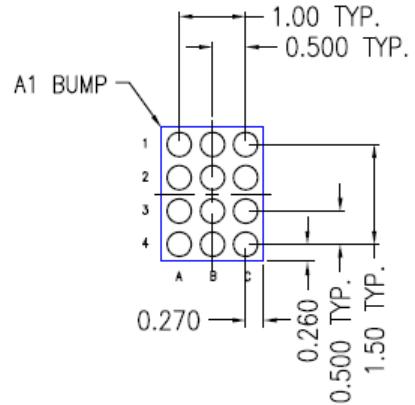
BUMP SIDE
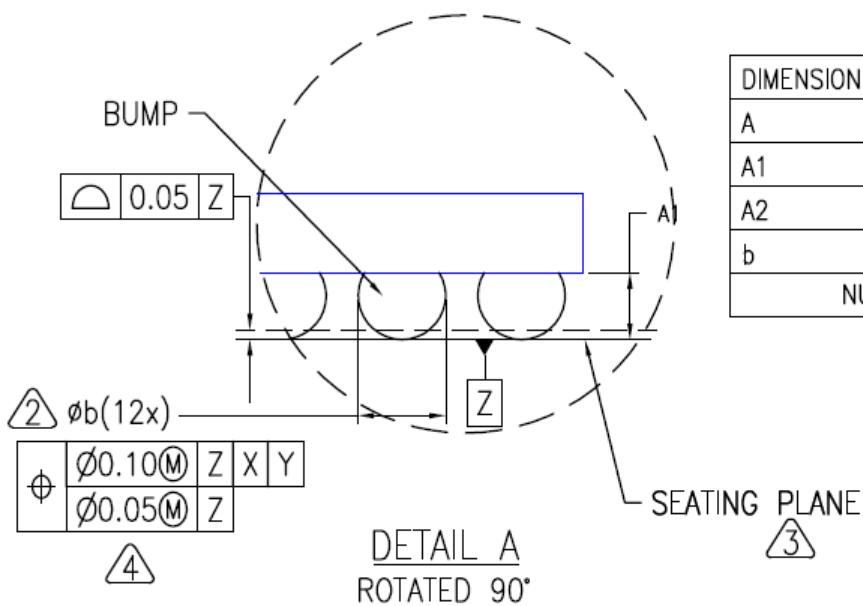
DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	0.555	0.61	0.665
A1	0.25	0.28	0.31
A2	0.305	0.33	0.355
b	0.316	0.366	0.416
NUMBER OF BUMPS 12			

DETAIL A
ROTATED 90°

NOTES:
1. DIMENSIONS AND TOLERANCE PER ASME Y 14.5M — 1994.
2. DIMENSION IS MEASURED AT THE MAXIMUM BUMP DIAMETER PARALLEL TO PRIMARY DATUM Z
3. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE BUMP.
4. BUMP POSITION DESIGNATION PER JESD 95-1, SPP-010.
5. THERE SHALL BE A MINIMUM CLEARANCE OF 0.10mm BETWEEN THE EDGE OF THE BUMP AND THE BODY EDGE.

Ordering Information

```
IDT    XXXXXX        XXX           X            X
      Device Type   Package    Temp. Range   Shipping
                                             Carrier
```

8	Tape and Reel
Blank	Tray

Blank	Commercial (0 to +70°C)

AHG	Chip Scale Package

AS4684A	0.5Ω Low Voltage, Dual SPDT Analog Switch

Revision History

Rev.	Originator	Date	Description of Change
A	Jamal Sarma	9/25/07	Created datasheet in new template; added marking diagram. This data sheet improves the V_{IH} for the chip from CMOS to TTL levels.

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For Sales
800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support
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Corporate Headquarters
Integrated Device Technology, Inc.
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