256K x 4 SRAM

SRAM MEMORY ARRAY

AVAILABLE AS MILITARY SPECIFICATIONS

•MIL-STD-883

FEATURES

- High Speed: 20, 25, 35, and 45
- Battery Backup: 2V data retention
- Low power standby
- High-performance, low-power CMOS double-metal process
- Single +5V (±10%) Power Supply
- Easy memory expansion with CE\ and OE\ options.
- All inputs and outputs are TTL compatible

OPTIONS MARKING

- **Timing**

20ns access	-20
25ns access	-25
35ns access	-35
45ns access	-45
55ns access	-55*
70ns access	-70*

- **Package(s)**

Ceramic DIP (400 mil)	C	No. 109
Ceramic Quad LCC (contact factory)	ECW	No. 206
Ceramic LCC	EC	No. 207
Ceramic Flatpack	F	No. 303
Ceramic SOJ	DCJ	No. 501

- **Operating Temperature Ranges**

Industrial (-40°C to +85°C)	IT
Military (-55°C to +125°C)	XT

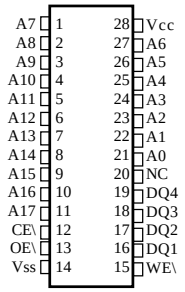
- 2V data retention/low power L

*Electrical characteristics identical to those provided for the 45ns access devices.

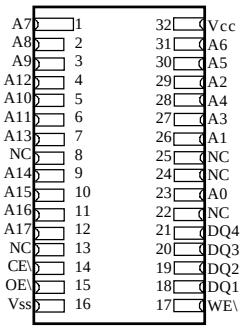
For more products and information please visit our web site at *www.austinsemiconductor.com*

PIN ASSIGNMENT
(Top View)

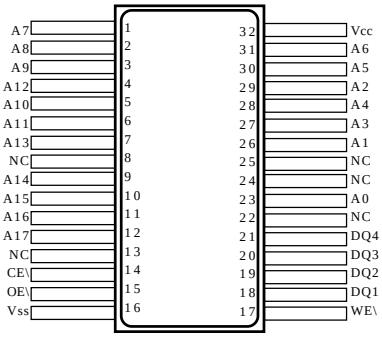
28-Pin DIP (C)
(400 MIL)



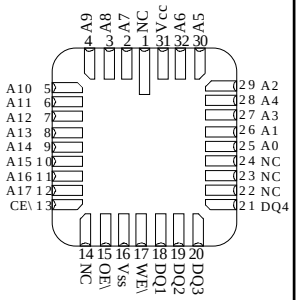
32-Pin LCC (EC)
32-Pin SOJ (DCJ)



32-Pin Flat Pack (F)



32-Pin LCC (ECW)



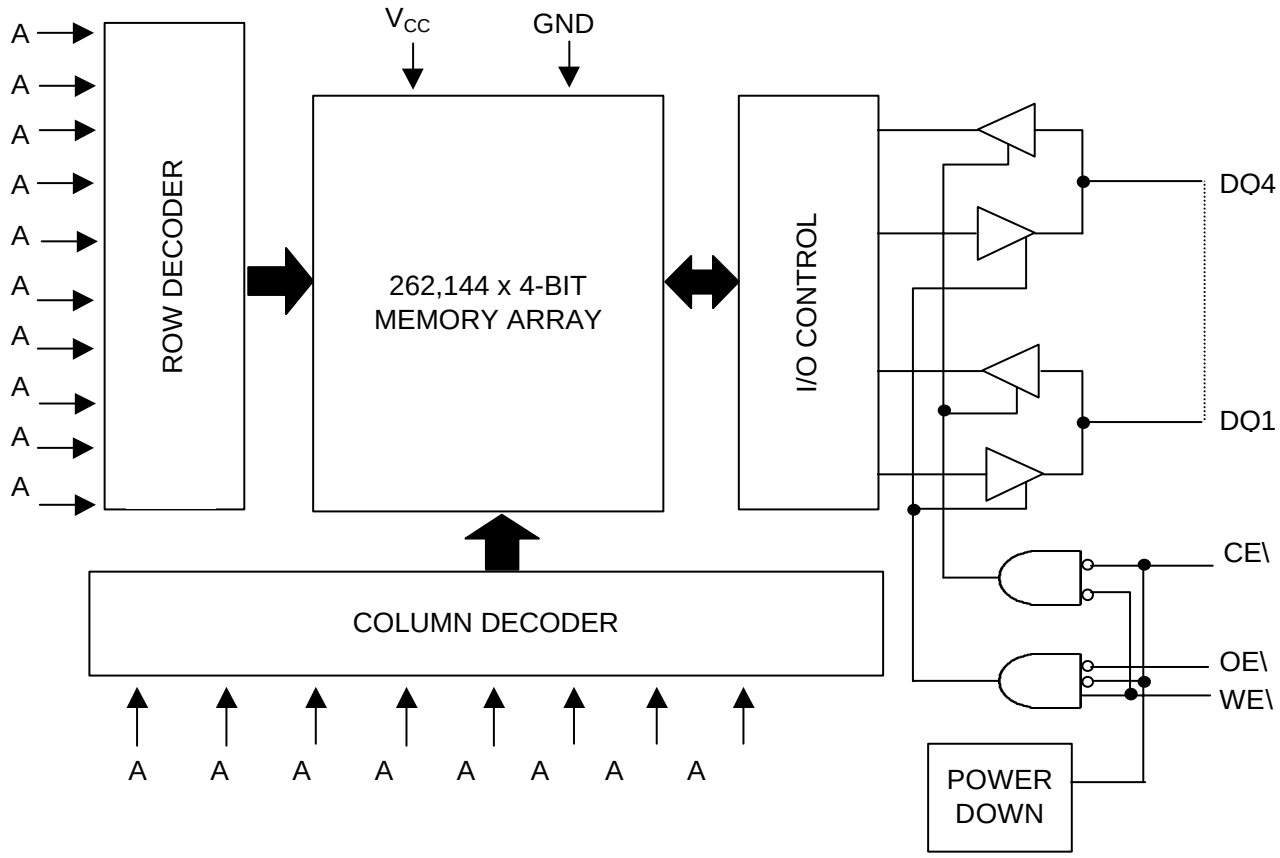
GENERAL DESCRIPTION

The Austin Semiconductor SRAM family employs high-speed, low power CMOS designs fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, ASI offers chip enable (CE\) and output enable (OE\) capability. These enhancements can place the outputs in High-Z for additional flexibility in system design. Writing to these devices is accomplished when write enable (WE\) and CE\ inputs are both LOW. Reading is accomplished when WE\ remains HIGH while CE\ and OE\ go LOW. The devices offer a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operation from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	OE\	CE\	WE\	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage Range (Vcc).....-.5V to +7.0V
Storage Temperature.....-65°C to +150°C
Voltage on any Pin Relative to Vss.....-.5V to Vcc+.5V
Max Junction Temperature.....+175°C
Lead Temperature (soldering 10 seconds).....+260°C
Power Dissipation .....1 W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-55^oC \leq T_C \leq 125^oC$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYM	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+0.5	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1
Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$	IL_I	-10	10	µA	
Output Leakage Current	Output(s) disabled $0V \leq V_{OUT} \leq V_{CC}$	IL_O	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX					
PARAMETER	CONDITIONS	SYM	-20	-25	-35	-45	UNITS	NOTES
Power Supply Current: Operating	WE\, CE\ ≤ V_{IL}; V_{CC} = MAX Output Open	I_{cc}	180	180	180	180	mA	3
Power Supply Current: Standby	CE\ ≥ V_{IH}; All Other Inputs ≤ V_{IL} or ≥ V_{IH}, V_{CC} = MAX	I_{SBT2}	25	25	25	25	mA	
	CE\ ≥ V_{CC} -0.2V; V_{CC} = MAX $V_{IL} \leq V_{SS}$ +0.2V $V_{IH} \geq V_{CC}$ -0.2V; f = 0 Hz*	I_{SBC}	16	16	16	16	mA	

** "L" version only.*

CAPACITANCE

PARAMETER	CONDITIONS	SYM	MAX	UNITS	NOTES
Input Capacitance	V_{IN} = 0V, T_A = 25°C, f = 1MHz V_{CC} = 5V	C_I	12	pF	4
Output Capacitance (DQ1-DQ4)		C_O	14	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($-55^{o}C \leq T_C \leq 125^{o}C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	SYMBOL	-20		-25		-35		-45		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ CYCLE											
READ cycle time	t_{RC}	20		25		35		45		ns	
Address access time	t_{AA}		20		25		35		45	ns	
Chip Enable access time	t_{ACE}		20		25		35		45	ns	
Output hold from address change	t_{OH}	3		3		3		3		ns	
Chip Enable to output in Low-Z	t_{LZCE}	3		3		3		3		ns	4, 6, 7
Chip disable to output in High-Z	t_{HZCE}		10		12		20		25	ns	4, 6, 7
Chip Enable to power-up time	t_{PU}	0		0		0		0		ns	4
Chip disable to power-down time	t_{PD}		20		25		35		45	ns	4
Output Enable access time	t_{AOE}		8		10		20		25	ns	
Output Enable to output in Low-Z	t_{LZOE}	0		0		0		0		ns	4, 6, 7
Output disable to output in High-Z	t_{HZOE}		8		10		20		25	ns	4, 6, 7
WRITE CYCLE											
WRITE cycle time	t_{WC}	20		25		35		45		ns	
Chip Enable to end of write	t_{CW}	15		20		30		35		ns	
Address valid to end of write	t_{AW}	15		20		30		35		ns	
Address setup time	t_{AS}	0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		ns	
WRITE pulse width	t_{WP}	15		20		30		35		ns	
Data setup time	t_{DS}	12		15		20		25		ns	
Data hold time	t_{DH}	0		0		0		0		ns	
Write disable to output in Low-Z	t_{LZWE}	3		3		3		3		ns	4, 6, 7
Write Enable to output in High-Z	t_{HZWE}	0	8	0	10	0	15	0	20	ns	4, 6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

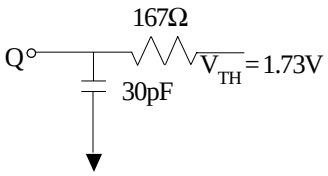


Fig. 1 Output Load Equivalent

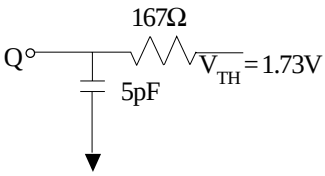


Fig. 2 Output Load Equivalent

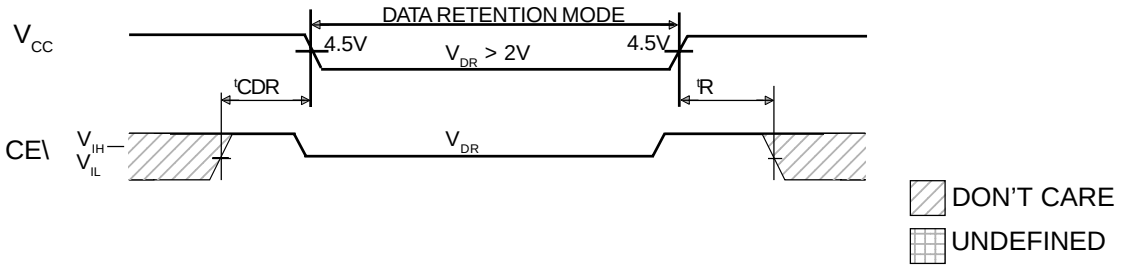
NOTES

1. All voltages referenced to V_{SS} (GND).
2. -3V for pulse width < 20ns
3. I_{CC} is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and f = 1 / ^{t}RC (MIN) Hz.
4. This parameter is guaranteed but not tested.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Minimum of 5pF for t_{EHQZ}, t_{OHQZ}, t_{ELQX}, t_{OLQX}, and t_{WHQX}.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE and ^{t}HZOE is less than ^{t}LZOE.
8. WE\ is HIGH for READ cycle.
9. Device is continuously selected. Chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable (CE\) and write enable (WE\) can initiate and terminate a WRITE cycle.

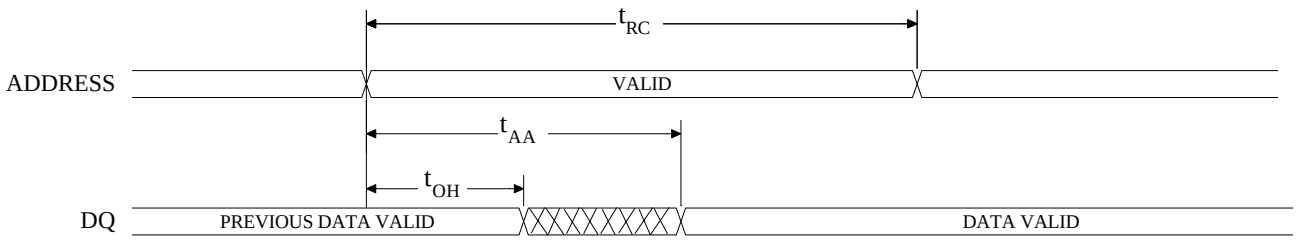
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYM	MIN	MAX	UNITS	NOTES
V_{CC} for Retention Data			V_{DR}	2		V	
Data Retention Current	CE\ ≥ (V_{CC}-0.2V) and V_{IN} ≥ (V_{CC}-0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}		5	mA	
Chip Deselect to Data Retention Time			t_{CDR}	0	--	ns	4
Operation Recovery Time			t_R	t_{RC}		ns	4, 11

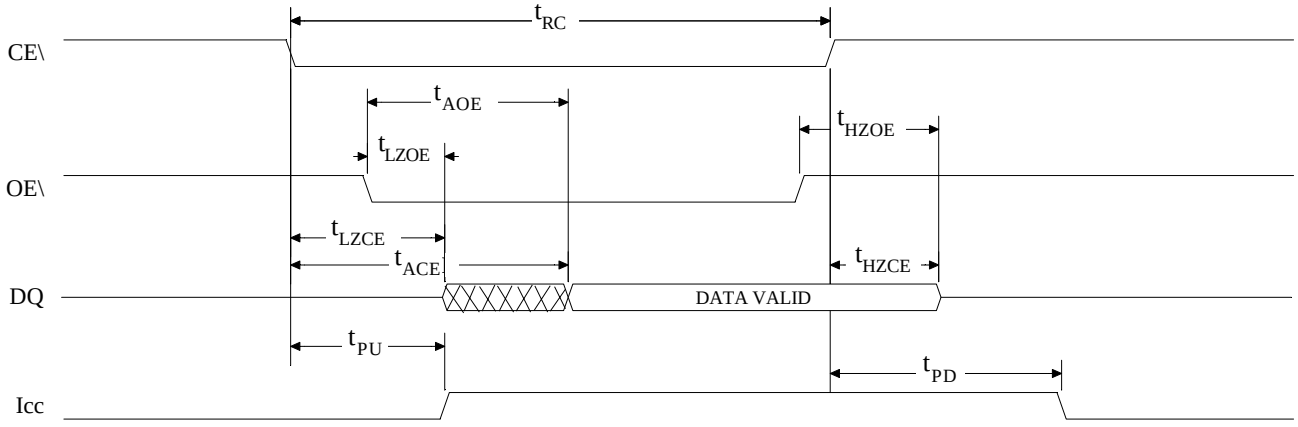
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]



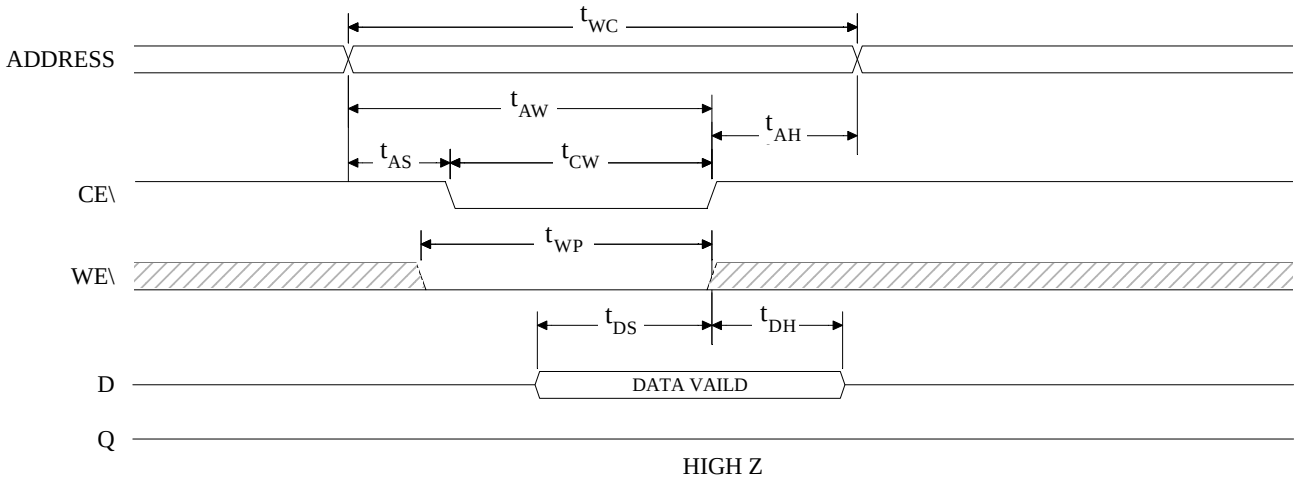
READ CYCLE NO. 2 [7, 8, 10]



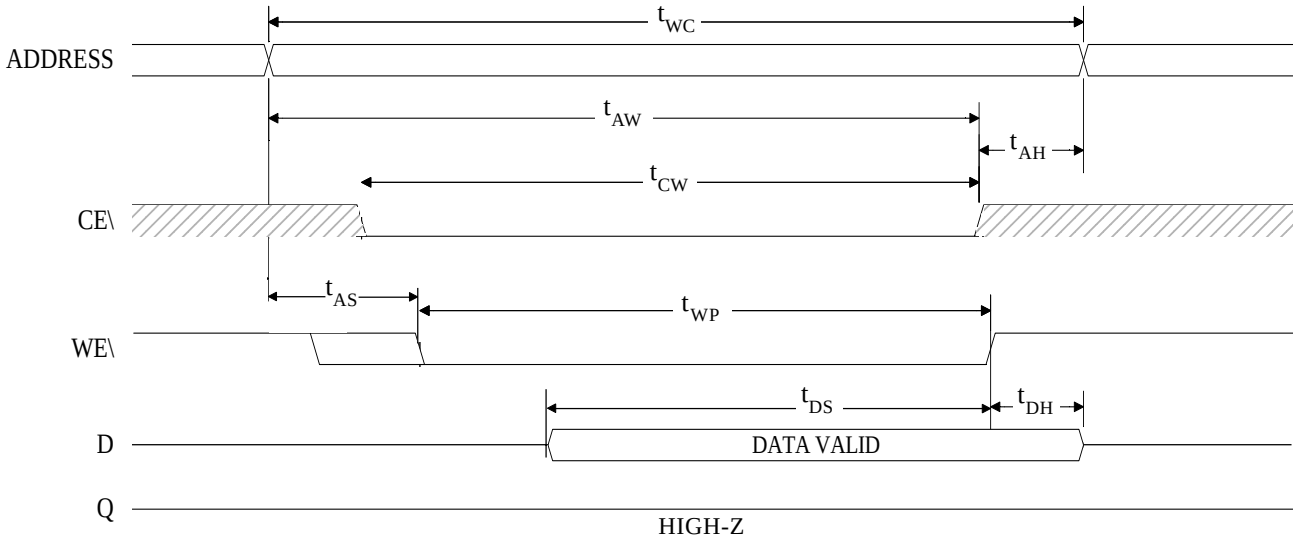
DON'T CARE

UNDEFINED

WRITE CYCLE NO. 1 [12]
(Chip Enabled Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enabled Controlled)

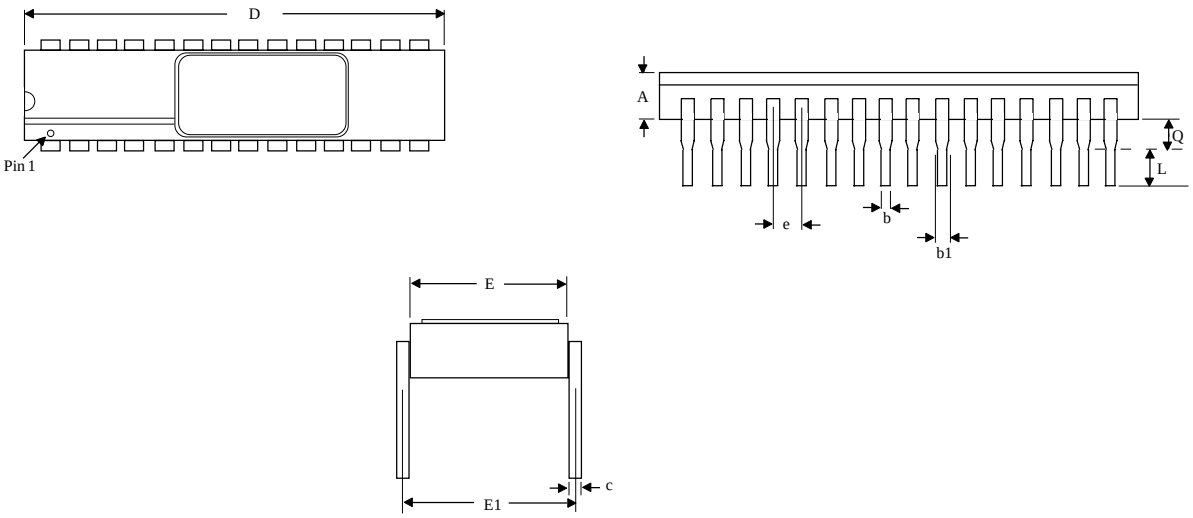


DON'T CARE
UNDEFINED

NOTE: Output enable (OE\) is inactive (HIGH).

MECHANICAL DEFINITIONS*

ASI Case #109 (Package Designator C)

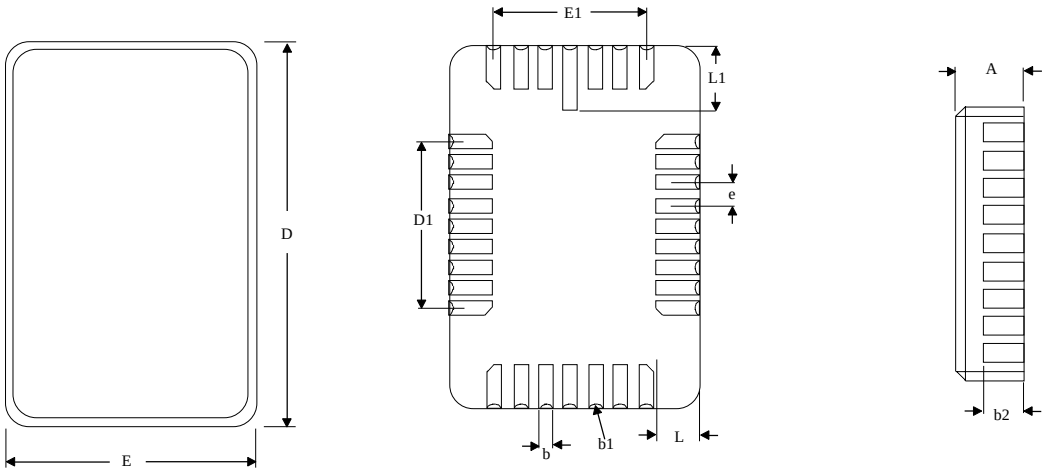


SYMBOL	ASI PACKAGE SPECIFICATIONS	
	MIN	MAX
A	0.090	0.110
b	0.016	0.020
b1	0.040	0.060
c	0.008	0.012
D	1.386	1.414
E	0.385	0.405
E1	0.390	0.410
e	0.090	0.110
L	0.125	0.175
Q	0.040	0.060

All measurements are in inches.

MECHANICAL DEFINITIONS*

ASI Case #206 (Package Designator ECW)

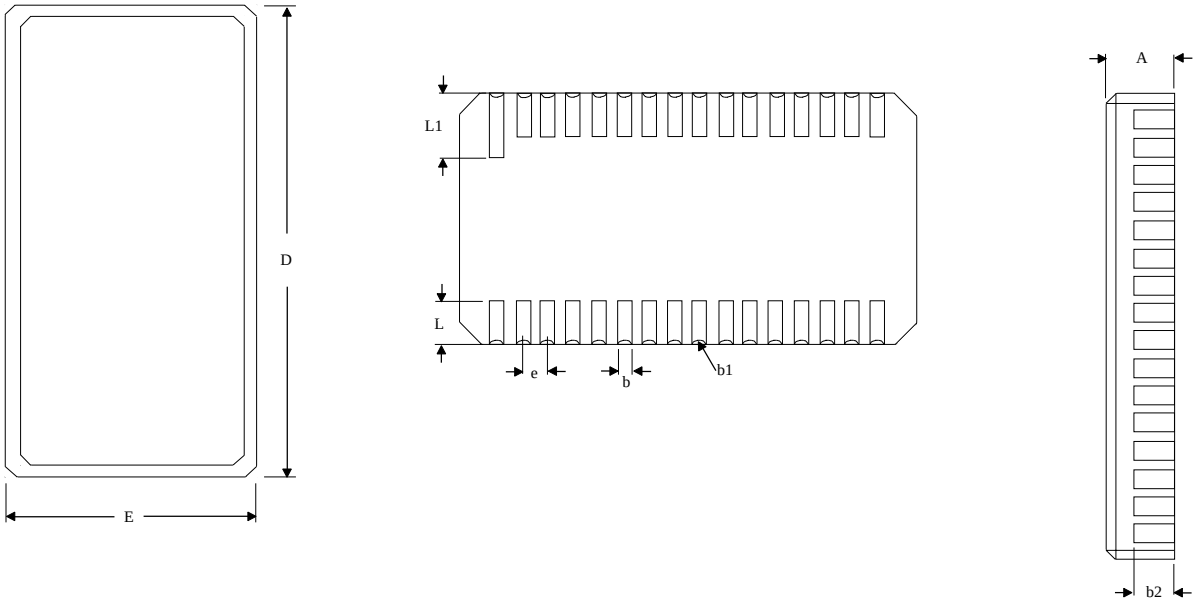


SYMBOL	ASI PACKAGE SPECIFICATIONS	
	MIN	MAX
A	0.077	0.093
b	0.022	0.028
b1	0.004	0.014
b2	0.054	0.066
D	0.742	0.758
D1	0.395	0.405
E	0.442	0.458
E1	0.295	0.305
e	0.045	0.055
L	0.045	0.055
L1	0.077	0.093

All measurements are in inches.

MECHANICAL DEFINITIONS*

ASI Case #207 (Package Designator EC)

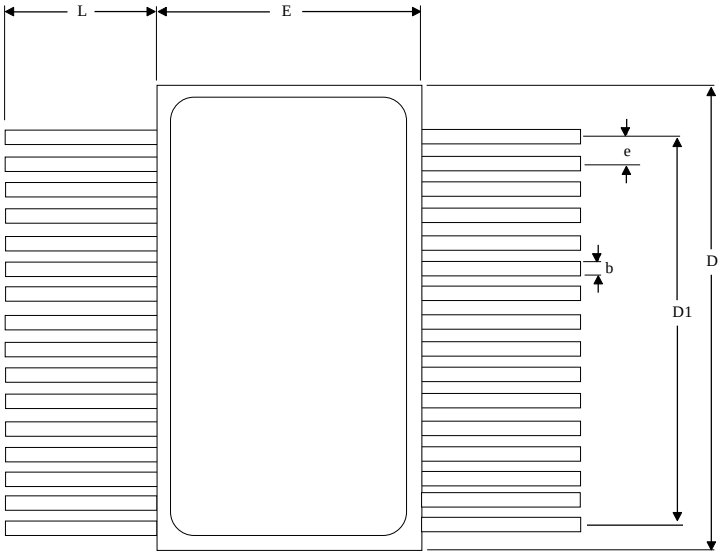


SYMBOL	ASI PACKAGE SPECIFICATIONS	
	MIN	MAX
A	0.080	0.100
b	0.022	0.028
b1	0.004	0.014
b2	0.054	0.066
D	0.815	0.835
E	0.392	0.408
e	0.045	0.055
L	0.070	0.080
L1	0.090	0.110

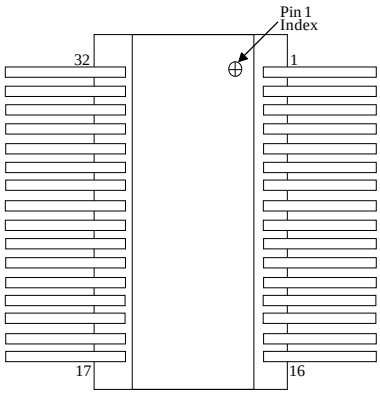
All measurements are in inches.

MECHANICAL DEFINITIONS*

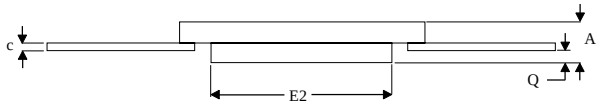
ASI Case #303 (Package Designator F)



Top View



Bottom View

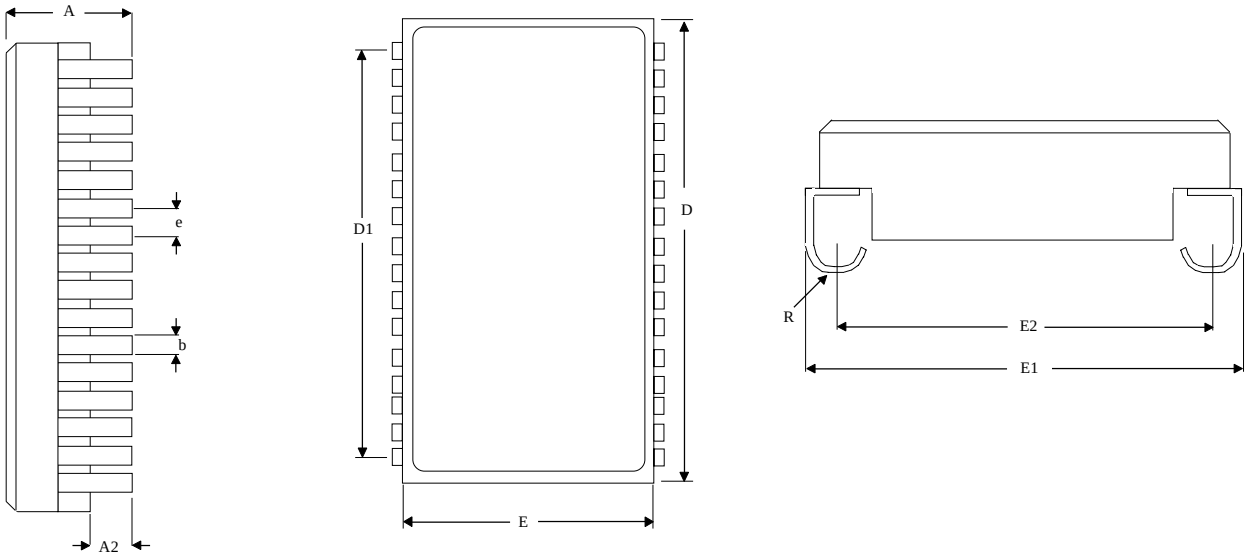


SYMBOL	ASI PACKAGE SPECIFICATIONS	
	MIN	MAX
A	---	0.125
b	0.015	0.019
c	0.004	0.006
D	0.812	0.828
D1	0.745	0.755
E	0.405	0.415
E2	0.324	0.336
e	0.045	0.055
L	0.290	0.310
Q	0.027	0.033

All measurements are in inches.

MECHANICAL DEFINITIONS*

ASI Case #501 (Package Designator DCJ)



SYMBOL	ASI PACKAGE SPECIFICATIONS	
	MIN	MAX
A	0.135	0.153
A2	0.026	0.036
b	0.015	0.019
D	0.812	0.828
D1	0.740	0.755
E	0.405	0.415
e	0.045	0.055
E1	0.435	0.445
E2	0.360	0.380
R	0.030	0.040

All measurements are in inches.

ORDERING INFORMATION

EXAMPLE: MT5C1005C-20L/IT

Device Number	Package Type	Speed ns	Options**	Process
MT5C1005	C	-20	L	/*
MT5C1005	C	-25	L	/*
MT5C1005	C	-35	L	/*
MT5C1005	C	-40	L	/*
MT5C1005	C	-55	L	/*
MT5C1005	C	-70	L	/*

EXAMPLE: MT5C1005EC-45/XT

Device Number	Package Type	Speed ns	Options**	Process
MT5C1005	EC ECW	-20	L	/*
MT5C1005	EC ECW	-25	L	/*
MT5C1005	EC ECW	-35	L	/*
MT5C1005	EC ECW	-40	L	/*
MT5C1005	EC ECW	-55	L	/*
MT5C1005	EC ECW	-70	L	/*

EXAMPLE: MT5C1005F-25L/883C

Device Number	Package Type	Speed ns	Options**	Process
MT5C1005	F	-20	L	/*
MT5C1005	F	-25	L	/*
MT5C1005	F	-35	L	/*
MT5C1005	F	-40	L	/*
MT5C1005	F	-55	L	/*
MT5C1005	F	-70	L	/*

EXAMPLE: MT5C1005DCJ-70/XT

Device Number	Package Type	Speed ns	Options**	Process
MT5C1005	DCJ	-20	L	/*
MT5C1005	DCJ	-25	L	/*
MT5C1005	DCJ	-35	L	/*
MT5C1005	DCJ	-40	L	/*
MT5C1005	DCJ	-55	L	/*
MT5C1005	DCJ	-70	L	/*

***AVAILABLE PROCESSES**

IT = Industrial Temperature Range -40°C to +85°C
XT = Extended Temperature Range -55°C to +125°C
883C = Full Military Processing -55°C to +125°C

**** OPTIONS**

L = 2V Data Retention/Low Power