

## Features

- 802.11b/g and Bluetooth Applications
- Low Insertion Loss:  
0.5 dB 2.4 GHz to 2.5 GHz band
- High Isolation: 32 dB Typical on  $R_x$
- Low Harmonics: <-70 dBc @ 20 dBm
- Flip-chip configuration
- RoHS\* Compliant

## Description

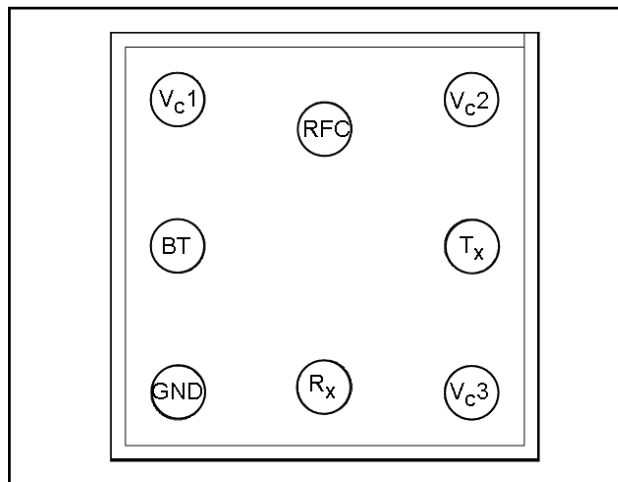
MA-COM's MASW-009276-000DIE is a bumped GaAs PHEMT MMIC SP3T switch. Typical applications are WLAN (802.11 b/g) and Bluetooth applications.

The MASW-009276-000DIE delivers high isolation, low insertion loss, and high linearity at 2.4 - 2.5 GHz. This device is fabricated using a 0.5 micron gate length GaAs pHEMT process. The process features full passivation for performance and reliability. This die features SnAg (2.5%) solder bumps for Wafer Level Chip Scale Package (WLCSP) applications.

## Ordering Information

Part Number	Package
MASW-009276-000D3K	Die in 3000 piece reel
MASW-009276-001SMB	Sample Board SP3T

## Die Bump Pad Layout (bump side up)



## Die Bump Pad Configuration

Name	Description
Vc1	Voltage Control 1
BT	Blue Tooth $T_x/R_x$ Port
GND	Ground
$R_x$	2.5 GHz $R_x$ Port
Vc3	Voltage Control 3
$T_x$	2.5 GHz $T_x$ Port
Vc2	Voltage Control 2
RFC	Antenna Port

## Absolute Maximum Ratings <sup>1,2</sup>

Parameter	Absolute Maximum
Input Power @ 3 V Control	+32 dBm
Input Power @ 5 V Control	+35 dBm
Operating Voltage	+8 volts
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

1. Exceeding any one or combination of these limits may cause permanent damage to this device.
2. M/A-COM does not recommend sustained operation near these survivability limits.

\* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

**ADVANCED:** Data Sheets contain information regarding a product M/A-COM Technology Solutions is considering for development. Performance is based on target specifications, simulated results, and/or prototype measurements. Commitment to develop is not guaranteed.

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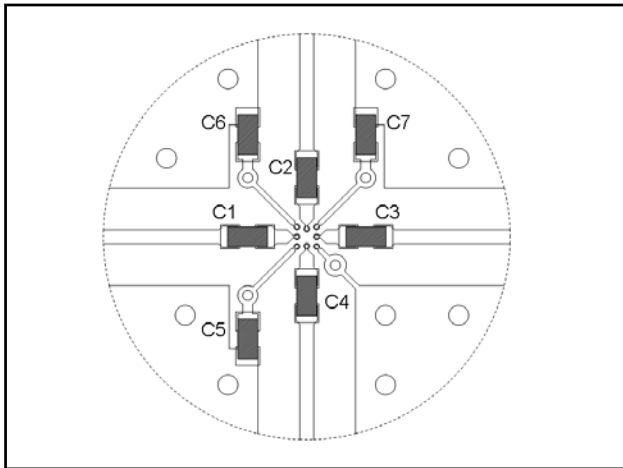
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**Electrical Specifications<sup>3</sup>:**  $T_A = 25^\circ\text{C}$ ,  $Z_0 = 50 \Omega$ ,  $V_c = 0 \text{ V} / 3 \text{ V}$ ,  $\text{Pin} = 0 \text{ dBm}$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Insertion Loss	RFC to Tx/Rx/BT, 2.4 GHz	dB	—	0.5	0.75
Isolation	RFC to Tx, 2.4 GHz	dB	20	24	—
	RFC to Rx, 2.4 GHz	dB	30	32	—
	RFC to BT, 2.4 GHz	dB	20	24	—
Return Loss	2.4 - 2.5 GHz	dB	—	15	—
IP3	RFC to Tx/Rx/BT, 2.4 GHz, 20 dBm Total Power, 1MHz Spacing	dBm	—	55	—
Input P1dB	RFC to Tx, 2.4 GHz	dBm	—	32	—
	RFC to Rx, 2.4 GHz	dBm	—	28	—
	RFC to BT, 2.4 GHz	dBm	—	32	—
Harmonics	RFC to Tx 2.4 GHz, 20 dBm	dBm	—	-75	—
Control Current	$ V_c  = 3 \text{ V}$	$\mu\text{A}$	—	<1	2

3. External blocking capacitors on all RF ports.

## Recommended PCB Configuration



## Parts List

Part	Value	Case Style
C1 - C4	39 pF	0402
C5 - C7	1000 pF	0402

## Truth Table<sup>4,5,6</sup>

$V_{c1}$	$V_{c2}$	$V_{c3}$	RFC-BT	RFC-T <sub>x</sub>	RFC-R <sub>x</sub>
1	0	0	On	Off	Off
0	1	0	Off	On	Off
0	0	1	Off	Off	On

- For positive voltage control, external DC blocking capacitors are required on all RF ports.
- Differential voltage,  $V(\text{state } 1) - V(\text{state } 0)$ , must be +2.7 V minimum and must not exceed +5 V.
- $0 = 0 \pm 0.3 \text{ V}$ ,  $1 = +2.7 \text{ V to } +5 \text{ V}$ .

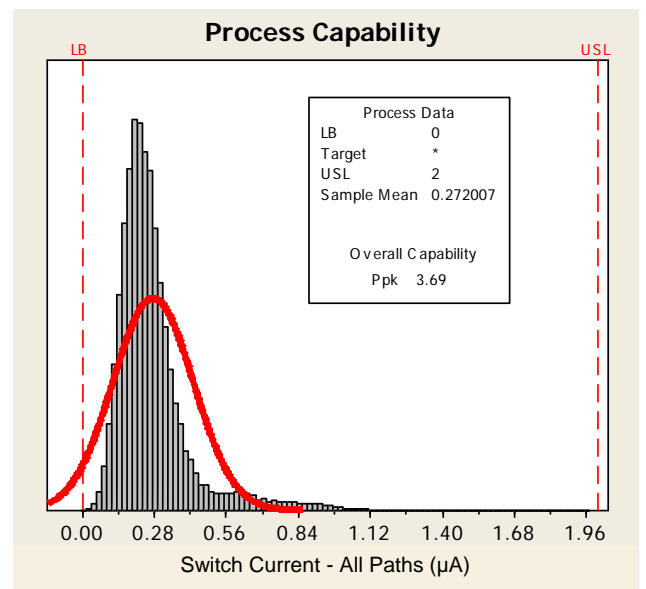
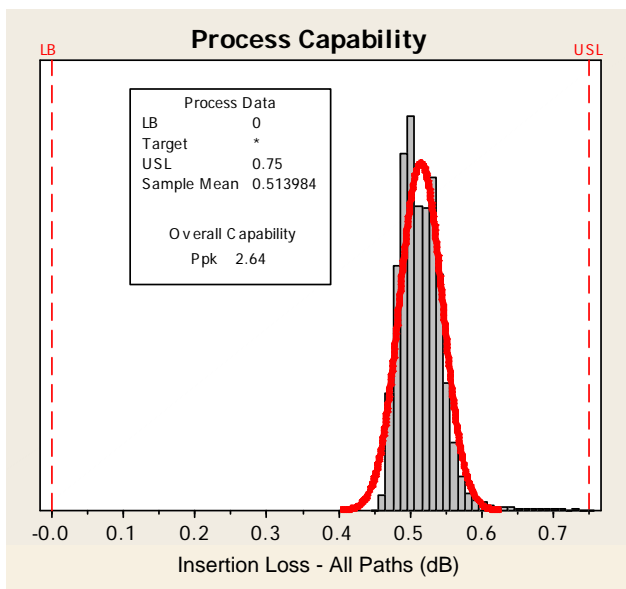
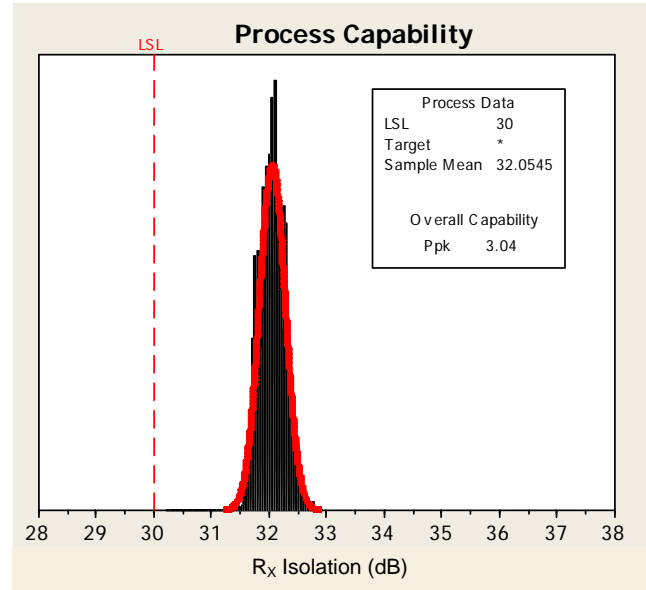
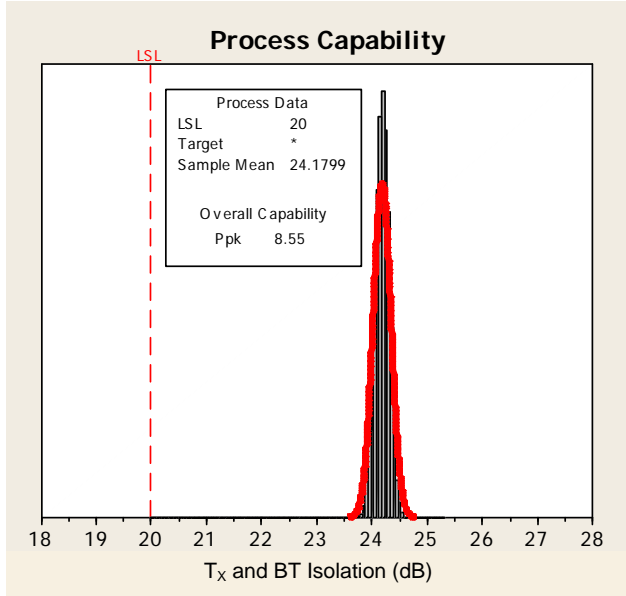
## Handling Procedures

Please observe the following precautions to avoid damage:

## Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

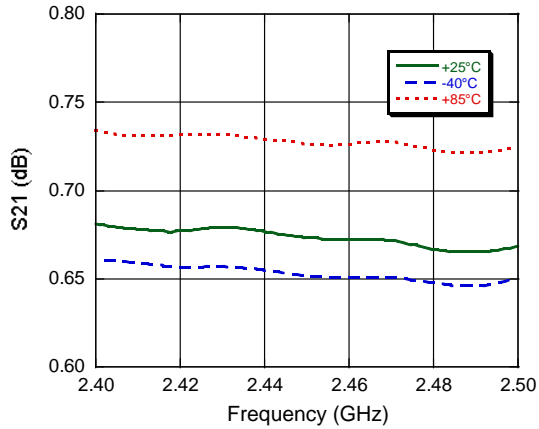
## Product Consistency Distribution Charts<sup>7</sup> (on wafer RF test)



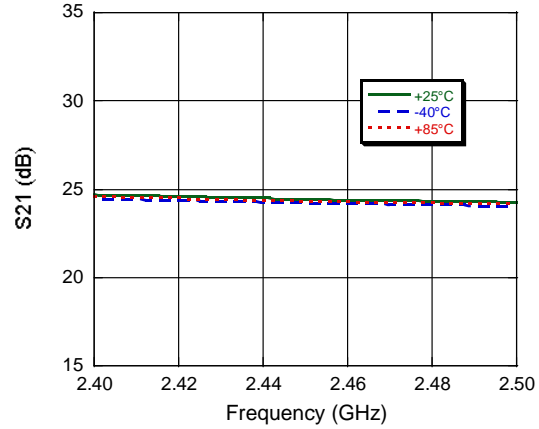
7. Represents >5 wafers, tested per electrical specifications, probed directly on the die to the solder bump:  $T_A = 25^\circ\text{C}$ ,  $Z_0 = 50 \Omega$ ,  $V_C = 0/3\text{V}$ ,  $P_{IN} = 0 \text{ dBm}$

## Typical Performance Curves (plots = chip on board assembly)

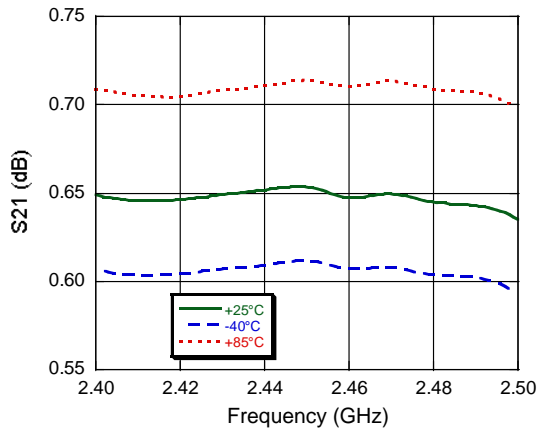
**$T_x$  Insertion Loss**



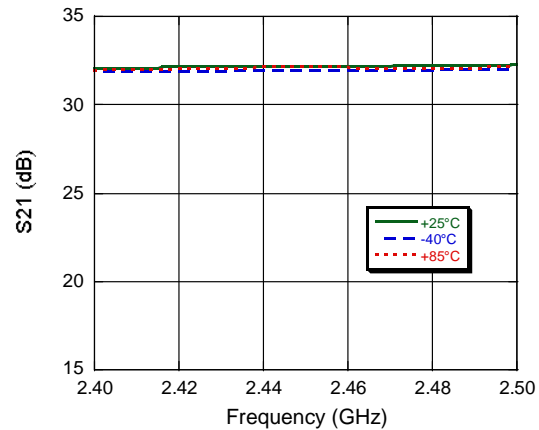
**$T_x$  Isolation**



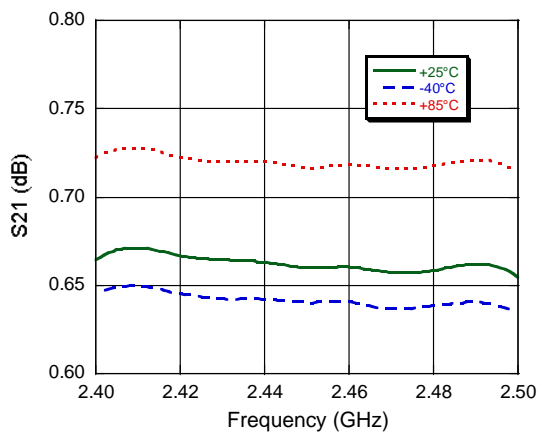
**$R_x$  Insertion Loss**



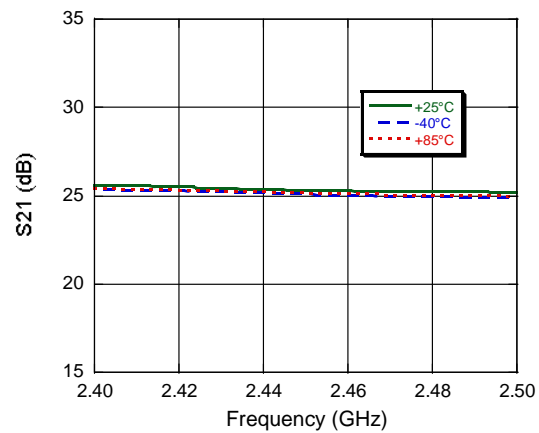
**$R_x$  Isolation**



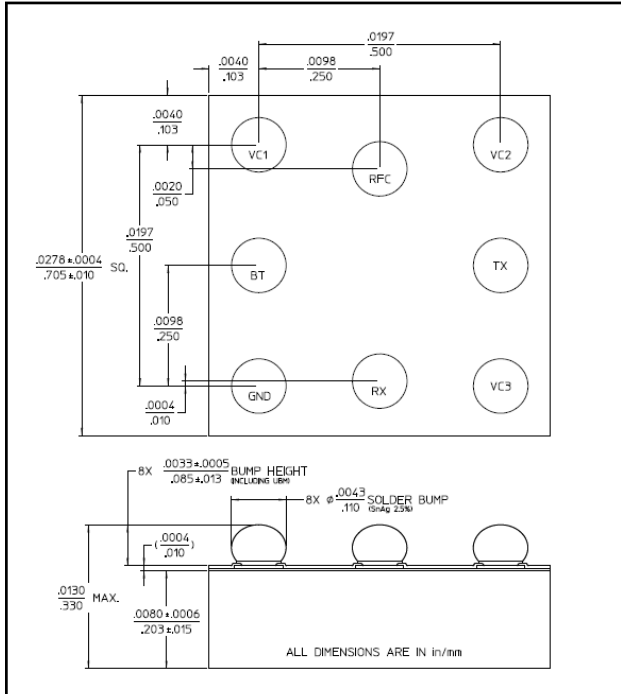
**BT Insertion Loss**



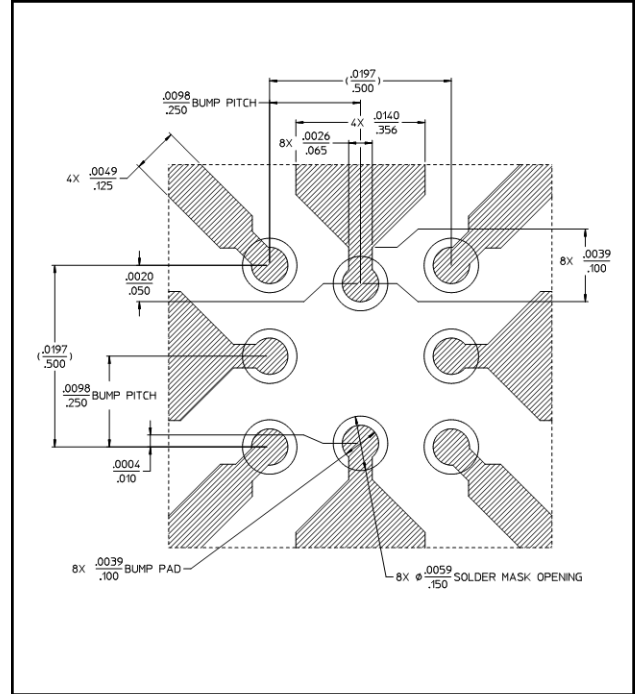
**BT Isolation**



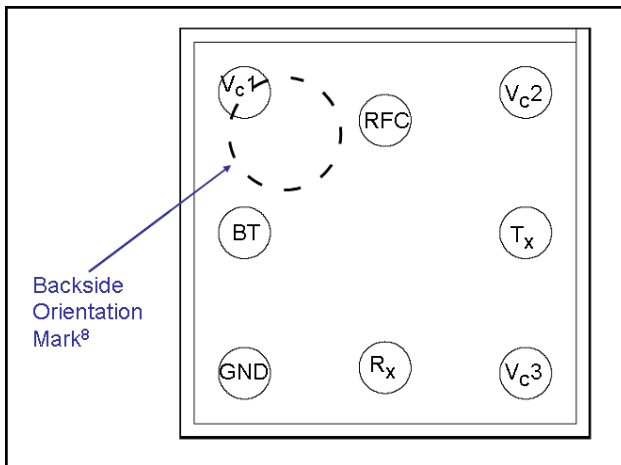
## Die Dimensions (Top and Side Views)



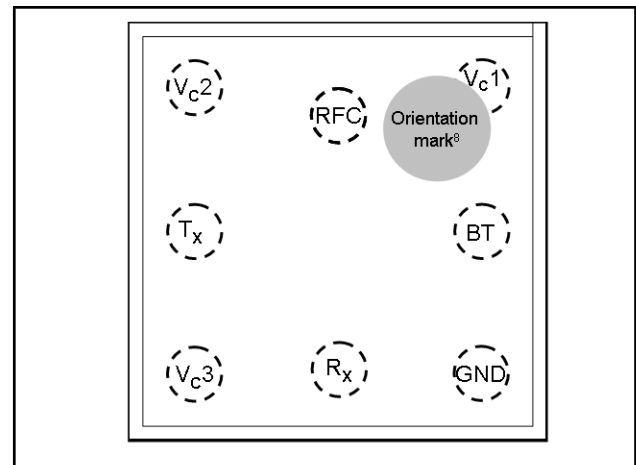
## PCB Top Metal / Solder Mask



## Die Bump Pad Layout - Top View (bump side up)



## Die Bump Pad Layout - Bottom View (bump side down - as installed on board)



8. Orientation mark is only on material that is shipped in tape and reel. The mark is not available on die shipped on grip ring.