# RTSX-S RadTolerant FPGAs

FuseLock™

## Designed for Space

- SEU-Hardened Registers Eliminate the Need to Implement Triple-Module Redundancy (TMR)
  - Immune to Single-Event Upsets (SEU) to $LET_{th}$ > 40 MeV-cm$^2$/mg,
  - SEU Rate < $10^{-10}$ Upset/Bit-Day in Worst-Case Geosynchronous Orbit
- Up to 100 krad (Si) Total Ionizing Dose (TID)
  - Parametric Performance Supported with Lot-Specific Test Data
- Single-Event Latch-Up (SEL) Immunity
- TM1019.5 Test Data Available
- QML Certified Devices

## High Performance

- 230 MHz System Performance
- 310 MHz Internal Performance
- 9.5 ns Input Clock to Output Pad

## Specifications

- 0.25 µm Metal-to-Metal Antifuse Process
- 48,000 to 108,000 Available System Gates
- Up to 2,012 SEU-Hardened Flip-Flops
- Up to 360 User-Programmable I/O Pins

## Features

- Very Low Power Consumption (Up to 68 mW at Standby)
- 3.3V and 5V Mixed Voltage
- Configurable I/O Support for 3.3V/5V PCI, LVTTL, TTL, and CMOS
  - 5V Input Tolerance and 5V Drive Strength
  - Slow Slew Rate Option
  - Configurable Weak Resistor Pull-Up/Down for Tristated Outputs at Power-Up
  - Hot-Swap Compliant with Cold-Sparing Support
- Secure Programming Technology Prevents Reverse Engineering and Design Theft
- 100% Circuit Resource Utilization with 100% Pin Locking
- Unique In-System Diagnostic and Verification Capability with Silicon Explorer II
- Low-Cost Prototyping Option
- Deterministic, User-Controllable Timing
- JTAG Boundary Scan Testing in Compliance with IEEE Standard 1149.1 – Dedicated JTAG Reset (TRST) Pin

*Table 1* • **RTSX-S Product Profile**

| **Device** | **RT54SX32S** | **RT54SX72S** |
|---|---|---|
| **Capacity** | | |
| Typical Gates | 32,000 | 72,000 |
| System Gates | 48,000 | 108,000 |
| **Logic Modules** | 2,880 | 6,036 |
| Combinatorial Cells | 1,800 | 4,024 |
| SEU-Hardened Register Cells (Dedicated Flip-Flops) | 1,080 | 2,012 |
| **Maximum Flip-Flops** | 1,980 | 4,024 |
| **Maximum User I/Os** | 227 | 360 |
| **Clocks** | 3 | 3 |
| **Quadrant Clocks** | 0 | 4 |
| **Speed Grades** | Std., –1 | Std., –1 |
| **Package** (by pin count) | | |
| CQFP | 208, 256 | 208, 256 |
| CCGA | | 624 |
| CCLG | 256 | |

# Ordering Information

RT54SX72S – 1 CQ 256 B

Application (Temperature Range)
- B = MIL-STD-883 Class B
- E = E-Flow (Actel Space Level Flow)
- M = Military Temperature

Package Lead Count

Package Type
- CQ = Ceramic Quad Flat Pack
- CG = Ceramic Column Grid Aray
- CC = Ceramic Chip Carrier Land Grid

Speed Grade
- Blank = Standard Speed
- 1 = Approximately 15% Faster than Standard

Part Number
- RT54SX32S = 32,000 RadTolerant Typical Gates
- RT54SX72S = 72,000 RadTolerant Typical Gates

# Ceramic Device Resources

| Device | User I/Os (including clock buffers) | | | |
|---|---|---|---|---|
| | CQFP 208-Pin | CQFP 256-Pin | CCLG 256-Pin | CCGA 624-Pin |
| RT54SX32S | 173 | 227 | 202 | – |
| RT54SX72S | 170 | 212 | – | 360 |

**Note:** *The 256-Pin CCLG available in Mil-Temp only.*

# Temperature Grade and Application Offering

| Package | RT54SX32S | RT54SX72S |
|---|---|---|
| CQ208 | B, E | B, E |
| CQ256 | B, E | B, E |
| CC256 | M | – |
| CG624 | – | B, E |

**Note:** *M = Military Temperature*
*B = MIL-STD-883 Class B*
*E = E-Flow*

## Speed Grade and Temperature/Application Matrix

| | Std. | –1 |
|---|---|---|
| M | ✓ | ✓ |
| B | ✓ | ✓ |
| E | ✓ | ✓ |

## QML Certification

Actel has achieved full QML certification, demonstrating that quality management procedures, processes, and controls are in place and comply with MIL-PRF-38535 (the performance specification used by the U.S. Department of Defense for monolithic integrated circuits).

## Actel MIL-STD-883 Class B Product Flow

| Step | Screen | 883 Method | 883 Class B Requirement |
|---|---|---|---|
| 1. | Internal Visual | 2010, Test Condition B | 100% |
| 2. | Temperature Cycling | 1010, Test Condition C | 100% |
| 3. | Constant Acceleration | 2001, Test Condition B or D, $Y_1$, Orientation Only | 100% |
| 4. | Particle Impact Noise Detection | 2020, Condition A | 100% |
| 5. | Seal<br>a. Fine<br>b. Gross | 1014 | <br>100%<br>100% |
| 6. | Visual Inspection | 2009 | 100% |
| 7. | Pre-Burn-In Electrical Parameters | In accordance with applicable Actel device specification | 100% |
| 8. | Dynamic Burn-In | 1015, Condition D, 160 hours at 125°C or 80 hours at 150°C | 100% |
| 9. | Interim (Post-Burn-In) Electrical Parameters | In accordance with applicable Actel device specification | 100% |
| 10. | Percent Defective Allowable | 5% | All Lots |
| 11. | Final Electrical Test<br><br>a. Static Tests<br>(1)25°C<br>(Subgroup 1, Table I)<br>(2)–55°C and +125°C<br>(Subgroups 2, 3, Table I)<br><br>b. Functional Tests<br>(1)25°C<br>(Subgroup 7, Table I)<br>(2)–55°C and +125°C<br>(Subgroups 8A and 8B, Table I)<br><br>c. Switching Tests at 25°C<br>(Subgroup 9, Table I) | In accordance with applicable Actel device specification, which includes a, b, and c:<br><br><br>5005<br><br>5005<br><br><br><br>5005<br><br>5005<br><br><br>5005 | <br><br>100%<br><br><br><br><br><br>100%<br><br><br><br><br><br>100% |
| 12. | External Visual | 2009 | 100% |

# Actel Extended Flow[1]

| Step | Screen | Method | Requirement |
|---|---|---|---|
| 1. | Destructive In-Line Bond Pull[3] | 2011, Condition D | Sample |
| 2. | Internal Visual | 2010, Condition A | 100% |
| 3. | Serialization | | 100% |
| 4. | Temperature Cycling | 1010, Condition C | 100% |
| 5. | Constant Acceleration | 2001, Condition B or D, $Y_1$ Orientation Only | 100% |
| 6. | Particle Impact Noise Detection | 2020, Condition A | 100% |
| 7. | Radiographic | 2012 (one view only) | 100% |
| 8. | Pre-Burn-In Test | In accordance with applicable Actel device specification | 100% |
| 9. | Dynamic Burn-In | 1015, Condition D, 240 hours at 125°C or 120 hours at 150°C minimum | 100% |
| 10. | Interim (Post-Burn-In) Electrical Parameters | In accordance with applicable Actel device specification | 100% |
| 11. | Static Burn-In | 1015, Condition C, 72 hours at 150°C or 144 hours at 125°C minimum | 100% |
| 12. | Interim (Post-Burn-In) Electrical Parameters | In accordance with applicable Actel device specification | 100% |
| 13. | Percent Defective Allowable (PDA) Calculation | 5%, 3% Functional Parameters at 25°C | All Lots |
| 14. | Final Electrical Test<br>a. Static Tests<br>(1)25°C<br>(Subgroup 1, Table1)<br>(2)–55°C and +125°C<br>(Subgroups 2, 3, Table 1)<br>b. Functional Tests<br>(1)25°C<br>(Subgroup 7, Table 15)<br>(2)–55°C and +125°C<br>(Subgroups 8A and B, Table 1)<br>c. Switching Tests at 25°C<br>(Subgroup 9, Table 1) | In accordance with Actel applicable device specification which includes a, b, and c:<br><br>5005<br><br>5005<br><br><br>5005<br><br>5005<br><br><br>5005 | 100%<br>100%<br><br><br><br><br>100%<br><br><br><br><br>100% |
| 15. | Seal<br>a. Fine<br>b. Gross | 1014 | 100% |
| 16. | External Visual | 2009 | 100% |

***Notes:***

1. *Actel offers Extended Flow for users requiring additional screening beyond MIL-STD-833, Class B requirement. Actel offers this Extended Flow incorporating the majority of the screening procedures as outlined in Method 5004 of MIL-STD-883, Class S. The exceptions to Method 5004 are shown in notes 2 and 4 below.*
2. *MIL-STD-883, Method 5004, requires a 100 percent radiation latch-up testing to Method 1020. Actel will NOT perform any radiation testing, and this requirement must be waived in its entirety.*
3. *Method 5004 requires a 100 percent, nondestructive bond-pull to Method 2003. Actel substitutes a destructive bond-pull to Method 2011 Condition D on a sample basis only.*
4. *Wafer lot acceptance complies to commercial standards only (requirement per Method 5007 is not performed).*

# Table of Contents

# General Description

RTSX-S RadTolerant FPGAs are enhanced versions of Actel's SX-A family of devices, specifically designed for enhanced radiation performance.

Featuring SEU-hardened D-type flip-flops that offer the benefits of Triple Module Redundancy (TMR) without the associated overhead, the RTSX-S family is a unique product offering for space applications. Manufactured using 0.25 µm technology at the Matsushita (MEC) facility in Japan, RTSX-S offers levels of radiation survivability far in excess of typical CMOS devices.

## Device Architecture

Actel's RTSX-S architecture, derived from the highly successful SX-A sea-of-modules architecture, has been designed to improve upset and total-dose performance in radiation environments.

With three layers of metal interconnect in the RT54SX32S and four metal layers in RT54SX72S, the RTSX-S family provides efficient use of silicon by locating the routing interconnect resources between the top two metal layers. This completely eliminates the channels of routing and interconnect resources between logic modules as found in traditional FPGAs. In a sea-of-modules architecture, the entire floor of the FPGA is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing.

The RTSX-S architecture adds several enhancements over the SX-A architecture to improve its performance in radiation environments, such as SEU-hardened flip-flops, wider clock lines, and stronger clock drivers.

## Programmable Interconnect Element

Interconnection between logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements. The antifuses are normally open circuit and form a permanent, low-impedance connection when programmed.

The metal-to-metal antifuse is made up of a combination of amorphous silicon and dielectric material with barrier metals and has a programmed ("on" state) resistance of 25 Ω with capacitance of 1.0 fF for low signal impedance (Figure 1-1).

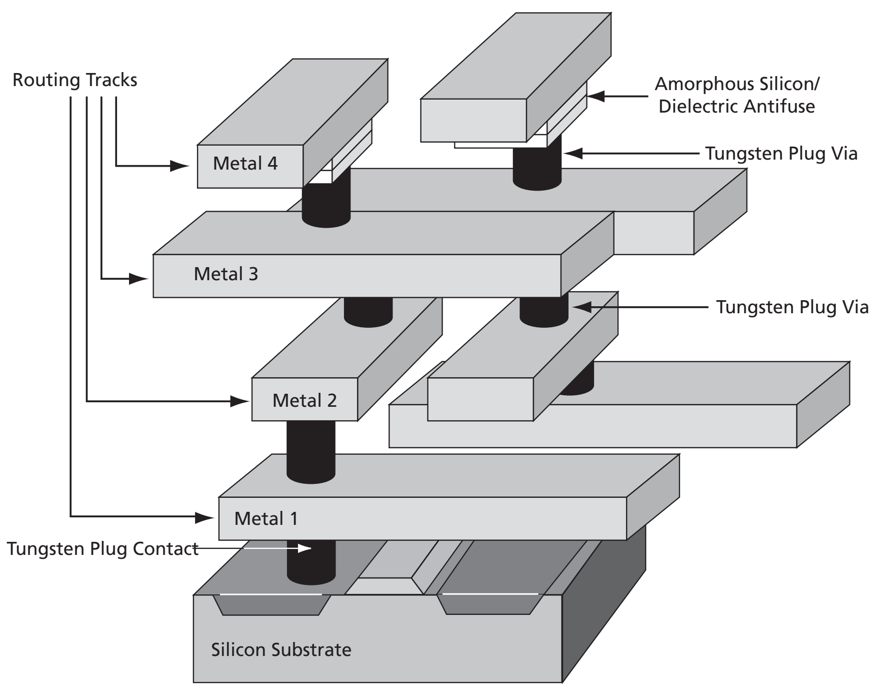


*Figure 1-1* • **RTSX-S Family Interconnect Elements**

These antifuse interconnects reside between the top two layers of metal and thereby enable the sea-of-modules architecture in an FPGA.

The extremely small size of these interconnect elements gives the RTSX-S family abundant routing resources and provides excellent protection against design theft. Reverse engineering is virtually impossible because it is extremely difficult to distinguish between programmed and unprogrammed antifuses. Additionally, since RTSX-S is a nonvolatile, single-chip solution, there is no configuration bitstream to intercept.

The RTSX-S interconnect (i.e., the antifuses and metal tracks) also has lower capacitance and resistance than that of any other device of similar capacity, leading to the fastest signal propagation in the industry for the radiation tolerance offered.

# I/O Structure

The RTSX-S family features a flexible I/O structure that supports 3.3V LVTTL, 5V TTL, 5V CMOS, and 3.3V and 5V PCI. All I/O standards are hot-swap compliant, cold-sparing capable, and 5V tolerant (except for 3.3V PCI).

In addition, each I/O on an RTSX-S device can be configured as an input, an output, a tristate output, or a bidirectional pin. Mixed I/O standards are allowed and can be set on a pin-by-pin basis. High or low slew rate can be set on individual output buffers (except for PCI, which defaults to high slew), as well as the power-up configuration (either pull-up or pull-down).

Even without the inclusion of dedicated I/O registers, these I/Os, in combination with array registers, can achieve clock-to-output-pad timing as fast as 9.5 ns. In most FPGAs, I/O cells that have embedded latches and flip-flops require instantiation in HDL code; this is a design complication not encountered in RTSX-S FPGAs. Fast pin-to-pin timing ensures that the device will have little trouble interfacing with any other device in the system, which in turn, enables parallel design of system components and reduces overall design time.

# Logic Modules

Actel's RTSX-S family provides two types of logic modules to the designer (Figure 1-2 on page 1-3): the register cell (R-cell) and the combinatorial cell (C-cell).

The C-cell implements a range of combinatorial functions with up to 5 inputs. Inclusion of the DB input and its associated inverter function dramatically increases the number of combinatorial functions that can be implemented in a single module from 800 options (as in previous architectures) to more than 4,000 in the RTSX-S architecture. An example of the improved flexibility enabled by the inversion capability is the ability to integrate a three-input exclusive-OR function into a single C-cell. This facilitates the construction of nine-bit parity-tree functions. At the same time, the C-cell structure is extremely synthesis-friendly, simplifying the overall design and reducing synthesis time.

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines) control signals. The R-cell registers feature programmable clock polarity, selectable on a register-by-register basis. This provides additional flexibility during mapping of synthesized functions into the RTSX-S FPGA. The clock source for the R-cell can be chosen from the hardwired clock, the routed clocks, or the internal logic.

While each SEU-hardened R-cell appears as a single D-type flip-flop to the user, each is implemented employing triple redundancy to achieve a LET threshold of greater than 40 MeV-cm$^2$/mg. Each TMR R-cell consists of three master-slave latch pairs, each with asynchronous, self-correcting feedback paths. The output of each latch on the master or slave side is voted with the outputs of the other two latches on that side. If one of the three latches is struck by an ion and starts to change state, the voting with the other two latches prevents the change from feeding back and permanently latching. Care was taken in the layout to ensure that a single ion strike could not affect more than one latch (see "R-Cell" section on page 2-23 for more details).

Actel has arranged all C-cell and R-cell logic modules into horizontal banks called Clusters. There are two types of clusters: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

To increase design efficiency and device performance, Actel has further organized these modules into SuperClusters. SuperCluster 1 is a two-wide grouping of Type 1 clusters. SuperCluster 2 is a two-wide group containing one Type 1 cluster and one Type 2 cluster. RTSX-S devices feature more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops (Figure 1-2 on page 1-3).

# Routing

R-cells and C-cells within Clusters and SuperClusters can be connected through the use of two innovative local routing resources called FastConnect and DirectConnect, which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters. This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance (Figure 1-3 on page 1-4 and Figure 1-4 on page 1-4).

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hardwired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering a maximum interconnect propagation delay of 0.4 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally-oriented routing resources known as segmented routing and high-drive routing. Actel's segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100-percent-automatic place-and-route software to minimize signal propagation delays.

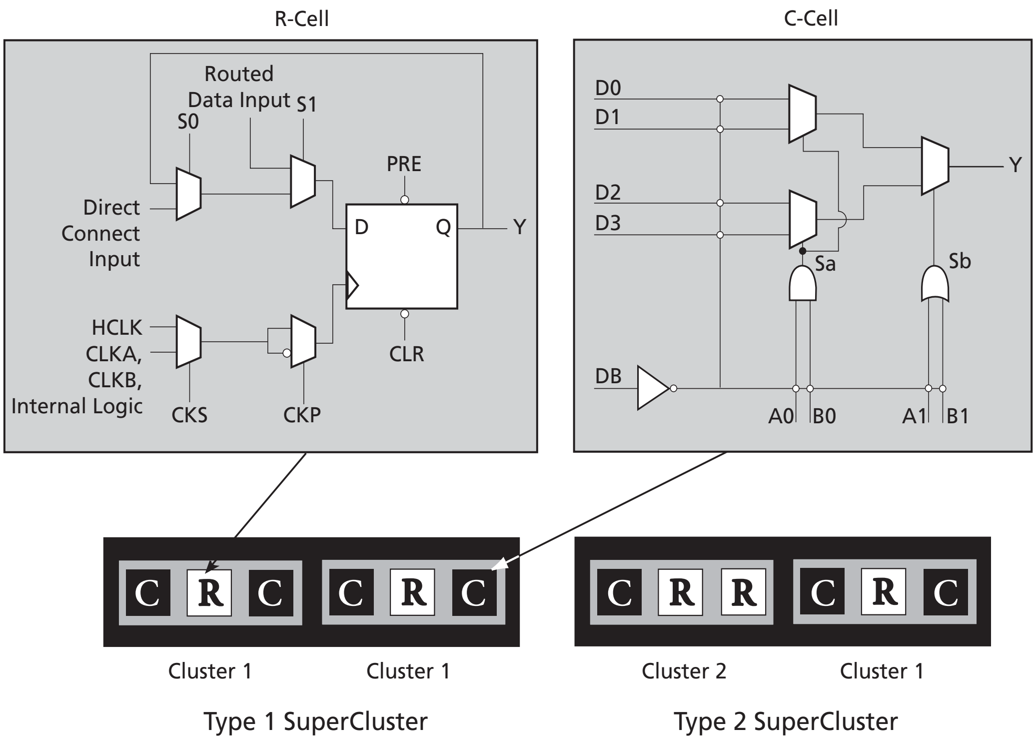


*Figure 1-2* • **R-Cell, C-Cell, and Cluster Organization**

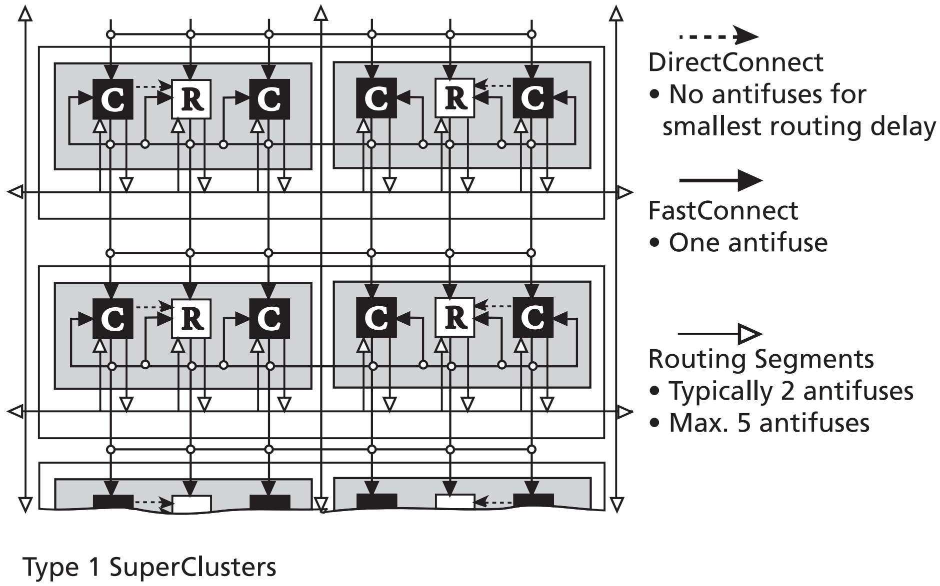


*Figure 1-3* • **DirectConnect and FastConnect for SuperCluster 1s**

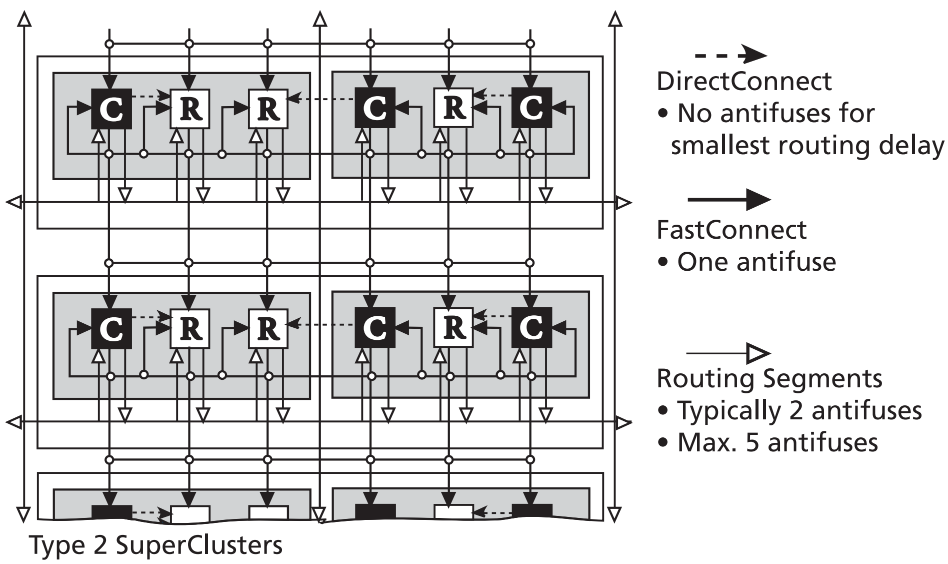


*Figure 1-4* • **DirectConnect and FastConnect for SuperCluster 2s**

## Global Resources

Actel’s high-drive routing structure provides three clock networks: hardwired clocks (HCLK), routed clocks (CLKA, CLKB), and quadrant clocks (QCLKA, QCLKB, QCLKC, QCLKD).

*Table 1-1* • **RTSX-S Global Resources**

| | RT54SX32S | RT54SX72S |
|---|---|---|
| Routed Clocks (CLKA, CLKB) | 2 | 2 |
| Hardwired Clocks (HCLK) | 1 | 1 |
| Quadrant Clocks (QCLKA, QCLKB, QCLKC, QCLKD) | 0 | 4 |

The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select MUX in each R-cell. HCLK cannot be connected to combinational logic. This provides a fast propagation path for the clock signal, enabling the 9.5 ns clock-to-out (pad-to-pad) performance of the RTSX-S devices.

The second type of clock, routed clocks, (CLKA, CLKB) are global clocks that can be sourced from either external pins or internal logic signals within the device. CLKA and CLKB may be connected to sequential cells (R-cells) or to combinational logic (C-cells).

The last type of clock, quadrant clocks, are only found in the RT54SX72S. Similar to the routed clocks, the four quadrant clocks (QCLKA, QCLKB, QCLKC, QCLKD) can be sourced from external pins or from internal logic signals within the device. Each of these clocks can individually drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants.

## Design Environment

The RTSX-S family of FPGAs is fully supported by both Actel's Libero™ Integrated Design Environment (IDE) and Designer FPGA Development software. Actel Libero IDE is a design management environment, seamlessly integrating design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify® for Actel from Synplicity®, ViewDraw for Actel from Mentor Graphics, Model*Sim*™ HDL Simulator from Mentor Graphics®, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Actel. Refer to the *Libero IDE flow* (located on Actel’s website) diagram for more information.

Actel's Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can select and lock package pins while only minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Actel’s integrated verification and logic analysis tool. Another tool included in the Designer software is the ACTgen macro builder, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design. Actel's Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and UNIX operating systems.

## Programming

Programming support is provided through Actel's Silicon Sculptor II, a single-site programmer driven via a PC-based GUI. Factory programming is available as well.

## Low-Cost Prototyping Solution

Since the enhanced radiation characteristics of radiation-tolerant devices are not required during the prototyping phase of the design, Actel has developed a prototyping solution for RTSX-S that utilizes commercial SX-A devices. The prototyping solution consists of two parts:

- A well-documented design flow that allows the customer to target an RTSX-S design to the equivalent commercial SX-A device
- Either footprint-compatible packages or protoyping sockets to adapt commercial SX-A packages to the RTAX-S package footprints

This methodology provides the user with a cost-effective solution while maintaining the short time-to-market associated with Actel FPGAs. Please see the application note *Prototyping for the RTSX-S Enhanced Aerospace FPGA* for more details

# In-System Diagnostic and Debug Capabilities

The RTXS-S family of FPGAs includes internal probe circuitry, allowing the designer to dynamically observe and analyze any signal inside the FPGA without disturbing normal device operation. Two individual signals can be brought out to two multipurpose pins (PRA and PRB) on the device. The probe circuitry is accessed and controlled via Silicon Explorer II, Actel's integrated verification and logic analysis tool, which attaches to the serial port of a PC and communicates with the FPGA via the JTAG port.

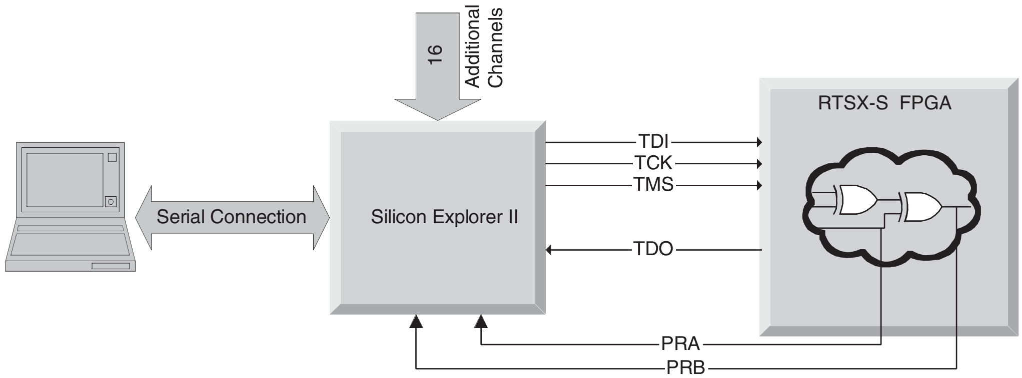


*Figure 1-5* • **Probe Setup**

## Radiation Survivability

The RTSX-S RadTolerant devices have varying total-dose radiation survivability. The ability of these devices to survive radiation effects is both device and lot dependent.

Total-dose results are summarized in two ways. The first summary is indicated by the maximum total-dose level achieved before the device fails to meet an individual performance specification but remains functional. For Actel FPGAs, the parameter that first exceeds the specification is $I_{CC}$ (standby supply current). The second summary is indicated by the maximum total dose achieved prior to the functional failure of the device.

Actel provides total-dose radiation test data on each lot. Reports are available on Actel's website or from Actel's local sales representatives. Listings of available lots and devices can also be provided.

For a radiation performance summary, see *Radiation Data*. This summary also shows single-event upset (SEU) and single-event latch-up (SEL) testing that has been performed on Actel FPGAs.

All radiation performance information is provided for informational purposes only and is not guaranteed. Total dose effects are lot-dependent, and Actel does not guarantee that future devices will continue to exhibit similar radiation characteristics. In addition, actual performance can vary widely due to a variety of factors, including but not limited to, characteristics of the orbit, radiation environment, proximity to the satellite exterior, the amount of inherent shielding from other sources within the satellite, and actual bare die variations. For these reasons, it is the sole responsibility of the user to determine whether the device will meet the requirements of the specific design.

## Summary

The RTSX-S family of RadTolerant FPGAs extends Actel's highly successful offering of FPGAs for radiation environments with the industry's first FPGA designed specifically for enhanced radiation performance.

# Related Documents

## Application Notes

*Simultaneous Switching Noise and Signal Integrity*
http://www.actel.com/documents/SSN_AN.pdf

*Implementation of Security in Actel Antifuse FPGAs*
http://www.actel.com/documents/Antifuse_Security_AN.pdf

*Using A54SX72A and RT54SX72S Quadrant Clocks*
http://www.actel.com/documents/QCLK_AN.pdf

*Actel eX, SX-A and RTSX-S I/Os*
http://www.actel.com/documents/AntifuseIO_AN.pdf

*IEEE Standard 1149.1 (JTAG) in the SX/RTSX/SX-A/eX/RT54SX-S Families*
http://www.actel.com/documents/SX_SXAJTAG_AN.pdf

*Prototyping for the RT54SX-S Enhanced Aerospace FPGA*
http://www.actel.com/documents/RTSXS_Proto_AN.pdf

*Actel CQFP to FBGA Adapter Socket Instructions*
http://www.actel.com/documents/CQ352-FPGA_Adapter_AN.pdf

*Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications*
http://www.actel.com/documents/HotSwapColdSparing_AN.pdf

## User's Guides and Manuals

*Antifuse Macro Library Guide*
http://www.actel.com/documents/libguide.pdf

*ACTgen Macros User's Guide*
http://www.actel.com/documents/genguide.pdf

*Libero IDE v5.2 User's Guide*
http://www.actel.com/documents/liberoUG.pdf

*Silicon Sculptor II User's Guide*
http://www.actel.com/techdocs/manuals/default.asp

## White Papers

*Design Security in Nonvolatile Flash and Antifuse FPGAs*
http://www.actel.com/documents/DesignSecurity_WP.pdf

*Understanding Actel Antifuse Device Security*
http://www.actel.com/documents/AntifuseSecurityWP.pdf

# Detailed Specifications

## General Conditions

*Table 2-1* • **Supply Voltages**

| $V_{CCA}$ | $V_{CCI}$ | Maximum Input Tolerance | Maximum Output Drive |
|---|---|---|---|
| 2.5V | 3.3V | 5V* | 3.3V |
| 2.5V | 5V | 5V | 5V |

**Note:** **3.3V PCI is not 5V tolerant*

*Table 2-2* • **Characteristics for All I/O Configurations**

| I/O Standard | Hot Swappable | Slew Rate Control | Power up Resistor Pull |
|---|---|---|---|
| TTL, LVTTL | Yes | Yes. Affects falling edge outputs only | Pull-up or Pull-down |
| 3.3V PCI | No | No. High slew rate only | Pull-up or Pull-down |
| 5V PCI | Yes | No. High slew rate only | Pull-up or Pull-down |

*Table 2-3* • **Time at which I/Os Become Active by Ramp Rate (At room temperature and nominal operating conditions)**

| Ramp Rate | 0.25V/ms | 0.025V/ms | 5V/ms | 2.5V/ms | 0.5V/ms | 0.25V/ms | 0.1V/ms | 0.025V/ms |
|---|---|---|---|---|---|---|---|---|
| **Units** | **ms** | **ms** | **ms** | **ms** | **ms** | **ms** | **ms** | **ms** |
| RT54SX32S | 10 | 100 | 0.46 | 0.74 | 2.8 | 5.2 | 12.1 | 47.2 |
| RT54SX72S | 10 | 100 | 0.41 | 0.67 | 2.6 | 5.0 | 12.1 | 47.2 |

## Power-Up and Power-Cycling

The RTSX-S family does not require any specific initial power-up sequence. However, if the power-up/down happens periodically (power-cycling) with an improper power sequence profile and not enough delay between the cycles, an in-rush current appears on $I_{CCI}$ under specific conditions. Therefore, if an application requires periodic power-cycling of the device, the following power sequence profile is recommended:

1. Power-up $V_{CCA}$ to at least 0.7V before powering-up $V_{CCI}$
2. If it is impossible to power-up $V_{CCA}$ before $V_{CCI}$, ensure that a suitable period of time is allowed between $V_{CCA}$ and $V_{CCI}$ power-down and subsequent power-up

The in-rush current phenomenon does not impact the long-term reliability of the device. Please see the application note *Power Cycling of RTSX-S Devices* for more details.

# Operating Conditions

## Absolute Maximum Conditions

Stresses beyond those listed in Table 2-4 may cause permanent damage to the device. Exposure to absolute maximum rated conditions may affect device reliability. Devices should not be operated outside the recommendations in Table 2-5.

*Table 2-4* • **Absolute Maximum Conditions**

| Symbol | Parameter | Limits | Units |
|---|---|---|---|
| $V_{CCI}$ | DC Supply Voltage | –0.3 to +6.0 | V |
| $V_{CCA}$ | DC Supply Voltage | –0.3 to +3.0 | V |
| $V_I$ | Input Voltage | –0.5 to + 6.0 | V |
| $V_I$ | Input Voltage for Bidirectional I/Os when using 3.3V PCI | –0.5 to $+V_{CCI}$ + 0.5 | V |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |

*Table 2-5* • **Recommended Operating Conditions**

| Parameter | Military | Units |
|---|---|---|
| Temperature Range (case temperature) | –55 to +125 | °C |
| 2.5V Power Supply Tolerance | 2.25 to 2.75 | V |
| 3.3V Power Supply Tolerance | 3.0 to 3.6 | V |
| 5V Power Supply Tolerance | 4.5 to 5.5 | V |

## Power Dissipation

A critical element of system reliability is the ability of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

A complete power evaluation should be performed early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device's maximum allowed junction temperature.

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To perform a power evaluation, follow these steps:

1. Estimate the power consumption of the application.
2. Calculate the maximum power allowed for the device and package.
3. Compare the estimated power and maximum power values.

### Estimating Power Dissipation

The total power dissipation for the RTSX-S family is the sum of the DC power dissipation and the AC power dissipation:

$$P_{Total} = P_{DC} + P_{AC}$$

*EQ 2-1*

### DC Power Dissipation

The power due to standby current is typically a small component of the overall power. The DC power dissipation is defined as:

$$P_{DC} = (I_{CC})*V_{CCA} + (I_{CC})*V_{CCI}$$

*EQ 2-2*

## AC Power Dissipation

The power dissipation of the RTSX-S family is usually dominated by the dynamic power dissipation. Dynamic power dissipation is a function of frequency, equivalent capacitance, and power supply voltage. The AC power dissipation is defined as follows:

$$P_{AC} = P_{C\text{-}Cells} + P_{R\text{-}Cells} + P_{CLKA} + P_{CLKB} + P_{HCLK} + P_{Output\ Buffer} + P_{Input\ Buffer}$$

*EQ 2-3*

or:

$$P_{AC} = V_{CCA}^2 * [(m * C_{EQCM} * fm)_{C\text{-}Cells} + (m * C_{EQSM} * fm)_{R\text{-}Cells} + (n * C_{EQI} * f_n)_{Input\ Buffer} + (p * (C_{EQO} + C_L) * f_p)_{Output\ Buffer} + (0.5 * (q_1 * C_{EQCR} * f_{q1}) + (r_1 * f_{q1}))_{CLKA} + (0.5 * (q_2 * C_{EQCR} * f_{q2}) + (r_2 * f_{q2}))_{CLKB} + (0.5 * (s_1 * C_{EQHV} * f_{s1}) + (C_{EQHF} * f_{s1}))_{HCLK}]$$

*EQ 2-4*

Where:

$C_{EQCM}$ = Equivalent capacitance of combinatorial modules (C-Cells) in pF

$C_{EQSM}$ = Equivalent capacitance of sequential modules (R-Cells) in pF

$C_{EQI}$ = Equivalent capacitance of input buffers in pF

$C_{EQO}$ = Equivalent capacitance of output buffers in pF

$C_{EQCR}$ = Equivalent capacitance of CLKA/B in pF

$C_{EQHV}$ = Variable capacitance of HCLK in pF

$C_{EQHF}$ = Fixed capacitance of HCLK in pF

$C_L$ = Output lead capacitance in pF

$f_m$ = Average logic module switching rate in MHz

$f_n$ = Average input buffer switching rate in MHz

$f_p$ = Average output buffer switching rate in MHz

$f_{q1}$ = Average CLKA rate in MHz

$f_{q2}$ = Average CLKB rate in MHz

$f_{s1}$ = Average HCLK rate in MHz

m = Number of logic modules switching at fm

n = Number of input buffers switching at fn

p = Number of output buffers switching at fp

$q_1$ = Number of clock loads on CLKA

$q_2$ = Number of clock loads on CLKB

$r_1$ = Fixed capacitance due to CLKA

$r_2$ = Fixed capacitance due to CLKB

$s_1$ = Number of clock loads on HCLK

x = Number of I/Os at logic low

y = Number of I/Os at logic high

*Table 2-6* • **Fixed Power Parameters**

| Parameter | RT54SX32S | RT54SX72S | Units |
|---|---|---|---|
| $C_{EQCM}$ | 3.00 | 3.00 | pF |
| $C_{EQSM}$ | 3.00 | 3.00 | pF |
| $C_{EQI}$ | 1.40 | 1.30 | pF |
| $C_{EQO}$ | 7.40 | 7.40 | pF |
| $C_{EQCR}$ | 3.50 | 3.50 | pF |
| $C_{EQHV}$ | 4.30 | 4.30 | pF |
| $C_{EQHF}$ | 300 | 690 | pF |
| $r_1$ | 100 | 245 | pF |
| $r_2$ | 100 | 245 | pF |
| $I_{CC}$ | 25 | 25 | mA |

## Guidelines for Estimating Power

The following guidelines are meant to represent worst-case scenarios; they can be generally used to predict the upper limits of power dissipation:

Logic Modules (m) = 20% of modules
Inputs Switching (n) = # inputs/4
Outputs Switching (p) = # output/4
CLKA Loads (q1) = 20% of R-cells
CLKB Loads (q2) = 20% of R-cells
Load Capacitance (CL) = 35 pF
Average Logic Module Switching Rate (fm) = f/10
Average Input Switching Rate (fn) =f/5
Average Output Switching Rate (fp) = f/10
Average CLKA Rate (fq1) = f/2
Average CLKB Rate (fq2) = f/2
Average HCLK Rate (fs1) = f
HCLK loads (s1) = 20% of R-cells

To assist customers in estimating the power dissipations of their designs, Actel has published the *eX, SX-A and RT54SX-S Power Calculator* worksheet.

# Thermal Characteristics

## Introduction

The temperature variable in Actel's Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient, case, or board temperatures. EQ 2-5, EQ 2-6, and EQ 2-7 give the relationship between thermal resistance, temperature gradient and power.

$$\theta_{ja} = \frac{T_j - T_a}{P}$$

*EQ 2-5*

$$\theta_{jc} = \frac{T_j - T_c}{P}$$

*EQ 2-6*

$$\theta_{jb} = \frac{T_j - T_b}{P}$$

*EQ 2-7*

Where:

$\theta_{ja}$ = Junction-to-air thermal resistance of the package. $\theta_{ja}$ numbers are located in Table 2-7.

$\theta_{jc}$ = Junction-to-case thermal resistance of the package. $\theta_{jc}$ numbers are located in Table 2-7.

$\theta_{jb}$ = Junction-to-board thermal resistance of the package. $\theta_{jb}$ for a 624-pin CCGA is located in the notes for Table 2-7.

$T_j$ = Junction Temperature

$T_a$ = Ambient Temperature

$T_b$ = Board Temperature

$T_c$ = Case Temperature

P = Power

## Package Thermal Characteristics

The device thermal characteristics $\theta_{jc}$ and $\theta_{ja}$ are given in Table 2-7. The thermal characteristics for $\theta_{ja}$ are shown with two different air flow rates. Note that the absolute maximum junction temperature is 150°C.

*Table 2-7* • **Package Thermal Characteristics**

| Package Type | Pin Count | $\theta_{jc}$ | $\theta_{ja}$ | | | Units |
|---|---|---|---|---|---|---|
| | | | Still Air | $\theta_{ja}$ 1.0m/s | $\theta_{ja}$ 2.5m/s | |
| Ceramic Quad Flat Pack (CQFP) | 208 | 2.0 [1] | 22 | 19.8 | 18.0 | °C/W |
| Ceramic Quad Flat Pack (CQFP) | 256 | 2.0 [1] | 20 | 16.5 | 15.0 | °C/W |
| Ceramic Quad Flat Pack (CQFP) with heatsink | 208 | 0.5 [1] | 21.0 | 17.3 | 15.7 | °C/W |
| Ceramic Quad Flat Pack (CQFP) with heatsink | 256 | 0.5 [1] | 19.0 | 15.7 | 14.2 | °C/W |
| Ceramic Chip Carrier Land Grid (CCLG) | 256 | 1.1 [1] | 12.1 | 10.0 | 9.1 | °C/W |
| Ceramic Column Grid Array (CCGA) | 624 | 6.5 [2] | 8.9 | 8.5 | 8.0 | °C/W |

***Notes:***

1. *$\theta_{jc}$ for CQFP and CCLG packages refers to the thermal resistance between the junction and the bottom of the package.*
2. *$\theta_{jc}$ for the CCGA 624 refers to the thermal resistance between the junction and the top surface of the package. Thermal resistance from junction to board ($\theta_{jb}$) for CG624 package is 3.4 °C/W.*

## Maximum Allowed Power Dissipation

Shown below are example calculations to estimate the maximum allowed power dissipation for a given device based on two different thermal environments while maintaining the device junction temperature at or below worst-case military operating conditions (125°C).

### Example 1:

This example assumes that there is still air in the environment. The heat flow is shown by the arrows in Figure 2-1 on page 2-5. The maximum ambient air temperature is assumed to be 50°C. The device package used is the 624-pin CCGA.

$$\text{Max. Allowed Power} = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{\theta_{ja}} = \frac{125°C - 50°C}{8.9°C/W} = 8.43W$$

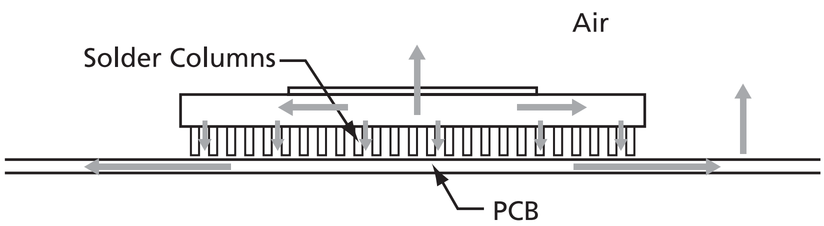


*Figure 2-1* • **Hear Flow When Air is Present**

**Example 2:**

This example assumes that the primary heat conduction path will be through the bottom of the package (neglecting the heat conducted through the package pins) to the board for a package mounted with thermal paste. The heat flow is shown by the arrows in Figure 2-2. The maximum board temperature is assumed to be 70°C. The device package used is the 352-pin CQFP. The thermal resistance ($\theta_{cb}$) of the thermal paste is assumed to be 0.58 °C/W.

$$\text{Max. Allowed Power} = \frac{T_j - T_b}{\theta_{jb}} = \frac{T_j - T_b}{\theta_{jc} + \theta_{cb}} = \frac{125°C - 70°C}{2.0°C/W + 0.58°C/W} = 21.32W$$

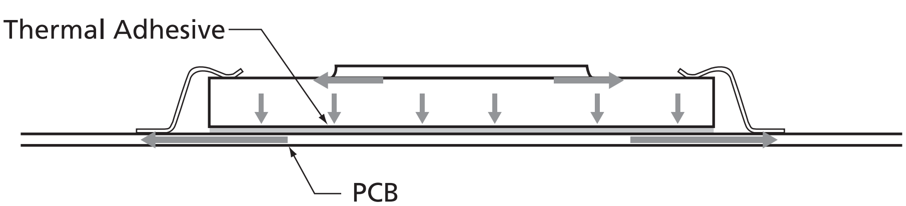


*Figure 2-2* • **Heat Flow in a Vacuum**

## Timing Derating

RTSX-S devices are manufactured in a CMOS process; therefore, device performance is dependent on temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing. The derating factors shown in Table 2-8 should be applied to all timing data contained within this datasheet.

*Table 2-8* • **Temperature and Voltage Derating Factors (Normalized to Worst-Case Military Conditions, $T_J$ = 125°C, $V_{CCA}$ = 2.25V)**

| $V_{CCA}$ | Junction Temperature ($T_J$) | | | | | | |
|---|---|---|---|---|---|---|---|
| | –55°C | –40°C | 0°C | 25°C | 70°C | 85°C | 125°C |
| 2.25 | 0.71 | 0.72 | 0.78 | 0.80 | 0.90 | 0.94 | 1.00 |
| 2.50 | 0.67 | 0.67 | 0.73 | 0.75 | 0.84 | 0.87 | 0.93 |
| 2.75 | 0.62 | 0.63 | 0.69 | 0.70 | 0.79 | 0.82 | 0.88 |

**Note:** *The user can set the junction temperature in Actel's Designer software to be any integer value in the range of –55°C to 175°C, and the core voltage to be any value between 2.25V and 2.75V.*

# Timing Model

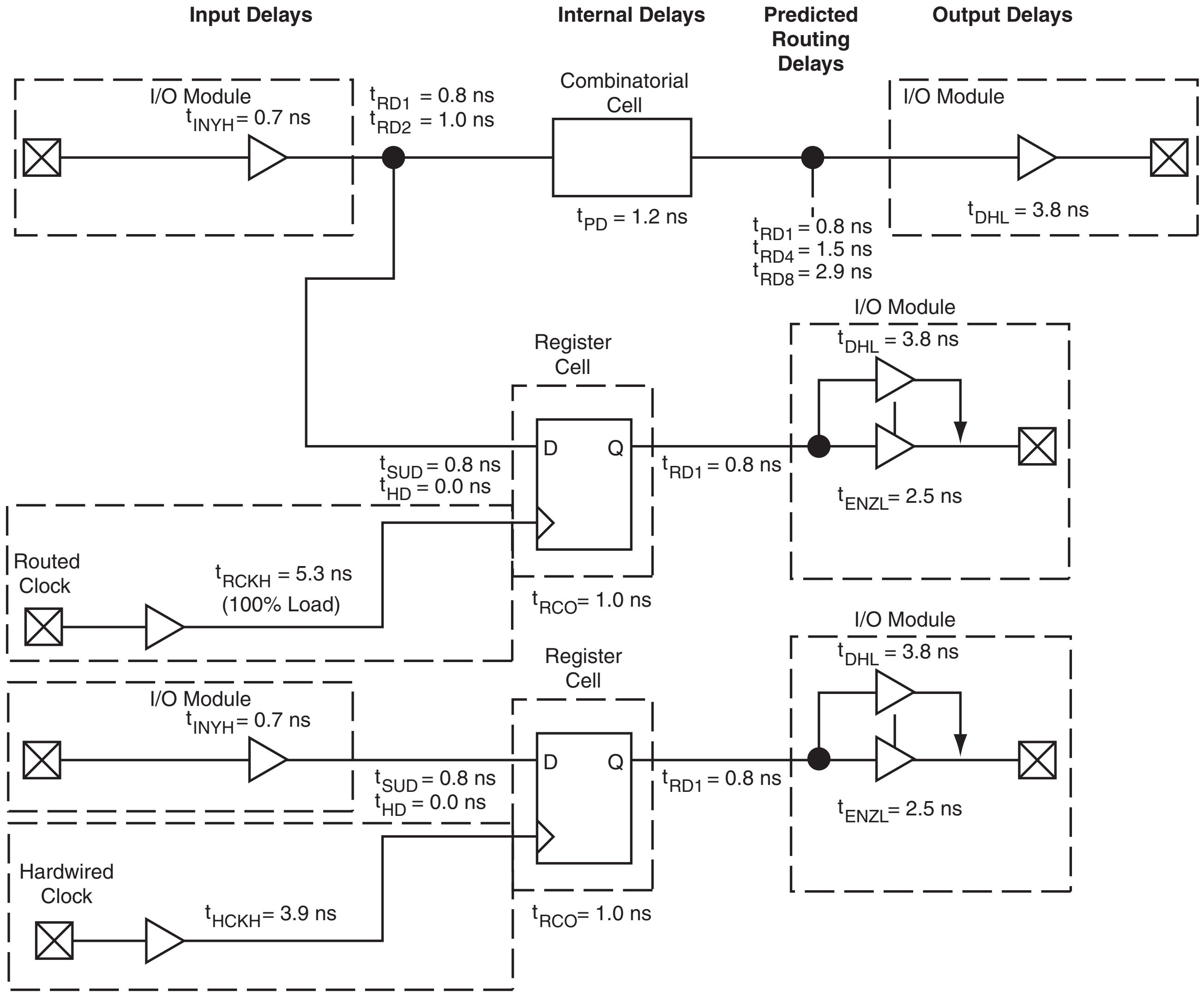


*Figure 2-3* • **RTSX-S Timing Model**
**Values shown for RT54SX32S, –1, 0 krad (Si), 5V TTL worst-case military conditions**

## Hardwired Clock

External Setup

$= (t_{INYH} + t_{RD2} + t_{SUD}) - t_{HCKH}$

$= 0.7 + 1.0 + 0.8 - 3.9 = -1.4$ ns

Clock-to-Out (Pad-to-Pad)

$= t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL}$

$= 3.9 + 1.0 + 0.8 + 3.8 = 9.5$ ns

## Routed Clock

External Setup

$= (t_{INYH} + t_{RD2} + t_{SUD}) - t_{RCKH}$

$= 0.7 + 1.0 + 0.8 - 5.3 = -2.8$ ns

Clock-to-Out (Pad-to-Pad)

$= t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL}$

$= 5.3 + 1.0 + 0.8 + 3.8 = 10.9$ ns

# I/O Specifications

## Pin Descriptions

### Supply Pins

**GND** **Ground**

Low supply voltage.

**$V_{CCI}$** **Supply Voltage**

Supply voltage for I/Os. See Table 2-1 on page 2-1.

**$V_{CCA}$** **Supply Voltage**

Supply voltage for Array. See Table 2-1 on page 2-1.

### Global Pins

**CLKA/B** **Routed Clock A and B**

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, 3.3V PCI, or 5V PCI specifications. The clock input is buffered prior to clocking the R-cells. When not used, this pin must be set Low or High on the board. When used, this pin should be held Low or High during power-up to avoid unwanted static power.

For RT54SX72S, these pins can be configured as user I/Os. When used, this pin offers a built-in programmable pull-up or pull-down resistor active during power-up only.

**QCLKA/B/C/D** **Quadrant Clock A, B, C, and D / I/O**

These four pins are the quadrant clock inputs and are only found on the RT54SX72S. They are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, 3.3V PCI or 5V PCI specifications. Each of these clock inputs can drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. The clock input is buffered prior to clocking the core cells.

These pins can be configured as user I/Os. When not used, these pins must not be left floating. They must be set Low or High on the board. When used, this pin offers a built-in programmable pull-up or pull-down resistor, active during power-up only.

**HCLK** **Dedicated (Hardwired) Array Clock**

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL, LVTTL, 3.3V PCI or 5V PCI specifications. This input is buffered prior to clocking the R-cells. It offers clock speeds independent of the number of R-cells being driven. When not used, this pin must not be left floating. It must be set to Low or High on the board. When used, this pin should be held Low or High during power-up to avoid unwanted static power.

### JTAG/Probe Pins

**PRA/PRB[1] I/O,** **Probe A/B**

The probe pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

**TCK[1], I/O** **Test Clock**

Test clock input for diagnostic probe and device programming. In flexible mode, TCK becomes active when the TMS pin is set Low (Table 2-32 on page 2-35). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

**TDI[1], I/O** **Test Data Input**

Serial input for boundary scan testing and diagnostic probe. In flexible mode, TDI is active when the TMS pin is set Low (Table 2-32 on page 2-35). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

**TDO[1], I/O** **Test Data Output**

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set Low (Table 2-32 on page 2-35). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer II is being used, TDO will act as an output when the "checksum" command is run. It will return to user I/O when "checksum" is complete.

**TMS[1]** **Test Mode Select**

The TMS pin controls the use of the IEEE 1149.1 boundary scan pins (TCK, TDI, TDO, TRST). In flexible mode when the TMS pin is set Low, the TCK, TDI, and TDO pins are boundary scan pins (Table 2-32 on page 2-35). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the "logic reset" state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The "logic reset" state is reached five TCK cycles after the TMS pin is set High. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

1. *These pins should be terminated with a 70 Ω resistor to preserve probing capabilities.*

**TRST** **Boundary Scan Reset Pin**

The TRST pin functions as an active-low input to asynchronously initialize or rest the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. For flight applications, the TRST pin should be hardwired to GND.

### User I/O

**I/O** **Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output levels are compatible with standard TTL, LVTTL, 3.3V/5V PCI, or 5V CMOS specifications. Unused I/O pins are automatically tristated by the Designer software. See "User I/O" section on page 2-8 for more details.

### Special Functions

**NC** **No Connection**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

## User I/O

The RTSX-S family features a flexible I/O structure that supports 3.3V LVTTL, 5V TTL, 5V CMOS, and 3.3V and 5V PCI. All I/O standards are hot-swap compliant, cold-sparing capable, and 5V tolerant (except for 3.3V PCI).

Each I/O module has an available power-up resistor of approximately 50 kΩ that can configure the I/O to a known state during power-up. Just slightly before $V_{CCA}$ reaches 2.5V, the resistors are disabled so the I/Os will behave normally. For more information about the power-up resistors, please see Actel's application note *SX-A and RTSX-S Devices in Hot-Swap and Cold Sparing Applications*.

RTSX-S inputs should be driven by high-speed push-pull devices with a low-resistance pull-up device. If the input voltage is greater than $V_{CCI}$ and a fast push-pull device is NOT used, the high-resistance pull-up of the driver and the internal circuitry of the RTSX-S I/O may create a voltage divider (when a user I/O is configured as an input, the associated output buffer is tristated). This voltage divider could pull the input voltage below specification for some devices connected to the driver. A logic '1' may not be correctly presented in this case. For example, if an open drain driver is used with a pull-up resistor to 5V to provide the logic '1' input, and $V_{CCI}$ is set to 3.3V on the RTSX-S device, the input signal may be pulled down by the RTSX-S input.

### Hot Swapping

RTSX-S I/Os can be configured to be hot swappable in compliance with the Compact PCI Specification. However, a 3.3V PCI device is not hot swappable. During power-up/down, all I/Os are tristated. $V_{CCA}$ and $V_{CCI}$ do not have to be stable during power-up/down. After the RTSX-S device is plugged into an electrically active system, the device will not degrade the reliability of or cause damage to the host system. The device's output pins are driven to a high impedance state until normal chip operating conditions are reached. Table 2-3 on page 2-1 summarizes the $V_{CCA}$ voltage at which the I/Os behave according to the user's design for an RTSX-S device at room temperature for various ramp-up rates. The data reported assumes a linear ramp-up profile to 2.5V. Refer to Actel's application note, *SX-A and RTSX-S Devices in Hot-Swap and Cold-Sparing Applications* for more information on hot swapping.

### Customizing the I/O

Each user I/O on an RTSX-S device can be configured as an input, an output, a tristate output, or a bidirectional pin. Mixed I/O standards are allowed and can be set on a pin-by-pin basis. High or low slew rates can be set on individual output buffers (except for PCI which defaults to high slew), as well as the power-up configuration (either pull-up or pull-down).

The user selects the desired I/O by setting the I/O properties in PinEditor, Actel's graphical pin-placement and I/O properties editor. See PinEditor online help for more information.

### Unused I/Os

All unused user I/Os are automatically tristated by Actel's Designer software. Although termination is not required, it is recommended that the user tie off all unused I/Os to GND externally. If the I/O clamp diode is disabled, then unused I/Os are 5V tolerant, otherwise unused I/Os are tolerant to $V_{CCI}$.

## I/O Macros

There are nine I/O macros available to the user for RTSX-S:

- CLKBUF/CLKBUFI: Clock Buffer, noninverting and inverting
- CLKBIBUF/CLKBIBUFI: Bidirectional Clock Buffer, noninverting and inverting
- QCLKBUF/QCLKBUFI: Quadrant Clock Buffer, noninverting and inverting
- QCLKBIBUF/QCLKBIBUFI: Quad Bidirectional Clock Buffer, noninverting and inverting
- HCLKBUF: Hardwired Clock Buffer
- INBUF: Input Buffer
- OUTBUF: Output Buffer
- TRIBUF: Tristate Buffer
- BIBUF: Bidirectional Buffer

*Table 2-9* • **User I/O Features**

| Function | Description |
|---|---|
| Input Buffer Threshold Selections | • 5V: CMOS, PCI, TTL<br>• 3.3V: PCI, LVTTL |
| Flexible Output Driver | • 5V: CMOS, PCI, TTL<br>• 3.3V: PCI, LVTTL<br>• Selectable on an individual I/O basis |
| Output Buffer | "Hot-Swap" Capability<br>• I/Os on an unpowered device does not sink the current (Power supplies are at 0V)<br>• Can be used for "cold sparing"<br>Individually selectable slew rate, high or low slew (The default is high slew rate). The slew rate selection only affects the falling edge of an output. There is no change on the rising edge of the output or any inputs. |
| Power-Up | Individually selectable pull-ups and pull-downs during power-up (default is to power-up in tristate mode)<br>Enables deterministic power-up of a device<br>$V_{CCA}$ and $V_{CCI}$ can be powered in any order |

## I/O Module Timing Characteristics

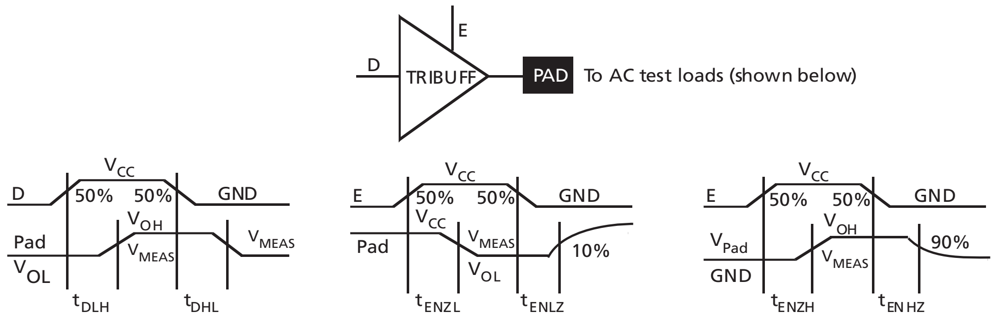


*Figure 2-4* • **Output Timing Model and Waveforms**

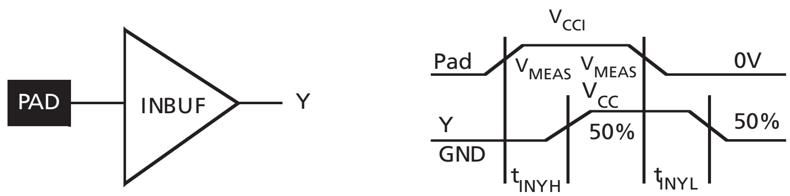


*Figure 2-5* • **Input Timing Model and Waveforms**

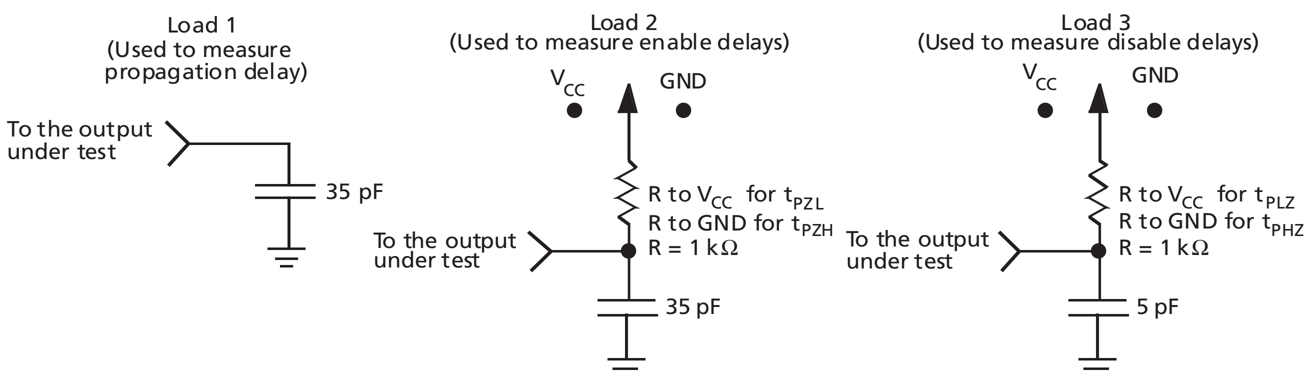


*Figure 2-6* • **AC Test Loads**

## 5V TTL and 3.3V LVTTL

*Table 2-10* • **5V TTL and 3.3V LVTTL Electrical Specifications**

| Symbol | Parameter | | Military Min. | Military Max. | Units |
|---|---|---|---|---|---|
| $V_{OH}$ | $V_{CCI}$ = Min, $V_I = V_{IH}$ or $V_{IL}$ | ($I_{OH}$ = -1mA) | 0.9 $V_{CCI}$ | | V |
| | $V_{CCI}$ = Min, $V_I = V_{IH}$ or $V_{IL}$ | ($I_{OH}$ = -8mA) | 2.4 | | V |
| $V_{OL}$ | $V_{CCI}$ = Min, $V_I = V_{IH}$ or $V_{IL}$ | ($I_{OL}$= 1mA) | | 0.1 $V_{CCI}$ | V |
| | $V_{CCI}$ = Min, $V_I = V_{IH}$ or $V_{IL}$ | ($I_{OL}$= 12mA) | | 0.4 | V |
| $V_{IL}$ | Input Low Voltage | | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | | V |
| $I_{IL}$/ $I_{IH}$ | Input Leakage Current, $V_{IN} = V_{CCI}$ or GND | | –20 | 20 | µA |
| $I_{OZ}$ | Tristate Output Leakage Current, $V_{OUT} = V_{CCI}$ or GND | | –20 | 20 | µA |
| $t_R$, $t_F$ | Input Transition Time | | | 10 | ns |
| $C_{IN}$ | Input Pin Capacitance[3] | | | 20 | pF |
| $C_{CLK}$ | CLK Pin Capacitance[3] | | | 20 | pF |
| $V_{MEAS}$ | Trip point for Input buffers and Measuring point for Output buffers | | 1.5 | | V |
| IV Curve[2] | Can be derived from the IBIS model on the web. | | | | |

***Notes:***

1. *The IBIS model can be found at www.actel.com/techdocs/models/ibis.html.*
2. *If $t_R/t_F$ exceeds the limit of 10 ns, Actel can guarantee reliability but not functionality.*
3. *Absolute maximum pin capacitance, which includes package and I/O input capacitance.*

## Timing Characteristics

*Table 2-11* • **RT54SX32S 5V TTL and 3.3V LVTTL I/O Module**
**Worst-Case Military Conditions $V_{CCA}$ = 2.25V, $T_J$ = 125°C, Radiation Level = 0 krad (Si)**

| | | '–1' Speed | | 'Std.' Speed | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **5V TTL Output Module Timing ($V_{CCI}$ = 4.5V)** | | | | | | |
| $t_{INYH}$ | Input Data Pad-to-Y High | | 0.7 | | 0.9 | ns |
| $t_{INYL}$ | Input Data Pad-to-Y Low | | 1.1 | | 1.3 | ns |
| $t_{DLH}$ | Data-to-Pad Low to High | | 3.1 | | 3.6 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 3.8 | | 4.4 | ns |
| $t_{DHLS}$ | Data-to-Pad High to Low – low slew | | 9.8 | | 11.5 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to Low | | 2.5 | | 3.0 | ns |
| $t_{DENZLS}$ | Enable-to-Pad, Z to Low – low slew | | 9.0 | | 10.6 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to High | | 3.1 | | 3.6 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, Low to Z | | 4.4 | | 5.3 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, High to Z | | 3.8 | | 4.4 | ns |
| $d_{TLH}$ | Delta Delay vs. Load Low to High | | 0.036 | | 0.046 | ns/pF |
| $d_{THL}$ | Delta Delay vs. Load High to Low | | 0.029 | | 0.038 | ns/pF |
| $d_{THLS}$ | Delta Delay vs. Load High to Low – low slew | | 0.049 | | 0.064 | ns/pF |
| **3.3V LVTTL Output Module Timing ($V_{CCI}$ = 3.0V)** | | | | | | |
| $t_{INYH}$ | Input Data Pad-to-Y High | | 0.8 | | 0.9 | ns |
| $t_{INYL}$ | Input Data Pad-to-Y Low | | 1.1 | | 1.3 | ns |
| $t_{DLH}$ | Data-to-Pad Low to High | | 4.1 | | 4.8 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 3.7 | | 4.4 | ns |
| $t_{DHLS}$ | Data-to-Pad High to Low – low slew | | 13.2 | | 15.6 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 2.9 | | 3.4 | ns |
| $t_{DENZLS}$ | Enable-to-Pad, Z to Low – low slew | | 12.7 | | 14.9 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 4.1 | | 4.8 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 3.7 | | 4.4 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 3.7 | | 4.4 | ns |
| $d_{TLH}$ | Delta Delay vs. Load Low to High | | 0.064 | | 0.081 | ns/pF |
| $d_{THL}$ | Delta Delay vs. Load High to Low | | 0.031 | | 0.040 | ns/pF |
| $d_{THLS}$ | Delta Delay vs. Load High to Low – low slew | | 0.069 | | 0.088 | ns/pF |

***Note:*** *Output delays based on 35 pF loading.*

*Table 2-12* • **RT54SX72S 5V TTL and 3.3V LVTTL I/O Module**
**Worst-Case Military Conditions $V_{CCA}$ = 2.25V, $T_J$ = 125°C, Radiation Level = 0 krad (Si)**

| | | '–1' Speed | | 'Std.' Speed | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **5V TTL Output Module Timing ($V_{CCI}$ = 4.5V)** | | | | | | |
| $t_{INYH}$ | Input Data Pad-to-Y High | | 0.7 | | 0.9 | ns |
| $t_{INYL}$ | Input Data Pad-to-Y Low | | 1.1 | | 1.3 | ns |
| $t_{DLH}$ | Data-to-Pad Low to High | | 3.2 | | 3.7 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 4.0 | | 4.7 | ns |
| $t_{DHLS}$ | Data-to-Pad High to Low – low slew | | 10.3 | | 12.1 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to Low | | 2.5 | | 3.0 | ns |
| $t_{DENZLS}$ | Enable-to-Pad, Z to Low – low slew | | 9.0 | | 10.6 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to High | | 3.2 | | 3.7 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, Low to Z | | 4.4 | | 5.3 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, High to Z | | 4.0 | | 4.7 | ns |
| $d_{TLH}$ | Delta Delay vs. Load Low to High | | 0.036 | | 0.046 | ns/pF |
| $d_{THL}$ | Delta Delay vs. Load High to Low | | 0.029 | | 0.038 | ns/pF |
| $d_{THLS}$ | Delta Delay vs. Load High to Low – low slew | | 0.049 | | 0.064 | ns/pF |
| **3.3V LVTTL Output Module Timing ($V_{CCI}$ = 3.0V)** | | | | | | |
| $t_{INYH}$ | Input Data Pad-to-Y High | | 1.0 | | 1.2 | ns |
| $t_{INYL}$ | Input Data Pad-to-Y Low | | 2.2 | | 2.5 | ns |
| $t_{DLH}$ | Data-to-Pad Low to High | | 4.0 | | 4.6 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 3.6 | | 4.2 | ns |
| $t_{DHLS}$ | Data-to-Pad High to Low – low slew | | 12.7 | | 14.9 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to L | | 2.9 | | 3.4 | ns |
| $t_{DENZLS}$ | Enable-to-Pad, Z to Low – low slew | | 12.7 | | 14.9 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to H | | 4.0 | | 4.6 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, L to Z | | 3.9 | | 4.4 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, H to Z | | 3.6 | | 4.2 | ns |
| $d_{TLH}$ | Delta Delay vs. Load Low to High | | 0.064 | | 0.081 | ns/pF |
| $d_{THL}$ | Delta Delay vs. Load High to Low | | 0.031 | | 0.04 | ns/pF |
| $d_{THLS}$ | Delta Delay vs. Load High to Low – low slew | | 0.069 | | 0.088 | ns/pF |

***Note:*** *Output delays based on 35 pF loading.*

## 5V CMOS

*Table 2-13* • **5V CMOS Electrical Specifications**

| Symbol | Parameter | | Military Min. | Military Max. | Units |
|---|---|---|---|---|---|
| $V_{OH}$ | $V_{CCI}$ = MIN,<br>$V_I = V_{CCI}$ or GND | ($I_{OH}$ = –20μA) | $V_{CCI}$ - 0.1 | | V |
| $V_{OL}$ | $V_{CCI}$ = MIN,<br>$V_I = V_{CCI}$ or GND | ($I_{OL}$= ±20μA) | | 0.1 | V |
| $V_{IL}$ | Input Low Voltage, $V_{OUT} = V_{VOL(max)}$ | | | $0.3V_{CC}$ | V |
| $V_{IH}$ | Input High Voltage, $V_{OUT} = V_{VOH(min)}$ | | $0.7V_{CC}$ | | V |
| $I_{OZ}$ | Tristate Output Leakage Current, $V_{OUT} = V_{CCI}$ or GND | | –20 | 20 | μA |
| $t_R$, $t_F$ | Input Transition Time | | | 10 | ns |
| $C_{IN}$ | Input Pin Capacitance[1] | | | 20 | pF |
| $C_{CLK}$ | CLK Pin Capacitance[1] | | | 20 | pF |
| $V_{MEAS}$ | Trip point for Input buffers and Measuring point for Output buffers | | 2.5 | | V |
| IV Curve | Can be derived from the IBIS model on the web.[2] | | | | |

***Notes:***

1. *Absolute maximum pin capacitance, which includes package and I/O input capacitance.*
2. *The IBIS model can be found at www.actel.com/techdocs/models/ibis.html.*

### Timing Characteristics

*Table 2-14* • **RT54SX32S 5V CMOS I/O Module**
**Worst-Case Military Conditions $V_{CCA}$ = 2.25V, $V_{CCI}$ = 4.5V, $T_J$ = 125°C, Radiation Level = 0 krad (Si)**

| Parameter | Description | '–1' Speed Min. | '–1' Speed Max. | 'Std.' Speed Min. | 'Std.' Speed Max. | Units |
|---|---|---|---|---|---|---|
| **5V CMOS Output Module Timing** | | | | | | |
| $t_{INYH}$ | Input Data Pad-to-Y High | | 0.7 | | 0.9 | ns |
| $t_{INYL}$ | Input Data Pad-to-Y Low | | 1.1 | | 1.3 | ns |
| $t_{DLH}$ | Data-to-Pad Low to High | | 3.4 | | 4.0 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 3.6 | | 4.2 | ns |
| $t_{DHLS}$ | Data-to-Pad High to Low – low slew | | 8.7 | | 10.3 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to Low | | 2.3 | | 2.8 | ns |
| $t_{DENZLS}$ | Enable-to-Pad, Z to Low – low slew | | 8.8 | | 10.4 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to High | | 3.6 | | 4.2 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, Low to Z | | 4.5 | | 5.3 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, High to Z | | 3.4 | | 4.0 | ns |
| $d_{TLH}$ | Delta Delay vs. Load Low to High | | 0.036 | | 0.046 | ns/pF |
| $d_{THL}$ | Delta Delay vs. Load High to Low | | 0.029 | | 0.038 | ns/pF |
| $d_{THLS}$ | Delta Delay vs. Load High to Low – low slew | | 0.049 | | 0.064 | ns/pF |

***Note:*** *Output delays based on 35 pF loading.*

*Table 2-15* • **RT54SX72S 5V CMOS I/O Module**
**Worst-Case Military Conditions $V_{CCA}$ = 2.25V, $V_{CCI}$ = 4.5V, $T_J$ = 125°C, Radiation Level = 0 krad (Si)**

| | | '–1' Speed | | 'Std.' Speed | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **5V CMOS Output Module Timing** | | | | | | |
| $t_{INYH}$ | Input Data Pad-to-Y High | | 0.7 | | 0.9 | ns |
| $t_{INYL}$ | Input Data Pad-to-Y Low | | 0.0 | | 0.0 | ns |
| $t_{DLH}$ | Data-to-Pad Low to High | | 3.6 | | 4.2 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 3.8 | | 4.5 | ns |
| $t_{DHLS}$ | Data-to-Pad High to Low – low slew | | 9.2 | | 10.8 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to Low | | 2.3 | | 2.8 | ns |
| $t_{DENZLS}$ | Enable-to-Pad, Z to Low – low slew | | 8.8 | | 10.4 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to High | | 3.8 | | 4.5 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, Low to Z | | 4.5 | | 5.3 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, High to Z | | 3.6 | | 4.2 | ns |
| $d_{TLH}$ | Delta Delay vs. Load Low to High | | 0.036 | | 0.046 | ns/pF |
| $d_{THL}$ | Delta Delay vs. Load High to Low | | 0.029 | | 0.038 | ns/pF |
| $d_{THLS}$ | Delta Delay vs. Load High to Low – low slew | | 0.049 | | 0.064 | ns/pF |

***Note:*** *Output delays based on 35 pF loading.*

## 5V PCI

The RTSX-S family supports 5V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

*Table 2-16* • **5V PCI DC Specifications**

| Symbol | Parameter | Condition | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_{CCA}$ | Supply Voltage for Array | | 2.25 | 2.75 | V |
| $V_{CCI}$ | Supply Voltage for I/Os | | 4.5 | 5.5 | V |
| $V_{IH}$ | Input High Voltage[1] | | 2.0 | $V_{CCI}$ + 0.5 | V |
| $V_{IL}$ | Input Low Voltage[1] | | –0.5 | 0.8 | V |
| $I_{IH}$ | Input High Leakage Current | $V_{IN}$ = 2.75 | | 70 | µA |
| $I_{IL}$ | Input Low Leakage Current | $V_{IN}$ = 0.5 | | –70 | µA |
| $V_{OH}$ | Output High Voltage | $I_{OUT}$ = –2 mA | 2.4 | | V |
| $V_{OL}$ | Output Low Voltage[2] | $I_{OUT}$ = 3 mA, 6 mA | | 0.55 | V |
| $C_{IN}$ | Input Pin Capacitance[3] | | | 10 | pF |
| $C_{CLK}$ | CLK Pin Capacitance | | 5 | 12 | pF |
| $V_{MEAS}$ | Trip Point for Input Buffers and Measuring Point for Output Buffers | | 1.5 | | V |

***Notes:***

1. *Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.*
2. *Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull-up must have 6 mA; the latter include, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.*
3. *Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK) with an exception granted to motherboard-only devices, which could be up to 16 pF in order to accommodate PGA packaging. This mean that components for expansion boards need to use alternatives to ceramic PGA packaging (i.e., PBGA,PQFP, SGA, etc.).*

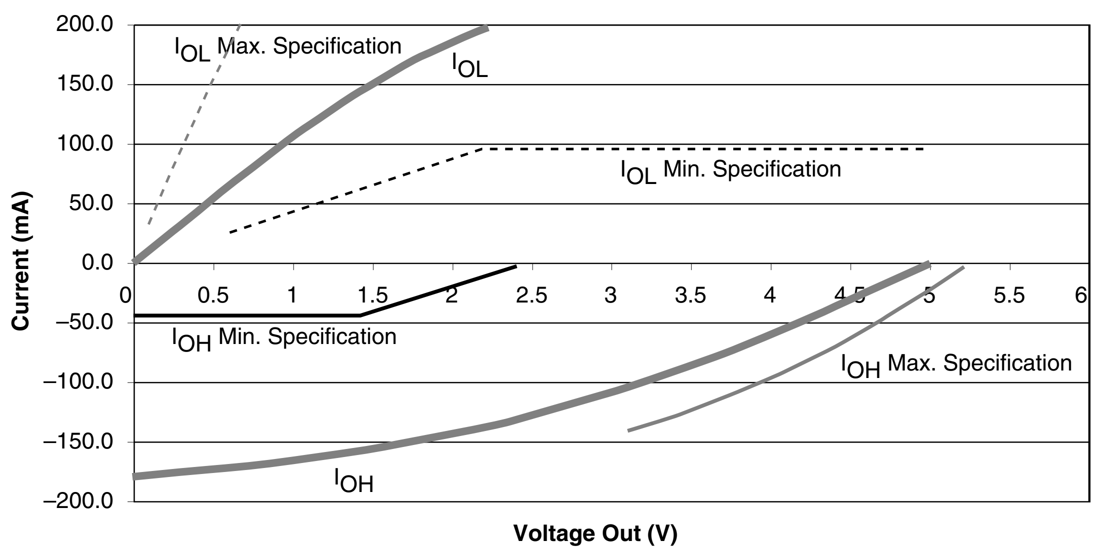


*Figure 2-7* • **5V PCI V/I Curve for RTSX-S**

### Equation A

$I_{OH} = 11.9 * (V_{OUT} - 5.25) * (V_{OUT} + 2.45)$

for $V_{CCI} > V_{OUT} > 3.1V$

### Equation B

$I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT})$

for $0V < V_{OUT} < 0.71V$

*Table 2-17* • **5V PCI AC Specifications**

| Symbol | Parameter | Condition | Min. | Max. | Units |
|---|---|---|---|---|---|
| $I_{OH(AC)}$ | Switching Current High | $0 < V_{OUT} < 1.4$ [1] | –44 | | mA |
| | | $1.4 < V_{OUT} < 2.4$ [1, 2] | $(–44 + (V_{OUT} – 1.4)/0.024)$ | | mA |
| | | $3.1 < V_{OUT} < V_{CCI}$ [1, 3] | | "Equation A" on page 2-16 | |
| | (Test Point) | $V_{OUT} = 3.1$ [3] | | –142 | mA |
| $I_{OL(AC)}$ | Switching Current Low | $V_{OUT} = 2.2$ [1] | 95 | | mA |
| | | $2.2 > V_{OUT} > 0.55$ [1] | $(V_{OUT}/0.023)$ | | mA |
| | | $0.71 > V_{OUT} > 0$ [1, 3] | | "Equation B" on page 2-16 | |
| | (Test Point) | $V_{OUT} = 0.71$ | | 206 | mA |
| $I_{CL}$ | Low Clamp Current | $–5 < V_{IN} \leq –1$ | $–25 + (V_{IN} + 1)/0.015$ | | mA |
| $slew_R$ | Output Rise Slew Rate | 0.4V to 2.4V load[4] | 1 | 5 | V/ns |
| $slew_F$ | Output Fall Slew Rate | 2.4V to 0.4V load[4] | 1 | 5 | V/ns |

***Notes:***

1. *Refer to the V/I curves in Figure 2-7 on page 2-16. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. The "Switching Current High" specification is not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.*
2. *Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.*
3. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (A and B) are provided with the respective curves in Figure 2-7 on page 2-16. The equation defined maximum should be met by the design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
4. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification (Figure 2-8). However, adherence to both the maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.*

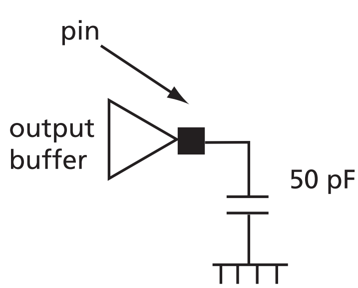


*Figure 2-8* • **5V PCI Output Loading**

## Timing Characteristics

*Table 2-18* • **RT54SX32S 5V PCI I/O Module**
**Worst-Case Military Conditions $V_{CCA}$ = 2.25V, $V_{CCI}$ = 4.5V, $T_J$= 125°C, Radiation Level = 0 krad (Si)**

| | | '–1' Speed | | 'Std.' Speed | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **5V PCI Output Module Timing** | | | | | | |
| $t_{INYH}$ | Input Data Pad-to-Y High | | 0.7 | | 0.9 | ns |
| $t_{INYL}$ | Input Data Pad-to-Y Low | | 1.1 | | 1.3 | ns |
| $t_{DLH}$ | Data-to-Pad Low to High | | 3.4 | | 4.0 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 4.1 | | 4.8 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to Low | | 2.8 | | 3.3 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to High | | 3.4 | | 4.0 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, Low to Z | | 4.9 | | 5.8 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, High to Z | | 4.1 | | 4.8 | ns |
| $d_{TLH}$ | Delta Delay vs. Load Low to High | | 0.036 | | 0.046 | ns/pF |
| $d_{THL}$ | Delta Delay vs. Load High to Low | | 0.029 | | 0.038 | ns/pF |

***Note:*** *Output delays based on 50 pF loading.*

*Table 2-19* • **RT54SX72S 5V PCI I/O Module**
**Worst-Case Military Conditions $V_{CCA}$ = 2.25V, $V_{CCI}$ = 4.5V, $T_J$= 125°C, Radiation Level = 0 krad (Si)**

| | | '–1' Speed | | 'Std.' Speed | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **5V PCI Output Module Timing** | | | | | | |
| $t_{INYH}$ | Input Data Pad-to-Y High | | 0.7 | | 0.9 | ns |
| $t_{INYL}$ | Input Data Pad-to-Y Low | | 1.1 | | 1.3 | ns |
| $t_{DLH}$ | Data-to-Pad Low to High | | 3.5 | | 4.1 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 4.3 | | 5.1 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to Low | | 2.8 | | 3.3 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to High | | 3.5 | | 4.1 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, Low to Z | | 4.9 | | 5.8 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, High to Z | | 4.3 | | 5.1 | ns |
| $d_{TLH}$ | Delta Delay vs. Load Low to High | | 0.036 | | 0.046 | ns/pF |
| $d_{THL}$ | Delta Delay vs. Load High to Low | | 0.029 | | 0.038 | ns/pF |

***Note:*** *Output delays based on 50 pF loading.*

## 3.3V PCI

The RTSX-S family supports 3.3V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

*Table 2-20* • **3.3 V PCI DC Specifications**

| Symbol | Parameter | Condition | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_{CCA}$ | Supply Voltage for Array | | 2.25 | 2.75 | V |
| $V_{CCI}$ | Supply Voltage for I/Os | | 3.0 | 3.6 | V |
| $V_{IH}$ | Input High Voltage | | $0.5V_{CCI}$ | $V_{CCI} + 0.5$ | V |
| $V_{IL}$ | Input Low Voltage | | –0.5 | $0.3V_{CCI}$ | V |
| $I_{IPU}$ | Input Pull-up Voltage[1] | | $0.7V_{CCI}$ | | V |
| $I_{IL}/I_{IH}$ | Input Leakage Current[2] | $0 < V_{IN} < V_{CCI}$ | | ±20 | µA |
| $V_{OH}$ | Output High Voltage | $I_{OUT}$ = –500 µA | $0.9V_{CCI}$ | | V |
| $V_{OL}$ | Output Low Voltage | $I_{OUT}$ = 1500 µA | | $0.1V_{CCI}$ | V |
| $C_{IN}$ | Input Pin Capacitance[3] | | | 10 | pF |
| $C_{CLK}$ | CLK Pin Capacitance | | 5 | 12 | pF |
| $V_{MEAS}$ | Trip point for Input buffers | | $0.4 * V_{CCI}$ | | V |
| | Output buffer measuring point - rising edge | | $0.285 * V_{CCI}$ | | |
| | Output buffer measuring point - falling edge | | $0.615 * V_{CCI}$ | | |

***Notes:***

1. *This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization should assure that the input buffer is conducting minimum current at this input $V_{IN}$.*
2. *Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.*
3. *Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK) with an exception granted to motherboard-only devices, which could be up to 16 pF, in order to accommodate PGA packaging. This means that components for expansion boards would need to use alternatives to ceramic PGA packaging.*

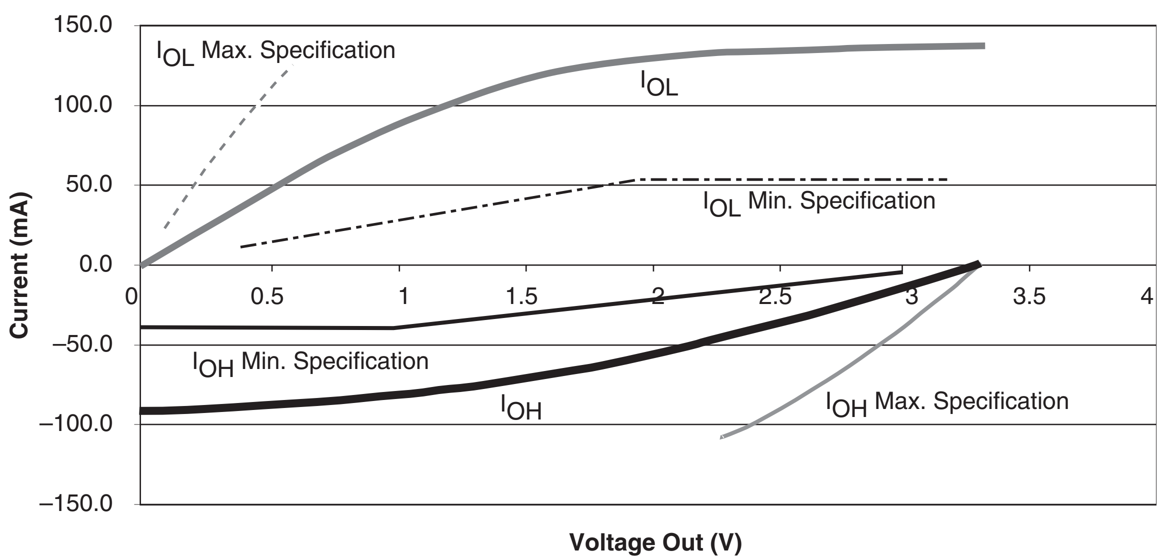


*Figure 2-9* • **3.3V PCI V/I Curve for the RTSX-S Family**

### Equation C

$I_{OH} = (98.0/V_{CCI}) * (V_{OUT} - V_{CCI}) * (V_{OUT} + 0.4V_{CCI})$

for $V_{CCI} > V_{OUT} > 0.7\ V_{CCI}$

### Equation D

$I_{OL} = (256/V_{CCI}) * V_{OUT} * (V_{CCI} - V_{OUT})$

for $0V < V_{OUT} < 0.18\ V_{CCI}$

*Table 2-21* • **3.3V PCI AC Specifications**

| Symbol | Parameter | Condition | Min. | Max. | Units |
|---|---|---|---|---|---|
| $I_{OH(AC)}$ | Switching Current High | $0 < V_{OUT} \le 0.3V_{CCI}$ [1] | $-12V_{CCI}$ | | mA |
| | | $0.3V_{CCI} \le V_{OUT} < 0.9V_{CCI}$ [1] | $(-17.1 + (V_{CCI} - V_{OUT}))$ | | mA |
| | | $0.7V_{CCI} < V_{OUT} < V_{CCI}$ [1, 2] | | "Equation C" on page 2-19 | |
| | (Test Point) | $V_{OUT} = 0.7V_{CC}$ [2] | | $-32V_{CCI}$ | mA |
| $I_{OL(AC)}$ | Switching Current Low | $V_{CCI} > V_{OUT} \ge 0.6V_{CCI}$ [1] | $16V_{CCI}$ | | mA |
| | | $0.6V_{CCI} > V_{OUT} > 0.1V_{CCI}$ [1] | $(26.7V_{OUT})$ | | mA |
| | | $0.18V_{CCI} > V_{OUT} > 0$ [1, 2] | | "Equation D" on page 2-19 | |
| | (Test Point) | $V_{OUT} = 0.18V_{CC}$ [2] | | $38V_{CCI}$ | mA |
| $I_{CL}$ | Low Clamp Current | $-3 < V_{IN} \le -1$ | $-25 + (V_{IN} + 1)/0.015$ | | mA |
| $I_{CH}$ | High Clamp Current | $V_{CCI} + 4 > V_{IN} \ge V_{CCI} + 1$ | $25 + (V_{IN} - V_{CCI} - 1)/0.015$ | | mA |
| $slew_R$ | Output Rise Slew Rate | $0.2V_{CCI}$ to $0.6V_{CCI}$ load [3] | 1 | 4 | V/ns |
| $slew_F$ | Output Fall Slew Rate | $0.6V_{CCI}$ to $0.2V_{CCI}$ load [3] | 1 | 4 | V/ns |

***Notes:***

1. *Refer to the V/I curves in Figure 2-9 on page 2-19. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half-size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. The "Switching Current High" specification is not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.*
2. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (C and D) are provided with the respective curves in Figure 2-9 on page 2-19. The equation defined maximum should be met by the design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
3. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load is optional (Figure 2-10); i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs.*

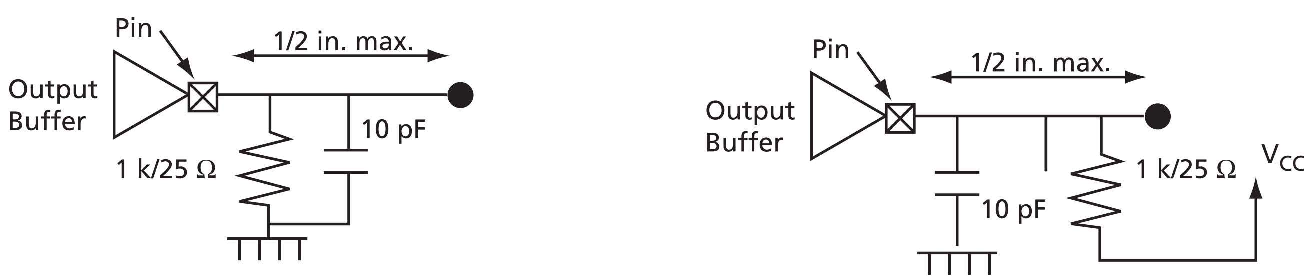


*Figure 2-10* • **3.3V PCI Output Loading**

## Timing Characteristics

*Table 2-22* • **RT54SX32S 3.3V PCI I/O Module**
**Worst-Case Military Conditions $V_{CCA}$ = 2.25V, $V_{CCI}$ = 3.0V, $T_J$ = 125°C, Radiation Level = 0 krad (Si)**

| | | '–1' Speed | | 'Std.' Speed | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **3.3V PCI Output Module Timing** | | | | | | |
| $t_{INYH}$ | Input Data Pad-to-Y High | | 0.8 | | 0.9 | ns |
| $t_{INYL}$ | Input Data Pad-to-Y Low | | 0.9 | | 1.1 | ns |
| $t_{DLH}$ | Data-to-Pad Low to High | | 3.0 | | 3.5 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 3.0 | | 3.5 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to Low | | 2.1 | | 2.5 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to High | | 3.0 | | 3.5 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, Low to Z | | 2.7 | | 3.9 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, High to Z | | 3.0 | | 3.5 | ns |
| $d_{TLH}$ | Delta Delay vs. Load Low to High | | 0.067 | | 0.085 | ns/pF |
| $d_{THL}$ | Delta Delay vs. Load High to Low | | 0.031 | | 0.040 | ns/pF |

**Note:** *Delays based on 10 pF loading and 25 Ω resistance.*

*Table 2-23* • **RT54SX72S 3.3V PCI I/O Module**
**Worst-Case Military Conditions $V_{CCA}$ = 2.25V, $V_{CCI}$ = 3.0V, $T_J$ = 125°C, Radiation Level = 0 krad (Si)**

| | | '–1' Speed | | 'Std.' Speed | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **3.3V PCI Output Module Timing** | | | | | | |
| $t_{INYH}$ | Input Data Pad-to-Y High | | 0.7 | | 0.8 | ns |
| $t_{INYL}$ | Input Data Pad-to-Y Low | | 0.9 | | 1.1 | ns |
| $t_{DLH}$ | Data-to-Pad Low to High | | 2.8 | | 3.3 | ns |
| $t_{DHL}$ | Data-to-Pad High to Low | | 2.8 | | 3.3 | ns |
| $t_{ENZL}$ | Enable-to-Pad, Z to Low | | 2.1 | | 2.5 | ns |
| $t_{ENZH}$ | Enable-to-Pad, Z to High | | 2.8 | | 3.3 | ns |
| $t_{ENLZ}$ | Enable-to-Pad, Low to Z | | 2.7 | | 3.9 | ns |
| $t_{ENHZ}$ | Enable-to-Pad, High to Z | | 2.8 | | 3.3 | ns |
| $d_{TLH}$ | Delta Delay vs. Load Low to High | | 0.067 | | 0.085 | ns/pF |
| $d_{THL}$ | Delta Delay vs. Load High to Low | | 0.031 | | 0.040 | ns/pF |

**Note:** *Delays based on 10 pF loading and 25 Ω resistance.*

# Module Specifications

## C-Cell

### Introduction

The C-cell is one of the two logic module types in the RTSX-S architecture. It is the combinatorial logic resource in the device. The RTSX-S architecture uses the same C-cell configuration as found in the SX and SX-A families.

The C-cell features the following (Figure 2-11):

- Eight-input MUX (data: D0-D3, select: A0, A1, B0, B1). User signals can be routed to any one of these inputs. C-cell inputs (A0, A1, B0, B1) can be tied to one of the either the routed or quad clocks (CLKA/B or QCLKA/B/C/D).
- Inverter (DB input) can be used to drive a complement signal of any of the inputs to the C-cell.
- A hardwired connection (direct connect) to the associated R-cell with a signal propagation time of less than 0.1 ns.

This layout of the C-cell enables the implementation of over 4,000 functions of up to five bits. For example, two C-cells can be used together to implement a four-input XOR function in a single cell delay.

The C-cell configuration is handled automatically for the user with Actel's extensive macro library (please see Actel's *Antifuse Macro Library Guide* for a complete listing of available RTSX-S macros).

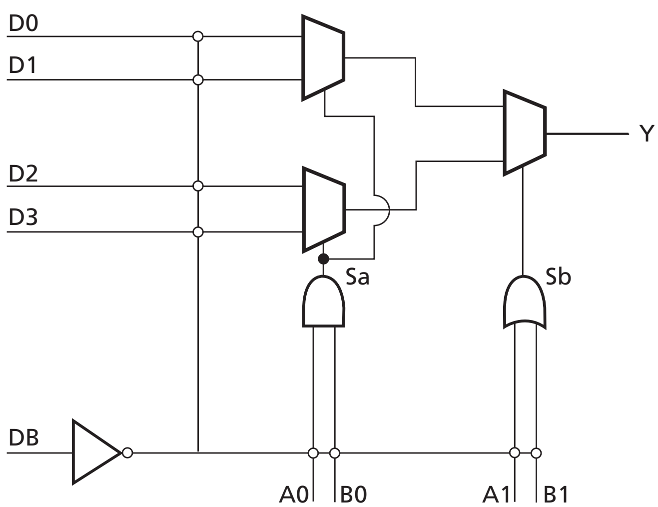


*Figure 2-11* • **C-Cell**

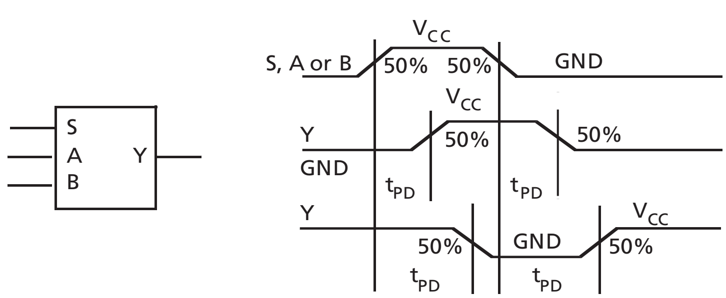


*Figure 2-12* • **C-Cell Timing Model and Waveforms**

## Timing Characteristics

*Table 2-24* • **C-Cell**
**Worst-Case Military Conditions $V_{CCA}$ = 2.25V, $V_{CCI}$ = 3.0V, $T_J$= 125°C, Radiation Level = 0 krad (Si)**

| | | '–1' Speed | | 'Std.' Speed | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **C-Cell Propagation Delays** | | | | | | |
| $t_{PD}$ | Internal Array Module | | 1.2 | | 1.4 | ns |

***Note:*** *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*

## R-Cell

### Introduction

The R-cell, the sequential logic resource of RTSX-S devices, is the second logic module type in the RTSX-S family architecture. The RTAX-S R-cell is an SEU-enhanced version of the SX and SX-A R-cell (Figure 2-13).

The main features of the R-cell include the following:

- Direct connection to the adjacent C-cell through the hardwired connection DCIN. DCIN is driven by the DCOUT of an adjacent C-cell via the Direct-Connect routing resource, providing a connection with less than 0.1 ns of routing delay.
- The R-cell can be used as a standalone flip-flop. It can be driven by any other C-cell or I/O modules through the regular routing structure (using DIN as a routable data input). This gives the option of using it as a 2:1 MUXed flip-flop as well.
- Independent active-low asynchronous clear (CLRB).
- Independent active-low asynchronous preset (PSETB). If both CLRB and PSETB are Low, CLRB has higher priority.
- Clock can be driven by any of the following (CKP input selects clock polarity):
  - The high-performance, hardwired, fast clock (HCLK)
  - One of the two routed clocks (CLKA/B)
  - One of the four quad clocks (QCLKA/B/C/D) in the case of the RT54SX72S
  - User signals
- S0, S1, PSETB, and CLRB can be driven by CLKA/B, QCLKA/B/C/D (for the RT54SX72S) or user signals.
- Routed Data Input and S1 can be driven by user signals.

As with the C-cell, the configuration of the R-cell to perform various functions is handled automatically for the user through Actel's extensive macro library (please see Actel's *Macro Library Guide* for a complete listing of available RTAX-S macros).

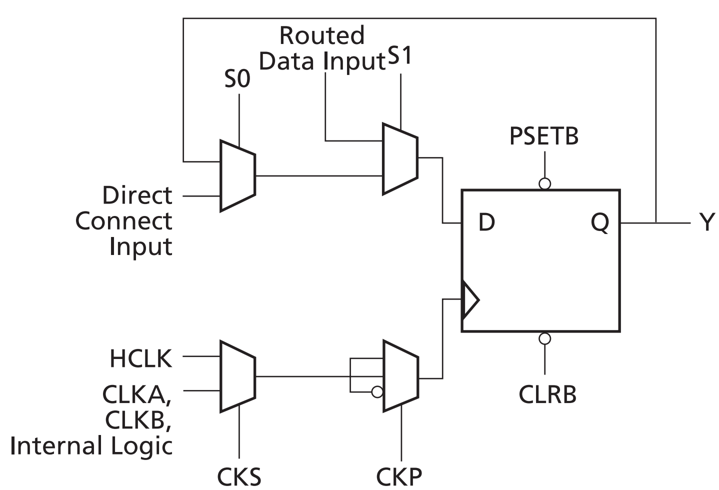


*Figure 2-13* • **R-Cell**

## SEU-Hardened D Flip-Flop

In order to meet the stringent SEU requirements of a LET threshold greater than 40MeV-$cm^2$/gm, the internal design of the R-cell was modified without changing the functionality of the cell.

Figure 2-14 is a simplified representation of how the D flip-flop in the R-cell is implemented in the SX-A architecture. The flip-flop consists of a master and a slave latch gated by opposite edges of the clock. Each latch is constructed by feeding back the output to the input stage. The potential problem in a space environment is that either of the latches can change state when hit by a particle with enough energy.

To achieve the SEU requirements, the D flip-flop in the RTSX-S R-cell is enhanced (Figure 2-15). Both the master and slave "latches" are each implemented with three latches. The asynchronous self-correcting feedback paths of each of the three latches is voted with the outputs of the other two latches. If one of the three latches is struck by an ion and starts to change state, the voting with the other two latches prevents the change from feeding back and permanently latching. Care was taken in the layout to ensure that a single ion strike could not affect more than one latch. Figure 2-16 shows a simplified schematic of the test circuitry that has been added to test the functionality of all the components of the flip-flop. The inputs to each of the three latches are independently controllable so the voting circuitry in the asynchronous self-correcting feedback paths can be tested exhaustively. This testing is performed on an unprogrammed array during wafer sort, final test, and post-burn-in test. This test circuitry cannot be used to test the flip-flops once the device has been programmed.

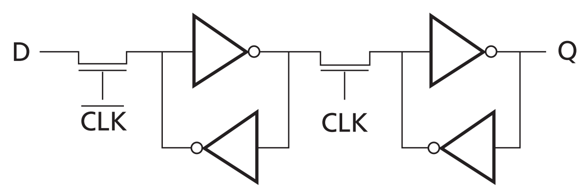


*Figure 2-14* • **SX-A R-Cell Implementation of a D Flip-Flop**

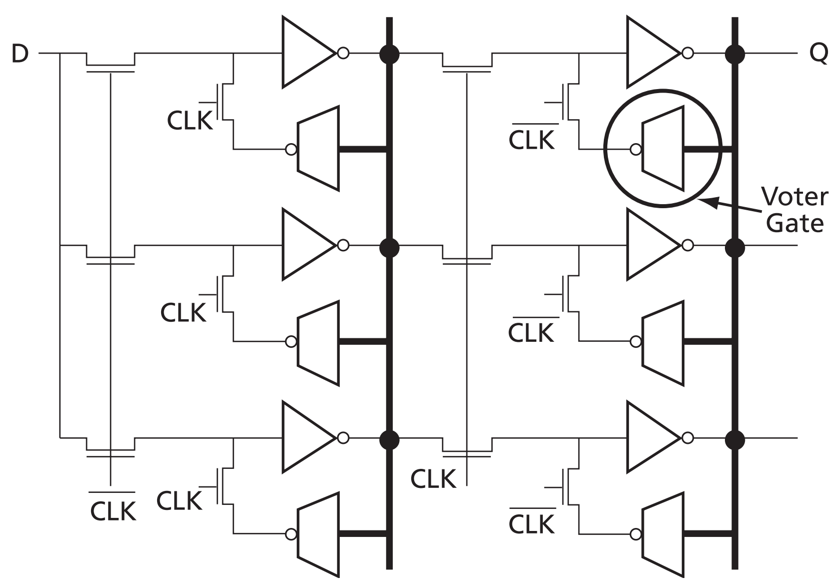


*Figure 2-15* • **RTSX-S R-Cell Implementation of D Flip-Flop Using Voter Gate Logic**

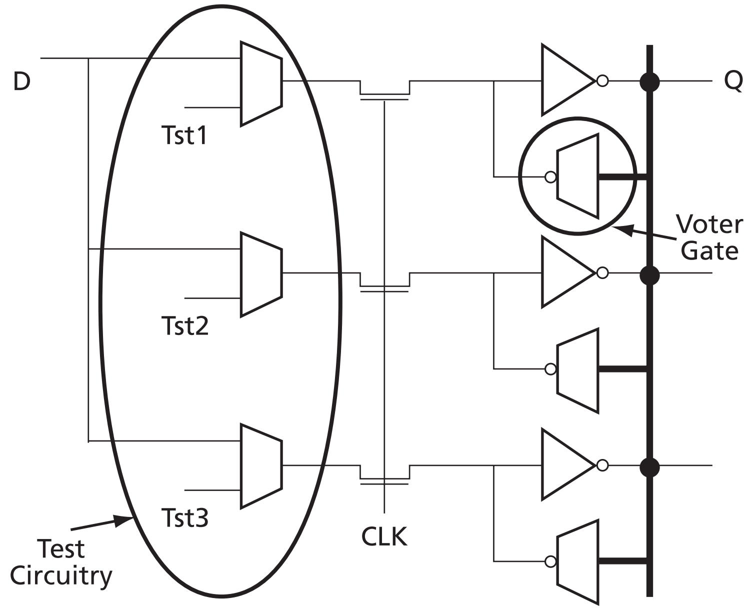


*Figure 2-16* • **R-Cell Implementation – Test Circuitry**

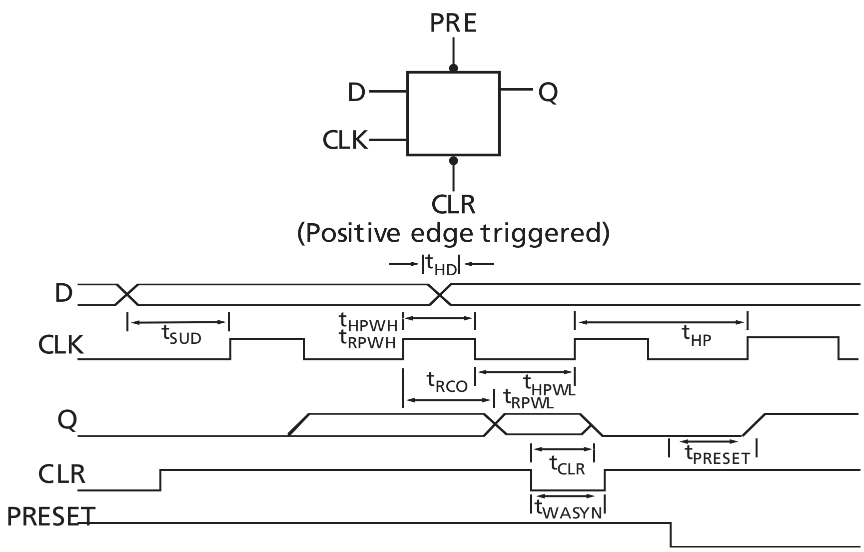


*Figure 2-17* • **R-Cell Tiing Models and Waveforms**

## Timing Characteristics

*Table 2-25* • **R-Cell**
**Worst-Case Military Conditions $V_{CCA}$ = 2.25V, $V_{CCI}$ = 3.0V, $T_J$ = 125°C, Radiation Level = 0 krad (Si)**

| | | '–1' Speed | | 'Std.' Speed | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **R-Cell Propagation Delays** | | | | | | |
| $t_{RCO}$ | Sequential Clock-to-Q | | 1.0 | | 1.2 | ns |
| $t_{CLR}$ | Asynchronous Clear-to-Q | | 0.8 | | 1.0 | ns |
| $t_{PRESET}$ | Asynchronous Preset-to-Q | | 1.1 | | 1.3 | ns |
| $t_{SUD}$ | Flip-Flop Data Input Set-Up | | 0.8 | | 1.0 | ns |
| $t_{HD}$ | Flip-Flop Data Input Hold | | 0.0 | | 0.0 | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | | 2.8 | | 3.3 | ns |
| $t_{RECASYN}$ | Asynchronous Recovery Time | | 0.7 | | 0.8 | ns |
| $t_{HASYN}$ | Asynchronous Hold Time | | 0.7 | | 0.8 | ns |

# Routing Specifications

## Routing Resources

The routing structure found in RTSX-S devices enables any logic module to be connected to any other logic module in the device while retaining high performance. There are multiple paths and routing resources that can be used to route one logic module to another, both within a SuperCluster and elsewhere on the chip.

There are three primary types of routing within the RTSX-S architecture: DirectConnect, FastConnect, and Vertical and Horizontal Routing.

### DirectConnect

DirectConnects provide a high-speed connection between an R-cell and its adjacent C-cell (Figure 1-3 and Figure 1-4 on page 1-4). This connection can be made from the Y output of the C-cell to the DirectConnect input of the R-cell by configuring of the S0 line of the R-cell. This provides a connection that does not require an antifuse and has a delay of less than 0.1 ns.

### FastConnect

For high-speed routing of logic signals, FastConnects can be used to build a short distance connection using a single antifuse (Figure 1-3 and Figure 1-4 on page 1-4). FastConnects provide a maximum delay of 0.4 ns. The outputs of each logic module connect directly to the output tracks within a SuperCluster. Signals on the output tracks can then be routed through a single antifuse connection to drive the inputs of logic modules either within one SuperCluster or in the SuperCluster immediately below.

### Horizontal and Vertical Routing

In addition to DirectConnect and FastConnect, the architecture makes use of two globally-oriented routing resources known as segmented routing and high-drive routing. Actel's segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100-percent-automatic place-and-route software to minimize signal propagation delays.

### Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for the initial design performance evaluation. Critical net delays can then be applied to the most time-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to six percent of the nets in a design may be designated as critical, while 90 percent of the nets in a design are typical.

### Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes five antifuse connections. This increases capacitance and resistance results in longer net delays for macros connected to long tracks. Typically up to six percent of nets in a fully utilized device require long tracks. Long tracks can cause a delay from 4.0 ns to 8.4 ns. This additional delay is represented statistically in higher fanout routing delays in the "Timing Characteristics" on page 2-28.

## Timing Characteristics

*Table 2-26* • **RT54SX32S**
**Worst-Case Military Conditions $V_{CCA}$ = 2.25V, $V_{CCI}$ = 3.0V, $T_J$ = 125°C, Radiation Level = 0 krad (Si)**

| | | '–1' Speed | | 'Std.' Speed | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **Predicted Routing Delays** | | | | | | |
| $t_{DC}$ | FO=1 Routing Delay, DirectConnect | | 0.1 | | 0.1 | ns |
| $t_{FC}$ | FO=1 Routing Delay, FastConnect | | 0.4 | | 0.4 | ns |
| $t_{RD1}$ | FO=1 Routing Delay | | 0.8 | | 0.9 | ns |
| $t_{RD2}$ | FO=2 Routing Delay | | 1.0 | | 1.2 | ns |
| $t_{RD3}$ | FO=3 Routing Delay | | 1.4 | | 1.6 | ns |
| $t_{RD4}$ | FO=4 Routing Delay | | 1.5 | | 1.8 | ns |
| $t_{RD8}$ | FO=8 Routing Delay | | 2.9 | | 3.4 | ns |
| $t_{RD12}$ | FO=12 Routing Delay | | 4.0 | | 4.7 | ns |

***Note:*** *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.*

*Table 2-27* • **RT54SX72S**
**Worst-Case Military Conditions $V_{CCA}$ = 2.25V, $V_{CCI}$ = 3.0V, $T_J$ = 125°C, Radiation Level = 0 krad (Si)**

| | | '–1' Speed | | 'Std.' Speed | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **Predicted Routing Delays** | | | | | | |
| $t_{DC}$ | FO=1 Routing Delay, DirectConnect | | 0.1 | | 0.1 | ns |
| $t_{FC}$ | FO=1 Routing Delay, FastConnect | | 0.4 | | 0.4 | ns |
| $t_{RD1}$ | FO=1 Routing Delay | | 0.9 | | 1.0 | ns |
| $t_{RD2}$ | FO=2 Routing Delay | | 1.2 | | 1.4 | ns |
| $t_{RD3}$ | FO=3 Routing Delay | | 1.8 | | 2.0 | ns |
| $t_{RD4}$ | FO=4 Routing Delay | | 1.9 | | 2.3 | ns |
| $t_{RD8}$ | FO=8 Routing Delay | | 3.7 | | 4.3 | ns |
| $t_{RD12}$ | FO=12 Routing Delay | | 5.1 | | 6.0 | ns |

***Note:*** *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.*

## Global Resources

One of the most important aspects of any FPGA architecture is its global resource or clock structure. The RTSX-S family provides flexible and easy-to-use global resources without the limitations normally found in other FPGA architectures.

The RTSX-S architecture contains three types of global resources, the HCLK (hardwired clock) and CLK (routed clock) and in the RT54SX72S, QCLK (quadrant clock). Each RTSX-S device is provided with one HCLK and two CLKs. The RT54SX72S has an additional four QCLKs.

### Hardwired Clock

The hardwired (HCLK) is a low-skew network that can directly drive the clock inputs of all R-cells in the device with no antifuse in the path. The HCLK is available everywhere on the chip.

Upon power-up of the RTSX-S device, four clock pulses must be detected on HCLK before the clock signal will be propagated to registers in the device.

### Routed Clocks

The routed clocks (CLKA and CLKB) are low-skew networks that can drive the clock inputs of all R-cells in the device (logically equivalent to the HCLK). CLK has the added flexibility in that it can drive the S0 (Enable), S1, PSETB, and CLRB inputs of R-cells as well as any of the inputs of any C-cell in the device. This allows CLKs to be used not only as clocks but also for other global signals or high fanout nets. Both CLKs are available everywhere on the chip.

If CLKA or CLKB pins are not used or sourced from signals, then these pins must be set as Low or High on the board. They must not be left floating (except in RTSX72S, where these clocks can be configured as regular I/Os).

### Quadrant Clocks

The RT54SX72S device provides four quadrant clocks (QCLKA, QCLKB, QCLKC, QCLKD) to the user, which can be sourced from external pins or from internal logic signals within the device. Each of these clocks can individually drive up to one full quadrant of the chip, or they can be grouped together to drive multiple quadrants (Figure 2-18). If QCLKs are not used as quadrant clocks, they can behave as regular I/Os. See Actel's application note *Using A54SX72A and RT54SX72S Quadrant Clocks* for more information.

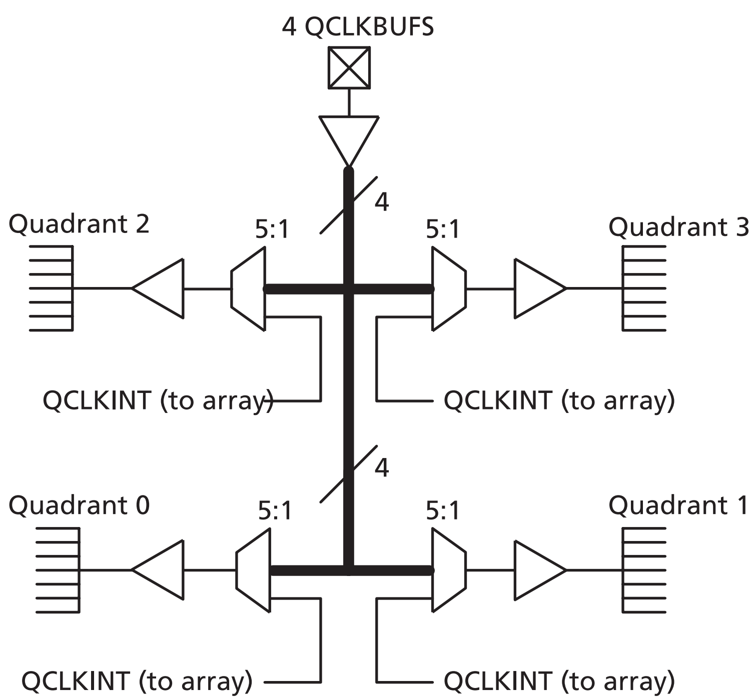


*Figure 2-18* • **RTSX-S QCLK Structure**

## Timing Characteristics

*Table 2-28* • **RT54SX32S at $V_{CCI}$ = 3.0V**
**Worst-Case Military Conditions $V_{CCA}$ = 2.25V, $V_{CCI}$ = 3.0V, $T_J$ = 125°C, Radiation Level = 0 krad (Si)**

| | | '–1' Speed | | 'Std.' Speed | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **Dedicated (Hardwired) Array Clock Network** | | | | | | |
| $t_{HCKH}$ | Pad to R-Cell Input Low to High | | 3.9 | | 4.6 | ns |
| $t_{HCKL}$ | Pad to R-Cell Input High to Low | | 3.9 | | 4.6 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 2.1 | | 2.5 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 2.1 | | 2.5 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 1.6 | | 1.9 | ns |
| $t_{HP}$ | Minimum Period | 4.2 | | 5.0 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 238 | | 200 | MHz |
| **Routed Array Clock Networks** | | | | | | |
| $t_{RCKH}$ | Pad to R-cell Input High to Low (Light Load)) | | 4.2 | | 4.9 | ns |
| $t_{RCHKL}$ | Pad to R-cell Input Low to High (Light Load)) | | 3.9 | | 4.6 | ns |
| $t_{RCKH}$ | Pad to R-cell Input Low to High (50% Load) | | 5.0 | | 5.9 | ns |
| $t_{RCKL}$ | Pad to R-cell Input High to Low (50% Load) | | 4.3 | | 5.1 | ns |
| $t_{RCKH}$ | Pad to R-cell Input Low to High (100% Load) | | 5.6 | | 6.5 | ns |
| $t_{RCKL}$ | Pad to R-cell Input High to Low (100% Load) | | 4.9 | | 5.7 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 2.1 | | 2.5 | | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 2.1 | | 2.5 | | ns |
| $t_{RCKSW}$ | Maximum Skew (Light Load) | | 2.8 | | 3.3 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% Load) | | 2.8 | | 3.3 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% Load) | | 2.8 | | 3.3 | ns |
| $t_{RP}$ | Minimum Period | 4.2 | | 5.0 | | ns |
| $f_{RMAX}$ | Maximum Frequency | | 238 | | 200 | MHz |

*Table 2-29* • **RT54SX32S at $V_{CCI}$ = 4.5V**
**Worst-Case Military Conditions $V_{CCA}$ = 2.25V, $V_{CCI}$ = 4.5V, $T_J$ = 125°C, Radiation Level = 0 krad (Si)**

| | | '–1' Speed | | 'Std.' Speed | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **Dedicated (Hardwired) Array Clock Network** | | | | | | |
| $t_{HCKH}$ | Pad to R-Cell Input Low to High | | 3.9 | | 4.6 | ns |
| $t_{HCKL}$ | Pad to R-Cell Input High to Low | | 3.9 | | 4.6 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 2.1 | | 2.5 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 2.1 | | 2.5 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 1.6 | | 1.9 | ns |
| $t_{HP}$ | Minimum Period | 4.2 | | 5.0 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 238 | | 200 | MHz |
| **Routed Array Clock Networks** | | | | | | |
| $t_{RCKH}$ | Pad to R-cell Input High to Low (Light Load)) | | 3.9 | | 4.6 | ns |
| $t_{RCHKL}$ | Pad to R-cell Input Low to High (Light Load)) | | 3.7 | | 4.4 | ns |
| $t_{RCKH}$ | Pad to R-cell Input Low to High (50% Load) | | 4.7 | | 5.6 | ns |
| $t_{RCKL}$ | Pad to R-cell Input High to Low (50% Load) | | 4.1 | | 4.9 | ns |
| $t_{RCKH}$ | Pad to R-cell Input Low to High (100% Load) | | 5.3 | | 6.2 | ns |
| $t_{RCKL}$ | Pad to R-cell Input High to Low (100% Load) | | 4.7 | | 5.5 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 2.1 | | 2.5 | | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 2.1 | | 2.5 | | ns |
| $t_{RCKSW}$ | Maximum Skew (Light Load) | | 2.8 | | 3.3 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% Load) | | 2.8 | | 3.3 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% Load) | | 2.8 | | 3.3 | ns |
| $t_{RP}$ | Minimum Period | 4.2 | | 5.0 | | ns |
| $f_{RMAX}$ | Maximum Frequency | | 238 | | 200 | MHz |

*Table 2-30* • **RT54SX72S at $V_{CCI}$ = 3.0V**
**Worst-Case Military Conditions $V_{CCA}$ = 2.25V, $V_{CCI}$ = 3.0V, $T_J$ = 125°C, Radiation Level = 0 krad (Si)**

| | | '–1' Speed | | 'Std.' Speed | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **Dedicated (Hardwired) Array Clock Network** | | | | | | |
| $t_{HCKH}$ | Pad to R-cell Input Low to High | | 3.2 | | 3.8 | ns |
| $t_{HCKL}$ | Pad to R-cell Input High to Low | | 3.5 | | 4.1 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 2.7 | | 3.2 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 2.7 | | 3.2 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 2.7 | | 3.1 | ns |
| $t_{HP}$ | Minimum Period | 5.4 | | 6.4 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 185 | | 156 | MHz |
| **Routed Array Clock Networks** | | | | | | |
| $t_{RCKH}$ | Pad to R-cell Input Low to High (Light Load)) | | 5.7 | | 6.7 | ns |
| $t_{RCKL}$ | Pad to R-cell Input High to Low (Light Load) | | 6.5 | | 7.7 | ns |
| $t_{RCKH}$ | Pad to R-cell Input Low to High (50% Load) | | 5.7 | | 6.7 | ns |
| $t_{RCKL}$ | Pad to R-cell Input High to Low (50% Load) | | 6.5 | | 7.7 | ns |
| $t_{RCKH}$ | Pad to R-cell Input Low to High (100% Load) | | 5.7 | | 6.7 | ns |
| $t_{RCKL}$ | Pad to R-cell Input High to Low (100% Load) | | 6.5 | | 7.7 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 2.7 | | 3.2 | | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 2.7 | | 3.2 | | ns |
| $t_{RCKSW}$ | Maximum Skew (Light Load) | | 5.1 | | 6.0 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% Load) | | 4.9 | | 5.8 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% Load) | | 4.9 | | 5.8 | ns |
| $t_{RP}$ | Minimum Period | 5.4 | | 6.4 | | ns |
| $f_{RMAX}$ | Maximum Frequency | | 185 | | 156 | MHz |
| **Quadrant Array Clock Networks** | | | | | | |
| $t_{QCKH}$ | Pad to R-cell Input Low to High (Light Load) | | 3.6 | | 4.2 | ns |
| $t_{QCKL}$ | Pad to R-cell Input High to Low (Light Load) | | 3.6 | | 4.2 | ns |
| $t_{QCKH}$ | Pad to R-cell Input Low to High (50% Load) | | 3.7 | | 4.3 | ns |
| $t_{QCKL}$ | Pad to R-cell Input High to Low (50% Load) | | 3.9 | | 4.5 | ns |
| $t_{QCKH}$ | Pad to R-cell Input Low to High (100% Load) | | 4.0 | | 4.7 | ns |
| $t_{QCKL}$ | Pad to R-cell Input High to Low (100% Load) | | 4.1 | | 4.8 | ns |
| $t_{QPWH}$ | Minimum Pulse Width High | 2.7 | | 3.2 | | ns |
| $t_{QPWL}$ | Minimum Pulse Width Low | 2.7 | | 3.2 | | ns |
| $t_{QCKSW}$ | Maximum Skew (Light Load) | | 0.6 | | 0.7 | ns |
| $t_{QCKSW}$ | Maximum Skew (50% Load) | | 1.0 | | 1.1 | ns |
| $t_{QCKSW}$ | Maximum Skew (100% Load) | | 1.0 | | 1.1 | ns |
| $t_{QP}$ | Minimum Period | 5.4 | | 6.4 | | ns |
| $f_{QMAX}$ | Maximum Frequency | | 185 | | 156 | MHz |

*Table 2-31* • **RT54SX72S at $V_{CCI}$ = 4.5V**
**Worst-Case Military Conditions $V_{CCA}$ = 2.25V, $V_{CCI}$ = 4.5V, $T_J$ = 125°C, Radiation Level = 0 krad (Si)**

| | | '–1' Speed | | 'Std.' Speed | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **Dedicated (Hardwired) Array Clock Network** | | | | | | |
| $t_{HCKH}$ | Pad to R-cell Input Low to High | | 4.1 | | 4.8 | ns |
| $t_{HCKL}$ | Pad to R-cell Input High to Low | | 4.1 | | 4.8 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 2.8 | | 3.3 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 2.8 | | 3.3 | | ns |
| $t_{HCKSW}$ | Maximum Skew | | 3.2 | | 3.7 | ns |
| $t_{HP}$ | Minimum Period | 5.6 | | 6.6 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 179 | | 152 | MHz |
| **Routed Array Clock Networks** | | | | | | |
| $t_{RCKH}$ | Pad to R-cell Input Low to High (Light Load)) | | 6.8 | | 8.0 | ns |
| $t_{RCKL}$ | Pad to R-cell Input High to Low (Light Load) | | 8.2 | | 9.7 | ns |
| $t_{RCKH}$ | Pad to R-cell Input Low to High (50% Load) | | 6.8 | | 8.0 | ns |
| $t_{RCKL}$ | Pad to R-cell Input High to Low (50% Load) | | 8.2 | | 9.7 | ns |
| $t_{RCKH}$ | Pad to R-cell Input Low to High (100% Load) | | 6.8 | | 8.0 | ns |
| $t_{RCKL}$ | Pad to R-cell Input High to Low (100% Load) | | 8.2 | | 9.7 | ns |
| $t_{RPWH}$ | Minimum Pulse Width High | 2.8 | | 3.3 | | ns |
| $t_{RPWL}$ | Minimum Pulse Width Low | 2.8 | | 3.3 | | ns |
| $t_{RCKSW}$ | Maximum Skew (Light Load) | | 7.0 | | 8.2 | ns |
| $t_{RCKSW}$ | Maximum Skew (50% Load) | | 6.8 | | 8.0 | ns |
| $t_{RCKSW}$ | Maximum Skew (100% Load) | | 6.8 | | 8.0 | ns |
| $t_{QP}$ | Minimum Period | 5.6 | | 6.6 | | ns |
| $f_{QMAX}$ | Maximum Frequency | | 179 | | 152 | MHz |
| **Quadrant Array Clock Networks** | | | | | | |
| $t_{QCKH}$ | Pad to R-cell Input Low to High (Light Load)) | | 3.9 | | 4.6 | ns |
| $t_{QCKL}$ | Pad to R-cell Input High to Low (Light Load) | | 4.2 | | 4.9 | ns |
| $t_{QCKH}$ | Pad to R-cell Input Low to High (50% Load) | | 4.2 | | 4.9 | ns |
| $t_{QCKL}$ | Pad to R-cell Input High to Low (50% Load) | | 4.5 | | 5.3 | ns |
| $t_{QCKH}$ | Pad to R-cell Input Low to High (100% Load) | | 4.5 | | 5.3 | ns |
| $t_{QCKL}$ | Pad to R-cell Input High to Low (100% Load) | | 5.0 | | 5.9 | ns |
| $t_{QPWH}$ | Minimum Pulse Width High | 2.8 | | 3.3 | | ns |
| $t_{QPWL}$ | Minimum Pulse Width Low | 2.8 | | 3.3 | | ns |
| $t_{QCKSW}$ | Maximum Skew (Light Load) | | 0.7 | | 0.8 | ns |
| $t_{QCKSW}$ | Maximum Skew (50% Load) | | 1.3 | | 1.5 | ns |
| $t_{QCKSW}$ | Maximum Skew (100% Load) | | 1.4 | | 1.6 | ns |
| $t_{QP}$ | Minimum Period | 5.6 | | 6.6 | | ns |
| $f_{QMAX}$ | Maximum Frequency | | 179 | | 152 | MHz |

## Global Resource Access Macros

The user can configure which global resource is used in the design as well as how each global resource is driven through the use of the following macros:

- HCLKBUF – used to drive the hardwired clock (HCLK) in both devices from an external pin
- CLKBUF and CLKBUFI – noninverting and inverting inputs used to drive either routed clock (CLKA or CLKB) in both devices from external pins
- CLKINT and CLKINTI – noninverting and inverting inputs used to drive either routed clock (CLKA or CLKB) in both devices from internal logic
- QCLKBUF and QCLKBUFI – noninverting and inverting inputs used to drive quadrant routed clocks (QCLKA/B/C/D) in the RT54SX72S from external pins
- QCLKINT and QCLKINTI – noninverting and inverting inputs used to drive quadrant routed clocks (QCLKA/B/C/D) in the RT54SX72S from internal logic
- QCLKBIBUF and QCLUKBIBUFI – noninverting and inverting inputs used to drive quadrant routed clocks (QCLKA/B/C/D) in the RT54SX72S alternatively from either external pins or internal logic

Figure 2-19, Figure 2-20, and Figure 2-21 illustrate the various global-resource access macros.

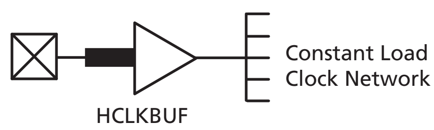


*Figure 2-19* • **Hardwired Clock Buffer**

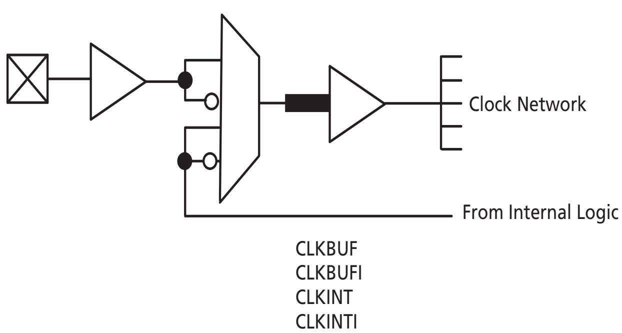


*Figure 2-20* • **Routed Clock Buffers in RT54SX32S**

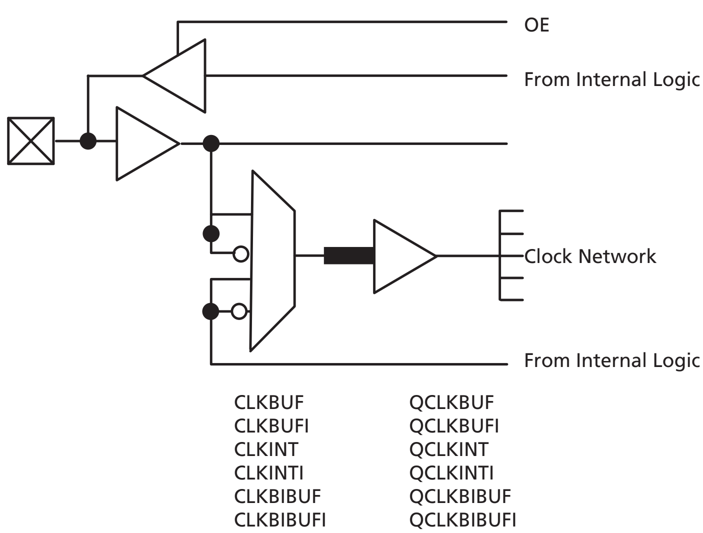


*Figure 2-21* • **Routed And Quadrant Clock Buffers in RT54SX72S**

# Other Architectural Features

## JTAG Interface

All RTSX-S devices are IEEE 1149.1 compliant and offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. The BST function is controlled through special JTAG pins (TMS, TDI, TCK, TDO, and TRST). The functionality of the JTAG pins is defined by two available modes: dedicated and flexible (Table 2-32). Note that TRST and TMS cannot be employed as user I/Os in either mode.

*Table 2-32* • **Boundary Scan Pin Functionality**

| Program Fuse Blown (Dedicated Test Mode) | Program Fuse Not Blown (Flexible Mode) |
|---|---|
| TCK, TDI, TDO are dedicated BST pins | TCK, TDI, TDO are flexible and may be used as user I/Os |
| No need for pull-up resistor for TMS | Use a pull-up resistor of 10 kΩ on TMS |

### Dedicated Mode

In dedicated mode, all JTAG pins are reserved for BST; users cannot employ them as regular I/Os. An internal pull-up resistor (on the order of 17 kΩ to 22 kΩ[2]) is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To enter dedicated mode, users need to reserve the JTAG pins in Actel's Designer software during device selection. To reserve the JTAG pins, users can check the "Reserve JTAG" box in the "Device Selection Wizard" in Actel's Designer software (Figure 2-22).


*Figure 2-22* • **Device Selection Wizard**

### Flexible Mode

In flexible mode, TDI, TCK, and TDO may be employed as either user I/Os or as JTAG input pins. The internal resistors on the TMS and TDI pins are not present in flexible JTAG mode.

To enter the flexible mode, users need to uncheck the "Reserve JTAG" box in the "Device Selection Wizard" in Designer software. TDI, TCK, and TDO pins may function as user I/Os or BST pins in flexible mode. This functionality is controlled by the BST TAP controller. The TAP controller receives two control inputs: TMS and TCK. Upon power-up, the TAP controller enters the Test-Logic-Reset state. In this state, TDI, TCK, and TDO function as user I/Os. The TDI, TCK, and TDO are transformed from user I/Os into BST pins when a rising edge on TCK is detected while TMS is at logic Low. To return to the Test-Logic-Reset state, in the absences of TRST assertion, TMS must be held High for at least five TCK cycles. An external, 10 kΩ pull-up resistor tied to $V_{CCI}$ should be placed on the TMS pin to pull it High by default.

Table 2-33 describes the different configurations of the BST pins and their functionality in different modes.

*Table 2-33* • **JTAG Pin Configurations and Functions**

| Mode | Designer "Reserve JTAG" Selection | TAP Controller State |
|---|---|---|
| Dedicated (JTAG) | Checked | Any |
| Flexible (User I/O) | Unchecked | Test-Logic-Reset |
| Flexible (JTAG) | Unchecked | Other |

### TRST Pin

The TRST pin functions as a dedicated boundary scan reset pin. An internal pull-up resistor is permanently enabled on the TRST pin. Additionally, the TRST pin must be grounded for flight applications. This will prevent Single-Event Upsets (SEU) in the TAP controller from inadvertently placing the device into JTAG mode.

### Probing Capabilities

RTSX-S devices also provide internal probing capability that is accessed with the JTAG pins.

## Silicon Explorer II Probe Interface

Actel's Silicon Explorer II is an integrated hardware and software solution that, in conjunction with Actel's Designer software, allows users to examine any of the internal nets of the device while it is operating in a prototype or a production system. The user can probe two nodes at a time without changing the placement or routing of the design and without using any additional device resources. Highlighted nets in Designer's ChipEditor can be accessed using Silicon Explorer II in order to observe their real time values.

2. *On a given device, the value of the internal pull-up resistor varies within 1 kΩ between the TMS and TDI pins.*

Silicon Explorer II's noninvasive method does not alter timing or loading effects, thus shortening the debug cycle. In addition, Silicon Explorer II does not require relayout or additional MUXes to bring signals out to external pins, which is necessary when using programmable logic devices from other suppliers. By eliminating multiple place-and-route cycles, the integrity of the design is maintained throughout the debug process.

Both members of the RTSX-S family have two external pads: PRA and PRB. These can be used to bring out two probe signals from the device. To disallow probing, the SFUS security fuse in the silicon signature has to be programmed. Table 2-34 shows the possible device configuration options and their effects on probing.

During probing, the Silicon Explorer II Diagnostic Hardware is used to control the TDI, TCK, TMS, and TDO pins to select the desired nets for debugging. The user simply assigns the selected internal nets in the Silicon Explorer II software to the PRA/PRB output pins for observation. Probing functionality is activated when the BST pins are in JTAG mode and the TRST pin is driven High. If the TRST pin is held Low, the TAP controller will remain in the Test-Logic-Reset state, so no probing can be performed. Silicon Explorer II automatically places the device into JTAG mode, but the user must drive the TRST pin High or allow the internal pull-up resistor to pull TRST High.

Silicon Explorer II connects to the host PC using a standard serial port connector. Connections to the circuit board are achieved using a nine-pin D-Sub connector (Figure 1-5 on page 1-6). Once the design has been placed-and-routed and the RTSX-S device has been programmed, Silicon Explorer II can be connected and the Silicon Explorer software can be launched.

Silicon Explorer II comes with an additional optional PC-hosted tool that emulates an 18-channel logic analyzer. Two channels are used to monitor two internal nodes, and 16 channels are available to probe external signals. The software included with the tool provides the user with an intuitive interface that allows for easy viewing and editing of signal waveforms.

*Table 2-34* • **Device Configuration Options for Probe Capability**

| JTAG Mode | TRST | Security Fuse Programmed | PRA and PRB[1] | TDI, TCK, and TDO[1] |
|---|---|---|---|---|
| Dedicated | Low | No | User I/O[2] | Probing Unavailable |
| Flexible | Low | No | User I/O[2] | User I/O[2] |
| Dedicated | High | No | Probe Circuit Outputs | Probe Circuit I/O |
| Flexible | High | No | Probe Circuit Outputs | Probe Circuit I/O |
| – | – | Yes | Probe Circuit Secured | Probe Circuit Secured |

***Notes:***

1. *Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports during probing. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.*
2. *If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. Unused pins are automatically tristated by the Designer software.*

## Security Fuses

Actel antifuse FPGAs, with FuseLock technology, offer the highest level of design security available in a programmable logic device. Since antifuse FPGAs are live at power-up, there is no bitstream that can be intercepted, and no bitstream or programming data is ever downloaded to the device, thus making device cloning impossible. In addition, special security fuses are hidden throughout the fabric of the device and may be programmed by the user to thwart attempts to reverse engineer the device by attempting to exploit either the programming or probing interfaces. Both invasive and noninvasive attacks against an RTSX-S device that access or bypass these security fuses will destroy access to the rest of the device. Refer to the *Understanding Actel Antifuse Device Security* white paper for more information.

Look for this symbol to ensure your valuable IP is secure(Figure 2-23).

*Figure 2-23* • **FuseLock Logo**

To ensure maximum security in RTSX-S devices, it is recommended that the user program the device security fuse (SFUS). When programmed, the Silicon Explorer II testing probes are disabled to prevent internal probing, and the programming interface is also disabled. All JTAG public instructions are still accessible by the user. For more information, refer to Actel's *Implementation of Security in Actel Antifuse FPGAs* application note.

## Programming

Device programming is supported through the Silicon Sculptor II, a single-site, robust and compact device-programmer for the PC. Two Silicon Sculptor IIs can be daisy-chained and controlled from a single PC host. With standalone software for the PC, Silicon Sculptor II is designed to allow concurrent programming of multiple units from the same PC when daisy-chained.

Silicon Sculptor II programs devices independently to achieve the fastest programming times possible. Each fuse is verified by Silicon Sculptor II to ensure correct programming. Furthermore, at the end of programming, there are integrity tests that are run to ensure that programming was completed properly. Not only does it test programmed and nonprogrammed fuses, Silicon Sculptor II also provides a self-test to extensively test its own hardware.

Programming an RTSX-S device using Silicon Sculptor II is similar to programming any other antifuse device. The procedure is as follows:

1. Load the .AFM file.
2. Select the device to be programmed.
3. Begin programming.

When the design is ready to go to production, Actel offers volume programming services either through distribution partners or via our In-House Programming Center. For more details on programming the RTSX-S devices, please refer to the *Silicon Sculptor II User's Guide*.

# Package Pin Assignments

## 208-Pin CQFP

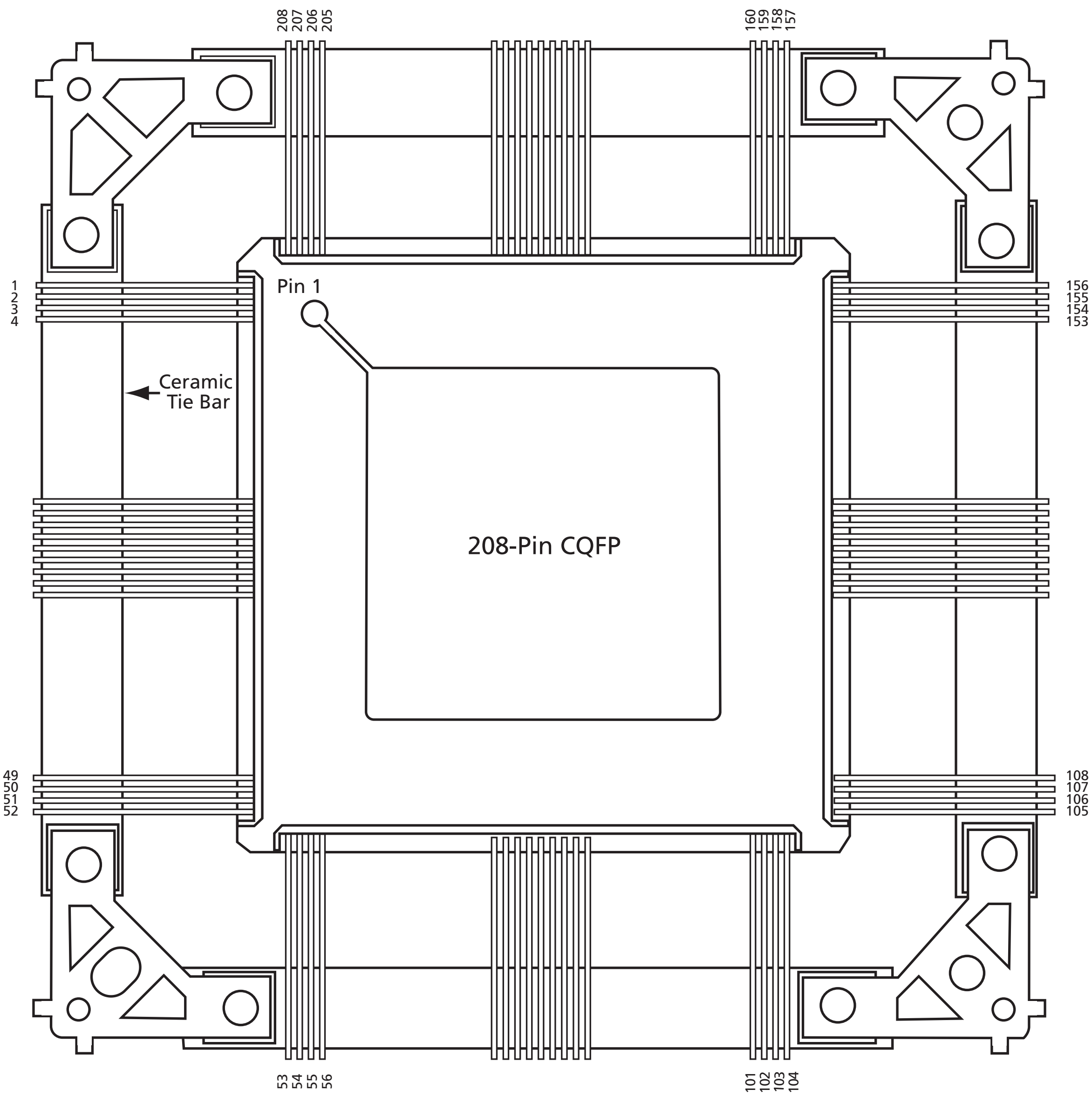


*Figure 3-1* • **208-Pin CQFP (Top View)**

| 208-Pin CQFP | | |
|---|---|---|
| Pin Number | RT54SX32S Function | RT54SX72S Function |
| 1 | GND | GND |
| 2 | TDI, I/O | TDI, I/O |
| 3 | I/O | I/O |
| 4 | I/O | I/O |
| 5 | I/O | I/O |
| 6 | I/O | I/O |
| 7 | I/O | I/O |
| 8 | I/O | I/O |
| 9 | I/O | I/O |
| 10 | I/O | I/O |
| 11 | TMS | TMS |
| 12 | $V_{CCI}$ | $V_{CCI}$ |
| 13 | I/O | I/O |
| 14 | I/O | I/O |
| 15 | I/O | I/O |
| 16 | I/O | I/O |
| 17 | I/O | I/O |
| 18 | I/O | GND |
| 19 | I/O | $V_{CCA}$ |
| 20 | I/O | I/O |
| 21 | I/O | I/O |
| 22 | I/O | I/O |
| 23 | I/O | I/O |
| 24 | I/O | I/O |
| 25 | NC | I/O |
| 26 | GND | GND |
| 27 | $V_{CCA}$ | $V_{CCA}$ |
| 28 | GND | GND |
| 29 | I/O | I/O |
| 30 | TRST | TRST |
| 31 | I/O | I/O |
| 32 | I/O | I/O |
| 33 | I/O | I/O |
| 34 | I/O | I/O |
| 35 | I/O | I/O |
| 36 | I/O | I/O |

***Note:*** *Pin 65 is a No Connect (NC) on Commercial A54SX32S-PQ208.*

| 208-Pin CQFP | | |
|---|---|---|
| Pin Number | RT54SX32S Function | RT54SX72S Function |
| 37 | I/O | I/O |
| 38 | I/O | I/O |
| 39 | I/O | I/O |
| 40 | $V_{CCI}$ | $V_{CCI}$ |
| 41 | $V_{CCA}$ | $V_{CCA}$ |
| 42 | I/O | I/O |
| 43 | I/O | I/O |
| 44 | I/O | I/O |
| 45 | I/O | I/O |
| 46 | I/O | I/O |
| 47 | I/O | I/O |
| 48 | I/O | I/O |
| 49 | I/O | I/O |
| 50 | I/O | I/O |
| 51 | I/O | I/O |
| 52 | GND | GND |
| 53 | I/O | I/O |
| 54 | I/O | I/O |
| 55 | I/O | I/O |
| 56 | I/O | I/O |
| 57 | I/O | I/O |
| 58 | I/O | I/O |
| 59 | I/O | I/O |
| 60 | $V_{CCI}$ | $V_{CCI}$ |
| 61 | I/O | I/O |
| 62 | I/O | I/O |
| 63 | I/O | I/O |
| 64 | I/O | I/O |
| 65 | NC | I/O |
| 66 | I/O | I/O |
| 67 | I/O | I/O |
| 68 | I/O | I/O |
| 69 | I/O | I/O |
| 70 | I/O | I/O |
| 71 | I/O | I/O |
| 72 | I/O | I/O |

***Note:*** *Pin 65 is a No Connect (NC) on Commercial A54SX32S-PQ208.*

| 208-Pin CQFP | | |
|---|---|---|
| Pin Number | RT54SX32S Function | RT54SX72S Function |
| 73 | I/O | I/O |
| 74 | I/O | QCLKA, I/O |
| 75 | I/O | I/O |
| 76 | PRB, I/O | PRB, I/O |
| 77 | GND | GND |
| 78 | $V_{CCA}$ | $V_{CCA}$ |
| 79 | GND | GND |
| 80 | NC | NC |
| 81 | I/O | I/O |
| 82 | HCLK | HCLK |
| 83 | I/O | $V_{CCI}$ |
| 84 | I/O | QCLKB, I/O |
| 85 | I/O | I/O |
| 86 | I/O | I/O |
| 87 | I/O | I/O |
| 88 | I/O | I/O |
| 89 | I/O | I/O |
| 90 | I/O | I/O |
| 91 | I/O | I/O |
| 92 | I/O | I/O |
| 93 | I/O | I/O |
| 94 | I/O | I/O |
| 95 | I/O | I/O |
| 96 | I/O | I/O |
| 97 | I/O | I/O |
| 98 | $V_{CCI}$ | $V_{CCI}$ |
| 99 | I/O | I/O |
| 100 | I/O | I/O |
| 101 | I/O | I/O |
| 102 | I/O | I/O |
| 103 | TDO, I/O | TDO, I/O |
| 104 | I/O | I/O |
| 105 | GND | GND |
| 106 | I/O | I/O |
| 107 | I/O | I/O |
| 108 | I/O | I/O |

***Note:*** *Pin 65 is a No Connect (NC) on Commercial A54SX32S-PQ208.*

| 208-Pin CQFP | | |
|---|---|---|
| Pin Number | RT54SX32S Function | RT54SX72S Function |
| 109 | I/O | I/O |
| 110 | I/O | I/O |
| 111 | I/O | I/O |
| 112 | I/O | I/O |
| 113 | I/O | I/O |
| 114 | $V_{CCA}$ | $V_{CCA}$ |
| 115 | $V_{CCI}$ | $V_{CCI}$ |
| 116 | I/O | GND |
| 117 | I/O | $V_{CCA}$ |
| 118 | I/O | I/O |
| 119 | I/O | I/O |
| 120 | I/O | I/O |
| 121 | I/O | I/O |
| 122 | I/O | I/O |
| 123 | I/O | I/O |
| 124 | I/O | I/O |
| 125 | I/O | I/O |
| 126 | I/O | I/O |
| 127 | I/O | I/O |
| 128 | I/O | I/O |
| 129 | GND | GND |
| 130 | $V_{CCA}$ | $V_{CCA}$ |
| 131 | GND | GND |
| 132 | NC | I/O |
| 133 | I/O | I/O |
| 134 | I/O | I/O |
| 135 | I/O | I/O |
| 136 | I/O | I/O |
| 137 | I/O | I/O |
| 138 | I/O | I/O |
| 139 | I/O | I/O |
| 140 | I/O | I/O |
| 141 | I/O | I/O |
| 142 | I/O | I/O |
| 143 | I/O | I/O |
| 144 | I/O | I/O |

***Note:*** *Pin 65 is a No Connect (NC) on Commercial A54SX32S-PQ208.*

| 208-Pin CQFP | | |
|---|---|---|
| Pin Number | RT54SX32S Function | RT54SX72S Function |
| 145 | $V_{CCA}$ | $V_{CCA}$ |
| 146 | GND | GND |
| 147 | I/O | I/O |
| 148 | $V_{CCI}$ | $V_{CCI}$ |
| 149 | I/O | I/O |
| 150 | I/O | I/O |
| 151 | I/O | I/O |
| 152 | I/O | I/O |
| 153 | I/O | I/O |
| 154 | I/O | I/O |
| 155 | I/O | I/O |
| 156 | I/O | I/O |
| 157 | GND | GND |
| 158 | I/O | I/O |
| 159 | I/O | I/O |
| 160 | I/O | I/O |
| 161 | I/O | I/O |
| 162 | I/O | I/O |
| 163 | I/O | I/O |
| 164 | $V_{CCI}$ | $V_{CCI}$ |
| 165 | I/O | I/O |
| 166 | I/O | I/O |
| 167 | I/O | I/O |
| 168 | I/O | I/O |
| 169 | I/O | I/O |
| 170 | I/O | I/O |
| 171 | I/O | I/O |
| 172 | I/O | I/O |
| 173 | I/O | I/O |
| 174 | I/O | I/O |
| 175 | I/O | I/O |
| 176 | I/O | I/O |
| 177 | I/O | I/O |
| 178 | I/O | QCLKD, I/O |
| 179 | I/O | I/O |
| 180 | CLKA | CLKA, I/O |

***Note:*** *Pin 65 is a No Connect (NC) on Commercial A54SX32S-PQ208.*

| 208-Pin CQFP | | |
|---|---|---|
| Pin Number | RT54SX32S Function | RT54SX72S Function |
| 181 | CLKB | CLKB, I/O |
| 182 | NC | NC |
| 183 | GND | GND |
| 184 | $V_{CCA}$ | $V_{CCA}$ |
| 185 | GND | GND |
| 186 | PRA, I/O | PRA, I/O |
| 187 | I/O | $V_{CCI}$ |
| 188 | I/O | I/O |
| 189 | I/O | I/O |
| 190 | I/O | QCLKC, I/O |
| 191 | I/O | I/O |
| 192 | I/O | I/O |
| 193 | I/O | I/O |
| 194 | I/O | I/O |
| 195 | I/O | I/O |
| 196 | I/O | I/O |
| 197 | I/O | I/O |
| 198 | I/O | I/O |
| 199 | I/O | I/O |
| 200 | I/O | I/O |
| 201 | $V_{CCI}$ | $V_{CCI}$ |
| 202 | I/O | I/O |
| 203 | I/O | I/O |
| 204 | I/O | I/O |
| 205 | I/O | I/O |
| 206 | I/O | I/O |
| 207 | I/O | I/O |
| 208 | TCK, I/O | TCK, I/O |

***Note:*** *Pin 65 is a No Connect (NC) on Commercial A54SX32S-PQ208.*

# 256-Pin CQFP

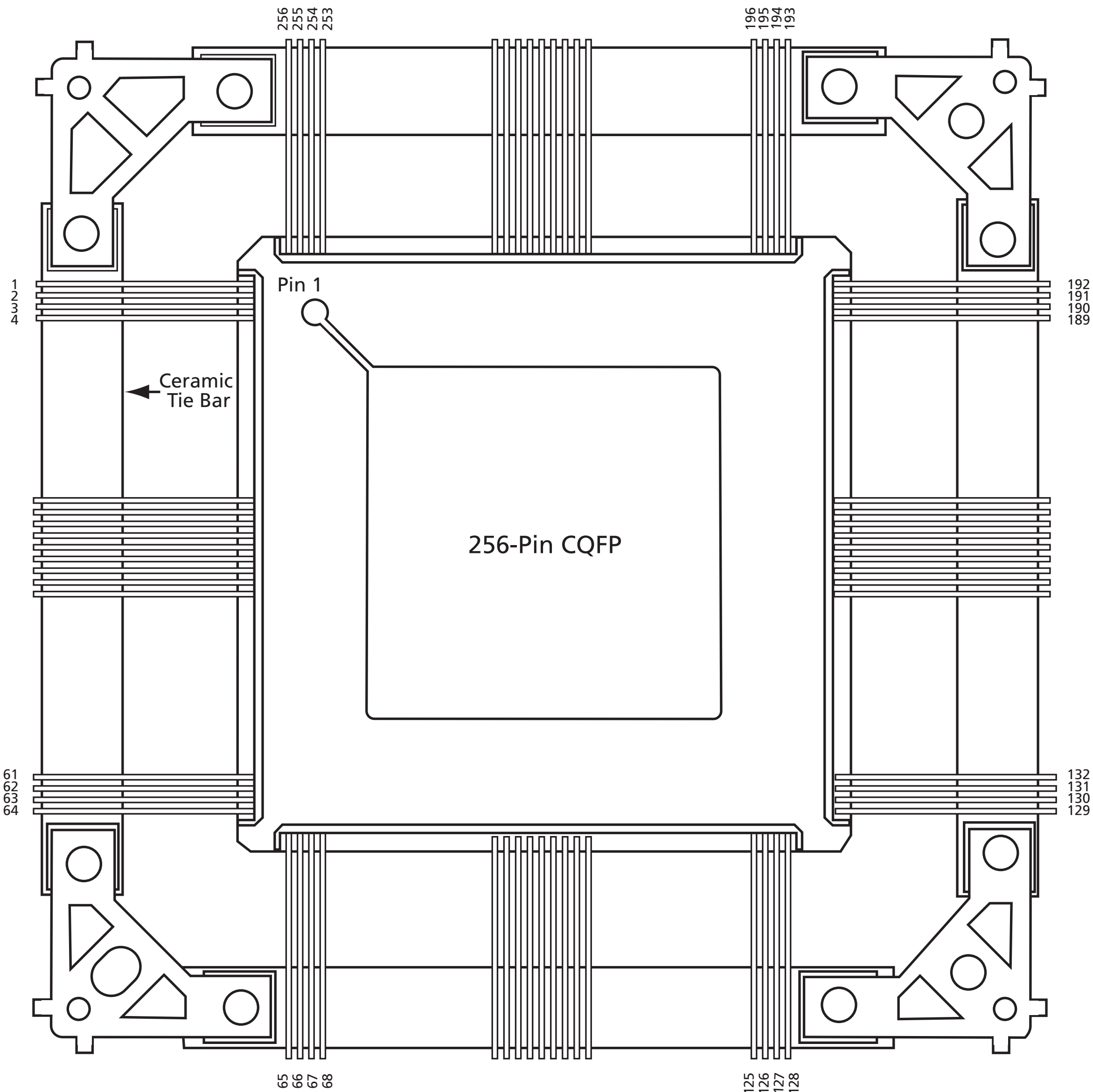


*Figure 3-2* • **256-Pin CQFP (Top View)**

| 256-Pin CQFP | | |
|---|---|---|
| **Pin Number** | **RT54SX32S Function** | **RT54SX72S Function** |
| 1 | GND | GND |
| 2 | TDI, I/O | TDI, I/O |
| 3 | I/O | I/O |
| 4 | I/O | I/O |
| 5 | I/O | I/O |
| 6 | I/O | I/O |
| 7 | I/O | I/O |
| 8 | I/O | I/O |
| 9 | I/O | I/O |
| 10 | I/O | I/O |
| 11 | TMS | TMS |
| 12 | I/O | I/O |
| 13 | I/O | I/O |
| 14 | I/O | I/O |
| 15 | I/O | I/O |
| 16 | I/O | I/O |
| 17 | I/O | $V_{CCI}$ |
| 18 | I/O | I/O |
| 19 | I/O | I/O |
| 20 | I/O | I/O |
| 21 | I/O | I/O |
| 22 | I/O | I/O |
| 23 | I/O | I/O |
| 24 | I/O | I/O |
| 25 | I/O | I/O |
| 26 | I/O | I/O |
| 27 | I/O | I/O |
| 28 | $V_{CCI}$ | $V_{CCI}$ |
| 29 | GND | GND |
| 30 | $V_{CCA}$ | $V_{CCA}$ |
| 31 | GND | GND |
| 32 | I/O | I/O |
| 33 | I/O | I/O |
| 34 | TRST | TRST |
| 35 | I/O | I/O |
| 36 | I/O | $V_{CCA}$ |
| 37 | I/O | GND |

| 256-Pin CQFP | | |
|---|---|---|
| **Pin Number** | **RT54SX32S Function** | **RT54SX72S Function** |
| 38 | I/O | I/O |
| 39 | I/O | I/O |
| 40 | I/O | I/O |
| 41 | I/O | I/O |
| 42 | I/O | I/O |
| 43 | I/O | I/O |
| 44 | I/O | I/O |
| 45 | I/O | I/O |
| 46 | $V_{CCA}$ | $V_{CCA}$ |
| 47 | I/O | $V_{CCI}$ |
| 48 | I/O | I/O |
| 49 | I/O | I/O |
| 50 | I/O | I/O |
| 51 | I/O | I/O |
| 52 | I/O | I/O |
| 53 | I/O | I/O |
| 54 | I/O | I/O |
| 55 | I/O | I/O |
| 56 | I/O | GND |
| 57 | I/O | I/O |
| 58 | I/O | I/O |
| 59 | GND | GND |
| 60 | I/O | I/O |
| 61 | I/O | I/O |
| 62 | I/O | I/O |
| 63 | I/O | I/O |
| 64 | I/O | I/O |
| 65 | I/O | I/O |
| 66 | I/O | I/O |
| 67 | I/O | I/O |
| 68 | I/O | I/O |
| 69 | I/O | I/O |
| 70 | I/O | I/O |
| 71 | I/O | I/O |
| 72 | I/O | I/O |
| 73 | I/O | $V_{CCI}$ |
| 74 | I/O | I/O |

| 256-Pin CQFP | | |
|---|---|---|
| **Pin Number** | **RT54SX32S Function** | **RT54SX72S Function** |
| 75 | I/O | I/O |
| 76 | I/O | I/O |
| 77 | I/O | I/O |
| 78 | I/O | I/O |
| 79 | I/O | I/O |
| 80 | I/O | I/O |
| 81 | I/O | I/O |
| 82 | I/O | I/O |
| 83 | I/O | I/O |
| 84 | I/O | I/O |
| 85 | I/O | I/O |
| 86 | I/O | I/O |
| 87 | I/O | I/O |
| 88 | I/O | I/O |
| 89 | I/O | QCLKA, I/O |
| 90 | PRB, I/O | PRB, I/O |
| 91 | GND | GND |
| 92 | $V_{CCI}$ | $V_{CCI}$ |
| 93 | GND | GND |
| 94 | $V_{CCA}$ | $V_{CCA}$ |
| 95 | I/O | I/O |
| 96 | HCLK | HCLK |
| 97 | I/O | I/O |
| 98 | I/O | QCLKB, I/O |
| 99 | I/O | I/O |
| 100 | I/O | I/O |
| 101 | I/O | I/O |
| 102 | I/O | I/O |
| 103 | I/O | I/O |
| 104 | I/O | I/O |
| 105 | I/O | I/O |
| 106 | I/O | I/O |
| 107 | I/O | I/O |
| 108 | I/O | I/O |
| 109 | I/O | I/O |
| 110 | GND | GND |
| 111 | I/O | I/O |

| 256-Pin CQFP | | |
|---|---|---|
| **Pin Number** | **RT54SX32S Function** | **RT54SX72S Function** |
| 112 | I/O | I/O |
| 113 | I/O | I/O |
| 114 | I/O | I/O |
| 115 | I/O | I/O |
| 116 | I/O | I/O |
| 117 | I/O | I/O |
| 118 | I/O | I/O |
| 119 | I/O | I/O |
| 120 | I/O | $V_{CCI}$ |
| 121 | I/O | I/O |
| 122 | I/O | I/O |
| 123 | I/O | I/O |
| 124 | I/O | I/O |
| 125 | I/O | I/O |
| 126 | TDO, I/O | TDO, I/O |
| 127 | I/O | I/O |
| 128 | GND | GND |
| 129 | I/O | I/O |
| 130 | I/O | I/O |
| 131 | I/O | I/O |
| 132 | I/O | I/O |
| 133 | I/O | I/O |
| 134 | I/O | I/O |
| 135 | I/O | I/O |
| 136 | I/O | I/O |
| 137 | I/O | I/O |
| 138 | I/O | I/O |
| 139 | I/O | I/O |
| 140 | I/O | I/O |
| 141 | $V_{CCA}$ | $V_{CCA}$ |
| 142 | I/O | $V_{CCI}$ |
| 143 | I/O | GND |
| 144 | I/O | $V_{CCA}$ |
| 145 | I/O | I/O |
| 146 | I/O | I/O |
| 147 | I/O | I/O |
| 148 | I/O | I/O |

| 256-Pin CQFP | | |
|---|---|---|
| Pin Number | RT54SX32S Function | RT54SX72S Function |
| 149 | I/O | I/O |
| 150 | I/O | I/O |
| 151 | I/O | I/O |
| 152 | I/O | I/O |
| 153 | I/O | I/O |
| 154 | I/O | I/O |
| 155 | I/O | I/O |
| 156 | I/O | I/O |
| 157 | I/O | I/O |
| 158 | GND | GND |
| 159 | NC | NC |
| 160 | GND | GND |
| 161 | $V_{CCI}$ | $V_{CCI}$ |
| 162 | I/O | $V_{CCA}$ |
| 163 | I/O | I/O |
| 164 | I/O | I/O |
| 165 | I/O | I/O |
| 166 | I/O | I/O |
| 167 | I/O | I/O |
| 168 | I/O | I/O |
| 169 | I/O | I/O |
| 170 | I/O | I/O |
| 171 | I/O | I/O |
| 172 | I/O | I/O |
| 173 | I/O | I/O |
| 174 | $V_{CCA}$ | $V_{CCA}$ |
| 175 | GND | GND |
| 176 | GND | GND |
| 177 | I/O | I/O |
| 178 | I/O | I/O |
| 179 | I/O | I/O |
| 180 | I/O | I/O |
| 181 | I/O | I/O |
| 182 | I/O | I/O |
| 183 | I/O | $V_{CCI}$ |
| 184 | I/O | I/O |
| 185 | I/O | I/O |

| 256-Pin CQFP | | |
|---|---|---|
| Pin Number | RT54SX32S Function | RT54SX72S Function |
| 186 | I/O | I/O |
| 187 | I/O | I/O |
| 188 | I/O | I/O |
| 189 | GND | GND |
| 190 | I/O | I/O |
| 191 | I/O | I/O |
| 192 | I/O | I/O |
| 193 | I/O | I/O |
| 194 | I/O | I/O |
| 195 | I/O | I/O |
| 196 | I/O | I/O |
| 197 | I/O | I/O |
| 198 | I/O | I/O |
| 199 | I/O | I/O |
| 200 | I/O | I/O |
| 201 | I/O | I/O |
| 202 | I/O | $V_{CCI}$ |
| 203 | I/O | I/O |
| 204 | I/O | I/O |
| 205 | I/O | I/O |
| 206 | I/O | I/O |
| 207 | I/O | I/O |
| 208 | I/O | I/O |
| 209 | I/O | I/O |
| 210 | I/O | I/O |
| 211 | I/O | I/O |
| 212 | I/O | I/O |
| 213 | I/O | I/O |
| 214 | I/O | I/O |
| 215 | I/O | I/O |
| 216 | I/O | I/O |
| 217 | I/O | I/O |
| 218 | I/O | QCLKD, I/O |
| 219 | CLKA | CLKA, I/O |
| 220 | CLKB | CLKB, I/O |
| 221 | $V_{CCI}$ | $V_{CCI}$ |
| 222 | GND | GND |

| 256-Pin CQFP | | |
|---|---|---|
| Pin Number | RT54SX32S Function | RT54SX72S Function |
| 223 | NC | NC |
| 224 | GND | GND |
| 225 | PRA, I/O | PRA, I/O |
| 226 | I/O | I/O |
| 227 | I/O | I/O |
| 228 | I/O | $V_{CCA}$ |
| 229 | I/O | I/O |
| 230 | I/O | I/O |
| 231 | I/O | QCLKC, I/O |
| 232 | I/O | I/O |
| 233 | I/O | I/O |
| 234 | I/O | I/O |
| 235 | I/O | I/O |
| 236 | I/O | I/O |
| 237 | I/O | I/O |
| 238 | I/O | I/O |
| 239 | I/O | I/O |
| 240 | GND | GND |
| 241 | I/O | I/O |
| 242 | I/O | I/O |
| 243 | I/O | I/O |
| 244 | I/O | I/O |
| 245 | I/O | I/O |
| 246 | I/O | I/O |
| 247 | I/O | I/O |
| 248 | I/O | I/O |
| 249 | I/O | $V_{CCI}$ |
| 250 | I/O | I/O |
| 251 | I/O | I/O |
| 252 | I/O | I/O |
| 253 | I/O | I/O |
| 254 | I/O | I/O |
| 255 | I/O | I/O |
| 256 | TCK, I/O | TCK, I/O |

# 256-Pin CCLG

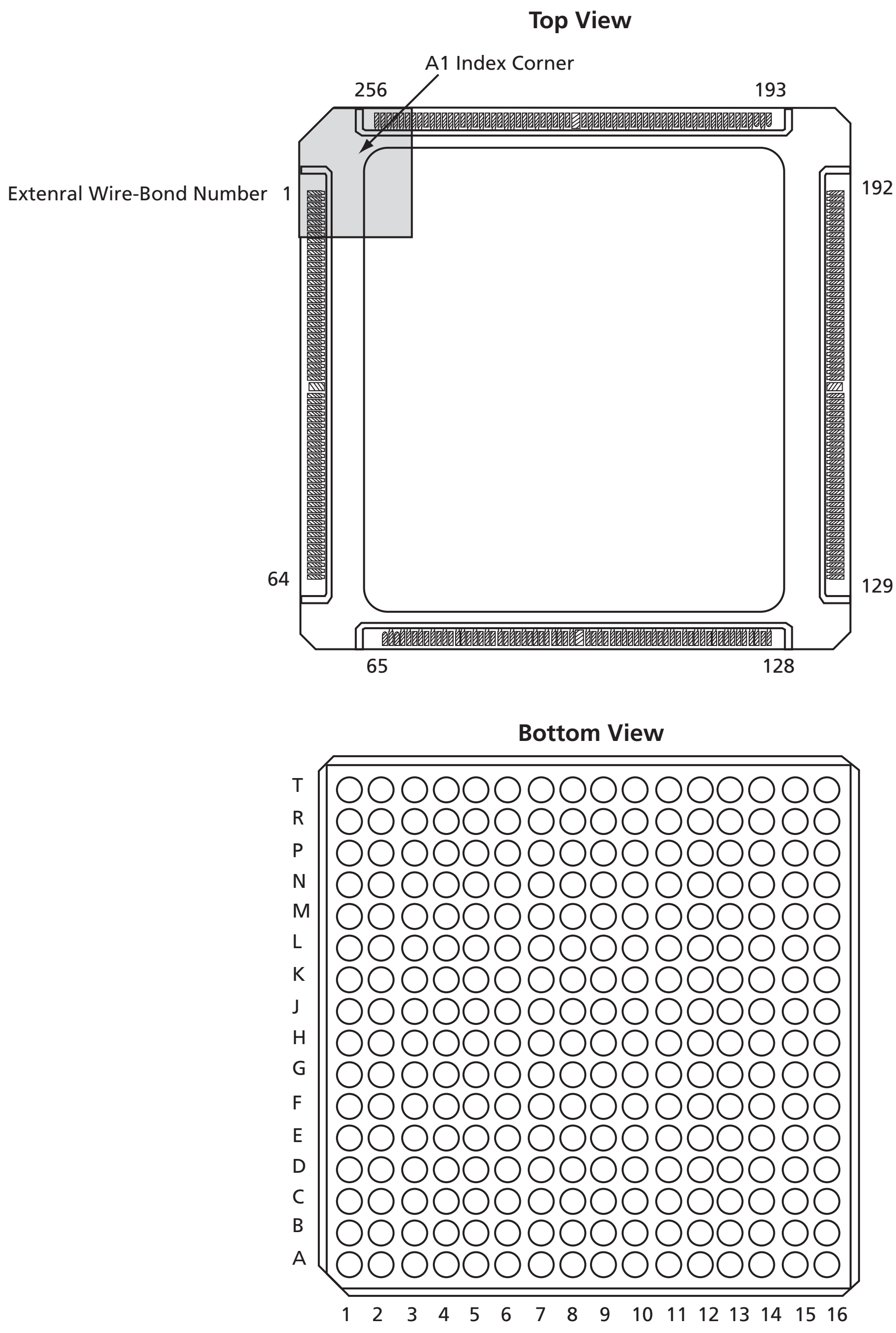


*Figure 3-3* • **256-Pin CCLG**

| 256-Pin CCLG* | | |
|---|---|---|
| Pin Number | External Wire-Bond Number | RT54SX32S Function |
| A1 | 1 | GND |
| A2 | 256 | TCK, I/O |
| A3 | 255 | I/O |
| A4 | 251 | I/O |
| A5 | 243 | I/O |
| A6 | 238 | I/O |
| A7 | 232 | I/O |
| A8 | 228 | I/O |
| A9 | 227 | CLKB |
| A10 | 221 | I/O |
| A11 | 216 | I/O |
| A12 | 209 | I/O |
| A13 | 203 | I/O |
| A14 | 200 | I/O |
| A15 | 2 | GND |
| A16 | 13 | GND |
| B1 | 242 | I/O |
| B2 | 22 | GND |
| B3 | 254 | I/O |
| B4 | 253 | I/O |
| B5 | 248 | I/O |
| B6 | 241 | I/O |
| B7 | 234 | I/O |
| B8 | 33 | $V_{CCA}$ |
| B9 | 222 | I/O |
| B10 | 220 | I/O |
| B11 | 212 | I/O |
| B12 | 207 | I/O |
| B13 | 202 | I/O |
| B14 | 198 | I/O |
| B15 | 32 | GND |
| B16 | 196 | I/O |
| C1 | 6 | I/O |
| C2 | 4 | TDI,I/O |

**Note:** *This table was sorted by the pin number.*

| 256-Pin CCLG* | | |
|---|---|---|
| Pin Number | External Wire-Bond Number | RT54SX32S Function |
| C3 | 65 | GND |
| C4 | 252 | I/O |
| C5 | 249 | I/O |
| C6 | 245 | I/O |
| C7 | 239 | I/O |
| C8 | 230 | I/O |
| C9 | 226 | CLKA |
| C10 | 218 | I/O |
| C11 | 210 | I/O |
| C12 | 201 | I/O |
| C13 | 197 | I/O |
| C14 | 211 | I/O |
| C15 | 178 | I/O |
| C16 | 195 | I/O |
| D1 | 12 | I/O |
| D2 | 8 | I/O |
| D3 | 10 | I/O |
| D4 | 7 | I/O |
| D5 | 250 | I/O |
| D6 | 244 | I/O |
| D7 | 237 | I/O |
| D8 | 229 | PRA, I/O |
| D9 | 217 | I/O |
| D10 | 208 | I/O |
| D11 | 206 | I/O |
| D12 | 199 | I/O |
| D13 | 205 | I/O |
| D14 | 173 | I/O |
| D15 | 190 | I/O |
| D16 | 188 | I/O |
| E1 | 16 | I/O |
| E2 | 15 | I/O |
| E3 | 9 | I/O |
| E4 | 11 | I/O |

**Note:** *This table was sorted by the pin number.*

| 256-Pin CCLG* | | |
|---|---|---|
| Pin Number | External Wire-Bond Number | RT54SX32S Function |
| E5 | 5 | I/O |
| E6 | 240 | I/O |
| E7 | 233 | I/O |
| E8 | 231 | I/O |
| E9 | 223 | I/O |
| E10 | 219 | I/O |
| E11 | 213 | I/O |
| E12 | 167 | I/O |
| E13 | 183 | I/O |
| E14 | 189 | I/O |
| E15 | 187 | I/O |
| E16 | 186 | I/O |
| F1 | 17 | I/O |
| F2 | 18 | I/O |
| F3 | 20 | I/O |
| F4 | 14 | TMS |
| F5 | 19 | I/O |
| F6 | 28 | I/O |
| F7 | 3 | $V_{CCI}$ |
| F8 | 23 | $V_{CCI}$ |
| F9 | 44 | $V_{CCI}$ |
| F10 | 55 | $V_{CCI}$ |
| F11 | 157 | I/O |
| F12 | 97 | $V_{CCA}$ |
| F13 | 177 | I/O |
| F14 | 185 | I/O |
| F15 | 184 | I/O |
| F16 | 181 | I/O |
| G1 | 24 | I/O |
| G2 | 25 | I/O |
| G3 | 27 | I/O |
| G4 | 26 | I/O |
| G5 | 21 | I/O |
| G6 | 66 | $V_{CCI}$ |

***Note:*** **This table was sorted by the pin number.*

| 256-Pin CCLG* | | |
|---|---|---|
| Pin Number | External Wire-Bond Number | RT54SX32S Function |
| G7 | 43 | GND |
| G8 | 54 | GND |
| G9 | 67 | GND |
| G10 | 77 | GND |
| G11 | 87 | $V_{CCI}$ |
| G12 | 169 | I/O |
| G13 | 180 | GND |
| G14 | 176 | I/O |
| G15 | 179 | $V_{CCA}$ |
| G16 | 175 | I/O |
| H1 | 29 | I/O |
| H2 | 31 | I/O |
| H3 | 160 | $V_{CCA}$ |
| H4 | 35 | TRST |
| H5 | 37 | I/O |
| H6 | 108 | $V_{CCI}$ |
| H7 | 86 | GND |
| H8 | 96 | GND |
| H9 | 107 | GND |
| H10 | 118 | GND |
| H11 | 128 | $V_{CCI}$ |
| H12 | 165 | I/O |
| H13 | 170 | I/O |
| H14 | 168 | I/O |
| H15 | 166 | I/O |
| H16 | 174 | I/O |
| J1 | 30 | I/O |
| J2 | 38 | I/O |
| J3 | 40 | I/O |
| J4 | 41 | I/O |
| J5 | 39 | I/O |
| J6 | 139 | $V_{CCI}$ |
| J7 | 127 | GND |
| J8 | 140 | GND |

***Note:*** **This table was sorted by the pin number.*

| 256-Pin CCLG* | | |
|---|---|---|
| Pin Number | External Wire-Bond Number | RT54SX32S Function |
| J9 | 151 | GND |
| J10 | 161 | GND |
| J11 | 150 | $V_{CCI}$ |
| J12 | 159 | I/O |
| J13 | 163 | I/O |
| J14 | 164 | I/O |
| J15 | 162 | I/O |
| J16 | 158 | I/O |
| K1 | 34 | I/O |
| K2 | 45 | I/O |
| K3 | 47 | I/O |
| K4 | 50 | $V_{CCA}$ |
| K5 | 48 | I/O |
| K6 | 171 | $V_{CCI}$ |
| K7 | 172 | GND |
| K8 | 182 | GND |
| K9 | 192 | GND |
| K10 | 204 | GND |
| K11 | 191 | $V_{CCI}$ |
| K12 | 153 | I/O |
| K13 | 155 | I/O |
| K14 | 156 | I/O |
| K15 | 152 | I/O |
| K16 | 154 | I/O |
| L1 | 36 | I/O |
| L2 | 46 | I/O |
| L3 | 51 | I/O |
| L4 | 58 | I/O |
| L5 | 52 | I/O |
| L6 | 91 | I/O |
| L7 | 194 | $V_{CCI}$ |
| L8 | 214 | $V_{CCI}$ |
| L9 | 235 | $V_{CCI}$ |
| L10 | 246 | $V_{CCI}$ |

**Note:** *This table was sorted by the pin number.*

| 256-Pin CCLG* | | |
|---|---|---|
| Pin Number | External Wire-Bond Number | RT54SX32S Function |
| L11 | 103 | I/O |
| L12 | 149 | I/O |
| L13 | 146 | I/O |
| L14 | 148 | I/O |
| L15 | 145 | I/O |
| L16 | 147 | I/O |
| M1 | 42 | I/O |
| M2 | 53 | I/O |
| M3 | 61 | I/O |
| M4 | 60 | I/O |
| M5 | 72 | I/O |
| M6 | 81 | I/O |
| M7 | 89 | I/O |
| M8 | 95 | PRB, I/O |
| M9 | 101 | I/O |
| M10 | 105 | I/O |
| M11 | 114 | I/O |
| M12 | 111 | I/O |
| M13 | 141 | I/O |
| M14 | 142 | I/O |
| M15 | 137 | I/O |
| M16 | 144 | I/O |
| N1 | 49 | I/O |
| N2 | 57 | I/O |
| N3 | 63 | I/O |
| N4 | 79 | I/O |
| N5 | 70 | I/O |
| N6 | 76 | I/O |
| N7 | 83 | I/O |
| N8 | 99 | I/O |
| N9 | 109 | I/O |
| N10 | 117 | I/O |
| N11 | 112 | I/O |
| N12 | 124 | I/O |

**Note:** *This table was sorted by the pin number.*

| 256-Pin CCLG* | | |
|---|---|---|
| Pin Number | External Wire-Bond Number | RT54SX32S Function |
| N13 | 121 | I/O |
| N14 | 133 | I/O |
| N15 | 135 | I/O |
| N16 | 136 | I/O |
| P1 | 59 | I/O |
| P2 | 138 | GND |
| P3 | 56 | I/O |
| P4 | 74 | I/O |
| P5 | 64 | I/O |
| P6 | 82 | I/O |
| P7 | 90 | I/O |
| P8 | 94 | I/O |
| P9 | 104 | I/O |
| P10 | 113 | I/O |
| P11 | 119 | I/O |
| P12 | 123 | I/O |
| P13 | 143 | $V_{CCA}$ |
| P14 | 131 | I/O |
| P15 | 132 | I/O |
| P16 | 134 | I/O |
| R1 | 62 | I/O |
| R2 | 215 | GND |
| R3 | 68 | I/O |
| R4 | 73 | I/O |
| R5 | 78 | I/O |
| R6 | 85 | I/O |
| R7 | 92 | I/O |
| R8 | 98 | I/O |
| R9 | 100 | HCLK |
| R10 | 106 | I/O |
| R11 | 115 | I/O |
| R12 | 120 | I/O |
| R13 | 126 | I/O |
| R14 | 130 | I/O |

***Note:*** **This table was sorted by the pin number.*

| 256-Pin CCLG* | | |
|---|---|---|
| Pin Number | External Wire-Bond Number | RT54SX32S Function |
| R15 | 225 | GND |
| R16 | 193 | GND |
| T1 | 236 | GND |
| T2 | 69 | I/O |
| T3 | 71 | I/O |
| T4 | 75 | I/O |
| T5 | 80 | I/O |
| T6 | 84 | I/O |
| T7 | 88 | I/O |
| T8 | 93 | I/O |
| T9 | 224 | $V_{CCA}$ |
| T10 | 102 | I/O |
| T11 | 110 | I/O |
| T12 | 116 | I/O |
| T13 | 122 | I/O |
| T14 | 125 | I/O |
| T15 | 129 | TDO,I/O |
| T16 | 247 | GND |

***Note:*** **This table was sorted by the pin number.*

| 256-Pin CCLG* | | |
|---|---|---|
| Pin Number | External Wire-Bond Number | RT54SX32S Function |
| A1 | 1 | GND |
| A15 | 2 | GND |
| F7 | 3 | $V_{CCI}$ |
| C2 | 4 | TDI,I/O |
| E5 | 5 | I/O |
| C1 | 6 | I/O |
| D4 | 7 | I/O |
| D2 | 8 | I/O |
| E3 | 9 | I/O |
| D3 | 10 | I/O |
| E4 | 11 | I/O |
| D1 | 12 | I/O |
| A16 | 13 | GND |
| F4 | 14 | TMS |
| E2 | 15 | I/O |
| E1 | 16 | I/O |
| F1 | 17 | I/O |
| F2 | 18 | I/O |
| F5 | 19 | I/O |
| F3 | 20 | I/O |
| G5 | 21 | I/O |
| B2 | 22 | GND |
| F8 | 23 | $V_{CCI}$ |
| G1 | 24 | I/O |
| G2 | 25 | I/O |
| G4 | 26 | I/O |
| G3 | 27 | I/O |
| F6 | 28 | I/O |
| H1 | 29 | I/O |
| J1 | 30 | I/O |
| H2 | 31 | I/O |
| B15 | 32 | GND |
| B8 | 33 | $V_{CCA}$ |
| K1 | 34 | I/O |

**Note:** *This table was sorted by the wire-bond number.*

| 256-Pin CCLG* | | |
|---|---|---|
| Pin Number | External Wire-Bond Number | RT54SX32S Function |
| H4 | 35 | TRST |
| L1 | 36 | I/O |
| H5 | 37 | I/O |
| J2 | 38 | I/O |
| J5 | 39 | I/O |
| J3 | 40 | I/O |
| J4 | 41 | I/O |
| M1 | 42 | I/O |
| G7 | 43 | GND |
| F9 | 44 | $V_{CCI}$ |
| K2 | 45 | I/O |
| L2 | 46 | I/O |
| K3 | 47 | I/O |
| K5 | 48 | I/O |
| N1 | 49 | I/O |
| K4 | 50 | $V_{CCA}$ |
| L3 | 51 | I/O |
| L5 | 52 | I/O |
| M2 | 53 | I/O |
| G8 | 54 | GND |
| F10 | 55 | $V_{CCI}$ |
| P3 | 56 | I/O |
| N2 | 57 | I/O |
| L4 | 58 | I/O |
| P1 | 59 | I/O |
| M4 | 60 | I/O |
| M3 | 61 | I/O |
| R1 | 62 | I/O |
| N3 | 63 | I/O |
| P5 | 64 | I/O |
| C3 | 65 | GND |
| G6 | 66 | $V_{CCI}$ |
| G9 | 67 | GND |
| R3 | 68 | I/O |

**Note:** *This table was sorted by the wire-bond number.*

| 256-Pin CCLG* | | |
|---|---|---|
| Pin Number | External Wire-Bond Number | RT54SX32S Function |
| T2 | 69 | I/O |
| N5 | 70 | I/O |
| T3 | 71 | I/O |
| M5 | 72 | I/O |
| R4 | 73 | I/O |
| P4 | 74 | I/O |
| T4 | 75 | I/O |
| N6 | 76 | I/O |
| G10 | 77 | GND |
| R5 | 78 | I/O |
| N4 | 79 | I/O |
| T5 | 80 | I/O |
| M6 | 81 | I/O |
| P6 | 82 | I/O |
| N7 | 83 | I/O |
| T6 | 84 | I/O |
| R6 | 85 | I/O |
| H7 | 86 | GND |
| G11 | 87 | $V_{CCI}$ |
| T7 | 88 | I/O |
| M7 | 89 | I/O |
| P7 | 90 | I/O |
| L6 | 91 | I/O |
| R7 | 92 | I/O |
| T8 | 93 | I/O |
| P8 | 94 | I/O |
| M8 | 95 | PRB, I/O |
| H8 | 96 | GND |
| F12 | 97 | $V_{CCA}$ |
| R8 | 98 | I/O |
| N8 | 99 | I/O |
| R9 | 100 | HCLK |
| M9 | 101 | I/O |
| T10 | 102 | I/O |

***Note:*** **This table was sorted by the wire-bond number.*

| 256-Pin CCLG* | | |
|---|---|---|
| Pin Number | External Wire-Bond Number | RT54SX32S Function |
| L11 | 103 | I/O |
| P9 | 104 | I/O |
| M10 | 105 | I/O |
| R10 | 106 | I/O |
| H9 | 107 | GND |
| H6 | 108 | $V_{CCI}$ |
| N9 | 109 | I/O |
| T11 | 110 | I/O |
| M12 | 111 | I/O |
| N11 | 112 | I/O |
| P10 | 113 | I/O |
| M11 | 114 | I/O |
| R11 | 115 | I/O |
| T12 | 116 | I/O |
| N10 | 117 | I/O |
| H10 | 118 | GND |
| P11 | 119 | I/O |
| R12 | 120 | I/O |
| N13 | 121 | I/O |
| T13 | 122 | I/O |
| P12 | 123 | I/O |
| N12 | 124 | I/O |
| T14 | 125 | I/O |
| R13 | 126 | I/O |
| J7 | 127 | GND |
| H11 | 128 | $V_{CCI}$ |
| T15 | 129 | TDO,I/O |
| R14 | 130 | I/O |
| P14 | 131 | I/O |
| P15 | 132 | I/O |
| N14 | 133 | I/O |
| P16 | 134 | I/O |
| N15 | 135 | I/O |
| N16 | 136 | I/O |

***Note:*** **This table was sorted by the wire-bond number.*

| 256-Pin CCLG* | | |
|---|---|---|
| Pin Number | External Wire-Bond Number | RT54SX32S Function |
| M15 | 137 | I/O |
| P2 | 138 | GND |
| J6 | 139 | $V_{CCI}$ |
| J8 | 140 | GND |
| M13 | 141 | I/O |
| M14 | 142 | I/O |
| P13 | 143 | $V_{CCA}$ |
| M16 | 144 | I/O |
| L15 | 145 | I/O |
| L13 | 146 | I/O |
| L16 | 147 | I/O |
| L14 | 148 | I/O |
| L12 | 149 | I/O |
| J11 | 150 | $V_{CCI}$ |
| J9 | 151 | GND |
| K15 | 152 | I/O |
| K12 | 153 | I/O |
| K16 | 154 | I/O |
| K13 | 155 | I/O |
| K14 | 156 | I/O |
| F11 | 157 | I/O |
| J16 | 158 | I/O |
| J12 | 159 | I/O |
| H3 | 160 | $V_{CCA}$ |
| J10 | 161 | GND |
| J15 | 162 | I/O |
| J13 | 163 | I/O |
| J14 | 164 | I/O |
| H12 | 165 | I/O |
| H15 | 166 | I/O |
| E12 | 167 | I/O |
| H14 | 168 | I/O |
| G12 | 169 | I/O |
| H13 | 170 | I/O |

**Note:** **This table was sorted by the wire-bond number.*

| 256-Pin CCLG* | | |
|---|---|---|
| Pin Number | External Wire-Bond Number | RT54SX32S Function |
| K6 | 171 | $V_{CCI}$ |
| K7 | 172 | GND |
| D14 | 173 | I/O |
| H16 | 174 | I/O |
| G16 | 175 | I/O |
| G14 | 176 | I/O |
| F13 | 177 | I/O |
| C15 | 178 | I/O |
| G15 | 179 | $V_{CCA}$ |
| G13 | 180 | GND |
| F16 | 181 | I/O |
| K8 | 182 | GND |
| E13 | 183 | I/O |
| F15 | 184 | I/O |
| F14 | 185 | I/O |
| E16 | 186 | I/O |
| E15 | 187 | I/O |
| D16 | 188 | I/O |
| E14 | 189 | I/O |
| D15 | 190 | I/O |
| K11 | 191 | $V_{CCI}$ |
| K9 | 192 | GND |
| R16 | 193 | GND |
| L7 | 194 | $V_{CCI}$ |
| C16 | 195 | I/O |
| B16 | 196 | I/O |
| C13 | 197 | I/O |
| B14 | 198 | I/O |
| D12 | 199 | I/O |
| A14 | 200 | I/O |
| C12 | 201 | I/O |
| B13 | 202 | I/O |
| A13 | 203 | I/O |
| K10 | 204 | GND |

**Note:** **This table was sorted by the wire-bond number.*

| 256-Pin CCLG* | | |
|---|---|---|
| Pin Number | External Wire-Bond Number | RT54SX32S Function |
| D13 | 205 | I/O |
| D11 | 206 | I/O |
| B12 | 207 | I/O |
| D10 | 208 | I/O |
| A12 | 209 | I/O |
| C11 | 210 | I/O |
| C14 | 211 | I/O |
| B11 | 212 | I/O |
| E11 | 213 | I/O |
| L8 | 214 | $V_{CCI}$ |
| R2 | 215 | GND |
| A11 | 216 | I/O |
| D9 | 217 | I/O |
| C10 | 218 | I/O |
| E10 | 219 | I/O |
| B10 | 220 | I/O |
| A10 | 221 | I/O |
| B9 | 222 | I/O |
| E9 | 223 | I/O |
| T9 | 224 | $V_{CCA}$ |
| R15 | 225 | GND |
| C9 | 226 | CLKA |
| A9 | 227 | CLKB |
| A8 | 228 | I/O |
| D8 | 229 | PRA, I/O |
| C8 | 230 | I/O |
| E8 | 231 | I/O |
| A7 | 232 | I/O |
| E7 | 233 | I/O |
| B7 | 234 | I/O |
| L9 | 235 | $V_{CCI}$ |
| T1 | 236 | GND |
| D7 | 237 | I/O |
| A6 | 238 | I/O |

**Note:** **This table was sorted by the wire-bond number.*

| 256-Pin CCLG* | | |
|---|---|---|
| Pin Number | External Wire-Bond Number | RT54SX32S Function |
| C7 | 239 | I/O |
| E6 | 240 | I/O |
| B6 | 241 | I/O |
| B1 | 242 | I/O |
| A5 | 243 | I/O |
| D6 | 244 | I/O |
| C6 | 245 | I/O |
| L10 | 246 | $V_{CCI}$ |
| T16 | 247 | GND |
| B5 | 248 | I/O |
| C5 | 249 | I/O |
| D5 | 250 | I/O |
| A4 | 251 | I/O |
| C4 | 252 | I/O |
| B4 | 253 | I/O |
| B3 | 254 | I/O |
| A3 | 255 | I/O |
| A2 | 256 | TCK, I/O |

**Note:** **This table was sorted by the wire-bond number.*

## 624-Pin CCGA

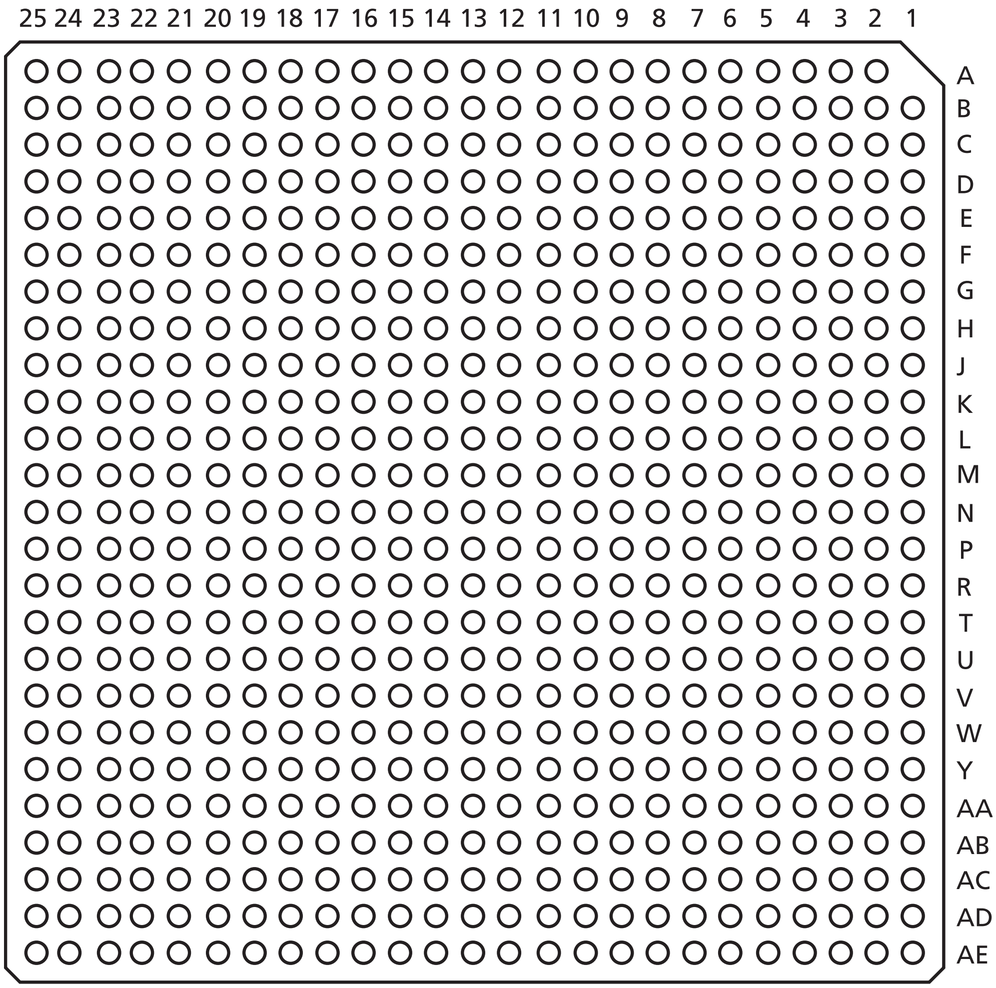


*Figure 3-4* • **624-Pin CCGA (Bottom View)**

| 624-Pin CCGA | |
|---|---|
| Pin Number | RT54SX72S Function |
| A2 | NC |
| A3 | NC |
| A4 | NC |
| A5 | I/O |
| A6 | I/O |
| A7 | I/O |
| A8 | I/O |
| A9 | I/O |
| A10 | I/O |
| A11 | I/O |
| A12 | I/O |
| A13 | GND |
| A14 | I/O |
| A15 | I/O |
| A16 | I/O |
| A17 | I/O |
| A18 | I/O |
| A19 | I/O |
| A20 | I/O |
| A21 | I/O |
| A22 | GND |
| A23 | NC |
| A24 | NC |
| A25 | NC |
| B1 | NC |
| B2 | GND |
| B3 | GND |
| B4 | $V_{CCI}$ |
| B5 | GND |
| B6 | I/O |
| B7 | I/O |
| B8 | $V_{CCI}$ |
| B9 | GND |
| B10 | I/O |
| B11 | I/O |
| B12 | I/O |
| B13 | I/O |
| B14 | CLKB, I/O |
| B15 | I/O |
| B16 | I/O |
| B17 | I/O |
| B18 | I/O |
| B19 | I/O |
| B20 | I/O |
| B21 | I/O |
| B22 | GND |
| B23 | $V_{CCI}$ |
| B24 | GND |
| B25 | NC |
| C1 | NC |
| C2 | $V_{CCI}$ |
| C3 | GND |
| C4 | I/O |
| C5 | I/O |
| C6 | I/O |
| C7 | I/O |
| C8 | I/O |
| C9 | I/O |
| C10 | I/O |
| C11 | QCLKC, I/O |
| C12 | I/O |
| C13 | PRA, I/O |
| C14 | CLKA, I/O |
| C15 | I/O |
| C16 | I/O |
| C17 | I/O |
| C18 | I/O |
| C19 | I/O |
| C20 | I/O |
| C21 | I/O |
| C22 | I/O |
| C23 | GND |
| C24 | $V_{CCI}$ |
| C25 | NC |
| D1 | GND |
| D2 | GND |
| D3 | TDI |
| D4 | GND |
| D5 | I/O |
| D6 | I/O |
| D7 | I/O |
| D8 | I/O |
| D9 | I/O |
| D10 | I/O |
| D11 | I/O |
| D12 | I/O |
| D13 | I/O |
| D14 | QCLKD, I/O |
| D15 | I/O |
| D16 | I/O |
| D17 | I/O |
| D18 | I/O |
| D19 | I/O |
| D20 | I/O |
| D21 | I/O |
| D22 | $V_{CCI}$ |
| D23 | GND |
| D24 | GND |
| D25 | GND |
| E1 | I/O |
| E2 | I/O |
| E3 | I/O |
| E4 | I/O |
| E5 | TCK, I/O |
| E6 | I/O |

| 624-Pin CCGA | |
|---|---|
| Pin Number | RT54SX72S Function |
| E7 | I/O |
| E8 | I/O |
| E9 | I/O |
| E10 | I/O |
| E11 | I/O |
| E12 | $V_{CCA}$ |
| E13 | GND |
| E14 | I/O |
| E15 | I/O |
| E16 | I/O |
| E17 | I/O |
| E18 | I/O |
| E19 | I/O |
| E20 | I/O |
| E21 | I/O |
| E22 | I/O |
| E23 | I/O |
| E24 | I/O |
| E25 | I/O |
| F1 | I/O |
| F2 | $V_{CCI}$ |
| F3 | I/O |
| F4 | I/O |
| F5 | I/O |
| F6 | NC |
| F7 | NC |
| F8 | I/O |
| F9 | NC |
| F10 | NC |
| F11 | NC |
| F12 | NC |
| F13 | I/O |
| F14 | I/O |
| F15 | NC |
| F16 | GND |

| 624-Pin CCGA | |
|---|---|
| Pin Number | RT54SX72S Function |
| F17 | I/O |
| F18 | I/O |
| F19 | I/O |
| F20 | I/O |
| F21 | I/O |
| F22 | I/O |
| F23 | I/O |
| F24 | I/O |
| F25 | I/O |
| G1 | I/O |
| G2 | I/O |
| G3 | TMS |
| G4 | I/O |
| G5 | I/O |
| G6 | I/O |
| G7 | $V_{CCI}$ |
| G8 | NC |
| G9 | NC |
| G10 | NC |
| G11 | NC |
| G12 | NC |
| G13 | NC |
| G14 | NC |
| G15 | NC |
| G16 | NC |
| G17 | NC |
| G18 | GND |
| G19 | $V_{CCI}$ |
| G20 | I/O |
| G21 | I/O |
| G22 | I/O |
| G23 | I/O |
| G24 | I/O |
| G25 | I/O |
| H1 | I/O |

| 624-Pin CCGA | |
|---|---|
| Pin Number | RT54SX72S Function |
| H2 | I/O |
| H3 | I/O |
| H4 | I/O |
| H5 | I/O |
| H6 | I/O |
| H7 | I/O |
| H8 | $V_{CCI}$ |
| H9 | NC |
| H10 | NC |
| H11 | NC |
| H12 | NC |
| H13 | NC |
| H14 | NC |
| H15 | NC |
| H16 | NC |
| H17 | NC |
| H18 | $V_{CCI}$ |
| H19 | I/O |
| H20 | I/O |
| H21 | I/O |
| H22 | I/O |
| H23 | I/O |
| H24 | GND |
| H25 | I/O |
| J1 | I/O |
| J2 | I/O |
| J3 | I/O |
| J4 | I/O |
| J5 | I/O |
| J6 | I/O |
| J7 | NC |
| J8 | NC |
| J9 | $V_{CCI}$ |
| J10 | NC |
| J11 | NC |

| 624-Pin CCGA | |
|---|---|
| Pin Number | RT54SX72S Function |
| J12 | NC |
| J13 | NC |
| J14 | NC |
| J15 | NC |
| J16 | NC |
| J17 | $V_{CCI}$ |
| J18 | NC |
| J19 | NC |
| J20 | I/O |
| J21 | $V_{CCA}$ |
| J22 | I/O |
| J23 | I/O |
| J24 | I/O |
| J25 | I/O |
| K1 | I/O |
| K2 | GND |
| K3 | I/O |
| K4 | I/O |
| K5 | I/O |
| K6 | GND |
| K7 | NC |
| K8 | NC |
| K9 | NC |
| K10 | GND |
| K11 | GND |
| K12 | GND |
| K13 | GND |
| K14 | GND |
| K15 | GND |
| K16 | GND |
| K17 | NC |
| K18 | NC |
| K19 | NC |
| K20 | I/O |
| K21 | I/O |

| 624-Pin CCGA | |
|---|---|
| Pin Number | RT54SX72S Function |
| K22 | I/O |
| K23 | I/O |
| K24 | I/O |
| K25 | I/O |
| L1 | I/O |
| L2 | I/O |
| L3 | I/O |
| L4 | I/O |
| L5 | I/O |
| L6 | I/O |
| L7 | NC |
| L8 | NC |
| L9 | NC |
| L10 | GND |
| L11 | GND |
| L12 | GND |
| L13 | GND |
| L14 | GND |
| L15 | GND |
| L16 | GND |
| L17 | NC |
| L18 | NC |
| L19 | NC |
| L20 | I/O |
| L21 | I/O |
| L22 | I/O |
| L23 | I/O |
| L24 | I/O |
| L25 | I/O |
| M1 | I/O |
| M2 | I/O |
| M3 | I/O |
| M4 | I/O |
| M5 | GND |
| M6 | I/O |

| 624-Pin CCGA | |
|---|---|
| Pin Number | RT54SX72S Function |
| M7 | NC |
| M8 | NC |
| M9 | NC |
| M10 | GND |
| M11 | GND |
| M12 | GND |
| M13 | GND |
| M14 | GND |
| M15 | GND |
| M16 | GND |
| M17 | NC |
| M18 | NC |
| M19 | NC |
| M20 | I/O |
| M21 | GND |
| M22 | I/O |
| M23 | I/O |
| M24 | GND |
| M25 | I/O |
| N1 | I/O |
| N2 | I/O |
| N3 | I/O |
| N4 | I/O |
| N5 | $V_{CCA}$ |
| N6 | I/O |
| N7 | $V_{CCA}$ |
| N8 | NC |
| N9 | NC |
| N10 | GND |
| N11 | GND |
| N12 | GND |
| N13 | GND |
| N14 | GND |
| N15 | GND |
| N16 | GND |

| 624-Pin CCGA | |
|---|---|
| Pin Number | RT54SX72S Function |
| N17 | NC |
| N18 | NC |
| N19 | $V_{CCA}$ |
| N20 | I/O |
| N21 | $V_{CCA}$ |
| N22 | I/O |
| N23 | I/O |
| N24 | $V_{CCI}$ |
| N25 | I/O |
| P1 | I/O |
| P2 | I/O |
| P3 | I/O |
| P4 | I/O |
| P5 | I/O |
| P6 | I/O |
| P7 | NC |
| P8 | NC |
| P9 | NC |
| P10 | GND |
| P11 | GND |
| P12 | GND |
| P13 | GND |
| P14 | GND |
| P15 | GND |
| P16 | GND |
| P17 | NC |
| P18 | NC |
| P19 | NC |
| P20 | I/O |
| P21 | GND |
| P22 | I/O |
| P23 | I/O |
| P24 | I/O |
| P25 | I/O |
| R1 | I/O |

| 624-Pin CCGA | |
|---|---|
| Pin Number | RT54SX72S Function |
| R2 | I/O |
| R3 | I/O |
| R4 | TRST |
| R5 | I/O |
| R6 | GND |
| R7 | NC |
| R8 | NC |
| R9 | NC |
| R10 | GND |
| R11 | GND |
| R12 | GND |
| R13 | GND |
| R14 | GND |
| R15 | GND |
| R16 | GND |
| R17 | NC |
| R18 | NC |
| R19 | NC |
| R20 | I/O |
| R21 | I/O |
| R22 | I/O |
| R23 | I/O |
| R24 | I/O |
| R25 | I/O |
| T1 | I/O |
| T2 | I/O |
| T3 | I/O |
| T4 | I/O |
| T5 | I/O |
| T6 | I/O |
| T7 | I/O |
| T8 | NC |
| T9 | NC |
| T10 | GND |
| T11 | GND |

| 624-Pin CCGA | |
|---|---|
| Pin Number | RT54SX72S Function |
| T12 | GND |
| T13 | GND |
| T14 | GND |
| T15 | GND |
| T16 | GND |
| T17 | NC |
| T18 | NC |
| T19 | NC |
| T20 | GND |
| T21 | I/O |
| T22 | I/O |
| T23 | I/O |
| T24 | I/O |
| T25 | I/O |
| U1 | I/O |
| U2 | I/O |
| U3 | I/O |
| U4 | I/O |
| U5 | I/O |
| U6 | I/O |
| U7 | I/O |
| U8 | NC |
| U9 | $V_{CCI}$ |
| U10 | NC |
| U11 | NC |
| U12 | NC |
| U13 | NC |
| U14 | NC |
| U15 | NC |
| U16 | NC |
| U17 | $V_{CCI}$ |
| U18 | NC |
| U19 | NC |
| U20 | I/O |
| U21 | I/O |

| 624-Pin CCGA | |
|---|---|
| Pin Number | RT54SX72S Function |
| U22 | I/O |
| U23 | I/O |
| U24 | I/O |
| U25 | I/O |
| V1 | I/O |
| V2 | I/O |
| V3 | I/O |
| V4 | $V_{CCA}$ |
| V5 | I/O |
| V6 | I/O |
| V7 | GND |
| V8 | $V_{CCI}$ |
| V9 | NC |
| V10 | NC |
| V11 | NC |
| V12 | NC |
| V13 | NC |
| V14 | NC |
| V15 | NC |
| V16 | NC |
| V17 | NC |
| V18 | $V_{CCI}$ |
| V19 | I/O |
| V20 | I/O |
| V21 | I/O |
| V22 | $V_{CCA}$ |
| V23 | I/O |
| V24 | I/O |
| V25 | I/O |
| W1 | I/O |
| W2 | $V_{CCI}$ |
| W3 | I/O |
| W4 | I/O |
| W5 | I/O |
| W6 | I/O |

| 624-Pin CCGA | |
|---|---|
| Pin Number | RT54SX72S Function |
| W7 | VCCI |
| W8 | NC |
| W9 | NC |
| W10 | NC |
| W11 | NC |
| W12 | NC |
| W13 | NC |
| W14 | NC |
| W15 | NC |
| W16 | NC |
| W17 | NC |
| W18 | I/O |
| W19 | $V_{CCI}$ |
| W20 | I/O |
| W21 | I/O |
| W22 | I/O |
| W23 | I/O |
| W24 | I/O |
| W25 | I/O |
| Y1 | I/O |
| Y2 | I/O |
| Y3 | I/O |
| Y4 | I/O |
| Y5 | I/O |
| Y6 | I/O |
| Y7 | I/O |
| Y8 | I/O |
| Y9 | I/O |
| Y10 | I/O |
| Y11 | NC |
| Y12 | GND |
| Y13 | I/O |
| Y14 | NC |
| Y15 | GND |
| Y16 | I/O |

| 624-Pin CCGA | |
|---|---|
| Pin Number | RT54SX72S Function |
| Y17 | I/O |
| Y18 | I/O |
| Y19 | I/O |
| Y20 | I/O |
| Y21 | I/O |
| Y22 | I/O |
| Y23 | I/O |
| Y24 | GND |
| Y25 | I/O |
| AA1 | GND |
| AA2 | GND |
| AA3 | I/O |
| AA4 | I/O |
| AA5 | GND |
| AA6 | I/O |
| AA7 | I/O |
| AA8 | I/O |
| AA9 | I/O |
| AA10 | I/O |
| AA11 | I/O |
| AA12 | I/O |
| AA13 | $V_{CCA}$ |
| AA14 | GND |
| AA15 | I/O |
| AA16 | I/O |
| AA17 | I/O |
| AA18 | I/O |
| AA19 | I/O |
| AA20 | I/O |
| AA21 | GND |
| AA22 | I/O |
| AA23 | I/O |
| AA24 | I/O |
| AA25 | GND |
| AB1 | NC |

| 624-Pin CCGA | |
|---|---|
| **Pin Number** | **RT54SX72S Function** |
| AB2 | $V_{CCI}$ |
| AB3 | I/O |
| AB4 | GND |
| AB5 | I/O |
| AB6 | I/O |
| AB7 | I/O |
| AB8 | I/O |
| AB9 | I/O |
| AB10 | I/O |
| AB11 | I/O |
| AB12 | QCLKA, I/O |
| AB13 | I/O |
| AB14 | I/O |
| AB15 | I/O |
| AB16 | I/O |
| AB17 | I/O |
| AB18 | I/O |
| AB19 | I/O |
| AB20 | I/O |
| AB21 | TDO, I/O |
| AB22 | $V_{CCI}$ |
| AB23 | I/O |
| AB24 | $V_{CCI}$ |
| AB25 | NC |
| AC1 | NC |
| AC2 | I/O |
| AC3 | GND |
| AC4 | I/O |
| AC5 | I/O |
| AC6 | I/O |
| AC7 | I/O |
| AC8 | I/O |
| AC9 | I/O |
| AC10 | I/O |
| AC11 | I/O |

| 624-Pin CCGA | |
|---|---|
| **Pin Number** | **RT54SX72S Function** |
| AC12 | PRB, I/O |
| AC13 | I/O |
| AC14 | HCLK |
| AC15 | I/O |
| AC16 | I/O |
| AC17 | I/O |
| AC18 | I/O |
| AC19 | I/O |
| AC20 | I/O |
| AC21 | I/O |
| AC22 | I/O |
| AC23 | GND |
| AC24 | I/O |
| AC25 | NC |
| AD1 | NC |
| AD2 | GND |
| AD3 | $V_{CCI}$ |
| AD4 | GND |
| AD5 | I/O |
| AD6 | I/O |
| AD7 | I/O |
| AD8 | I/O |
| AD9 | I/O |
| AD10 | $V_{CCI}$ |
| AD11 | I/O |
| AD12 | I/O |
| AD13 | I/O |
| AD14 | I/O |
| AD15 | I/O |
| AD16 | GND |
| AD17 | I/O |
| AD18 | I/O |
| AD19 | I/O |
| AD20 | I/O |
| AD21 | I/O |

| 624-Pin CCGA | |
|---|---|
| **Pin Number** | **RT54SX72S Function** |
| AD22 | GND |
| AD23 | $V_{CCI}$ |
| AD24 | GND |
| AD25 | NC |
| AE1 | NC |
| AE2 | NC |
| AE3 | NC |
| AE4 | GND |
| AE5 | I/O |
| AE6 | I/O |
| AE7 | I/O |
| AE8 | I/O |
| AE9 | I/O |
| AE10 | I/O |
| AE11 | I/O |
| AE12 | I/O |
| AE13 | I/O |
| AE14 | QCLKB, I/O |
| AE15 | I/O |
| AE16 | I/O |
| AE17 | I/O |
| AE18 | I/O |
| AE19 | I/O |
| AE20 | I/O |
| AE21 | I/O |
| AE22 | GND |
| AE23 | NC |
| AE24 | NC |
| AE25 | NC |

# Datasheet Information

## List of Changes

The following table lists critical changes that were made to the current version of the document.

| Previous version | Changes in current version (v2.2) | Page |
|---|---|---|
| v2.1 | The "Ordering Information" was updated. | 1-ii |
| v2.0 | In Table 2-13, the $I_{OH}$ = –20µA and $I_{OL}$ = ±20µA. | 2-14 |
| Advanced v1.6 | Maximum user I/O in "RTSX-S Product Profile" was updated for the RT54SX72S. | 1-i |
| | Table 2-4 was updated. | 2-2 |
| | The "Power Dissipation" section is new. | 2-2 |
| | The "Thermal Characteristics" section is new. | 2-4 |
| | Table 2-8 was updated. | 2-5 |
| | The "Timing Model" was updated. | 2-6 |
| | The "User I/O" section is new. | 2-8 |
| | Table 2-11 and Table 2-12 were updated. | 2-12, 2-13 |
| | Table 2-14 and Table 2-15 were updated. | 2-14, 2-15 |
| | Table 2-18 and Table 2-19 were updated. | 2-18, 2-18 |
| | Table 2-22 and Table 2-23 were updated. | 2-21, 2-21 |
| | The "Module Specifications"section is new. | 2-22 |
| | The "Routing Specifications" section is new. | 2-27 |
| | The "Global Resources" section is new. | 2-29 |
| | QCLK timing data added to Table 2-26 and Table 2-27 | 2-30, 2-31 |
| | The "Other Architectural Features" section is new. | 2-35 |
| | Table 2-34 was updated. | 2-36 |
| | "208-Pin CQFP" pin table for RT54SX72S was updated. | 3-1 |
| | "256-Pin CQFP" pin table for RT54SX72S was updated. | 3-5 |
| | "624-Pin CCGA" pin table for RT54SX72S was updated. | 3-19 |

| Previous version | Changes in current version (v2.2) | Page |
|---|---|---|
| Advanced v1.5 | The "RTSX-S Product Profile" were updated. | page 1 |
| | The "Clock Resources" section was updated. | page 7 |
| | "I/O Modules" was updated. | page 10 |
| | The "RTSX-S Timing Model" figure was updated. | page 23 |
| | The "Input Buffer Delays" figure was updated. | page 24 |
| | The "RTSX-S Timing Model" section on page 23 was updated. | page 23 |
| | The Timing Characteristics were updated on the following pages. | 25–27, 31–32 |
| Advanced v1.4 | The "RTSX-S Product Profile" table on page 1 was updated. | page 1 |
| | The "Ordering Information" section on page 2 was updated. | page 2 |
| | The "Product Plan" table on page 2 was updated. | page 2 |
| | The "Ceramic Device Resources" table on page 2 was updated. | page 2 |
| | The "SEU Hardened DFF Description" section on page 3 was updated. | page 3 |
| | The "Power Cycling" section on page 12 is new. | page 12 |
| | The "Actel MIL-STD-883 Class B Product Flow" table on page 20 was updated. | page 20 |
| | The "Actel Extended Flow[1]" table on page 21 was updated. | page 21 |
| | The "256-Pin CCLG*" table on page 45 is new. | page 45 |
| Advanced v1.3 | On the CQ208 package for the RT54SX72S, pin 13, the function is I/O and not $V_{CCI}$. | page 37 |
| Advanced v1.2.3 | The "RTSX-S Product Profile" table on page 1 table has been updated. | page 1 |
| | The "Ceramic Device Resources" section on page 2 | page 2 |
| | The "Clock Resources" section on page 7 has been updated. | page 7 |
| | Table 1 on page 9 is new. | page 7 |
| | The "I/O Modules" section on page 10 and have been updated. | page 10 |
| | Table 2 on page 10 has been updated. | page 10 |
| | The "Hot Swapping" section on page 10 has been updated. | page 10 |
| | Table 3 on page 11 is new. | page 11 |
| | Table 4 on page 11 has been updated. | page 11 |
| | The "Development Tool Support" section on page 13 has been updated. | page 13 |
| | The "Design Considerations" section on page 14 has been updated. | page 14 |
| | The "Pin Description" section on page 37 has been updated. | page 37 |
| | The CG624 (Bottom View) on page 50 is new. | page 50 |
| Advanced v1.1.2 | The "DC Specifications (3.3V PCI Operation)" section on page 18 was updated. | page 18 |

| Previous version | Changes in current version (v2.2) | Page |
|---|---|---|
| Advanced v0.3 | The "Programmable Interconnect Element" section on page 5 has been updated. | page 5 |
| | The "I/O Modules" section on page 10 and Table 2 | page 10 |
| | The "Boundary Scan Testing (BST)" section on page 12 has been updated. | page 12 |
| | The "Dedicated Mode" section on page 12 has been updated. | page 12 |
| | The "Flexible Mode" section on page 12 has been updated. | page 12 |
| | Table 7 on page 13 was changed. | page 13 |
| | The "TRST Pin" section on page 13 has been updated. | page 13 |
| | The "Probing Capabilities" section on page 13 has been updated. | page 13 |
| | Table 8 on page 13 is new. | page 13 |
| | The "Development Tool Support" section on page 13 was changed. | page 13 |
| | The "Recommended Operating Conditions" section on page 14 has been updated. | page 14 |
| | The "3.3V LVTTL and 5V TTL Electrical Specifications" table on page 15 was changed. | page 15 |
| | The "5V CMOS Electrical Specifications" table on page 15 is new. | page 15 |
| | The "5V PCI Compliance for the RTSX-S Family" table on page 16 | page 16 |
| | The "Actel MIL-STD-883 Class B Product Flow" table on page 20 has been updated. | page 20 |
| | The "Actel Extended Flow[1]" table on page 21 has been updated. | page 21 |
| | The "RTSX-S Timing Model" table on page 23 and the "Hard-Wired Clock" equation were updated. | page 23 |
| | The "Pin Description" section on page 37 was updated. | page 37 |
| Advanced v0.2 | The "Product Plan" table on page 2 has been updated. | 2 |
| | The "Clock Resources" table on page 7 has been updated. | 8 |
| | The "Performance" table on page 9, "I/O Modules" table on page 10, "Hot Swapping" table on page 10, "Boundary Scan Testing (BST)" table on page 12, "TRST Pin" table on page 13, "Development Tool Support" table on page 13, and "RTSX-S Probe Circuit Control Pins" table on page 13 have changed. | 9-11 |
| | The "Absolute Maximum Ratings*" table on page 14 and "Recommended Operating Conditions" table on page 14 have been updated. | 11 |
| | The "3.3V LVTTL and 5V TTL Electrical Specifications" table on page 15 and "5V CMOS Electrical Specifications" table on page 15 are new. | 12 |
| | The "RTSX-S Timing Model" on page 23 was updated. | 22 |
| | New slew rates were added to the "RT54SX32S Timing Characteristics" on page 30, page 31, and page 36. | 29, 30, 35 |

| Previous version | Changes in current version (v2.2) | Page |
|---|---|---|
| Advanced v0.1.1 | The TRSTB pin was incorrectly named and changed to TRST. | All |
| | In the "RTSX-S Product Profile" table on page 1, the User I/Os have changed. | 1 |
| | In the "Ceramic Device Resources" table on page 2, the User I/Os have changed. | 2 |
| | The Clock Networks section has changed to "Clock Resources" table on page 7. | 8 |
| | The "TRST Pin" table on page 13 has changed. | 10 |
| | The"Design Considerations" table on page 14 Design Considerations section has changed. | 11 |
| | In the "2.5V/3.3V/5V Operating Conditions" table on page 14 section, the "Absolute Maximum Ratings*" table on page 14 changed. The $I_{IO}$ row containing the I/O Source Sink Current was deleted. | 12 |
| | Equation 2 in the "Junction Temperature ($T_J$)" table on page 22 was corrected. | 15 |
| | Note that the "Package Characteristics and Mechanical Drawings" section has been eliminated from the data sheet. The mechanical drawings are now contained in a separate document, "Package Characteristics and Mechanical Drawings," available on the Actel web site. | |

# Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definitions of these categories are as follows:

## Product Brief

The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

## Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

## Unmarked (production)

This datasheet version contains information that is considered to be final.

## Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

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