SDRAM

1M x 16 SDRAM

512K x 16bit x 2Banks Synchronous DRAM

FEATURES

Fast access time: 5/6/7 ns

- Fast clock rate: 200/166/143 MHz
- Self refresh mode: standard and low power
- Internal pipelined architecture
- 512K word x 16-bit x 2-bank
- Programmable Mode registers
  - CAS# Latency: 1, 2, or 3
  - Burst Length: 1, 2, 4, 8, or full page
  - Burst Type: interleaved or linear burst
  - Burst stop function
- Individual byte controlled by LDQM and UDQM
- Auto Refresh and Self Refresh
- 4096 refresh cycles/64ms
- CKE power down mode
- JEDEC standard +3.3V±0.3V power supply
- Interface: LVTTL
- 50-pin 400 mil plastic TSOP II package
- 60-ball, 6.4x10.1mm VFBGA package
- Lead Free Package available for both TSOP II and VFBGA
- Low Operating Current for T431616E

Key Specifications

T431616D/E		-5/6/7
t_{CK3}	Clock Cycle time(min.)	**5/6/7ns**
t_{RAS}	Row Active time(max.)	**35/42/42 ns**
t_{AC3}	Access time from CLK(max.)	**4.5/5/5.5 ns**
t_{RC}	Row Cycle time(min.)	**48/54/63 ns**

GRNERAL DESCRIPTION

The T431616D/E SDRAM is a high-speed CMOS synchronous DRAM containing 16 Mbits. It is internally configured as a dual 512K word x 16 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 512K x 16 bit banks is organized as 2048 rows by 256 columns by 16 bits. Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of a BankActivate command which is then followed by a Read or Write command.

The T431616D/E provides for programmable Read or Write burst lengths of 1, 2, 4, 8, or full page, with a burst termination option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The refresh functions, either Auto or Self Refresh are easy to use. By having a programmable mode register, the system can choose the most suitable modes to maximize its performance. These devices are well suited for applications requiring high memory bandwidth and particularly well suited to high performance PC applications

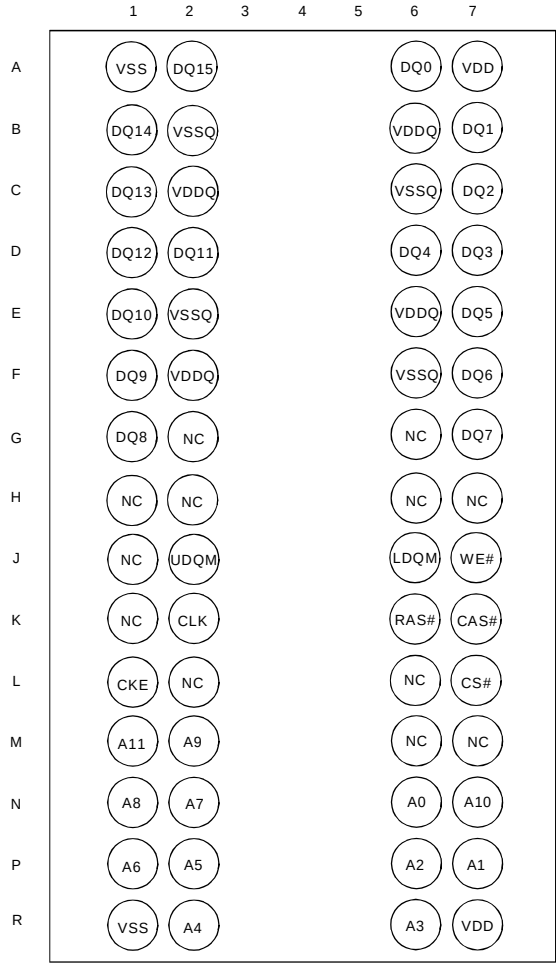
ORDERING INFORMATION

Part Number	Frequency	Package
T431616D-5S/C	200MHz	TSOP II / VFBGA
T431616D-5SG/CG	200MHz	TSOP II / VFBGA
T431616D-6S/C	166MHz	TSOP II / VFBGA
T431616D-6SG/CG	166MHz	TSOP II / VFBGA
T431616D-7S/C	143MHz	TSOP II / VFBGA
T431616D-7SG/CG	143MHz	TSOP II / VFBGA
T431616E-7S/C	143MHz	TSOP II / VFBGA
T431616E-7SG/CG	143MHz	TSOP II / VFBGA

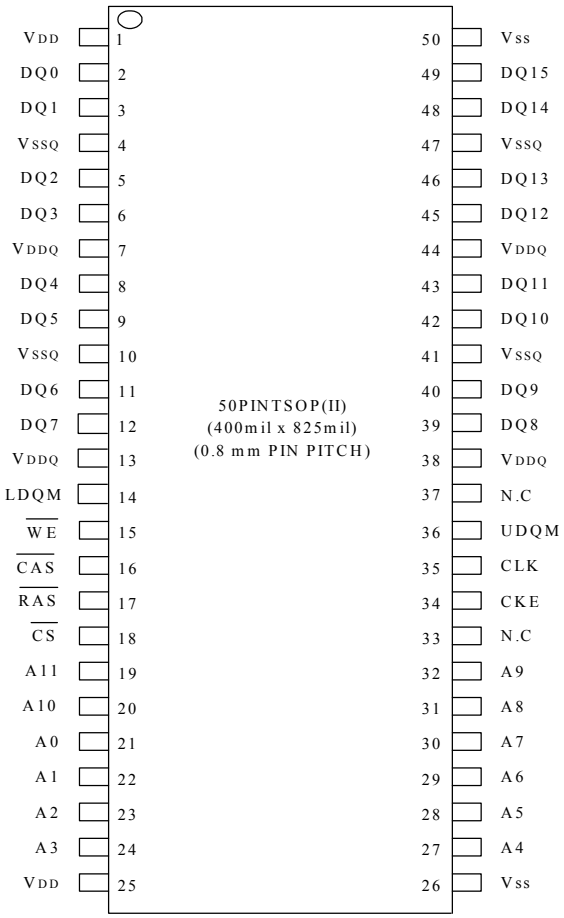
G : indicates Lead Free Package

PIN ARRANGEMENT

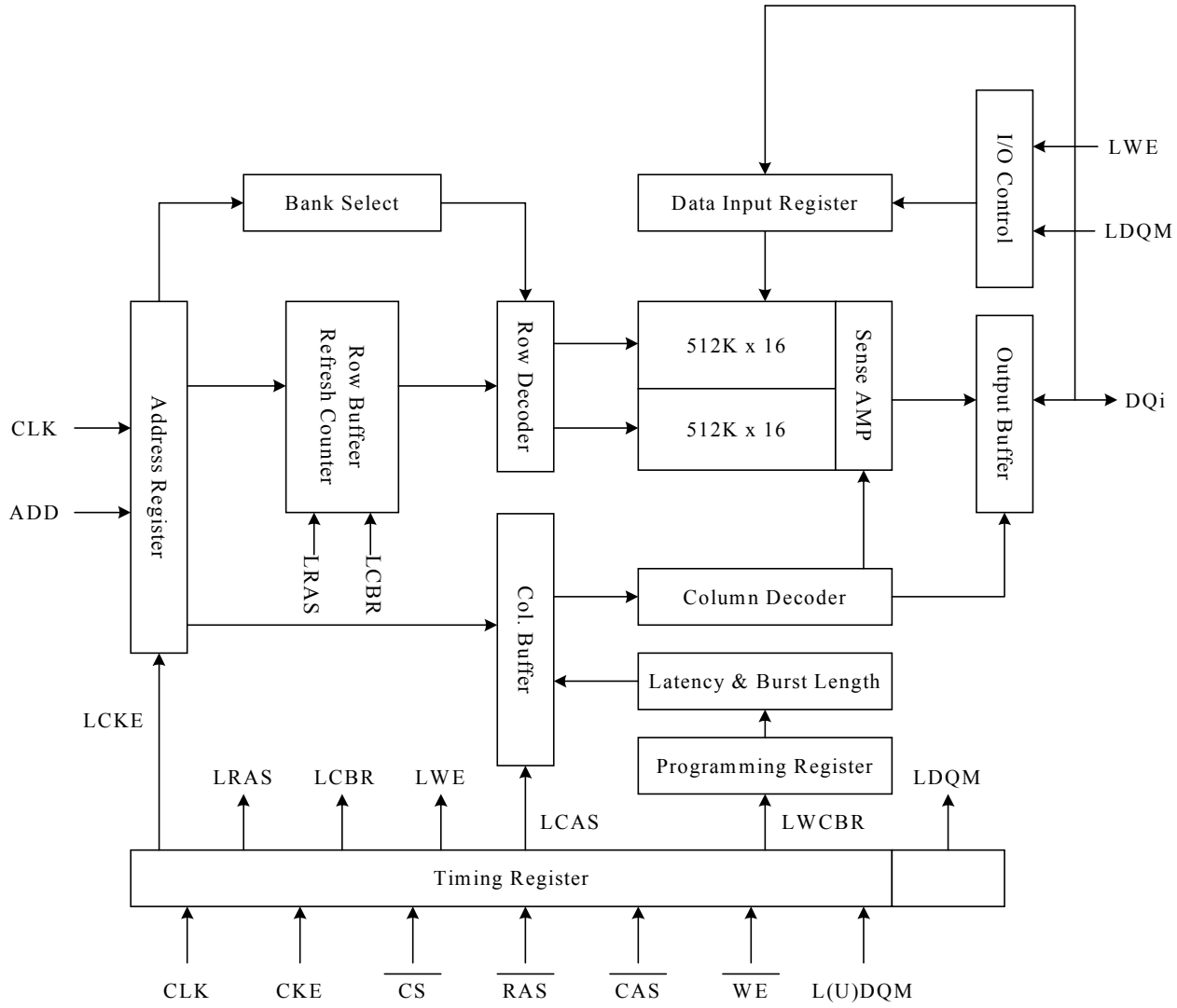
BGA (Top View)



TSOP-II (Top View)



BLOCK DIAGRAM



Pin Descriptions (Table 1. Pin Details of T431616D/E)

Symbol	Type	Description
CLK	Input	**Clock:** CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
CKE	Input	**Clock Enable:** CKE activates(HIGH) and deactivates(LOW) the CLK signal. If CKE goes low synchronously with clock(set-up and hold time same as other inputs), the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. When both banks are in the idle state, deactivating the clock controls the entry to the Power Down and Self Refresh modes. CKE is synchronous except after the device enters Power Down and Self Refresh modes, where CKE becomes asynchronous until exiting the same mode. The input buffers, including CLK, are disabled during Power Down and Self Refresh modes, providing low standby power.
A11	Input	**Bank Select:** A11(BS) defines to which bank the BankActivate, Read, Write, or BankPrecharge command is being applied.
A0-A10	Input	**Address Inputs:** A0-A10 are sampled during the BankActivate command (row address A0-A10) and Read/Write command (column address A0-A7 with A10 defining Auto Precharge) to select one location out of the 256K available in the respective bank. During a Precharge command, A10 is sampled to determine if both banks are to be precharged (A10 = HIGH). The address inputs also provide the op-code during a Mode Register Set command.
CS#	Input	**Chip Select:** CS# enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when CS# is sampled HIGH. CS# provides for external bank selection on systems with multiple banks. It is considered part of the command code.
RAS#	Input	**Row Address Strobe:** The RAS# signal defines the operation commands in conjunction with the CAS# and WE# signals and is latched at the positive edges of CLK. When RAS# and CS# are asserted "LOW" and CAS# is asserted "HIGH," either the BankActivate command or the Precharge command is selected by the WE# signal. When the WE# is asserted "HIGH," the BankActivate command is selected and the bank designated by BS is turned on to the active state. When the WE# is asserted "LOW," the Precharge command is selected and the bank designated by BS is switched to the idle state after the precharge operation.
CAS#	Input	**Column Address Strobe:** The CAS# signal defines the operation commands in conjunction with the RAS# and WE# signals and is latched at the positive edges of CLK. When RAS# is held "HIGH" and CS# is asserted "LOW," the column access is started by asserting CAS# "LOW." Then, the Read or Write command is selected by asserting WE# "LOW" or "HIGH."
WE#	Input	**Write Enable:** The WE# signal defines the operation commands in conjunction with the RAS# and CAS# signals and is latched at the positive edges of CLK. The WE# input is used to select the BankActivate or Precharge command and Read or Write command.
LDQM, UDQM	Input	**Data Input/Output Mask:** LDQM and UDQM are byte specific, nonpersistent I/O buffer controls. The I/O buffers are placed in a high-z state when LDQM/UDQM is sampled HIGH. Input data is masked when LDQM/UDQM is sampled HIGH during a write cycle. Output data is masked (two-clock latency) when LDQM/UDQM is sampled HIGH during a read cycle. UDQM masks DQ15-DQ8, and LDQM masks DQ7-DQ0.
DQ0-DQ15	Input/Output	**Data I/O:** The DQ0-15 input and output data are synchronized with the positive edges of CLK. The I/Os are byte-maskable during Reads and Writes.
NC	-	**No Connect:** These pins should be left unconnected.
V_{DDQ}	Supply	**DQ Power:** Provide isolated power to DQs for improved noise immunity. (3.3V$\pm$ 0.3V)
V_{SSQ}	Supply	**DQ Ground:** Provide isolated ground to DQs for improved noise immunity. (0 V)
V_{DD}	Supply	**Power Supply:** +3.3V $\pm$ 0.3V
V_{SS}	Supply	**Ground**

Operation Mode

Fully synchronous operations are performed to latch the commands at the positive edges of CLK. Table 2 shows the truth table for the operation commands.

Table 2. Truth Table (Note (1), (2))

Command	State	CKE_{n-1}	CKE_n	DQM(6)	A11	A10	A0-9	CS#	RAS#	CAS#	WE#
BankActivate	Idle(3)	H	X	X	V	V	V	L	L	H	H
BankPrecharge	Any	H	X	X	V	L	X	L	L	H	L
PrechargeAll	Any	H	X	X	X	H	X	L	L	H	L
Write	Active(3)	H	X	X	V	L	V	L	H	L	L
Write and AutoPrecharge	Active(3)	H	X	X	V	H	V	L	H	L	L
Read	Active(3)	H	X	X	V	L	V	L	H	L	H
Read and Autoprecharge	Active(3)	H	X	X	V	H	V	L	H	L	H
Mode Register Set	Idle	H	X	X	V	V	V	L	L	L	L
No-Operation	Any	H	X	X	X	X	X	L	H	H	H
Burst Stop	Active(4)	H	X	X	X	X	X	L	H	H	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
AutoRefresh	Idle	H	H	X	X	X	X	L	L	L	H
SelfRefresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
SelfRefresh Exit	Idle (SelfRefresh)	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Clock Suspend Mode Entry	Active	H	L	X	X	X	X	X	X	X	X
Power Down Mode Entry	Any(5)	H	L	X	X	X	X	H	X	X	X
								L	H	H	H
Clock Suspend Mode Exit	Active	L	H	X	X	X	X	X	X	X	X
Power Down Mode Exit	Any (PowerDown)	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Data Write/Output Enable	Active	H	X	L	X	X	X	X	X	X	X
Data Mask/Output Disable	Active	H	X	H	X	X	X	X	X	X	X

Note: 1. V=Valid X=Don't Care L=Low level H=High level
2. CKE_n signal is input level when commands are provided.
CKE_{n-1} signal is input level one clock cycle before the commands are provided.
3. These are states of bank designated by BS signal.
4. Device state is 1, 2, 4, 8, and full page burst operation.
5. Power Down Mode can not enter in the burst operation.
When this command is asserted in the burst cycle, device state is clock suspend mode.
6. LDQM and UDQM

Commands

1 BankPrecharge command

(RAS# = "L", CAS# = "H", WE# = "L", A11 = “V”, A10 = "L", A0-A9 = Don't care)

The BankPrecharge command precharges the bank disignated by A11 signal. The precharged bank is switched from the active state to the idle state. This command can be asserted anytime after t_{RAS}(min.) is satisfied from the BankActivate command in the desired bank. The maximum time any bank can be active is specified by t_{RAS}(max.). Therefore, the precharge function must be performed in any active bank within t_{RAS}(max.). At the end of precharge, the precharged bank is still in the idle state and is ready to be activated again.

2 PrechargeAll command

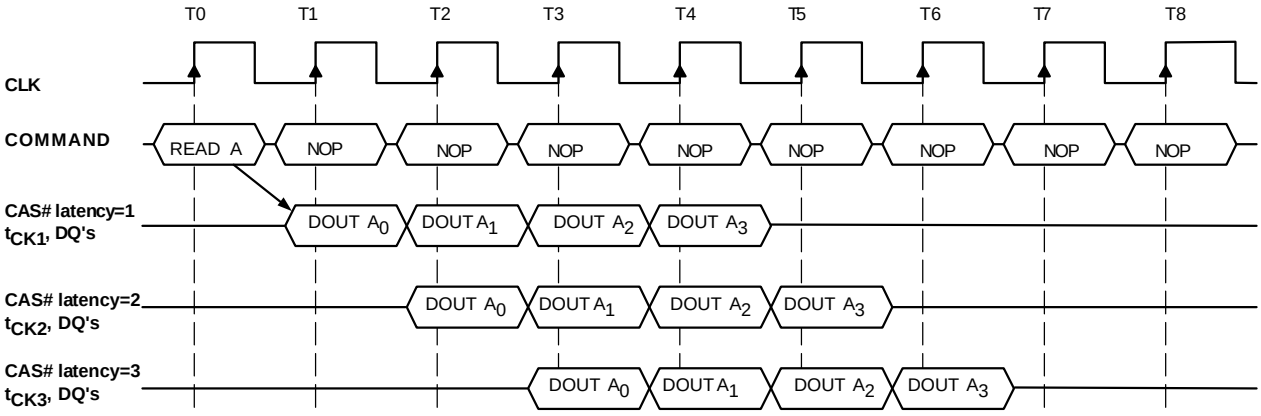
(RAS# = "L", CAS# = "H", WE# = "L", A11 = Don't care, A10 = "H", A0-A9 = Don't care)

The PrechargeAll command precharges both banks simultaneously and can be issued even if both banks are not in the active state. Both banks are then switched to the idle state.

3 Read command

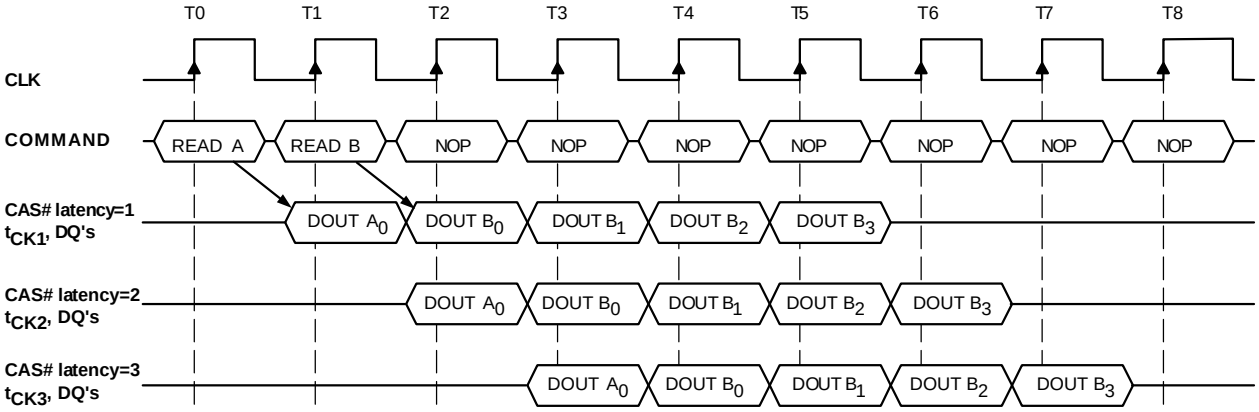
(RAS# = "H", CAS# = "L", WE# = "H", A11= “V”, A9 = "L", A0-A7 = Column Address)

The Read command is used to read a burst of data on consecutive clock cycles from an active row in an active bank. The bank must be active for at least t_{RCD}(min.) before the Read command is issued. During read bursts, the valid data-out element from the starting column address will be available following the CAS# latency after the issue of the Read command. Each subsequent data-out element will be valid by the next positive clock edge (refer to the following figure). The DQs go into high-impedance at the end of the burst unless other command is initiated. The burst length, burst sequence, and CAS# latency are determined by the mode register, which is already programmed. A full-page burst will continue until terminated (at the end of the page it will wrap to column 0 and continue).



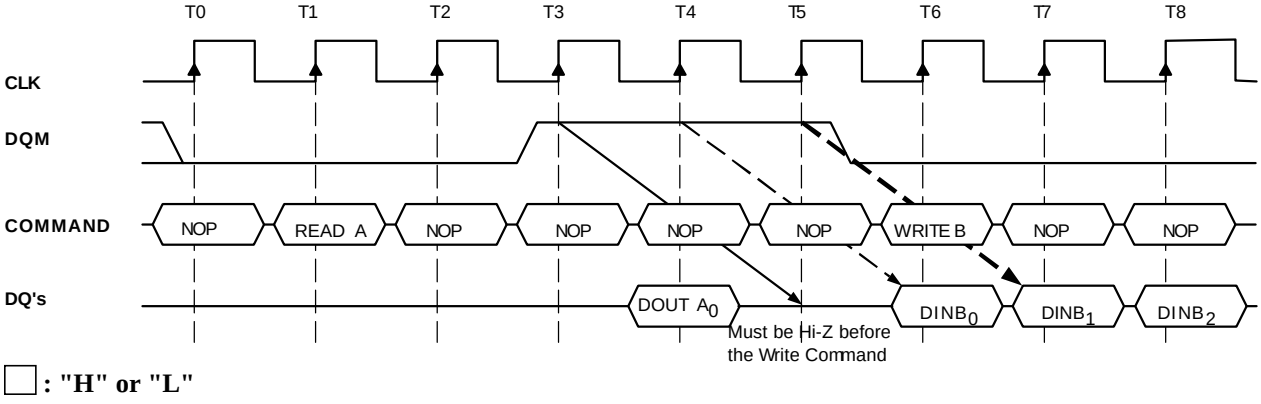
Burst Read Operation(Burst Length = 4, CAS# Latency = 1, 2, 3)

The read data appears on the DQs subject to the values on the LDQM/UDQM inputs two clocks earlier (i.e. LDQM/UDQM latency is two clocks for output buffers). A read burst without the auto precharge function may be interrupted by a subsequent Read or Write command to the same bank or the other active bank before the end of the burst length. It may be interrupted by a BankPrecharge/ PrechargeAll command to the same bank too. The interrupt coming from the Read command can occur on any clock cycle following a previous Read command (refer to the following figure).

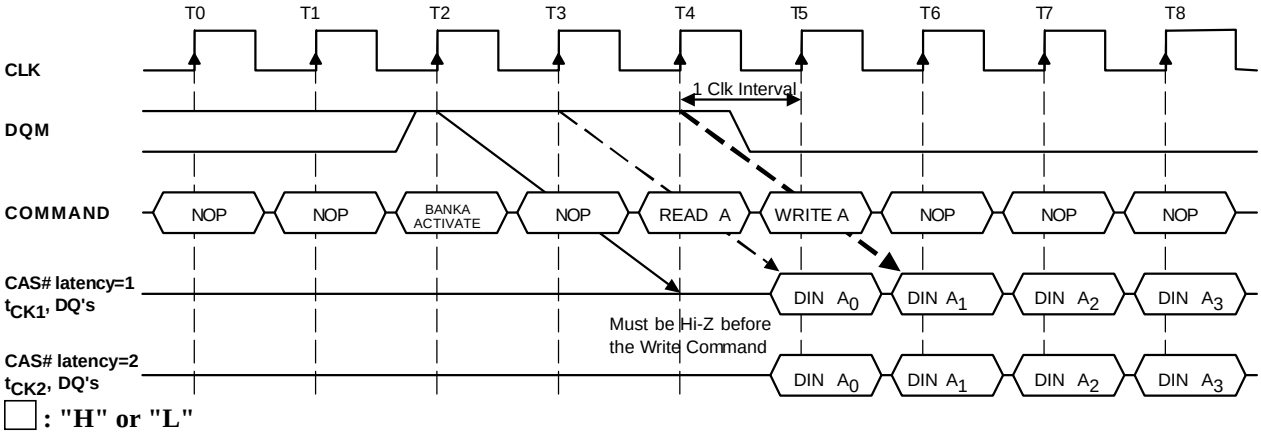


Read Interrupted by a Read (Burst Length = 4, CAS# Latency = 1, 2, 3)

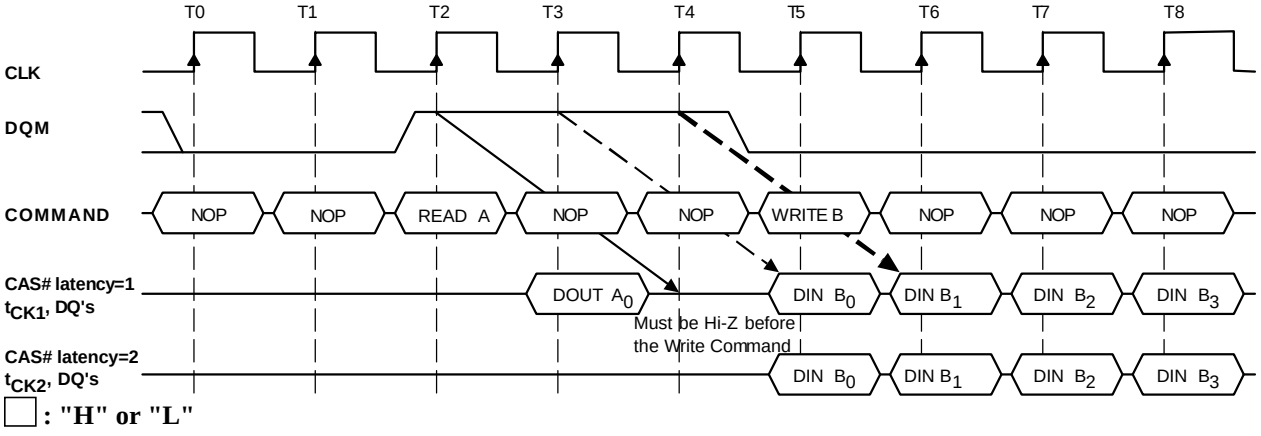
The LDQM/UDQM inputs are used to avoid I/O contention on the DQ pins when the interrupt comes from a Write command. The LDQM/UDQM must be asserted (HIGH) at least two clocks prior to the Write command to suppress data-out on the DQ pins. To guarantee the DQ pins against I/O contention, a single cycle with high-impedance on the DQ pins must occur between the last read data and the Write command (refer to the following three figures). If the data output of the burst read occurs at the second clock of the burst write, the LDQM/UDQM must be asserted (HIGH) at least one clock prior to the Write command to avoid internal bus contention.



Read to Write Interval (Burst Length ≥ 4, CAS# Latency = 3)

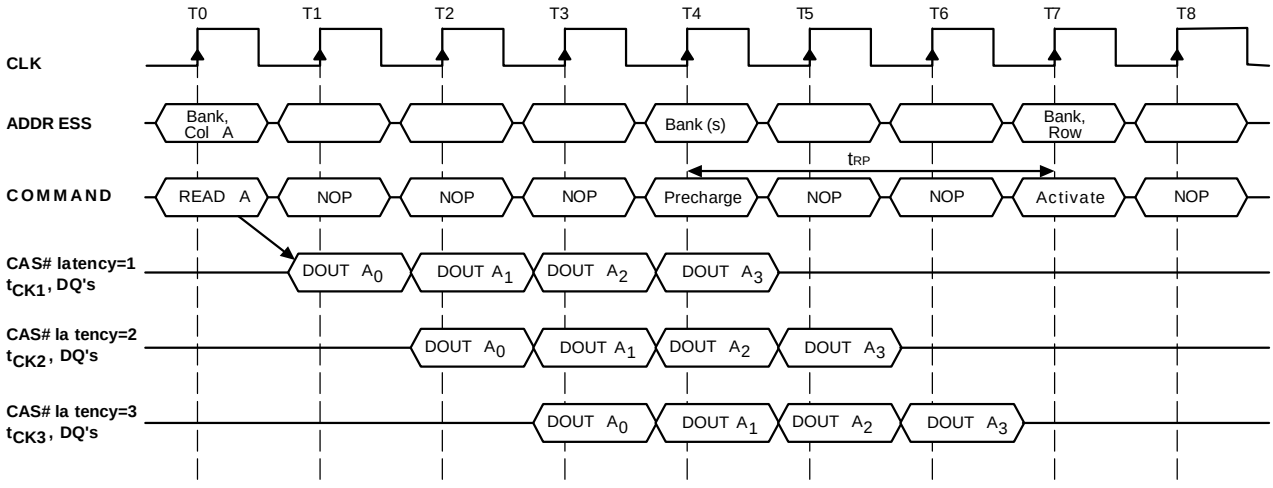


Read to Write Interval (Burst Length ≥ 4, CAS# Latency = 1, 2)



Read to Write Interval (Burst Length ≥ 4, CAS# Latency = 1, 2)

A read burst without the auto precharge function may be interrupted by a BankPrecharge/ PrechargeAll command to the same bank. The following figure shows the optimum time that BankPrecharge/ PrechargeAll command is issued in different CAS# latency.



Read to Precharge (CAS# Latency = 1, 2, 3)

4 Read and AutoPrecharge command

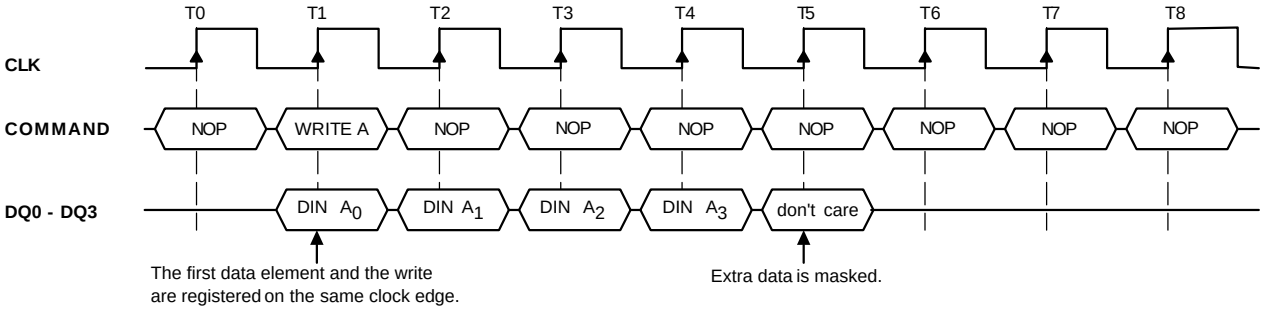
(RAS# = "H", CAS# = "L", WE# = "H", A11 = "V", A10 = "H", A0-A7 = Column Address)

The Read and AutoPrecharge command automatically performs the precharge operation after the read operation. Once this command is given, any subsequent command cannot occur within a time delay of {t_{RP}(min.) + burst length}. At full-page burst, only the read operation is performed in this command and the auto precharge function is ignored.

5 Write command

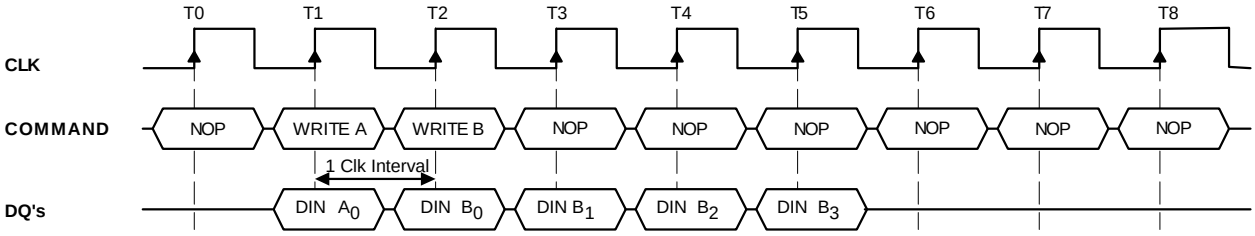
(RAS# = "H", CAS# = "L", WE# = "L", A11 = "V", A10 = "L", A0-A7 = Column Address)

The Write command is used to write a burst of data on consecutive clock cycles from an active row in an active bank. The bank must be active for at least t_{RCD}(min.) before the Write command is issued. During write bursts, the first valid data-in element will be registered coincident with the Write command. Subsequent data elements will be registered on each successive positive clock edge (refer to the following figure). The DQs remain with high-impedance at the end of the burst unless another command is initiated. The burst length and burst sequence are determined by the mode register, which is already programmed. A full-page burst will continue until terminated (at the end of the page it will wrap to column 0 and continue).



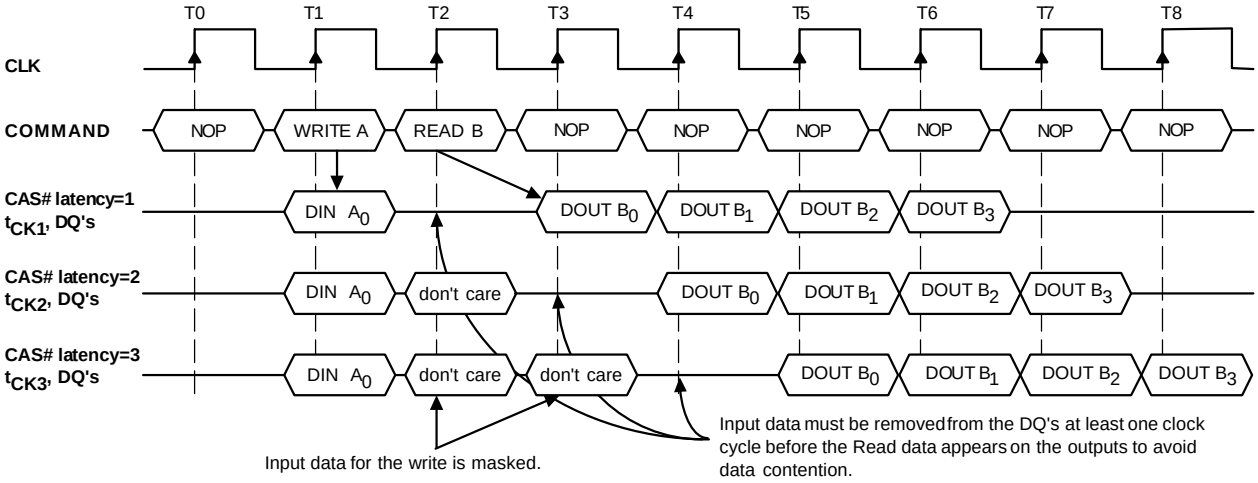
Burst Write Operation (Burst Length = 4, CAS# Latency = 1, 2, 3)

A write burst without the auto precharge function may be interrupted by a subsequent Write, BankPrecharge/PrechargeAll, or Read command before the end of the burst length. An interrupt coming from Write command can occur on any clock cycle following the previous Write command (refer to the following figure).



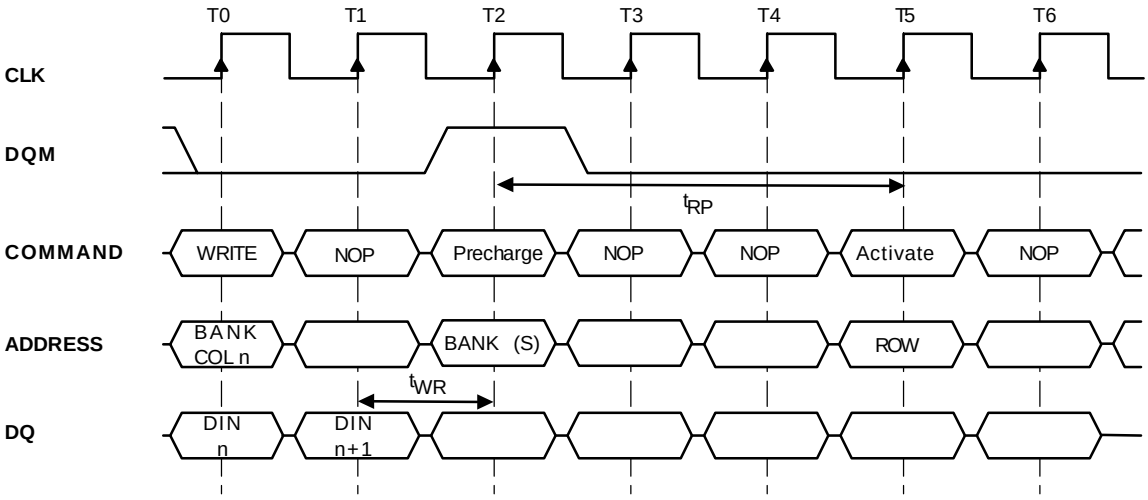
Write Interrupted by a Write (Burst Length = 4, CAS# Latency = 1, 2, 3)

The Read command that interrupts a write burst without auto precharge function should be issued one cycle after the clock edge in which the last data-in element is registered. In order to avoid data contention, input data must be removed from the DQs at least one clock cycle before the first read data appears on the outputs (refer to the following figure). Once the Read command is registered, the data inputs will be ignored and writes will not be executed.



Write Interrupted by a Read (Burst Length = 4, CAS# Latency = 1, 2, 3)

The BankPrecharge/PrechargeAll command that interrupts a write burst without the auto precharge function should be issued *m* cycles after the clock edge in which the last data-in element is registered, where *m* equals t_{WR}/t_{CK} rounded up to the next whole number. In addition, the LDQM/UDQM signals must be used to mask input data, starting with the clock edge following the last data-in element and ending with the clock edge on which the BankPrecharge/PrechargeAll command is entered (refer to the following figure).



: don't care

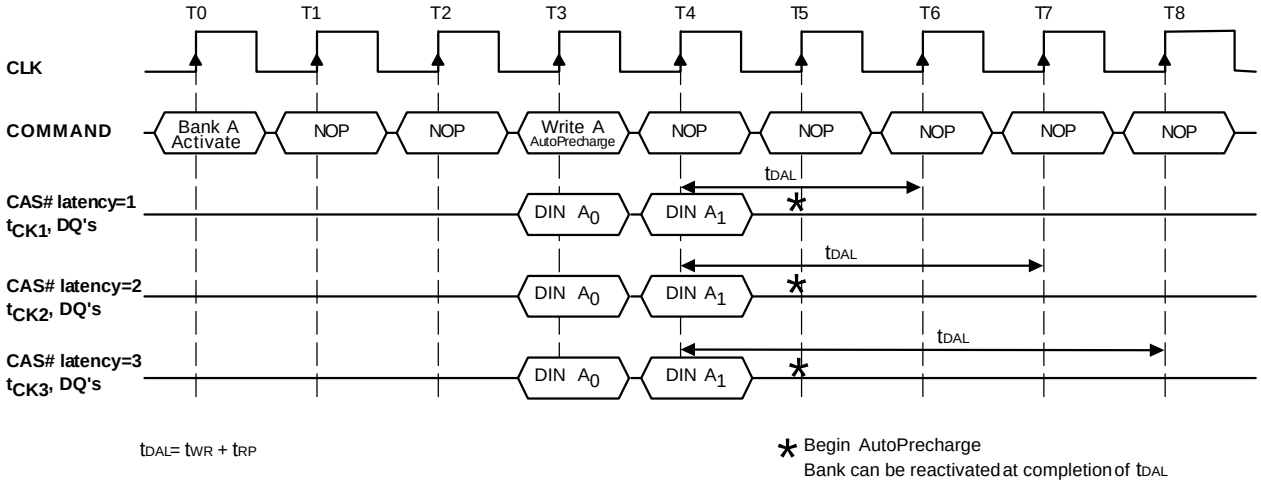
Note: The LDQM/UDQM can remain low in this example if the length of the write burst is 1 or 2.

Write to Precharge

6 Write and AutoPrecharge command (refer to the following figure)

(RAS# = "H", CAS# = "L", WE# = "L", A11 = "V", A10 = "H", A0-A7 = Column Address)

The Write and AutoPrecharge command performs the precharge operation automatically after the write operation. Once this command is given, any subsequent command can not occur within a time delay of {(burst length -1) + t_{WR} + t_{RP}(min.)}. At full-page burst, only the write operation is performed in this command and the auto precharge function is ignored.

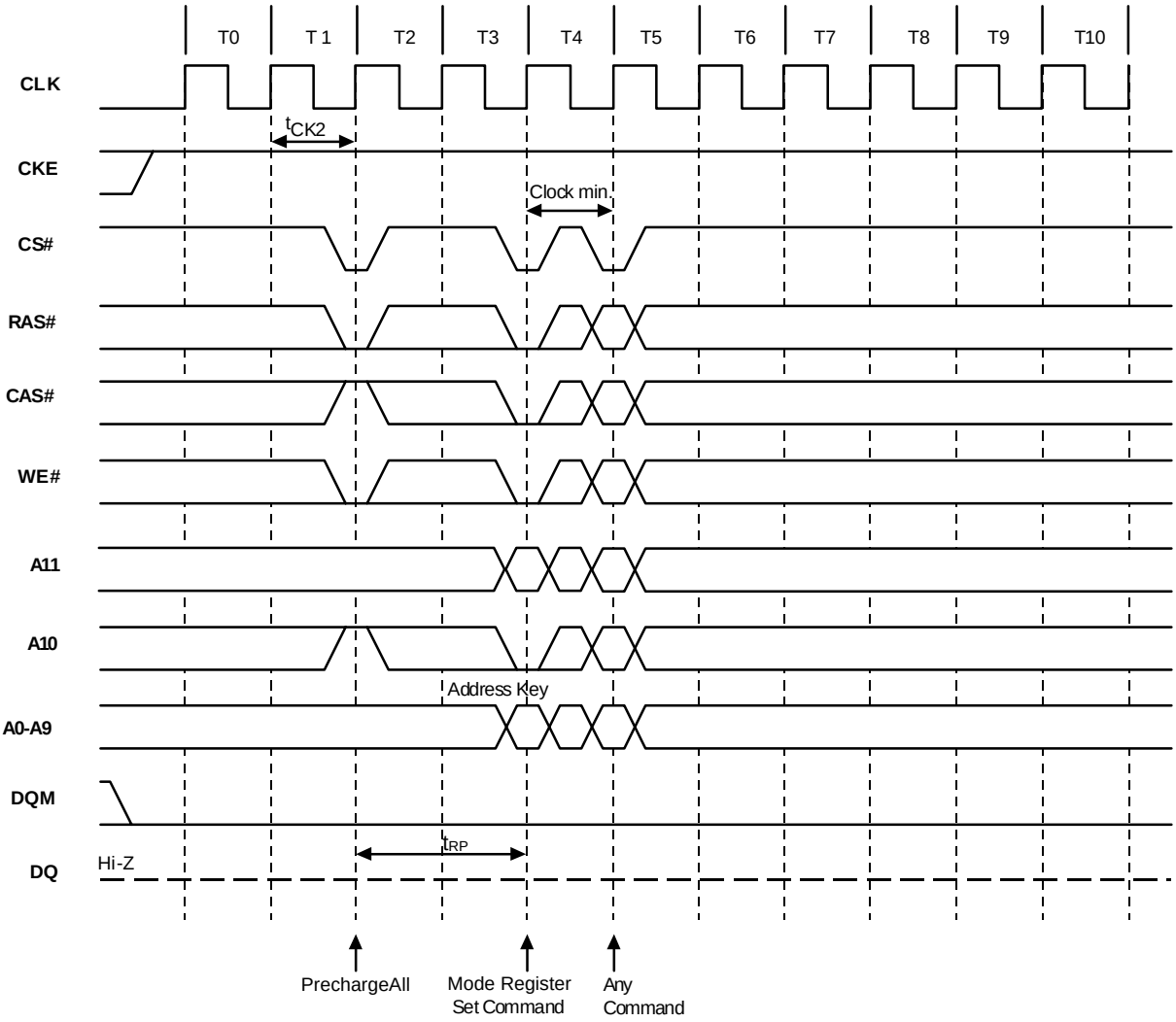


Burst Write with Auto-Precharge (Burst Length = 2, CAS# Latency = 1, 2, 3)

7 Mode Register Set command

(RAS# = "L", CAS# = "L", WE# = "L", A11 = "V", A10 = "V", A0-A9 = Register Data)

The mode register stores the data for controlling the various operating modes of SDRAM. The Mode Register Set command programs the values of CAS# latency, Addressing Mode and Burst Length in the Mode register to make SDRAM useful for a variety of different applications. The default values of the Mode Register after power-up are undefined; therefore this command must be issued at the power-up sequence. The state of pins A0~A9 and A11 in the same cycle is the data written to the mode register. One clock cycle is required to complete the write in the mode register (refer to the following figure). The contents of the mode register can be changed using the same command and the clock cycle requirements during operation as long as both banks are in the idle state.



Mode Register Set Cycle (CAS# Latency = 1, 2, 3)

The mode register is divided into various fields depending on functionality.

- Burst Length Field (A2~A0)

  This field specifies the data length of column access using the A2~A0 pins and selects the Burst Length to be 1, 2, 4, 8, or full page.

A2	A1	A0	Burst Length
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Full Page

- Addressing Mode Select Field (A3)

  The Addressing Mode can be one of two modes, Interleave Mode or Sequential Mode. Sequential Mode supports burst length of 1, 2, 4, 8, or full page, but Interleave Mode only supports burst length of 4 and 8.

A3	Addressing Mode
0	Sequential
1	Interleave

--- Addressing Sequence of Sequential Mode

An internal column address is performed by increasing the address from the column address which is input to the device. The internal column address is varied by the Burst Length as shown in the following table. When the value of column address, (n + m), in the table is larger than 255, only the least significant 8 bits are effective.

Data n	0	1	2	3	4	5	6	7	-	255	256	257	-
Column Address	n	n+1	n+2	n+3	n+4	n+5	n+6	n+7	-	n+255	n	n+1	-
Burst Length	2 words:												
	4 words:												
	8 words:												
	Full Page: Column address is repeated until terminated.												

--- Addressing Sequence of Interleave Mode

A column access is started in the input column address and is performed by inverting the address bits in the sequence shown in the following table.

Data n	Column Address								Burst Length	
Data 0	A7	A6	A5	A4	A3	A2	A1	A0	4 words	8 words
Data 1	A7	A6	A5	A4	A3	A2	A1	A0#		
Data 2	A7	A6	A5	A4	A3	A2	A1#	A0		
Data 3	A7	A6	A5	A4	A3	A2	A1#	A0#		
Data 4	A7	A6	A5	A4	A3	A2#	A1	A0		
Data 5	A7	A6	A5	A4	A3	A2#	A1	A0#		
Data 6	A7	A6	A5	A4	A3	A2#	A1#	A0		
Data 7	A7	A6	A5	A4	A3	A2#	A1#	A0#		

- CAS# Latency Field (A6~A4)

  This field specifies the number of clock cycles from the assertion of the Read command to the first read data. The minimum whole value of CAS# Latency depends on the frequency of CLK. The minimum whole value satisfying the following formula must be programmed into this field.

  $t_{CAC}(min) \leq$ CAS# Latency X t_{CK}

A6	A5	A4	CAS# Latency
0	0	0	Reserved
0	0	1	1 clock
0	1	0	2 clocks
0	1	1	3 clocks
1	X	X	Reserved

- Test Mode field (A8~A7)

  These two bits are used to enter the test mode and must be programmed to "00" in normal operation.

A8	A7	Test Mode
0	0	normal mode
0	1	Vendor Use Only
1	X	Vendor Use Only

- Single Write Mode (A9)

  This bit is used to select the write mode. When the BS bit is "0", the Burst-Read-Burst-Write mode is selected. When the BS bit is "1", the Burst-Read-Single-Write mode is selected.

A9	Single Write Mode
0	Burst-Read-Burst-Write
1	Burst-Read-Single-Write

Note: A10 and A11 should stay “L” during mode set cycle.

8 No-Operation command

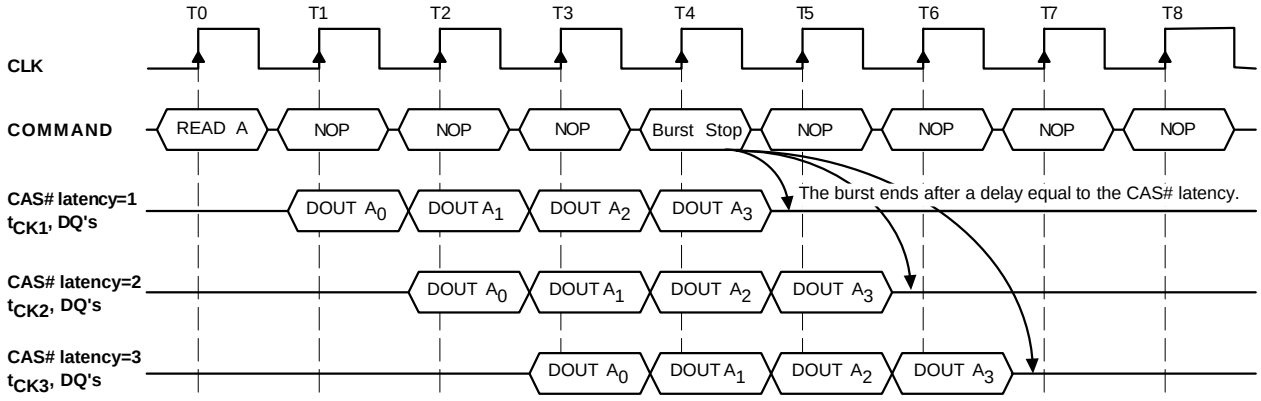
(RAS# = "H", CAS# = "H", WE# = "H")

The No-Operation command is used to perform a NOP to the SDRAM which is selected (CS# is Low). This prevents unwanted commands from being registered during idle or wait states.

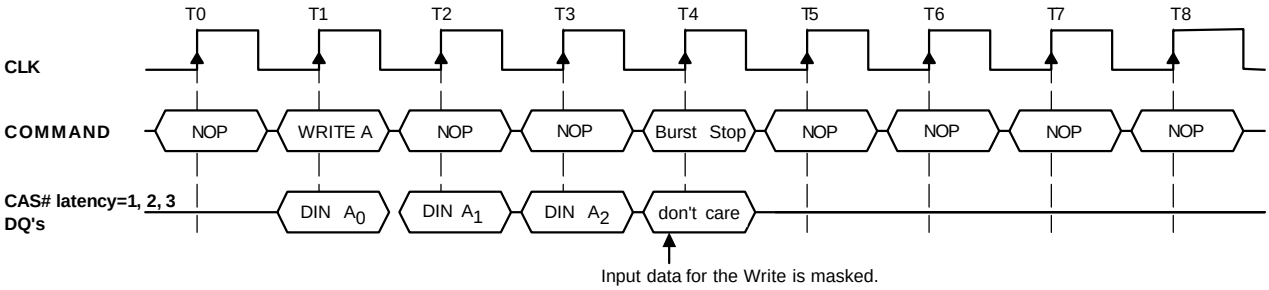
9 Burst Stop command

(RAS# = "H", CAS# = "H", WE# = "L")

The Burst Stop command is used to terminate either fixed-length or full-page bursts. This command is only effective in a read/write burst without the auto precharge function. The terminated read burst ends after a delay equal to the CAS# latency (refer to the following figure). The termination of a write burst is shown in the following figure.



Termination of a Burst Read Operation (Burst Length • 4, CAS# Latency = 1, 2, 3)



Termination of a Burst Write Operation (Burst Length = X, CAS# Latency = 1, 2, 3)

10 Device Deselect command

(CS# = "H")

The Device Deselect command disables the command decoder so that the RAS#, CAS#, WE# and Address inputs are ignored, regardless of whether the CLK is enabled. This command is similar to the No Operation command.

11 AutoRefresh command (refer to Figures 3 & 4 in Timing Waveforms)

(RAS# = "L", CAS# = "L", WE# = "H",CKE = "H", A11 = "Don't care, A0-A9 = Don't care)

The AutoRefresh command is used during normal operation of the SDRAM and is analogous to CAS#-before-RAS# (CBR) Refresh in conventional DRAMs. This command is non-persistent, so it must be issued each time a refresh is required. The addressing is generated by the internal refresh controller. This makes the address bits a "don't care" during an AutoRefresh command. The internal refresh counter increments automatically on every auto refresh cycle to all of the rows. The refresh operation must be performed 2048 times within 32ms. The time required to complete the auto refresh operation is specified by t_{RC}(min.). To provide the AutoRefresh command, both banks need to be in the idle state and the device must not be in power down mode (CKE is high in the previous cycle). This command must be followed by NOPs until the auto refresh operation is completed. The precharge time requirement, t_{RP}(min), must be met before successive auto refresh operations are performed.

12 SelfRefresh Entry command (refer to Figure 5 in Timing Waveforms)

(RAS# = "L", CAS# = "L", WE# = "H", CKE = "L", A0-A9 = Don't care)

The SelfRefresh is another refresh mode available in the SDRAM. It is the preferred refresh mode for data retention and low power operation. Once the SelfRefresh command is registered, all the inputs to the SDRAM become "don't care" with the exception of CKE, which must remain LOW. The refresh addressing and timing is internally generated to reduce power consumption. The SDRAM may remain in SelfRefresh mode for an indefinite period. The SelfRefresh mode is exited by restarting the external clock and then asserting HIGH on CKE (SelfRefresh Exit command).

13 SelfRefresh Exit command (refer to Figure 5 in Timing Waveforms)

(CKE = "H", CS# = "H" or CKE = "H", RAS# = "H", CAS# = "H", WE# = "H")

This command is used to exit from the SelfRefresh mode. Once this command is registered, NOP or Device Deselect commands must be issued for t_{RC}(min.) because time is required for the completion of any bank currently being internally refreshed. If auto refresh cycles in bursts are performed during normal operation, a burst of 4096 auto refresh cycles should be completed just prior to entering and just after exiting the SelfRefresh mode.

14 Clock Suspend Mode Entry / PowerDown Mode Entry command (refer to Figures 6, 7, and 8 in Timing Waveforms)

(CKE = "L")

When the SDRAM is operating the burst cycle, the internal CLK is suspended(masked) from the subsequent cycle by issuing this command (asserting CKE "LOW"). The device operation is held intact while CLK is suspended. On the other hand, when both banks are in the idle state, this command performs entry into the PowerDown mode. All input and output buffers (except the CKE buffer) are turned off in the PowerDown mode. The device may not remain in the Clock Suspend or PowerDown state longer than the refresh period (64ms) since the command does not perform any refresh operations.

15 Clock Suspend Mode Exit / PowerDown Mode Exit command (refer to Figures 6, 7, and 8 in Timing Waveforms, CKE= "H")

When the internal CLK has been suspended, the operation of the internal CLK is reinitiated from the subsequent cycle by providing this command (asserting CKE "HIGH"). When the device is in the PowerDown mode, the device exits this mode and all disabled buffers are turned on to the active state. t_{PDE}(min.) is required when the device exits from the PowerDown mode. Any subsequent commands can be issued after one clock cycle from the end of this command.

16 Data Write / Output Enable, Data Mask / Output Disable command (LDQM/UDQM = "L", "H")

During a write cycle, the LDQM/UDQM signal functions as a Data Mask and can control every word of the input data. During a read cycle, the LDQM/UDQM functions as the controller of output buffers. LDQM/UDQM is also used for device selection, byte selection and bus control in a memory system. LDQM controls DQ0 to DQ7, UDQM controls DQ8 to DQ15.

Absolute Maximum Rating

Symbol	Item	Rating	Unit	Note
		-5/6/7		
V_{IN}, V_{OUT}	Input, Output Voltage	- 1.0 ~ 4.6	V	1
V_{DD}, V_{DDQ}	Power Supply Voltage	-1.0 ~ 4.6	V	1
T_{OPR}	Operating Temperature	0 ~ 70	°C	1
T_{STG}	Storage Temperature	- 55 ~ 125	°C	1
P_D	Power Dissipation	1	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

Recommended D.C. Operating Conditions (Ta = -0~70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V_{DD}	Power Supply Voltage	3.0	3.3	3.6	V	2
V_{DDQ}	Power Supply Voltage(for I/O Buffer)	3.0	3.3	3.6	V	2
V_{IH}	LVTTL Input High Voltage	2.0	-	V_{DDQ}+0.3	V	2
V_{IL}	LVTTL Input Low Voltage	- 0.3	-	0.8	V	2

Capacitance (V_{DD} = 3.3V, f = 1MHz, Ta = 25°C)

Symbol	Parameter	Min.	Max.	Unit
C_I	Input Capacitance	2	5	pF
$C_{I/O}$	Input/Output Capacitance	4	7	pF

Note: These parameters are periodically sampled and are not 100% tested.

Recommended D.C. Operating Conditions (V_{DD} = 3.3V ± 0.3V, Ta = 0~70°C)

Description/Test condition		Symbol	- 5/6/7(T431616D) Max.	- 7(T431616E) Max.	Unit	Note
Operating Current $t_{RC} \geq t_{RC}$(min), Outputs Open, Input signal one transition per one cycle	1 bank operation	I_{DD1}	130/115/100	40	mA	3
Precharge Standby Current in non-power down mode $t_{CK} = t_{CK}$(min), CS# ≥ V_{IH}, CKE = V_{IH} Input signals are changed once during 30ns.		I_{DD2N}	25	15		3
Precharge Standby Current in power down mode $t_{CK} = t_{CK}$(min), CKE ≤ V_{IL}(max)		I_{DD2P}	2	0.8		3
Precharge Standby Current in power down mode $t_{CK} = \infty$, CKE ≤ V_{IL}(max)		I_{DD2PS}	2	0.8		
Active Standby Current in power down mode CKE ≤ V_{IL}(max), $t_{CK} = t_{CK}$(min)		I_{DD3P}	2	1.5		3
Active Standby Current in non-power down mode CKE ≥ V_{IL}(max), $t_{CK} = t_{CK}$(min)		I_{DD3N}	40	20		
Operating Current (Burst mode) $t_{CK}=t_{CK}$(min), Outputs Open, Multi-bank interleave,gapless data		I_{DD4}	165/150/140	40		3, 4
Refresh Current $t_{RC} \geq t_{RC}$(min)		I_{DD5}	115/100/90	40		3
Self Refresh Current $V_{IH} \geq V_{DD}$ - 0.2, 0V ≤ V_{IL} ≤ 0.2V		I_{DD6}	2	0.6		

Parameter	Description	Min.	Max.	Unit	Note
I_{IL}	Input Leakage Current (0V ≤ V_{IN} ≤ V_{DD}, All other pins not under test = 0V)	- 10	10	uA	
I_{OL}	Output Leakage Current Output disable, 0V ≤ V_{OUT} ≤ V_{DDQ})	- 10	10	uA	
V_{OH}	LVTTL Output "H" Level Voltage (I_{OUT} = -2mA)	2.4	-	V	
V_{OL}	LVTTL Output "L" Level Voltage (I_{OUT} = 2mA)	-	0.4	V	

Electrical Characteristics and Recommended A.C. Operating Conditions

(V_{DD} = 3.3V±0.3V, Ta = -0~70°C) (Note: 5, 6, 7, 8)

Symbol	A.C. Parameter		- 5/6/7/7L		Unit	Note
			Min.	Max.		
t_{RC}	Row cycle time (same bank)		48/54/63/63		ns	9
t_{RCD}	RAS# to CAS# delay (same bank)		15/16/16/16			9
t_{RP}	Precharge to refresh/row activate command (same bank)		15/16/16/16			9
t_{RRD}	Row activate to row activate delay (different banks)		10/12/14/14			9
t_{RAS}	Row activate to precharge time (same bank)		35/42/42/42	100,000		
t_{WR}	Write recovery time		2		Cycle	
t_{CK1}	Clock cycle time	CL* = 1	-/20/20/20		ns	10
t_{CK2}		CL* = 2	-/7/8/8			
t_{CK3}		CL* = 3	5/6/7/7			
t_{CH}	Clock high time		2/2/2.5/2.5			11
t_{CL}	Clock low time		2/2/2.5/2.5			11
t_{AC1}	Access time from CLK (positive edge)	CL* = 1		-/8/13/13		11
t_{AC2}		CL* = 2		-/6/6.5/6.5		
t_{AC3}		CL* = 3		4.5/5/5.5/5.5		
t_{CCD}	CAS# to CAS# Delay time		1		Cycle	
t_{OH}	Data output hold time		1.8/2/2/2		ns	10
t_{LZ}	Data output low impedance		1			
t_{HZ}	Data output high impedance			3/4/5/5		8
t_{IS}	Data/Address/Control Input set-up time		2			11
t_{IH}	Data/Address/Control Input hold time		1			11
t_{PDE}	PowerDown Exit set-up time		2			
t_{REF}	Refresh time			64	ms	

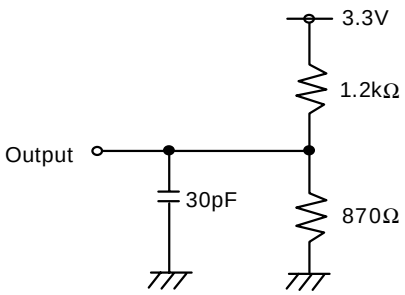
* CL is CAS# Latency.

Note:

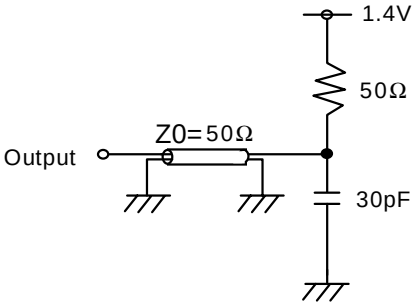
1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to VSS. VIH(Max)=4.6 for pulse width≤5ns.VIL(Min)=-1.5Vfor pulse width≤5ns.
3. These parameters depend on the cycle rate and these values are measured by the cycle rate under the minimum value of tCK and tRC. Input signals are changed one time during tCK.
4. These parameters depend on the output loading. Specified values are obtained with the output open.
5. Power-up sequence is described in Note 12.
6. A.C. Test Conditions

LVTTL Interface

Reference Level of Output Signals	1.4V / 1.4V
Output Load	Reference to the Under Output Load (B)
Input Signal Levels	2.4V / 0.4V
Transition Time (Rise and Fall) of Input Signals	1ns
Reference Level of Input Signals	1.4V



LVTTL D.C. Test Load (A)



LVTTL A.C. Test Load (B)

7. Transition times are measured between V_{IH} and V_{IL}. Transition(rise and fall) of input signals are in a fixed slope (1 ns).
8. t_{HZ} defines the time in which the outputs achieve the open circuit condition and are not at reference levels.
9. These parameters account for the number of clock cycle and depend on the operating frequency of the clock as follows:
   the number of clock cycles = specified value of timing/Clock cycle time
   (count fractions as a whole number)
10. If clock rising time is longer than 1 ns, (t_R / 2 -0.5) ns should be added to the parameter.
11. Assumed input rise and fall time t_T (t_R & t_F) = 1 ns

    If t_R or t_F is longer than 1 ns, transient time compensation should be considered, i.e., [(tr + tf)/2 - 1] ns should be added to the parameter.
12. Power up Sequence

    Power up must be performed in the following sequence.
    1) Power must be applied to V_{DD} and V_{DDQ}(simultaneously) when all input signals are held "NOP" state and both CKE = "H" and LDQM/UDQM = "H." The CLK signals must be started at the same time.
    2) After power-up, a pause of 200us minimum is required. Then, it is recommended that LDQM/UDQM is held "HIGH" (V_{DD} levels) to ensure DQ output is in high impedance.
    3) Both banks must be precharged.
    4) Mode Register Set command must be asserted to initialize the Mode register.
    5) A minimum of 2 Auto-Refresh dummy cycles must be required before or after the Mode Register Set command in step 4 to stabilize the internal circuitry of the device.

Timing Waveforms

Figure 1. AC Parameters for Write Timing (Burst Length=4, CAS# Latency=2)

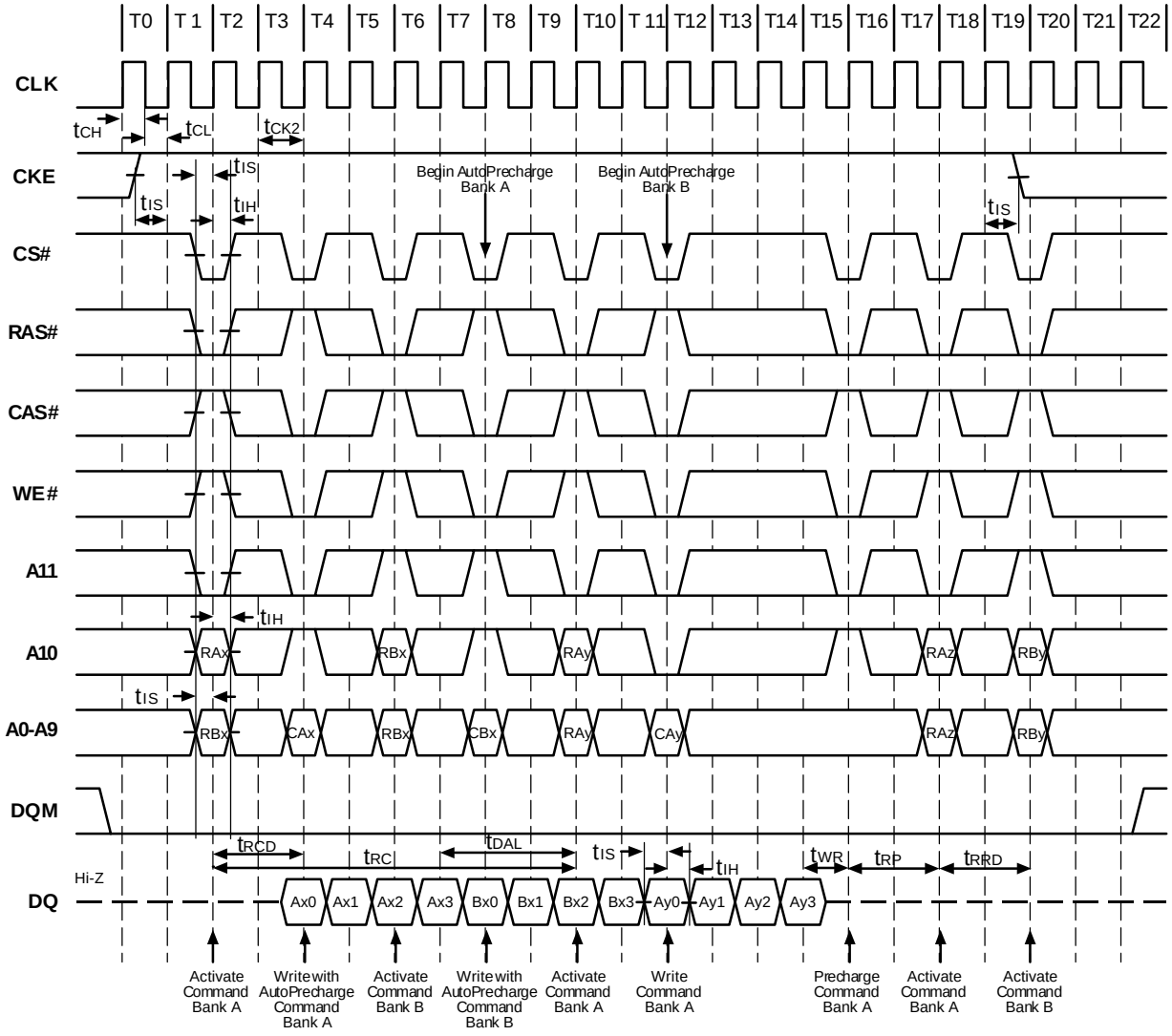


Figure 2. AC Parameters for Read Timing (Burst Length=2, CAS# Latency=2)

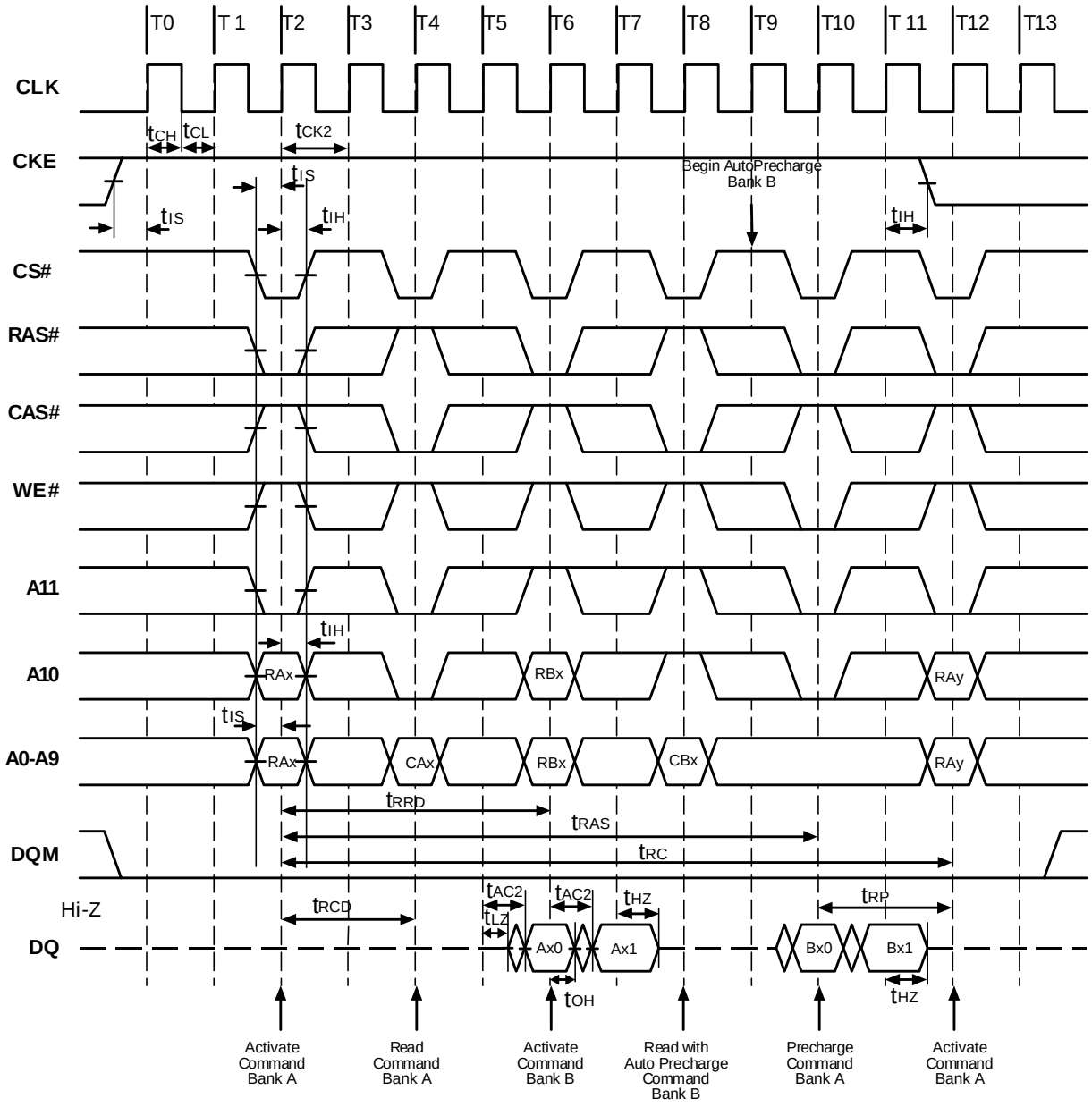


Figure 3. Auto Refresh (CBR) (Burst Length=4, CAS# Latency=2)

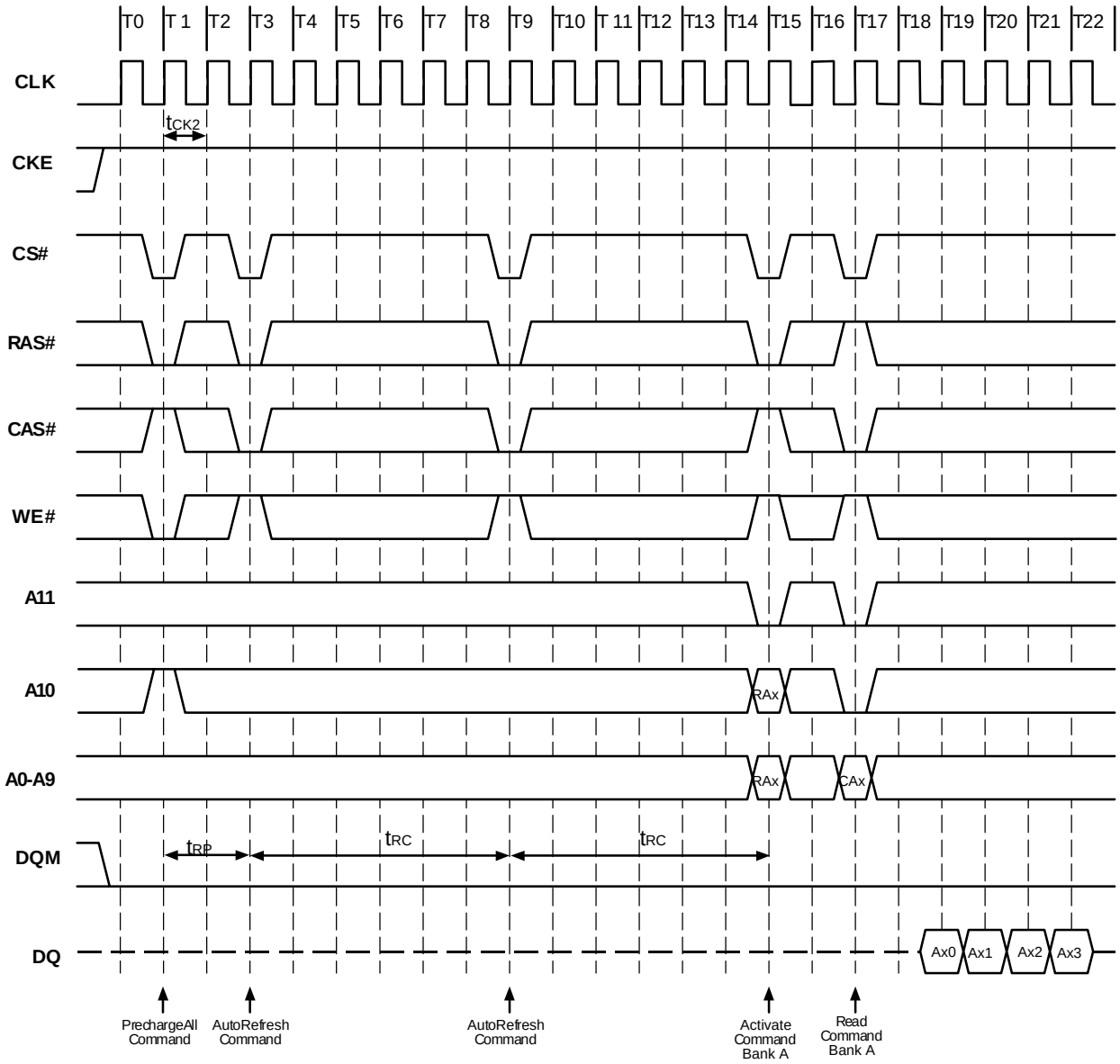
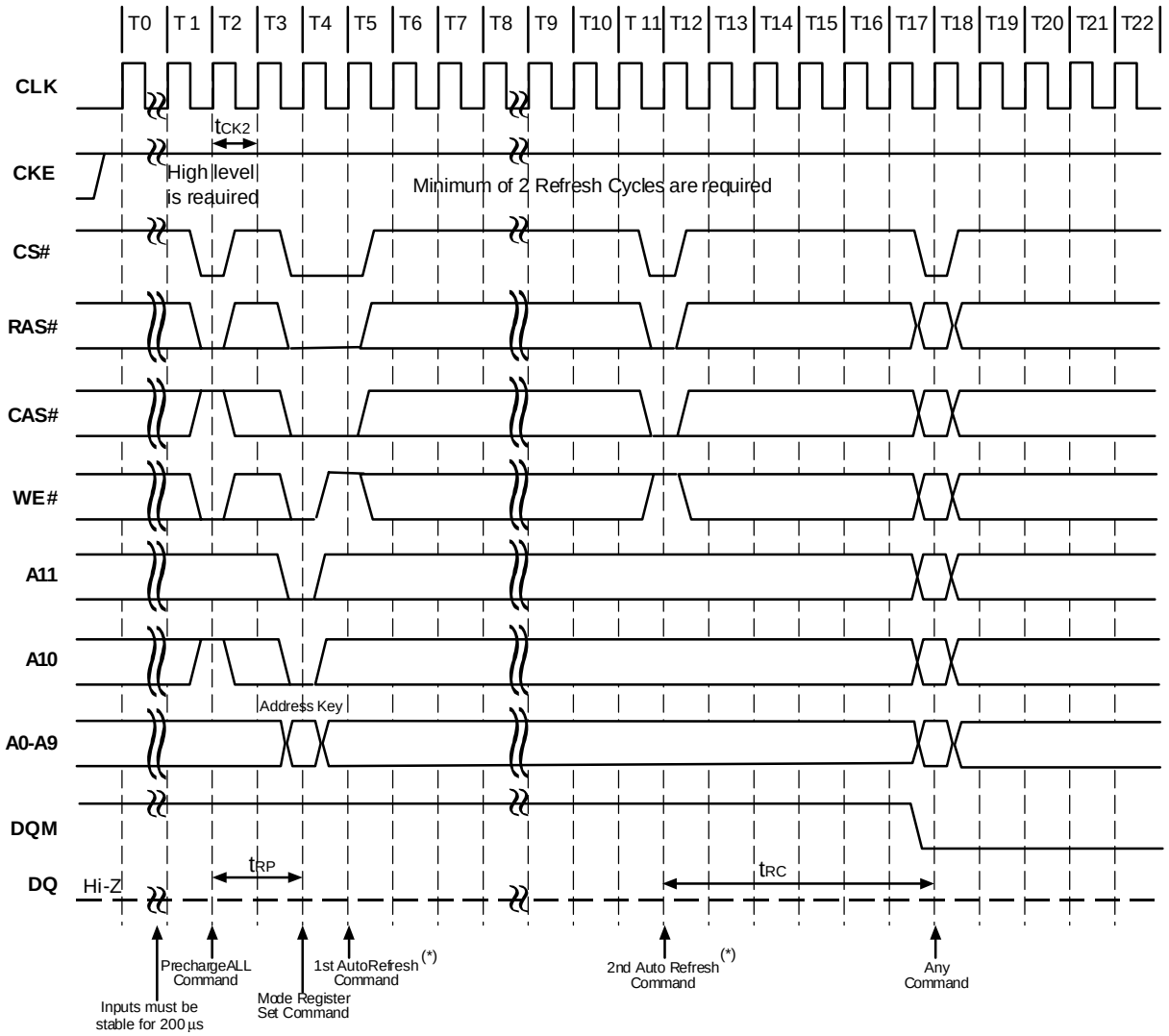
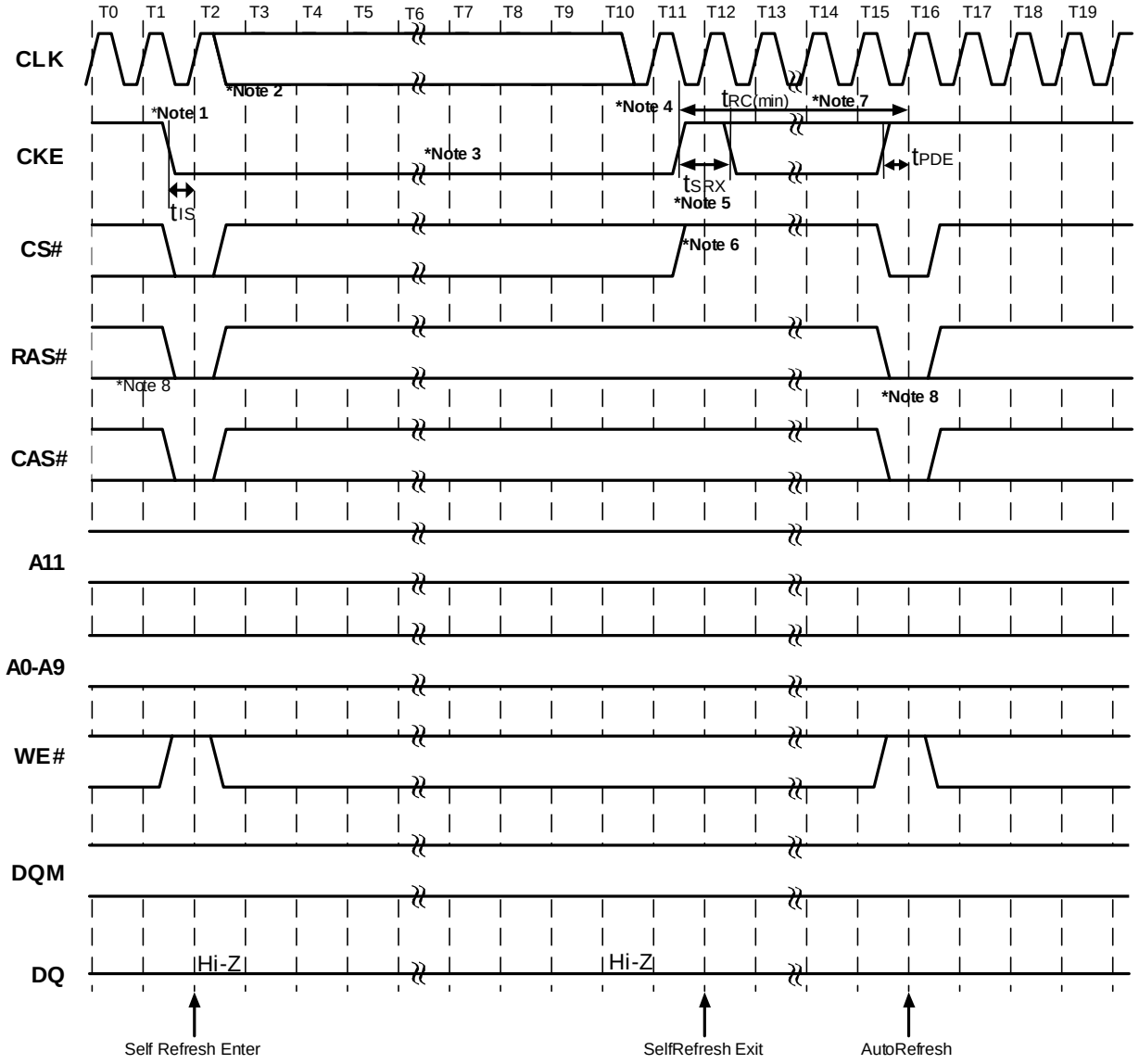


Figure 4. Power on Sequene and Auto Refresh (CBR)



Note (*) : The Auto Refresh command can be issued before or after Mode Register Set command

Figure 5. Self Refresh Entry & Exit Cycle



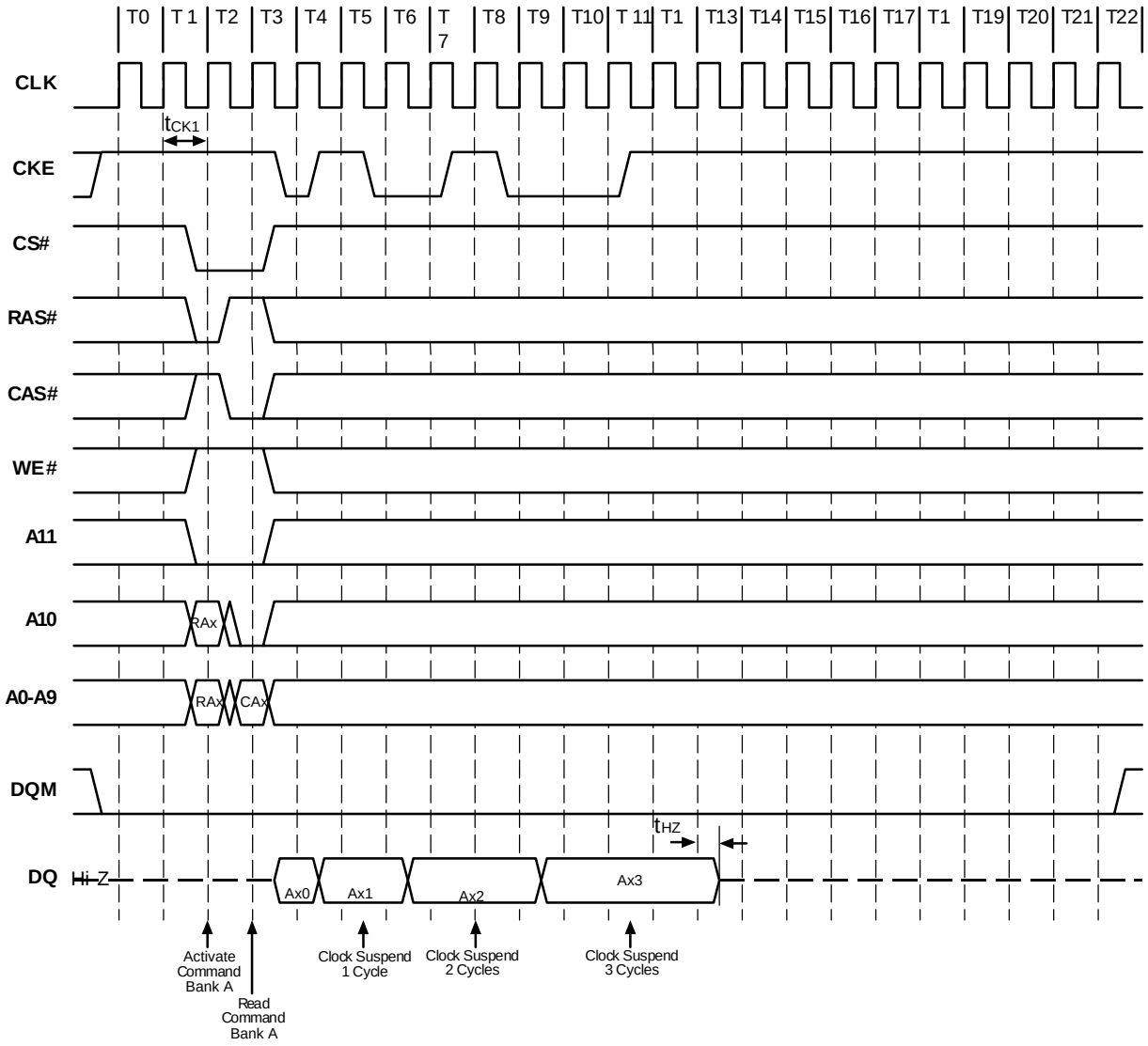
Note: To Enter SelfRefresh Mode

1. CS#, RAS# & CAS# with CKE should be low at the same clock cycle.
2. After 1 clock cycle, all the inputs including the system clock can be don't care except for CKE.
3. The device remains in SelfRefresh mode as long as CKE stays "low".
   Once the device enters SelfRefresh mode, minimum t_{RAS} is required before exit from SelfRefresh.

To Exit SelfRefresh Mode

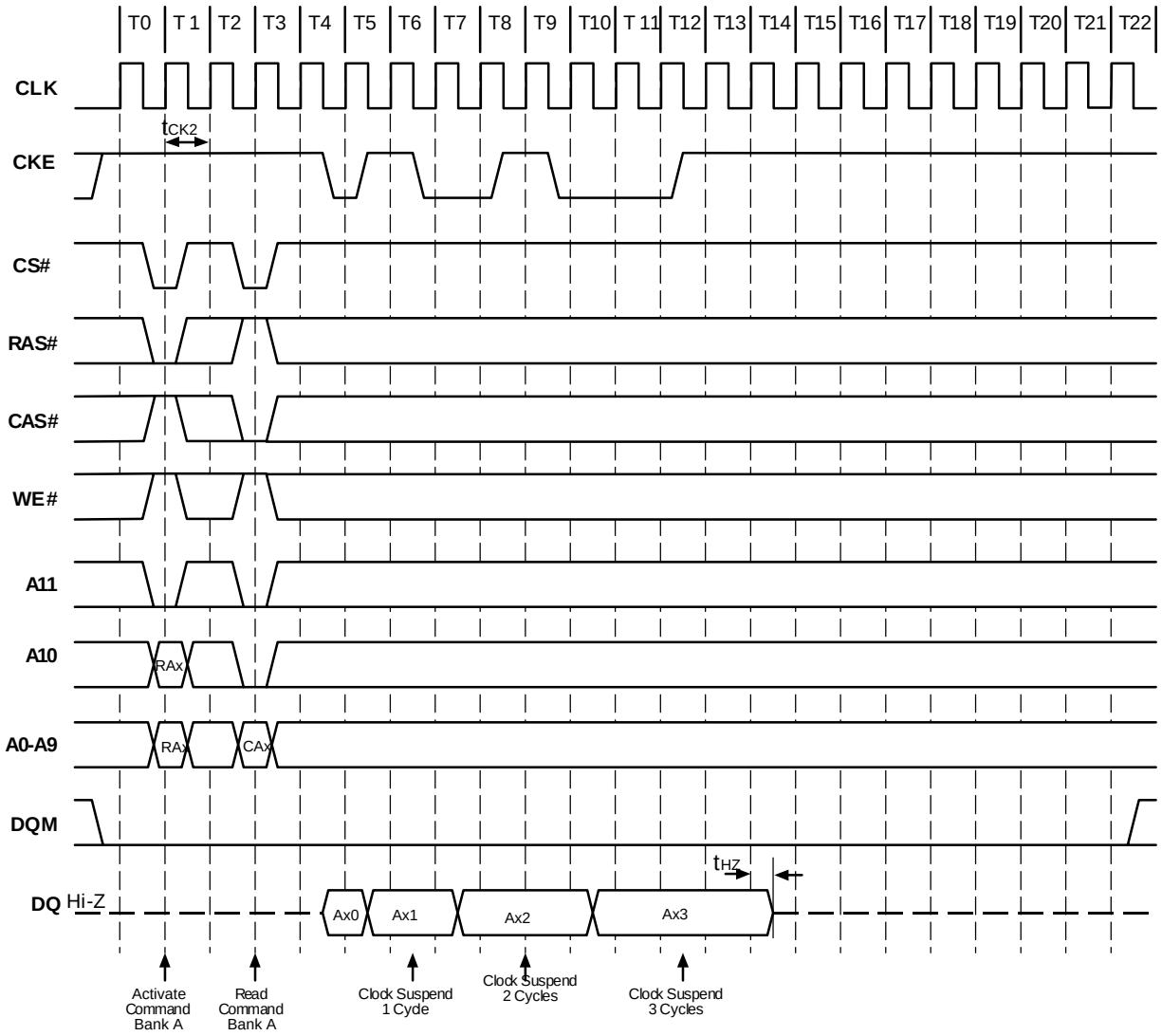
1. System clock restart and be stable before returning CKE high.
2. Enable CKE and CKE should be set high for minimum time of t_{SRX}.
3. CS# starts from high.
4. Minimum t_{RC} is required after CKE going high to complete SelfRefresh exit.
5. 2048 cycles of burst AutoRefresh is required before SelfRefresh entry and after SelfRefresh exit if the system uses burst refresh.

Figure 6.1. Clock Suspension During Burst Read (Using CKE)
(Burst Length=4, CAS# Latency=1)



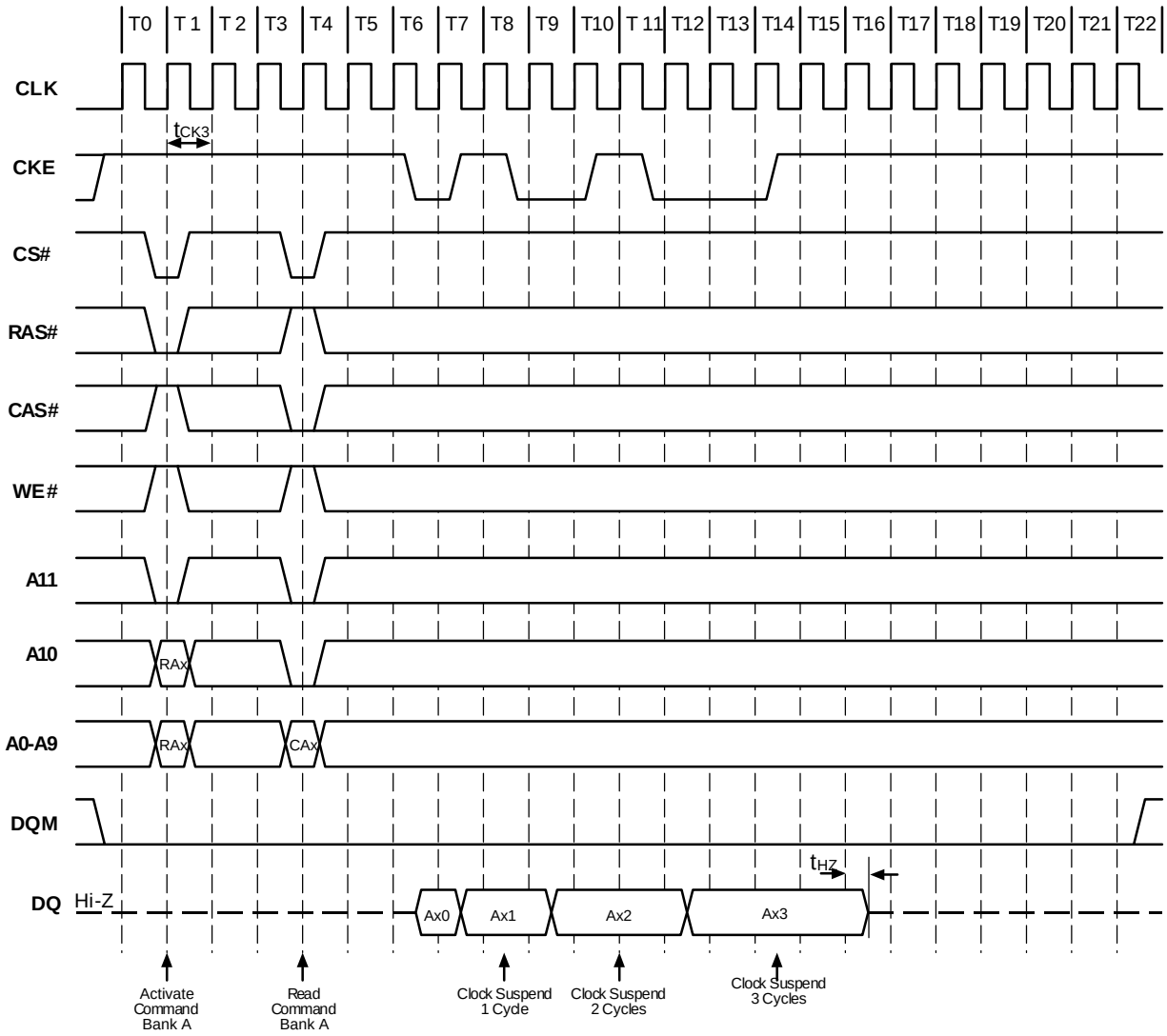
Note: CKE to CLK disable/enable = 1 clock

Figure 6.2. Clock Suspension During Burst Read (Using CKE)
(Burst Length=4, CAS# Latency=2)



Note: CKE to CLK disable/enable = 1 clock

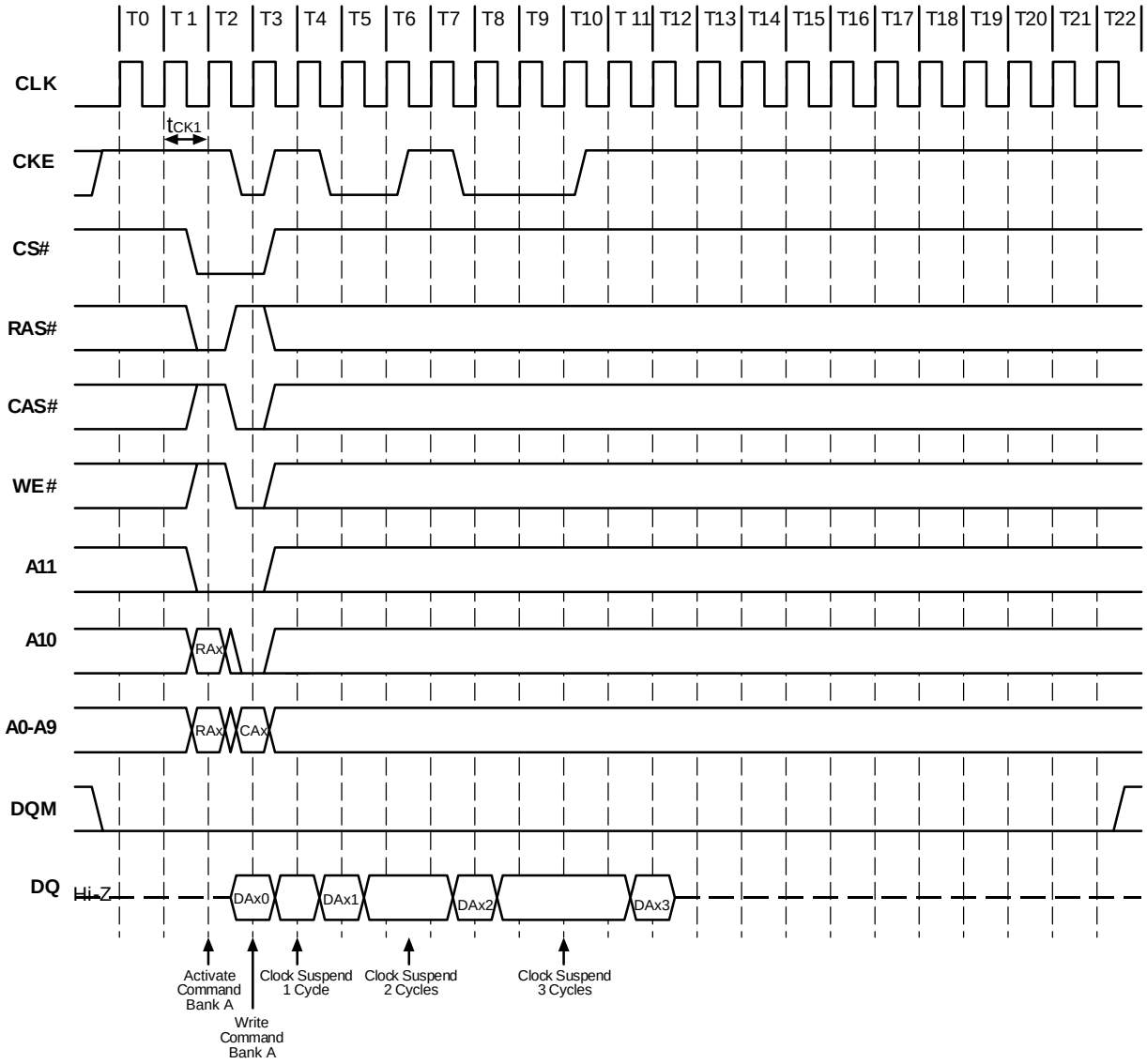
Figure 6.3. Clock Suspension During Burst Read (Using CKE)
(Burst Length=4, CAS# Latency=3)



Note: CKE to CLK disable/enable = 1 clock

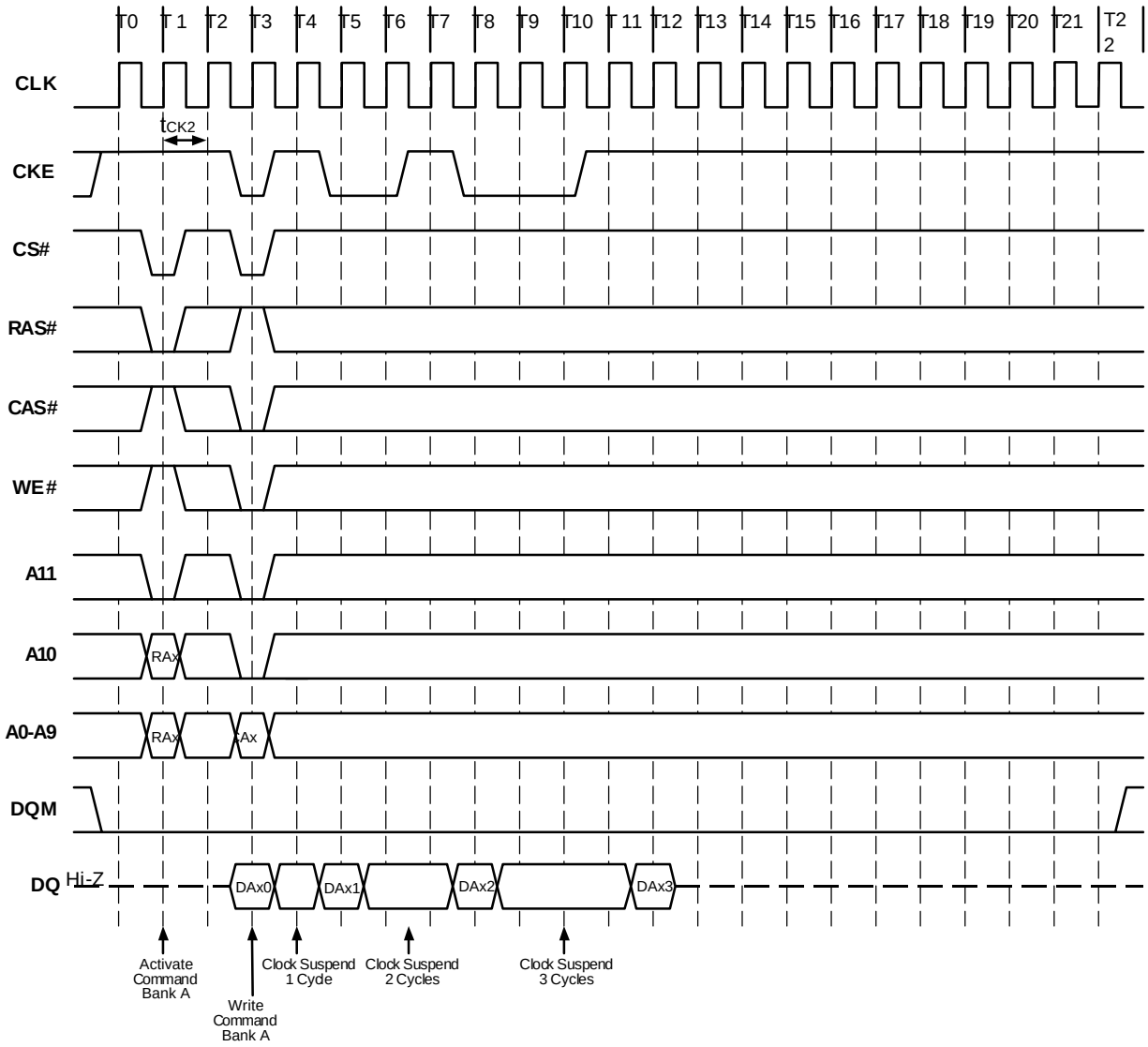
Figure 7.1. Clock Suspension During Burst Write (Using CKE)

(Burst Length = 4, CAS# Latency = 1)



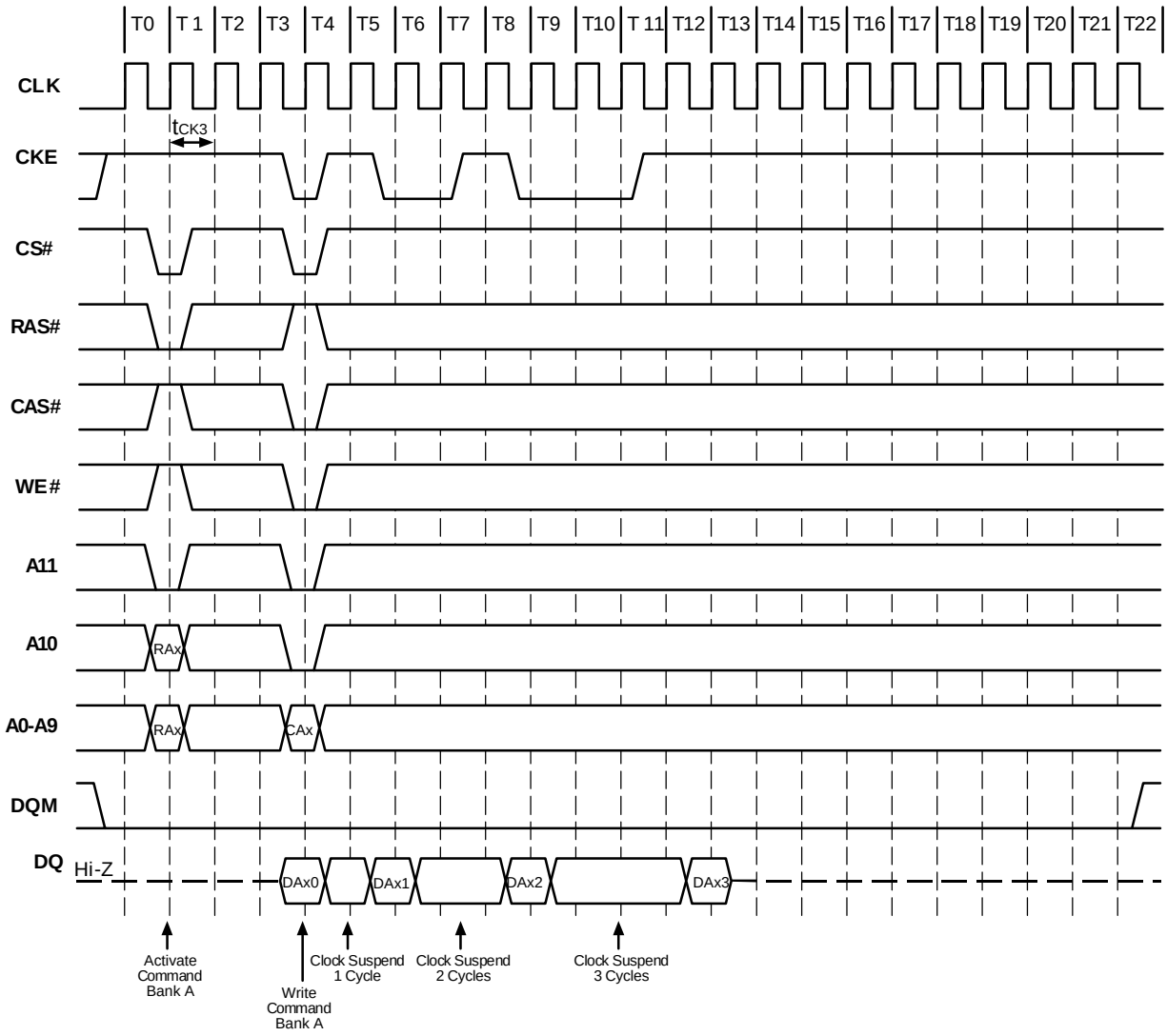
Note: CKE to CLK disable/enable = 1 clock

Figure 7.2. Clock Suspension During Burst Write (Using CKE)
(Burst Length=4, CAS# Latency=2)



Note: CKE to CLK disable/enable = 1 clock

Figure 7.3. Clock Suspension During Burst Write (Using CKE)
(Burst Length=4, CAS# Latency=3)



Note: CKE to CLK disable/enable = 1 clock

Figure 8. Power Down Mode and Clock Mask (Burst Lenght=4, CAS# Latency=2)

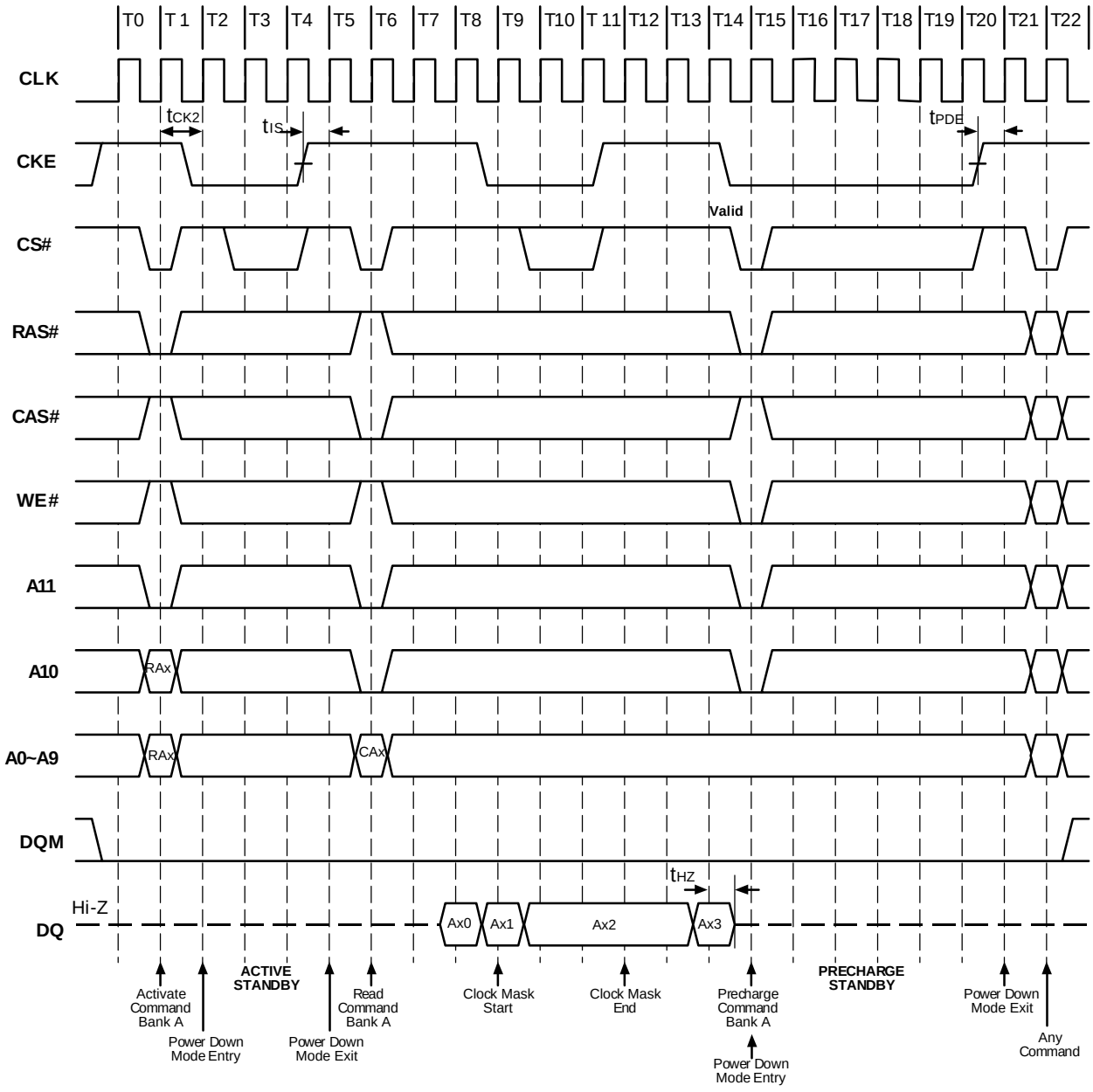


Figure 9.1. Random Column Read (Page within same Bank)
(Burst Length=4, CAS# Latency=1)

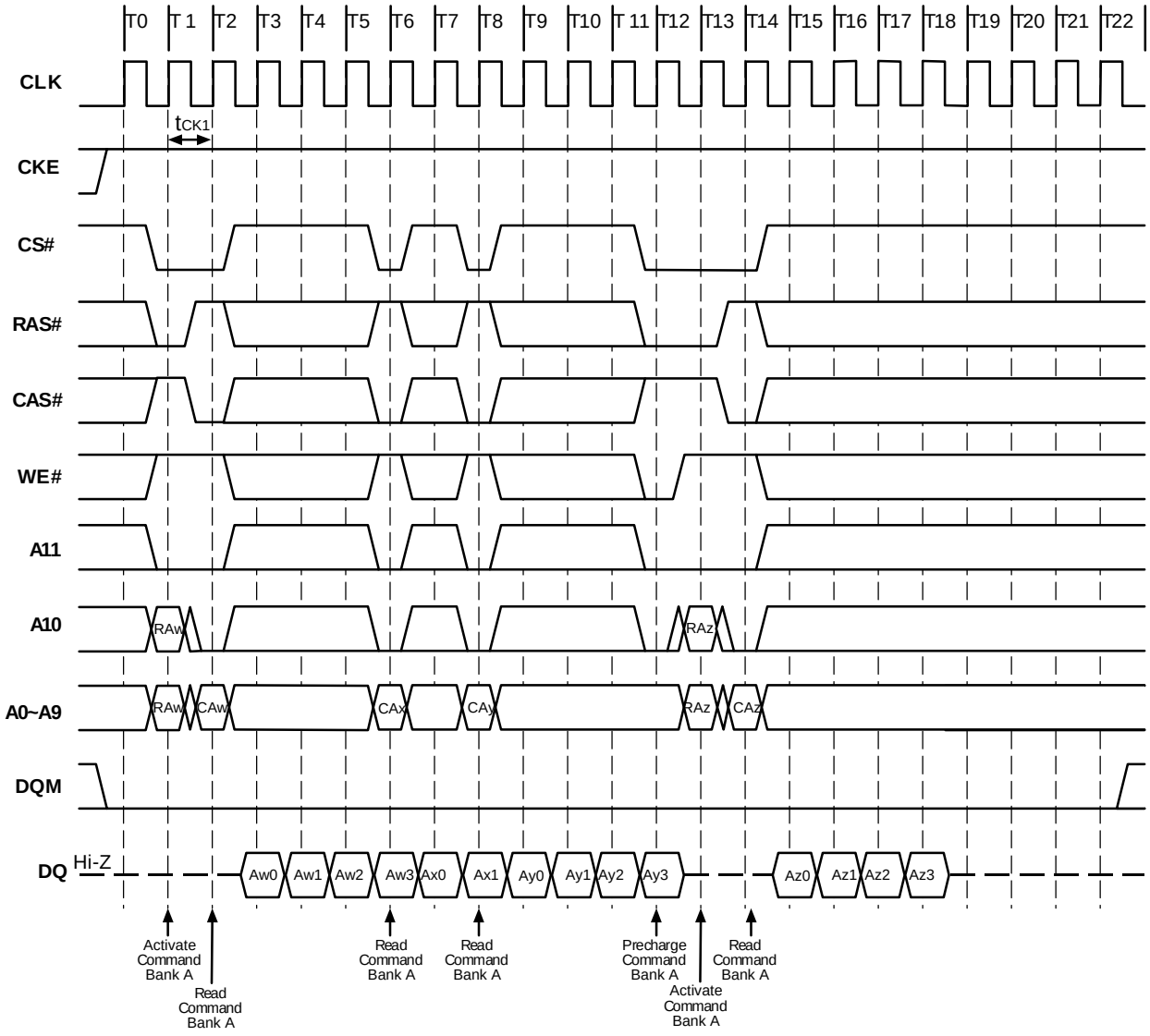


Figure 9.2. Random Column Read (Page within same Bank)
(Burst Length=4, CAS# Latency=2)

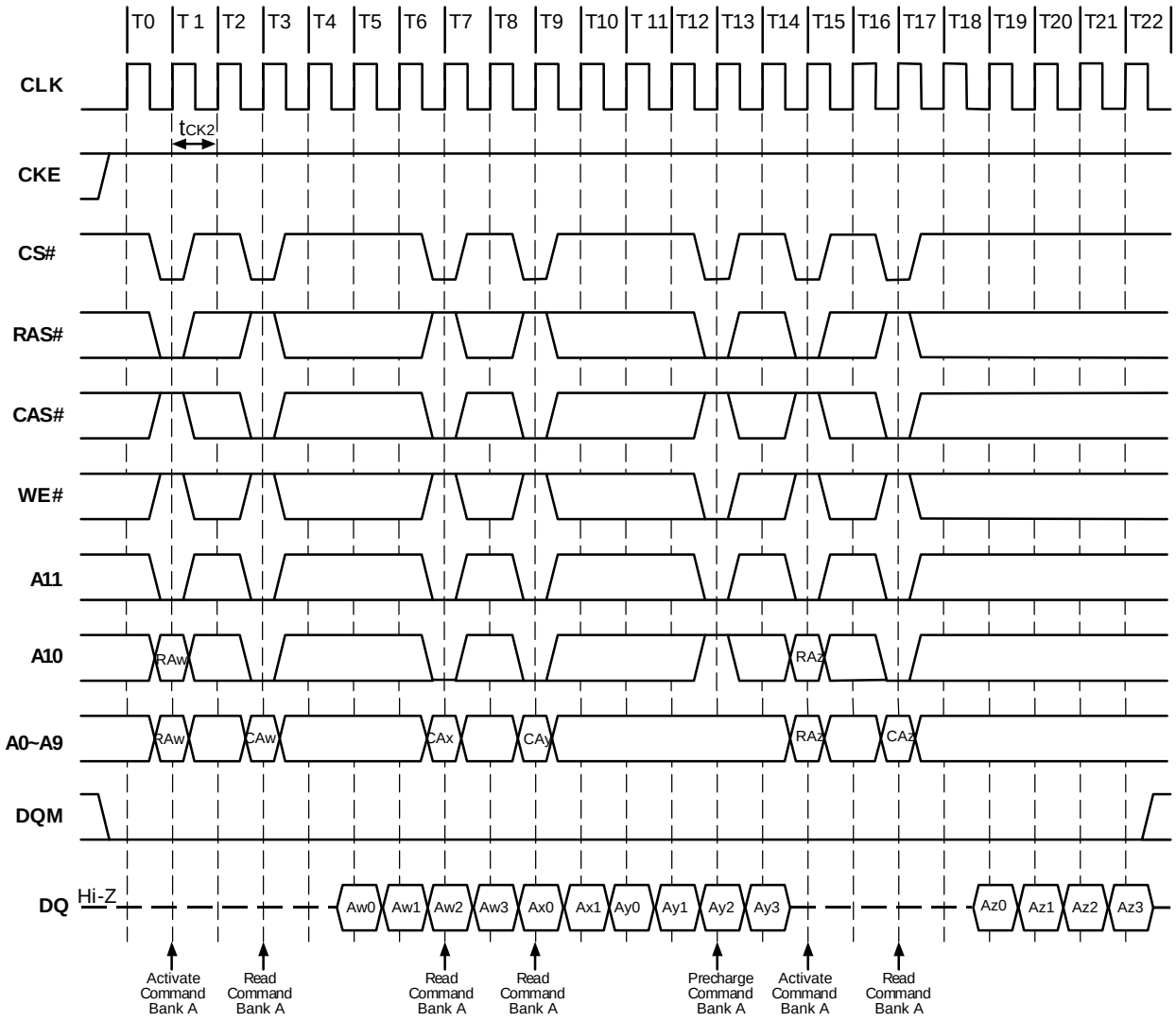


Figure 9.3. Random Column Read (Page within same Bank)
(Burst Length=4, CAS# Latency=3)

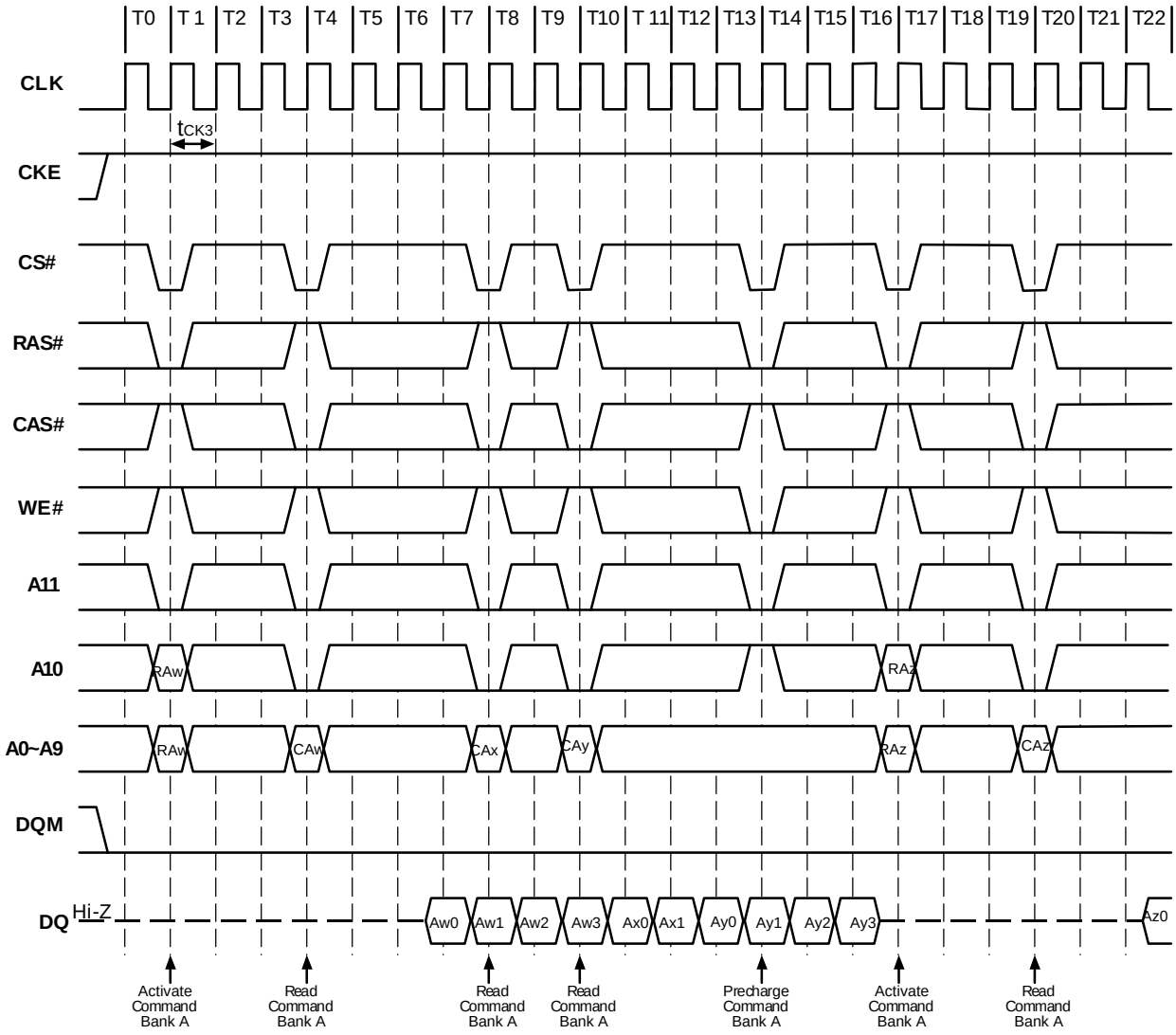


Figure 10.1. Random Column Write (Page within same Bank)
(Burst Length=4, CAS# Latency=1)

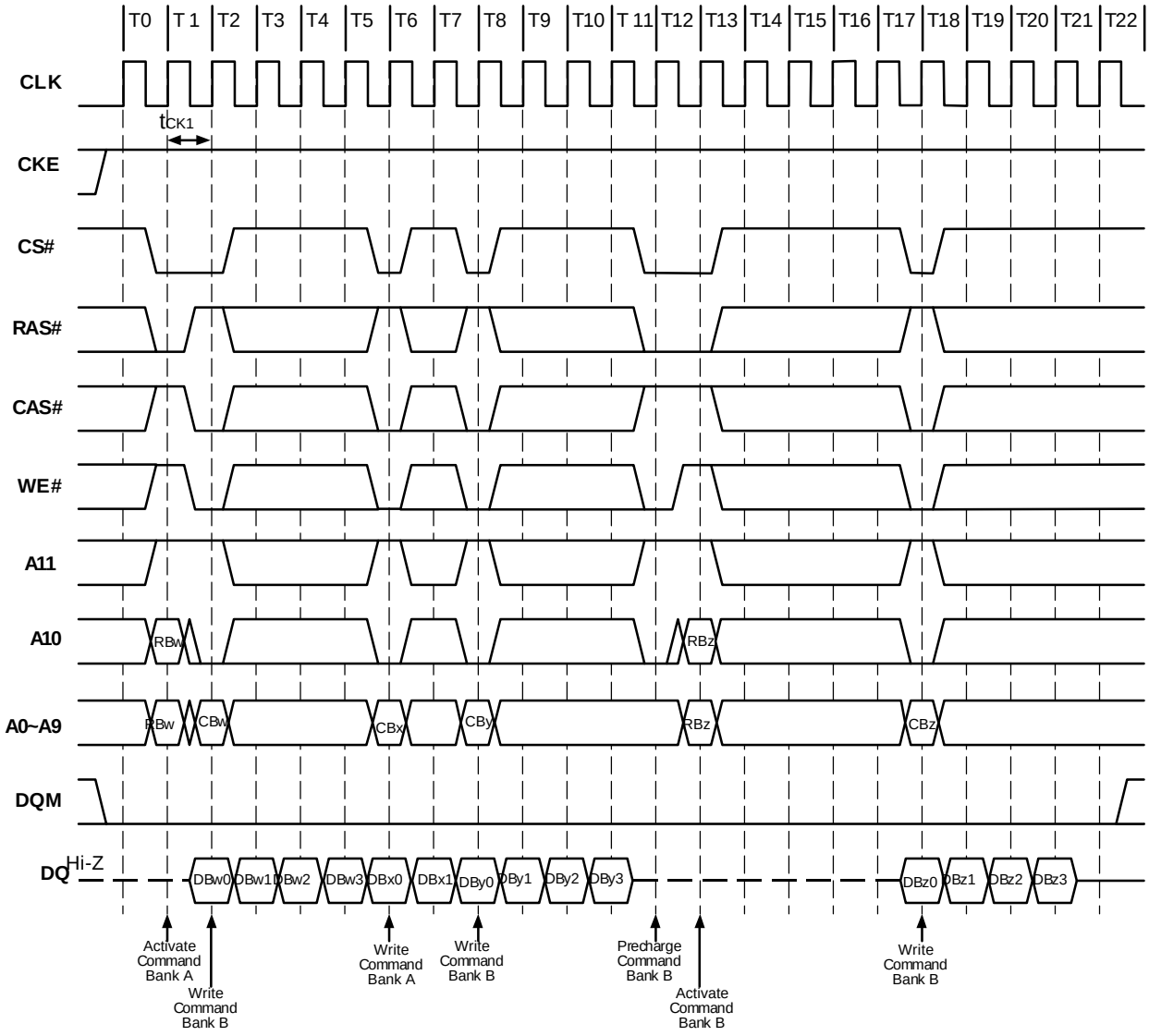


Figure 10.2. Random Column Write (Page within same Bank)
(Burst Length=4, CAS# Latency=2)

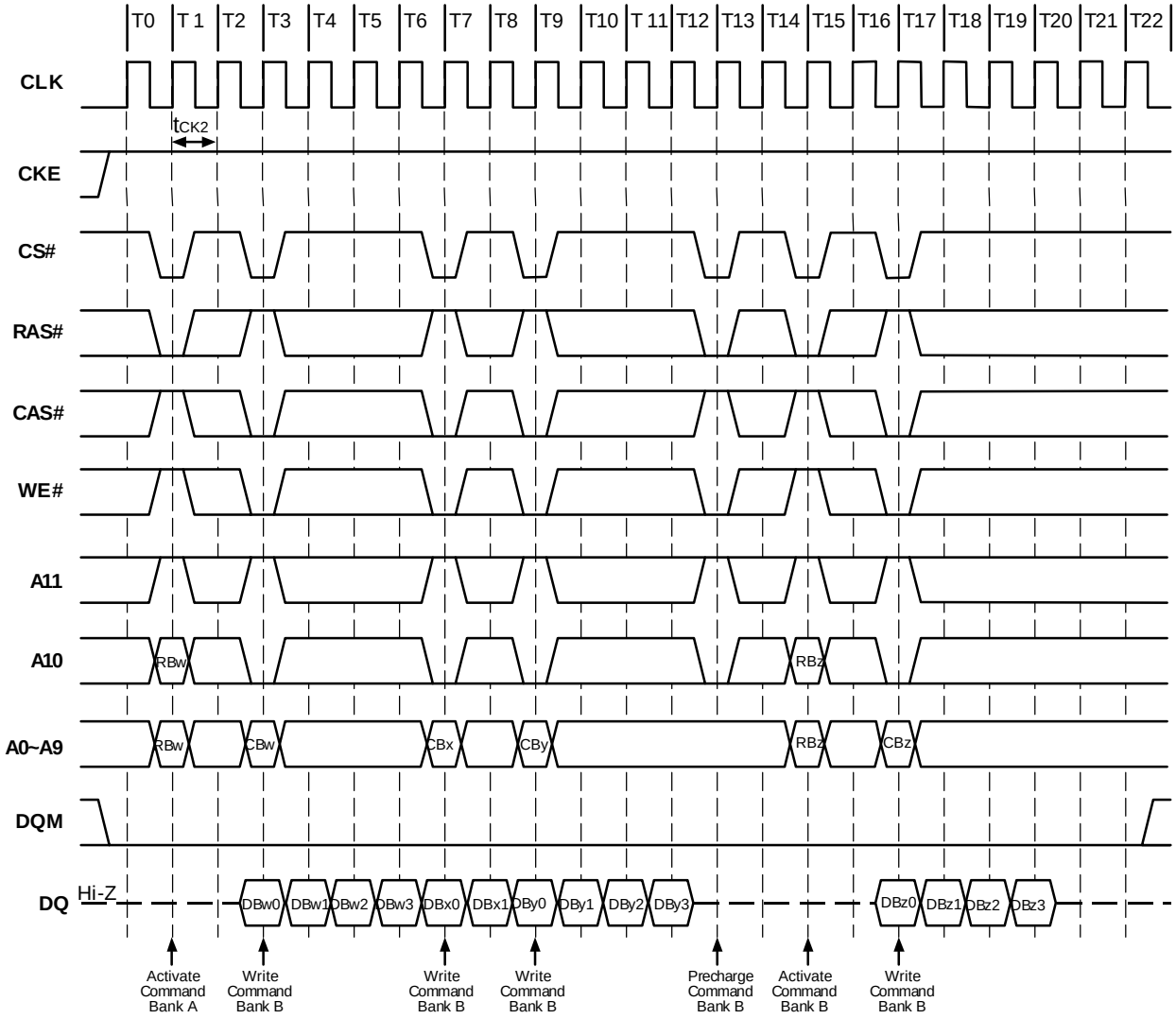


Figure 10.3. Random Column Write (Page within same Bank)
(Burst Length=4, CAS# Latency=3)

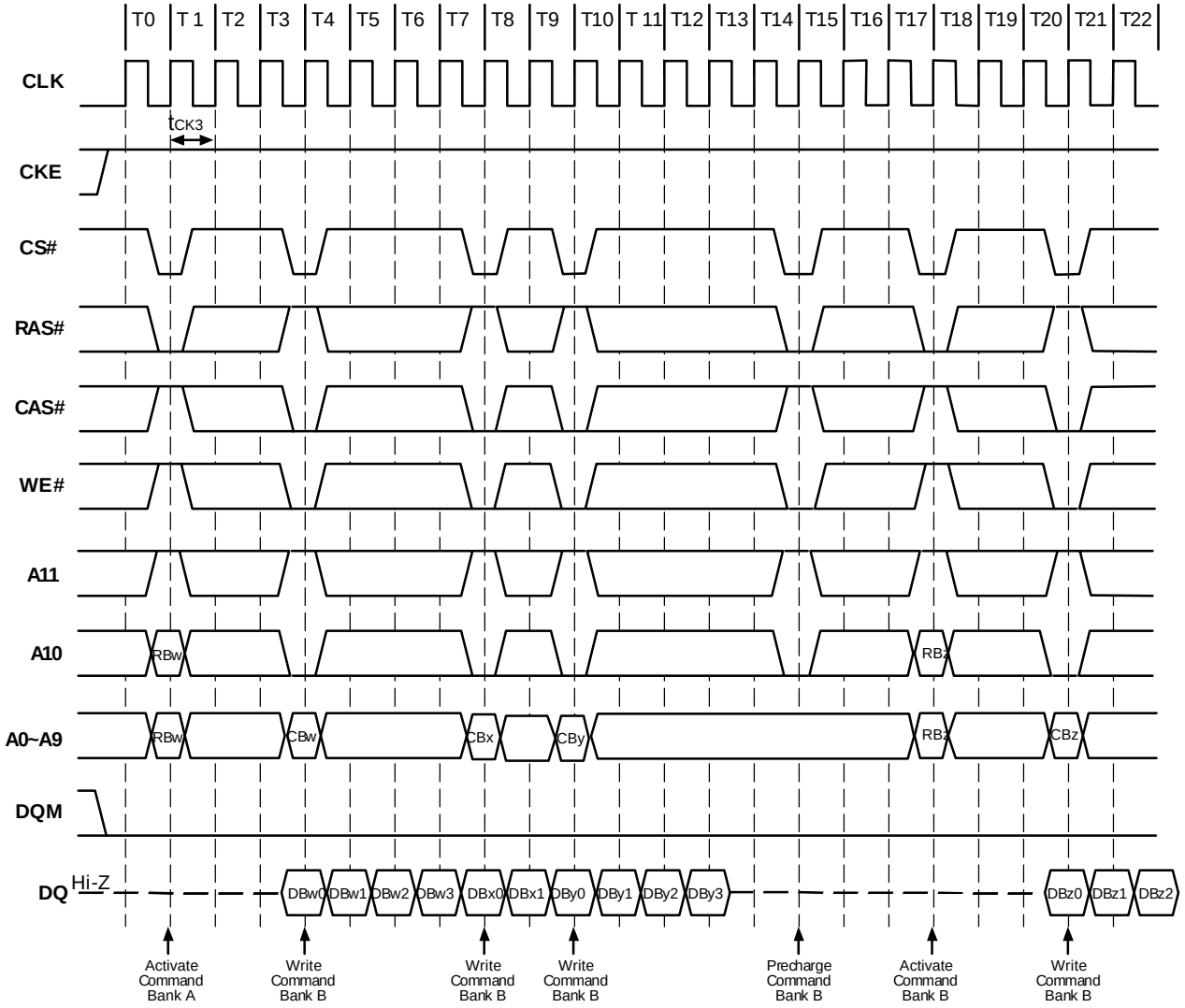


Figure 11.1. Random Row Read (Interleaving Banks)
(Burst Length=8, CAS# Latency=1)

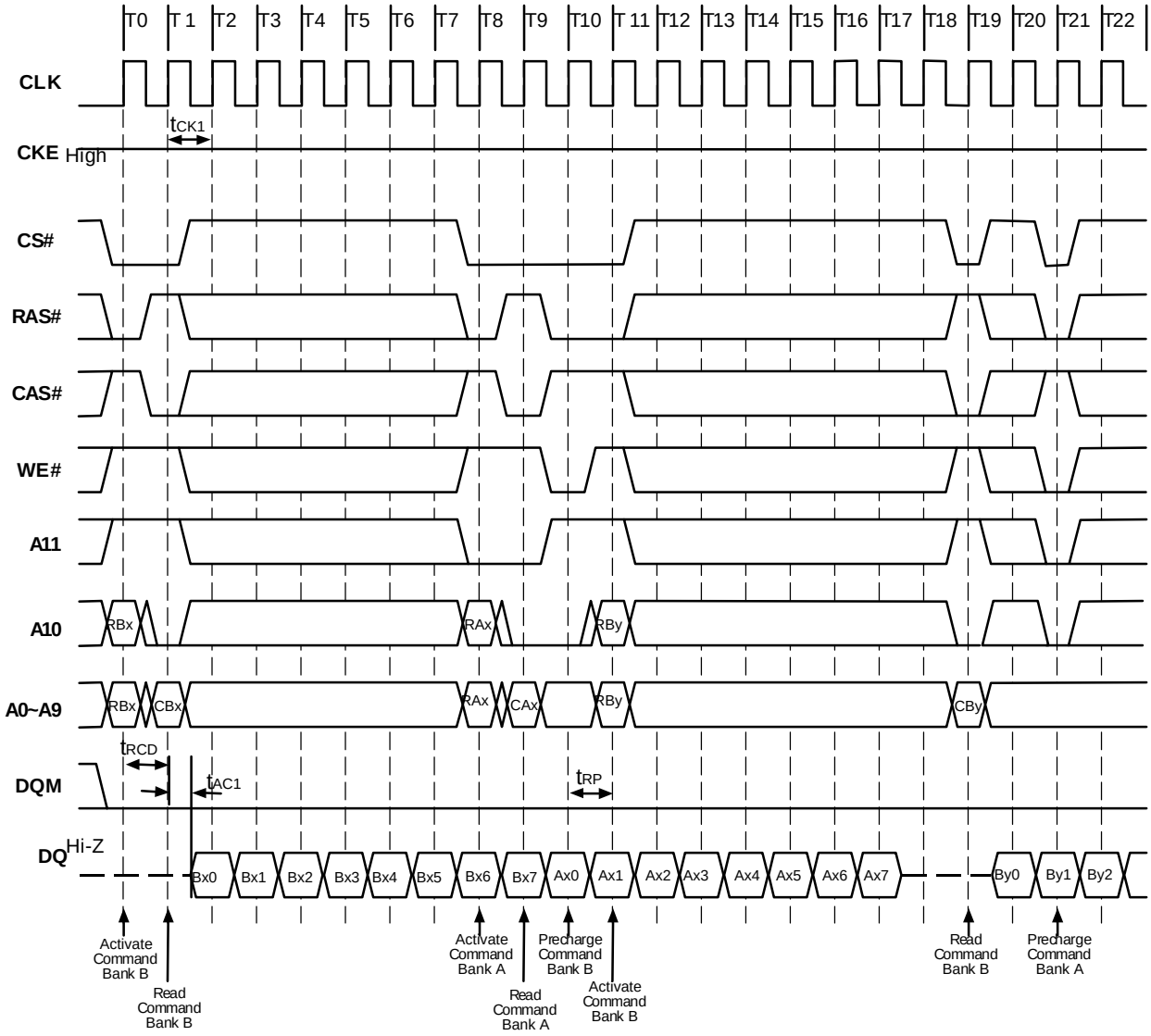


Figure 11.2. Random Row Read (Interleaving Banks)
(Burst Length=8, CAS# Latency=2)

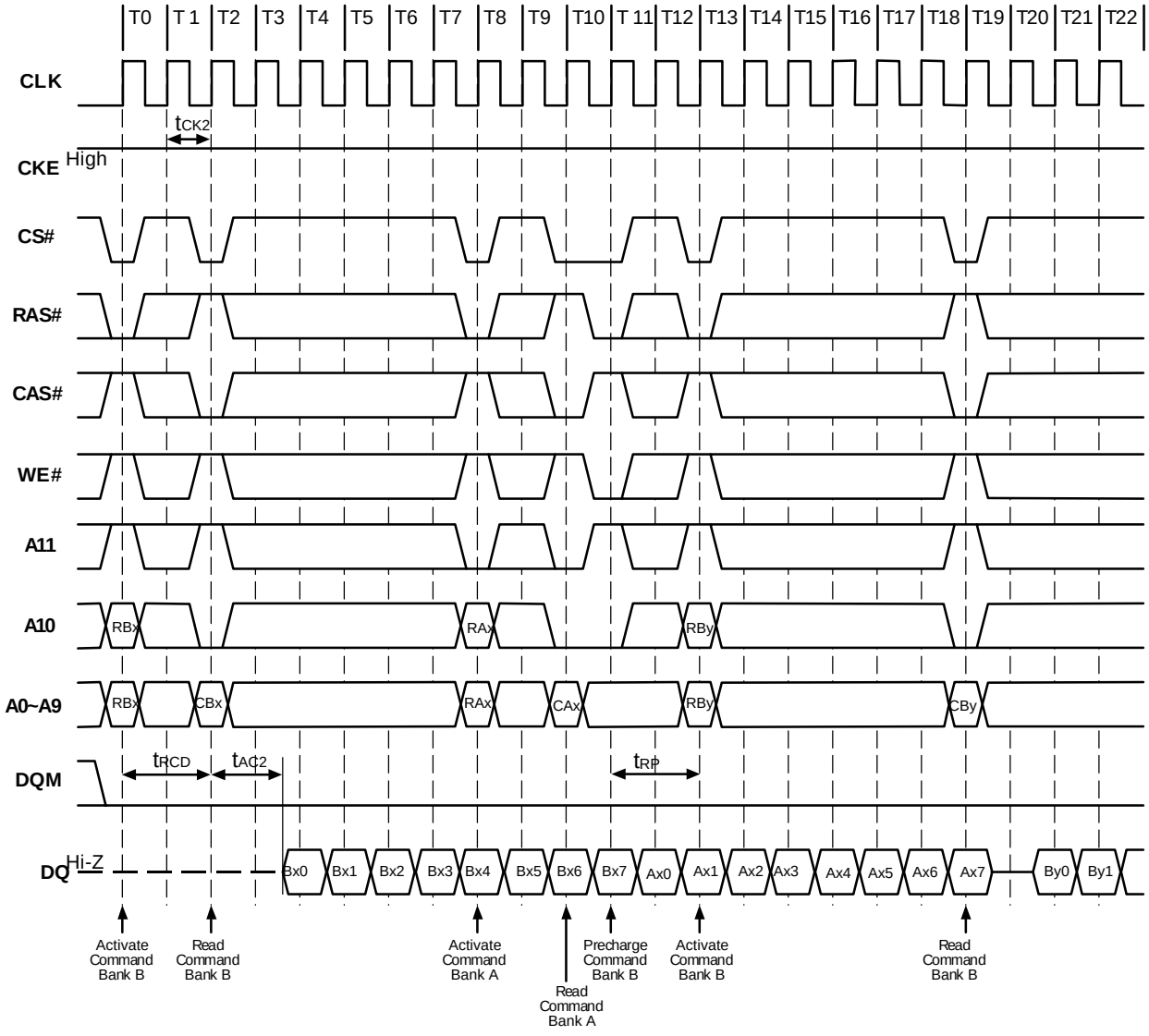


Figure 11.3. Random Row Read (Interleaving Banks)
(Burst Length=8, CAS# Latency=3)

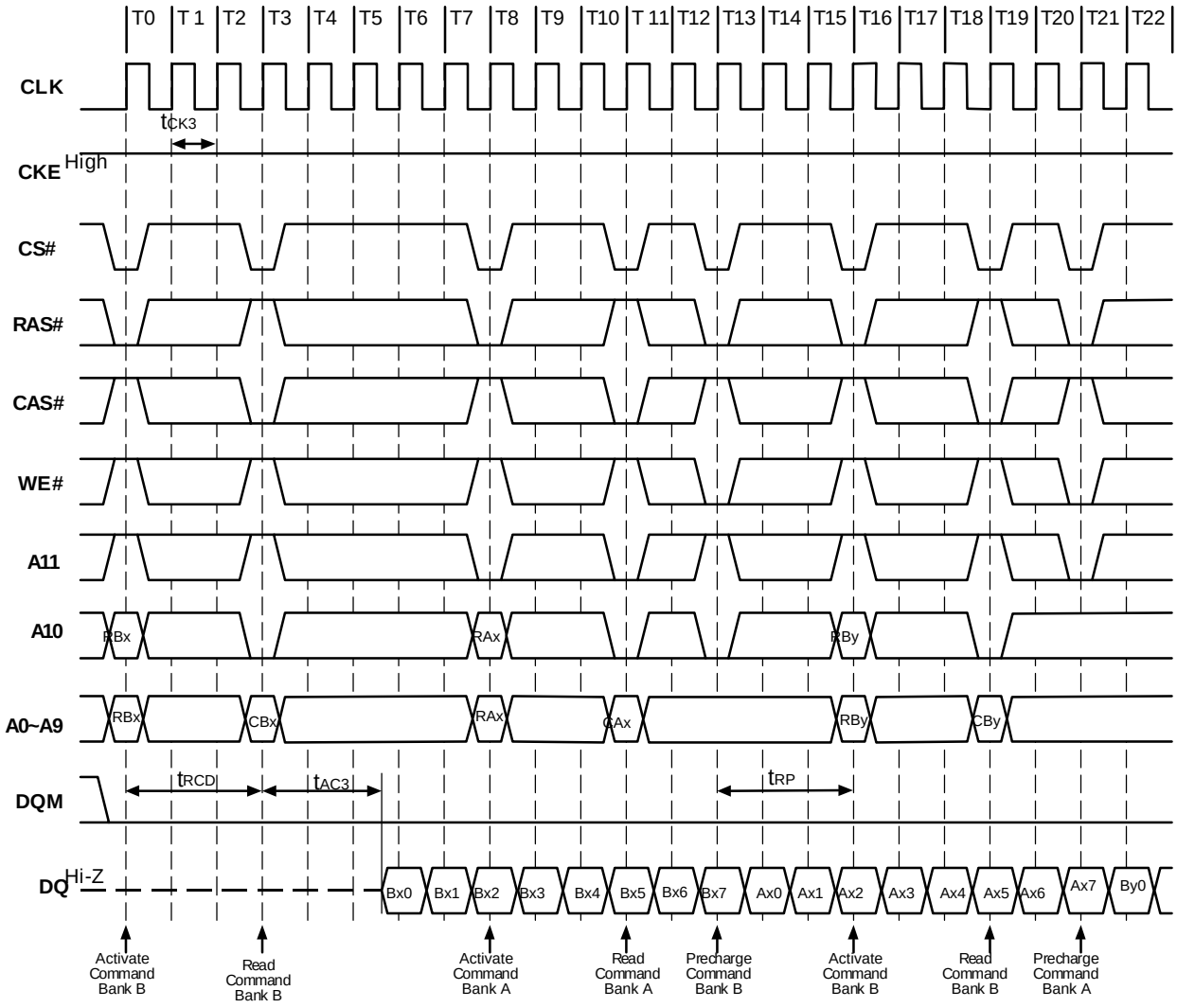


Figure 12.1. Random Row Write (Interleaving Banks)
(Burst Length=8, CAS# Latency=1)

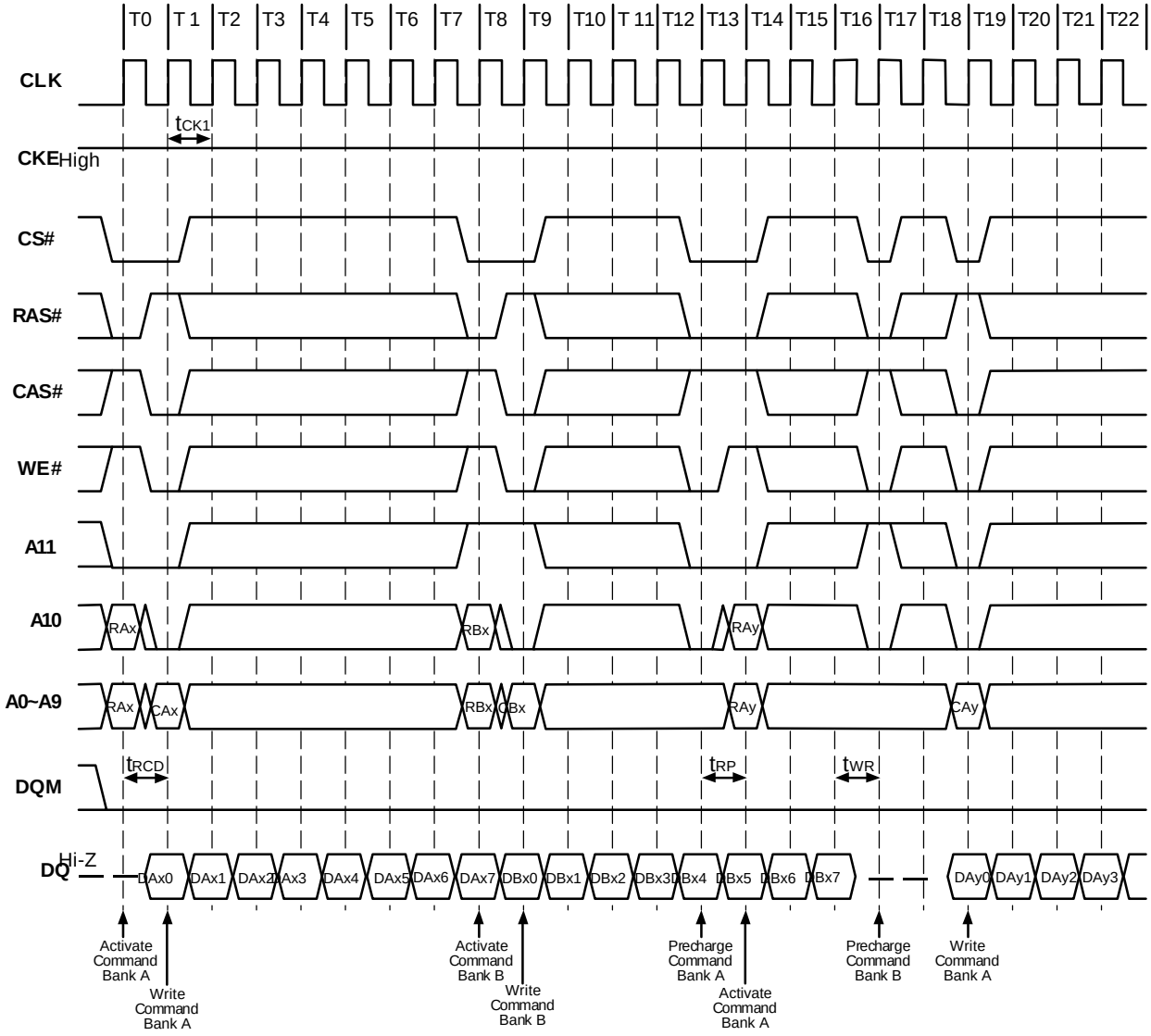
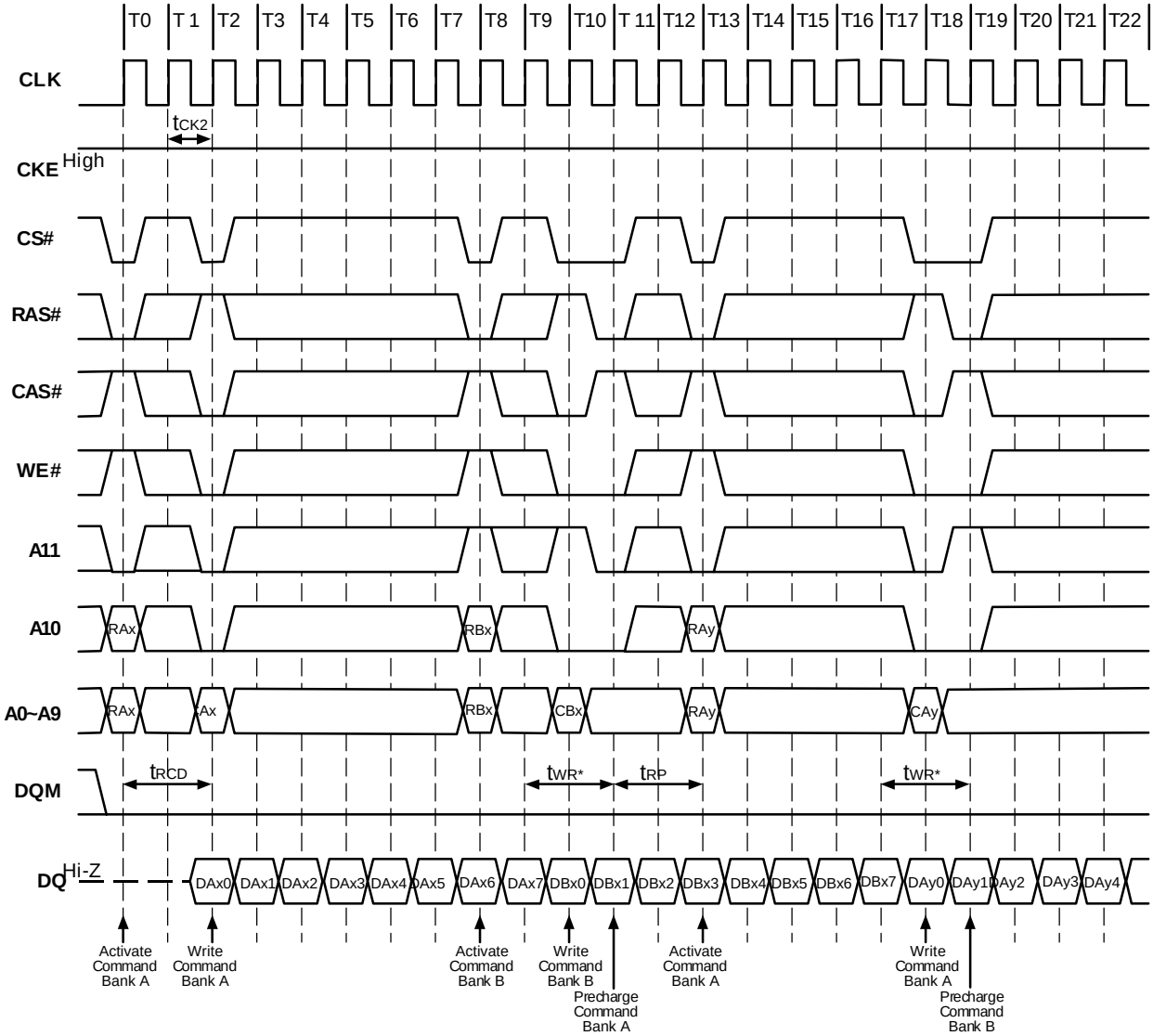
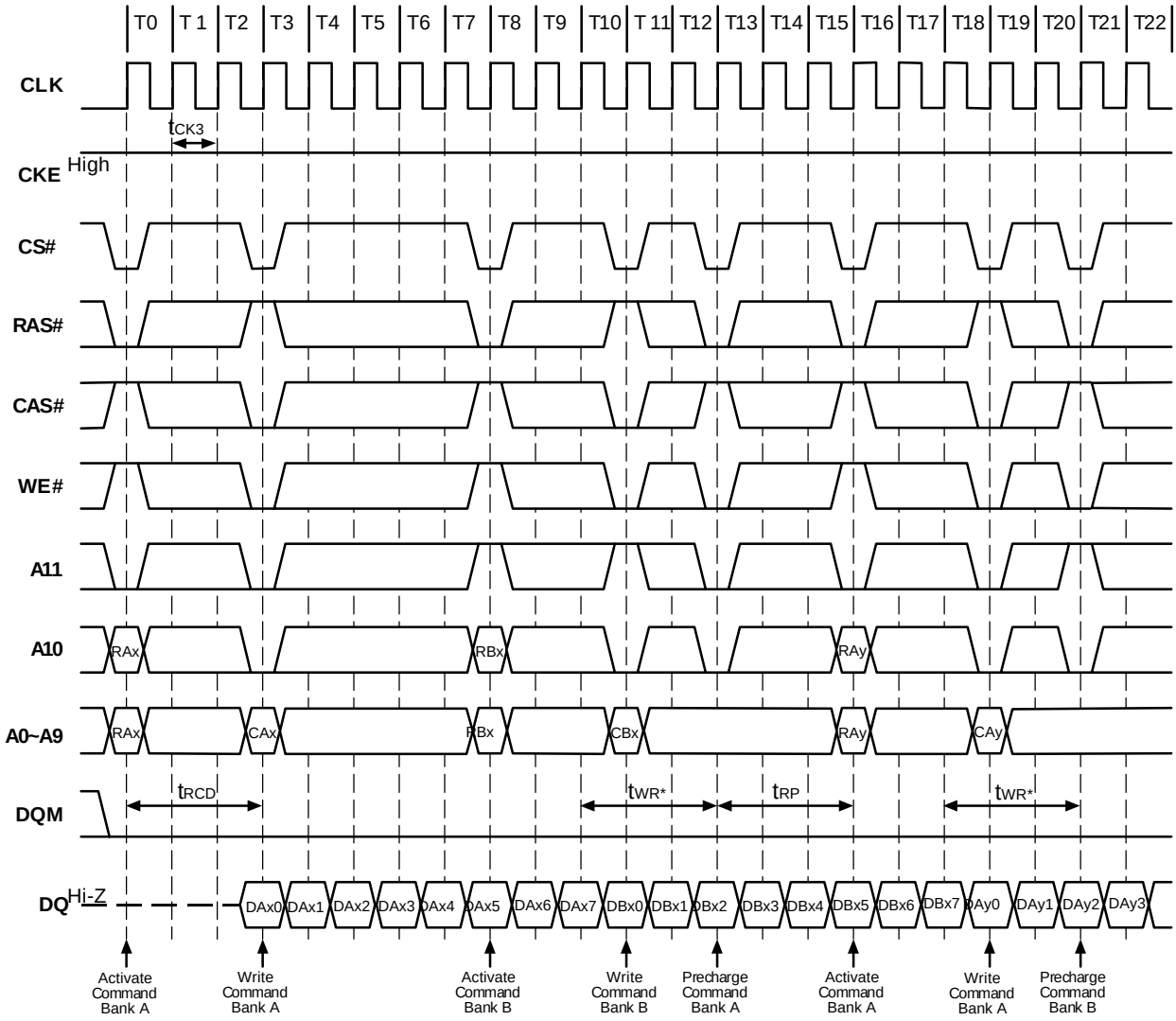


Figure 12.2. Random Row Write (Interleaving Banks)
(Burst Length=8, CAS# Latency=2)



***** $t_{WR} > t_{WR}(\text{min.})$

Figure 12.3. Random Row Write (Interleaving Banks)
(Burst Length=8, CAS# Latency=3)



* $t_{WR} > t_{WR}(min.)$

Figure 13.1. Read and Write Cycle (Burst Length=4, CAS# Latency=1)

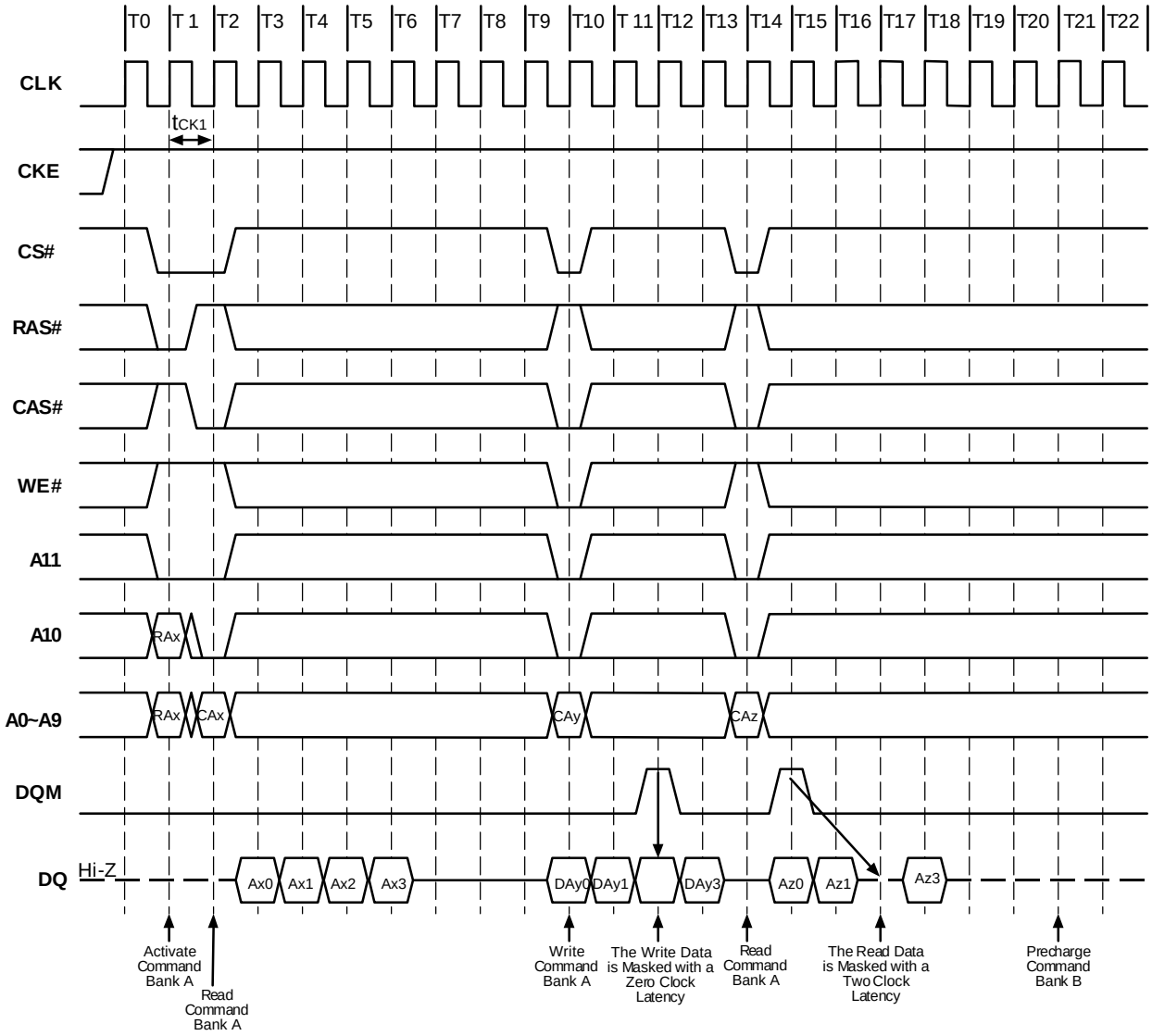


Figure 13.2. Read and Write Cycle (Burst Length=4, CAS# Latency=2)

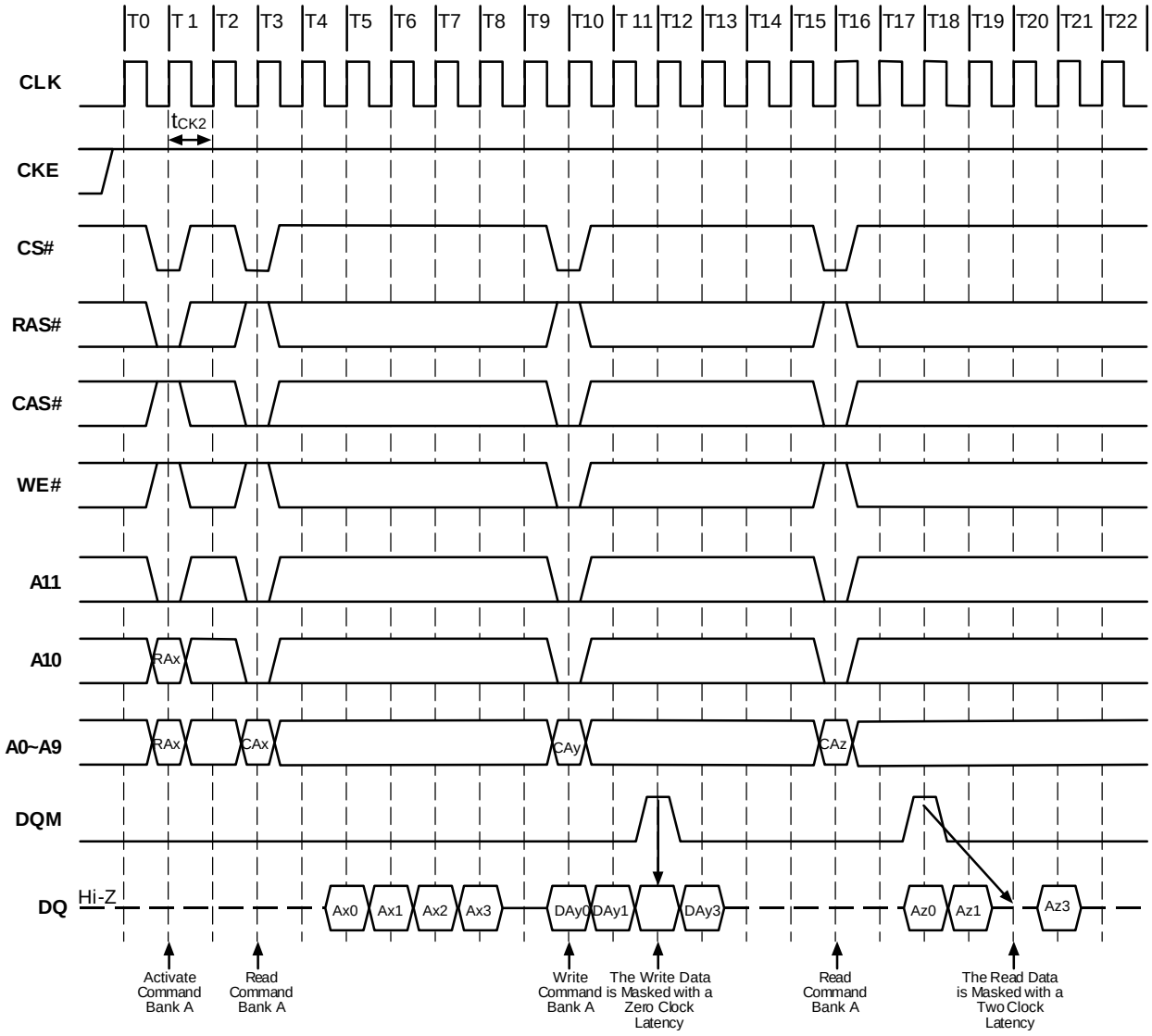


Figure 13.3. Read and Write Cycle (Burst Length=4, CAS# Latency=3)

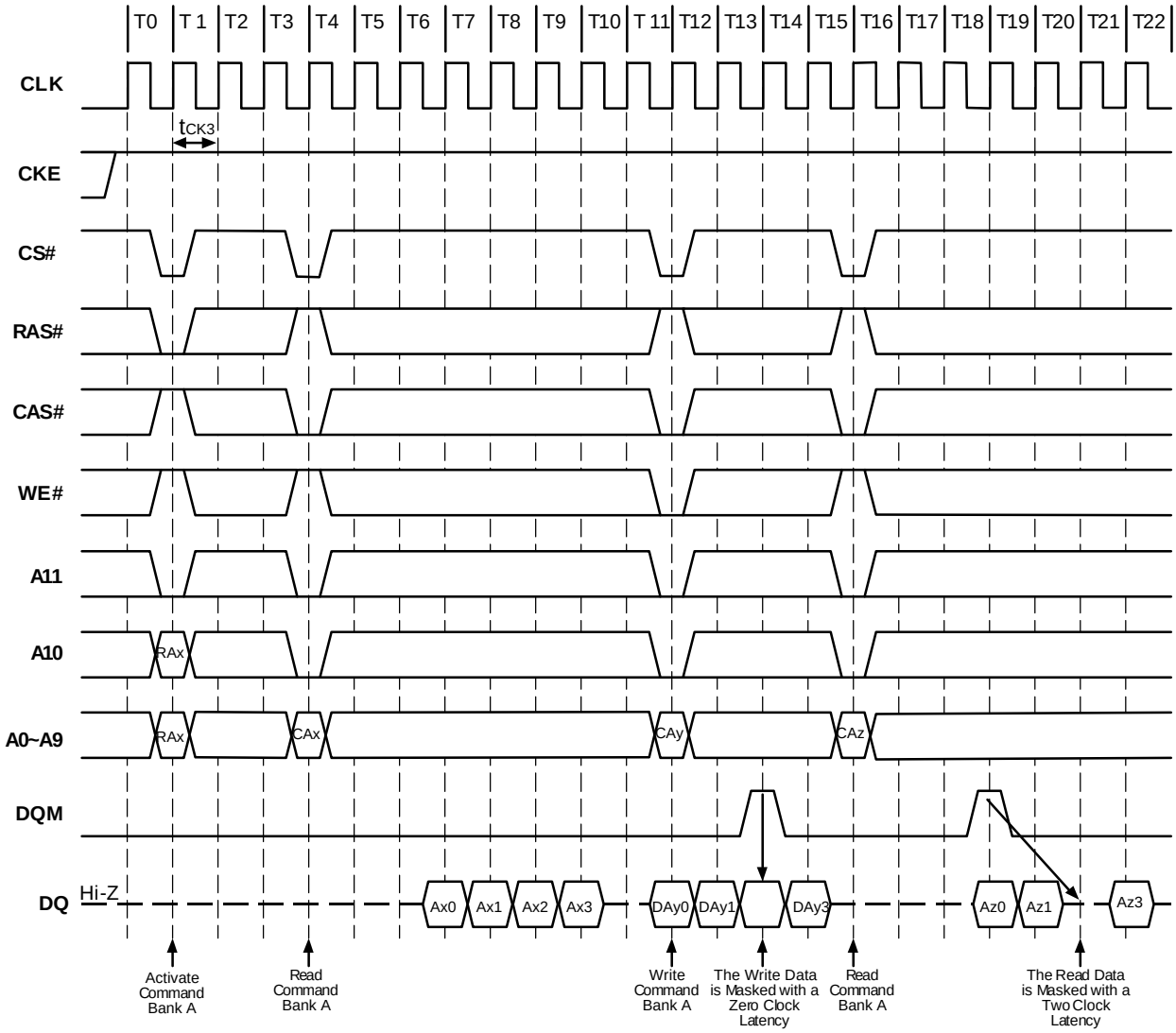


Figure 14.1. Interleaving Column Read Cycle (Burst Length=4, CAS# Latency=1)

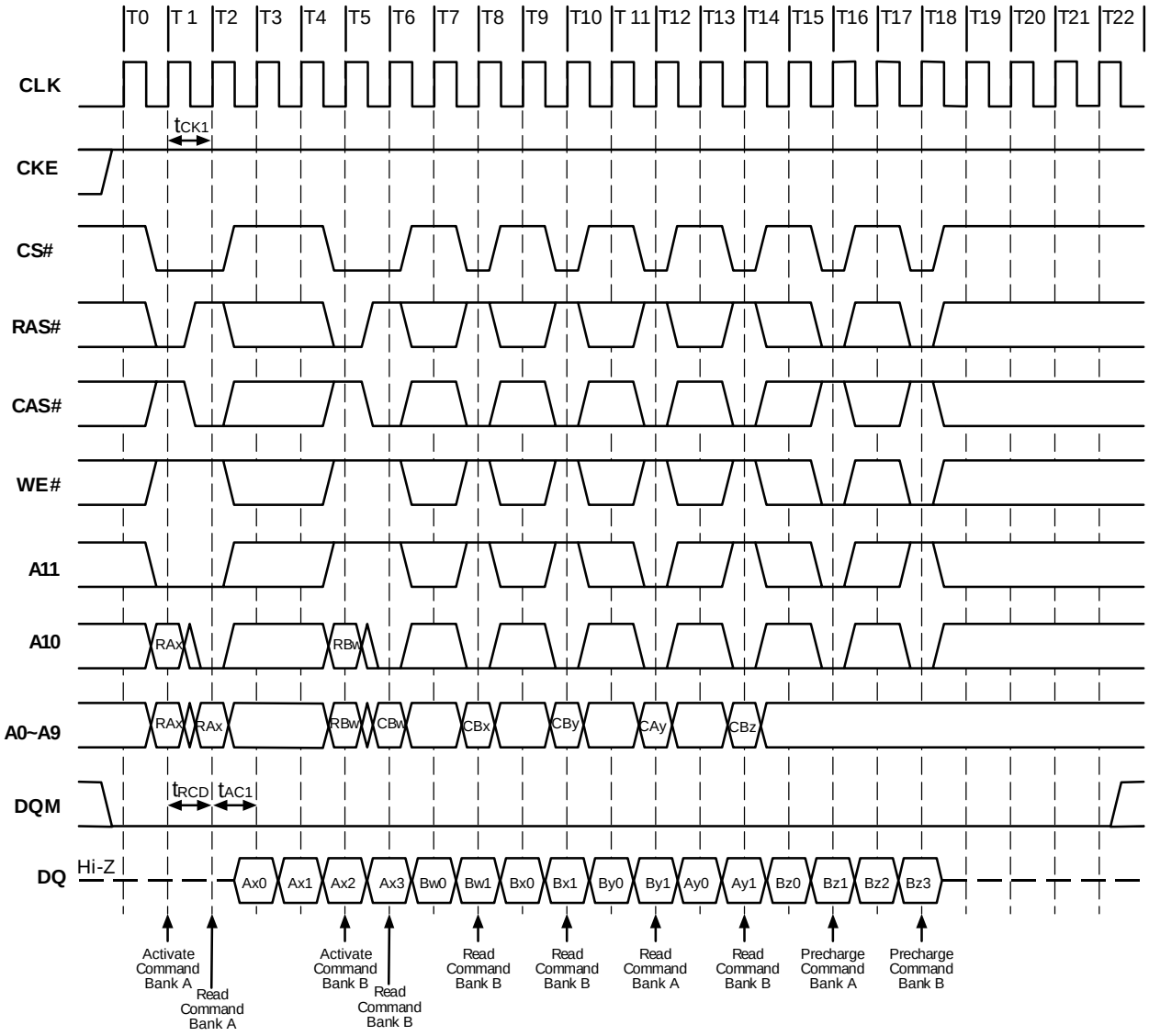


Figure 14.2. Interleaving Column Read Cycle (Burst Length=4, CAS# Latency=2)

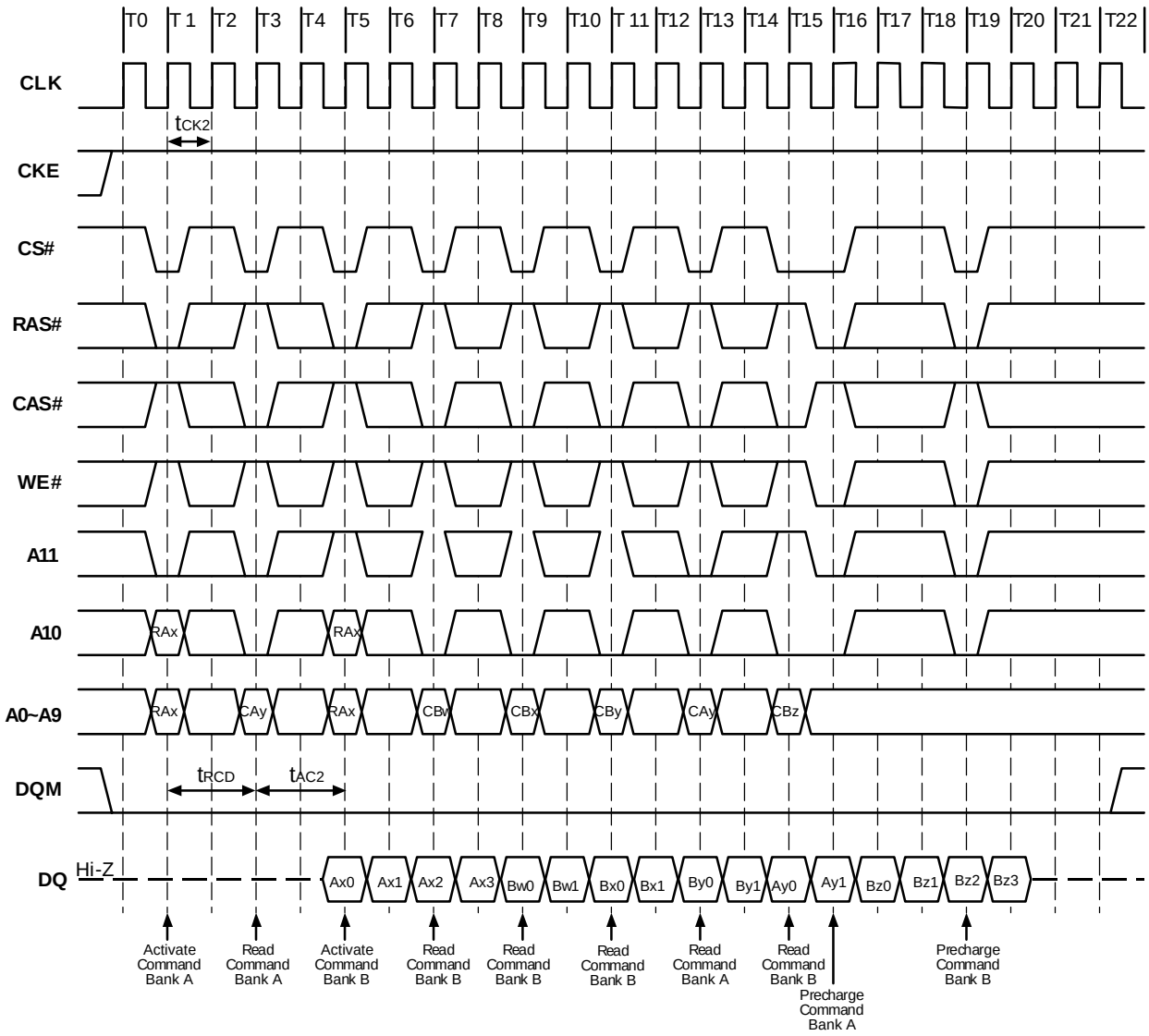


Figure 14.3. Interleaved Column Read Cycle (Burst Length=4, CAS# Latency=3)

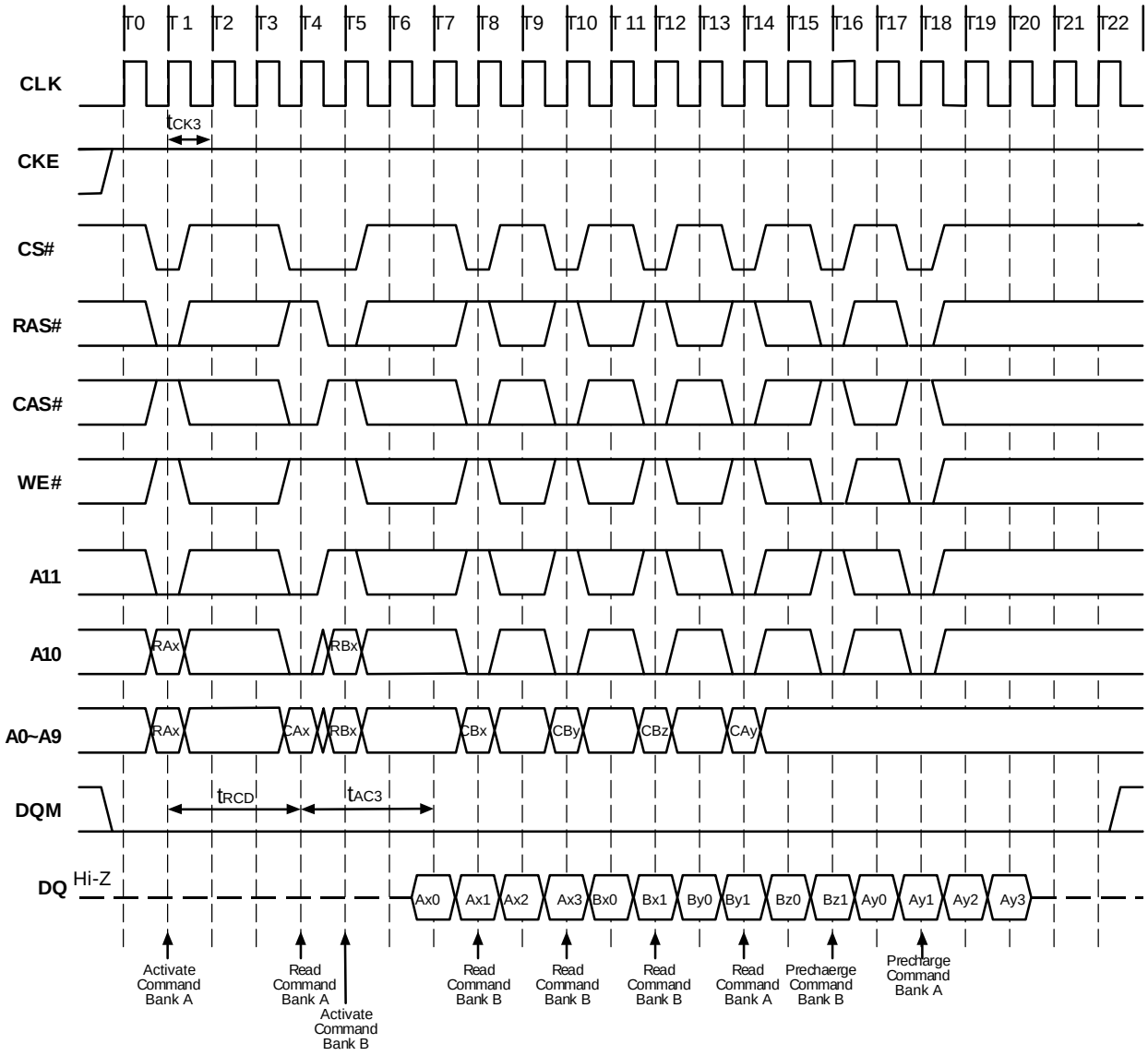


Figure 15.1. Interleaved Column Write Cycle (Burst Length=4, CAS# Latency=1)

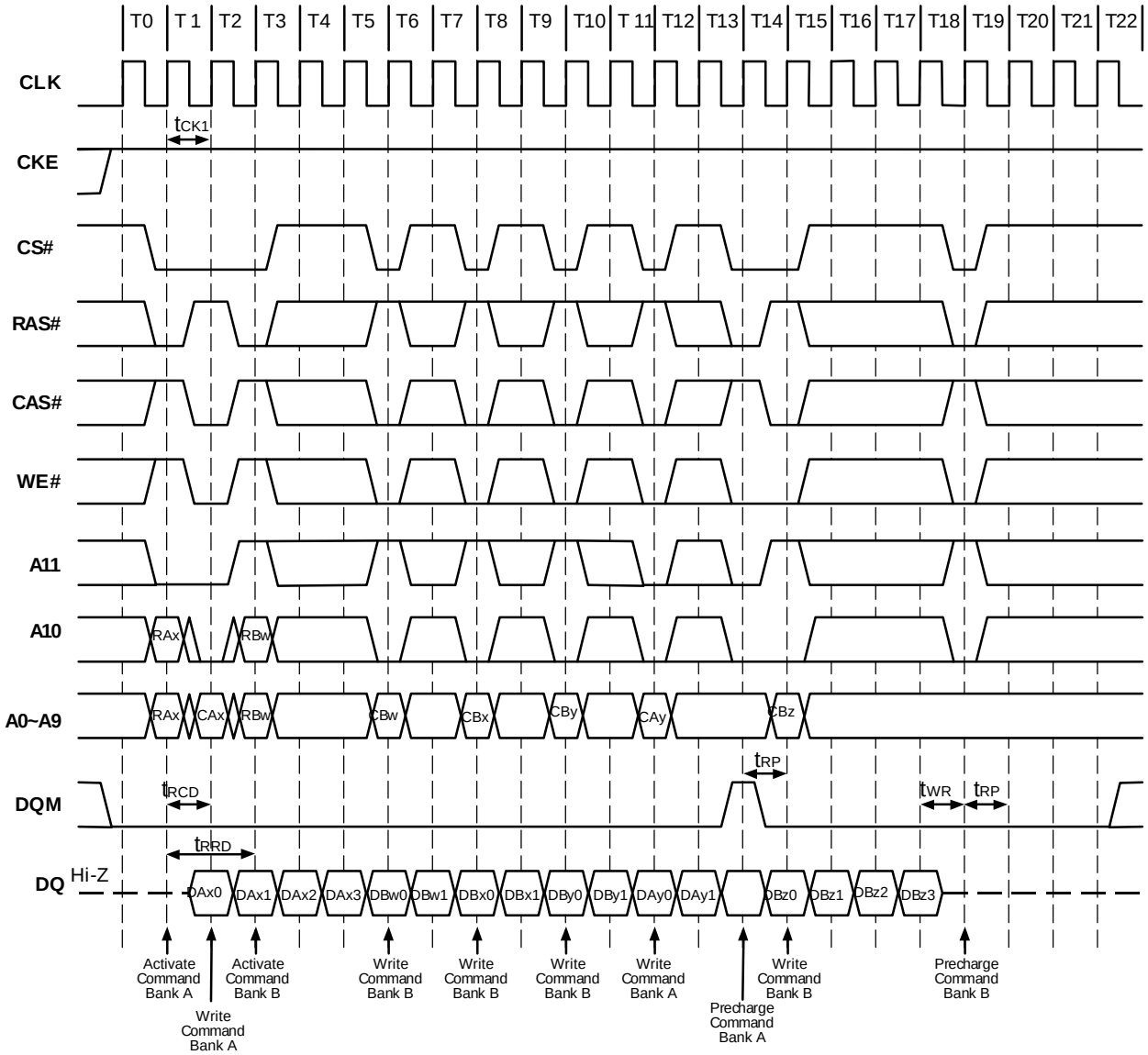


Figure 15.2. Interleaved Column Write Cycle (Burst Length=4, CAS# Latency=2)

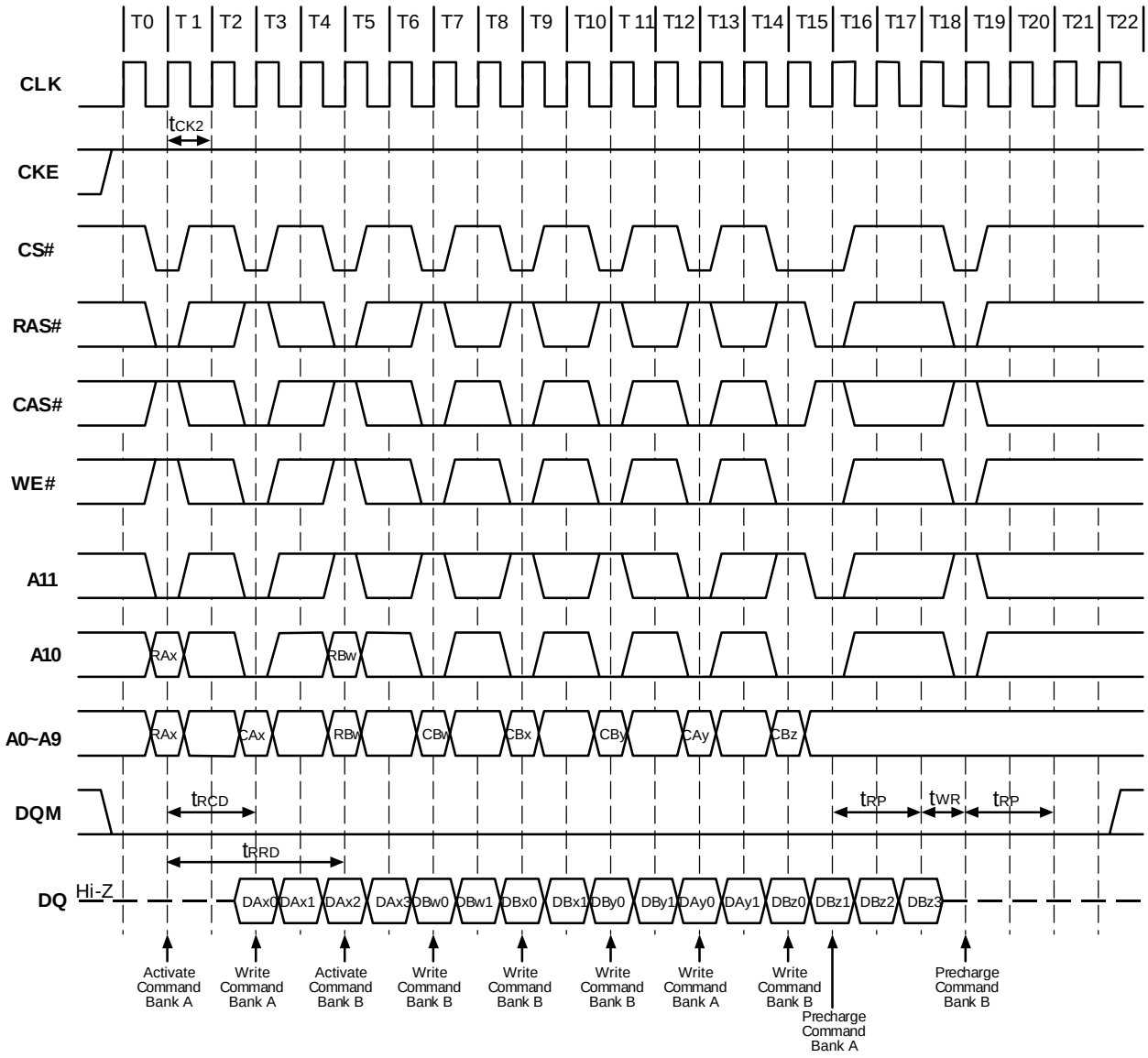


Figure 15.3. Interleaved Column Write Cycle (Burst Length=4, CAS# Latency=3)

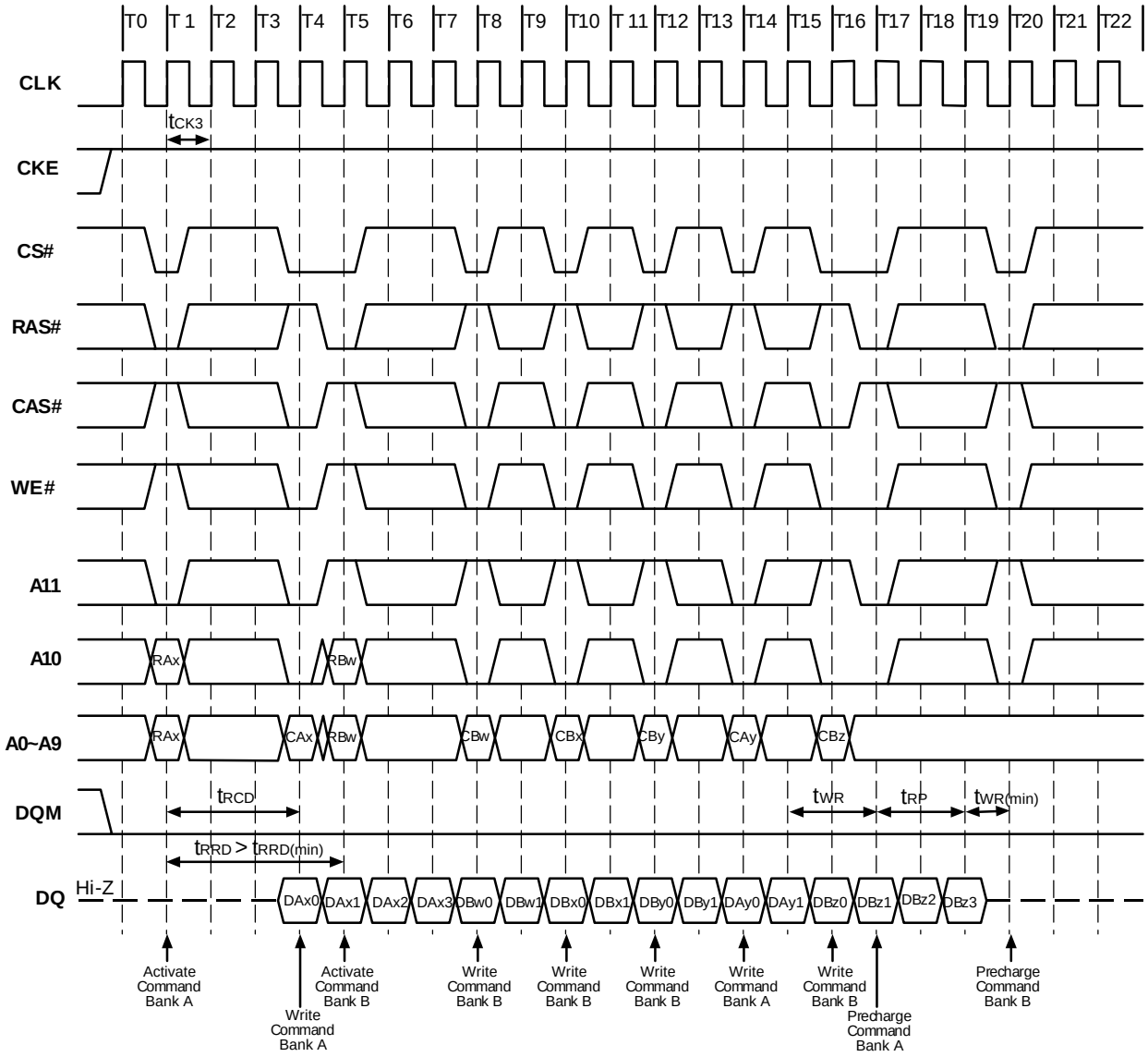


Figure 16.1. Auto Precharge after Read Burst (Burst Length=4, CAS# Latency=1)

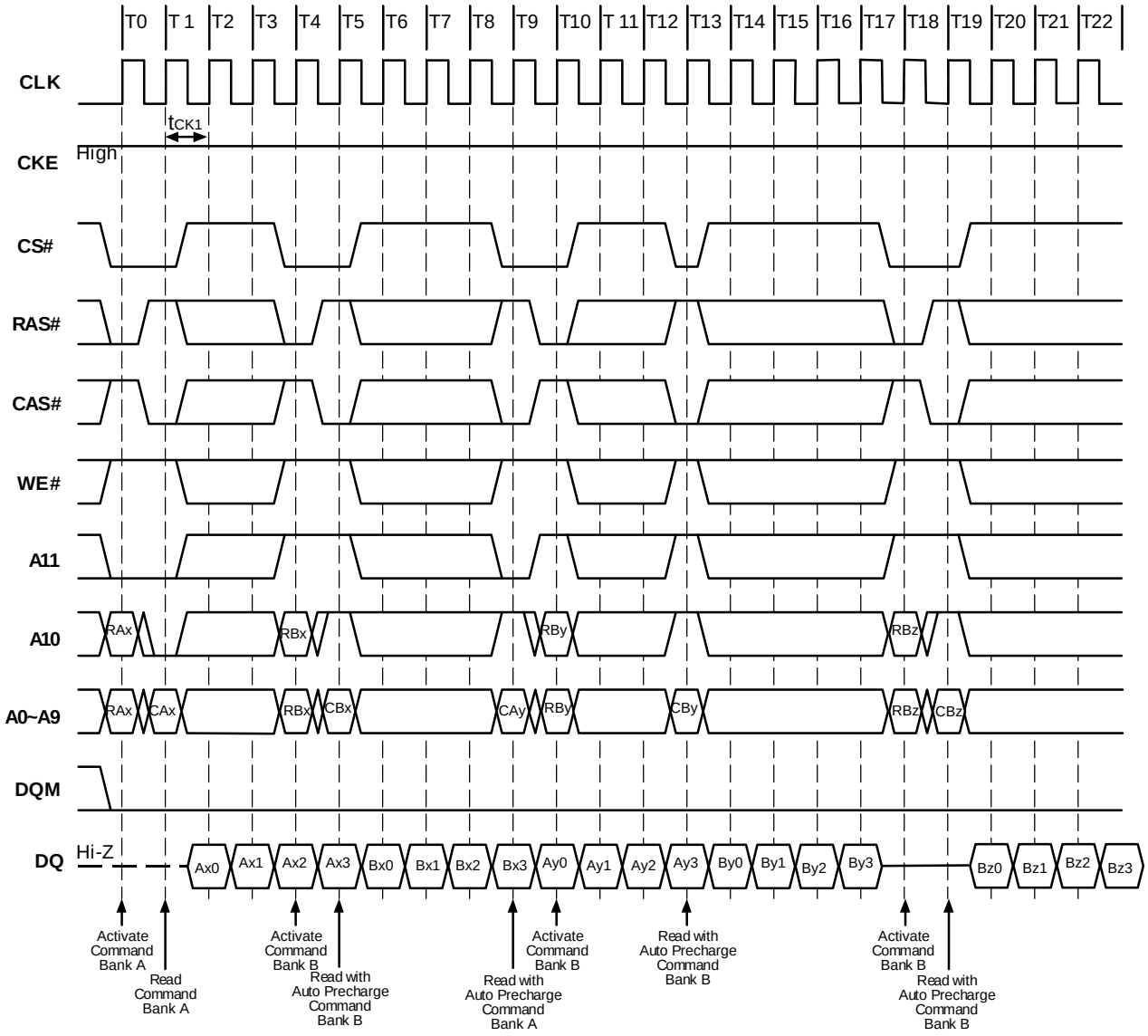


Figure 16.2. Auto Precharge after Read Burst (Burst Length=4, CAS# Latency=2)

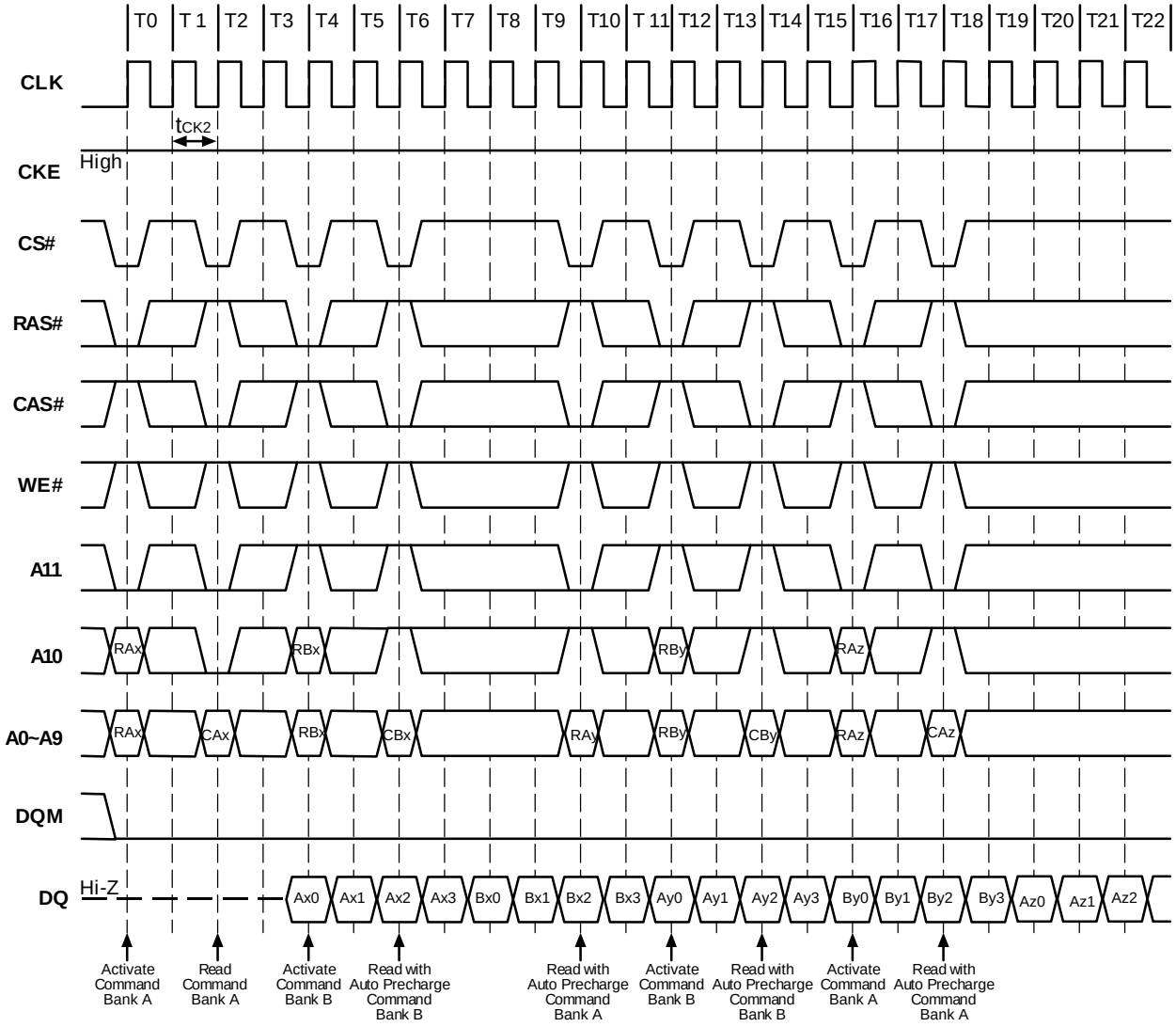


Figure 16.3. Auto Precharge after Read Burst (Burst Length=4, CAS# Latency=3)

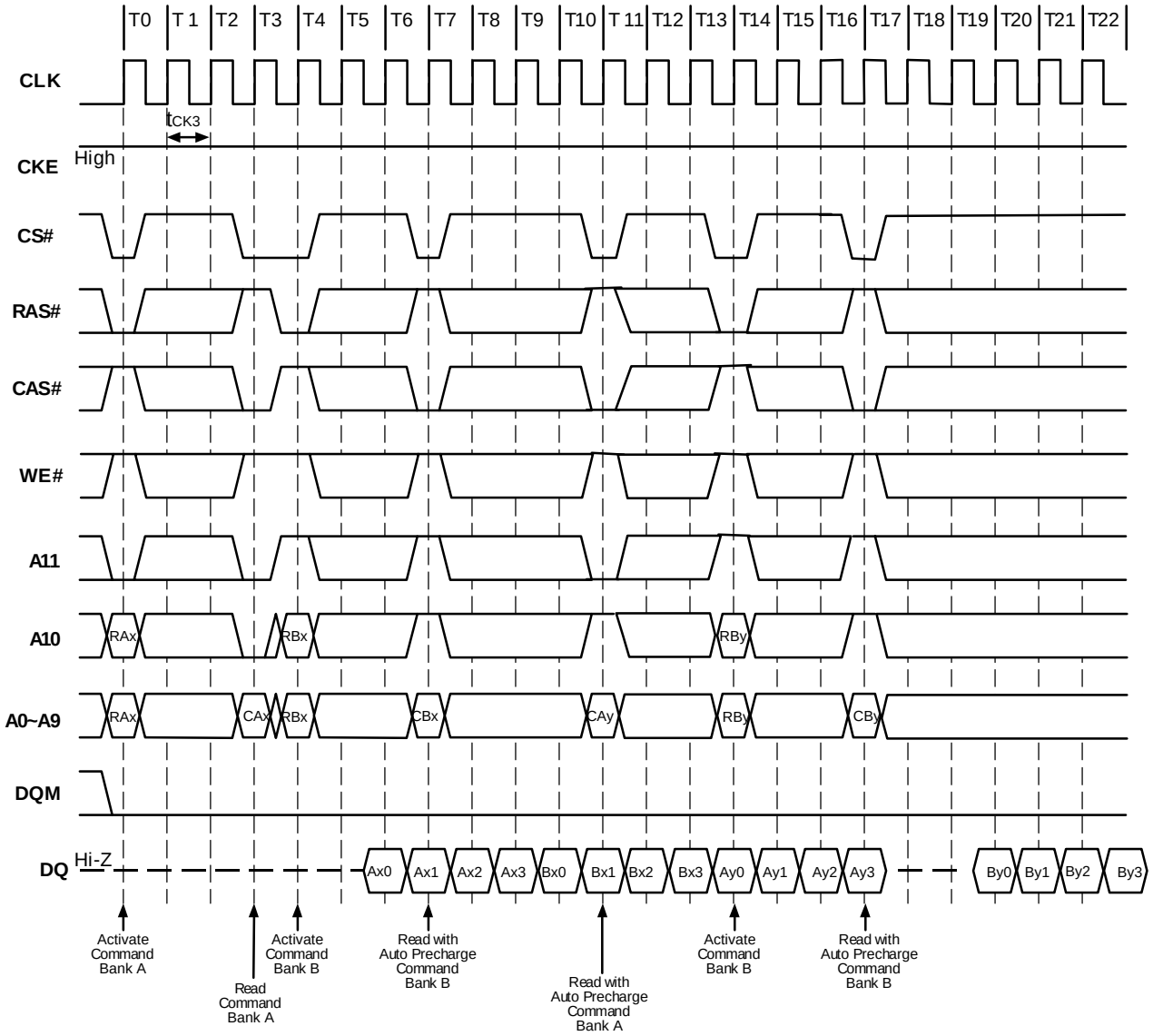


Figure 17.1. Auto Precharge after Write Burst (Burst Length=4, CAS# Latency=1)

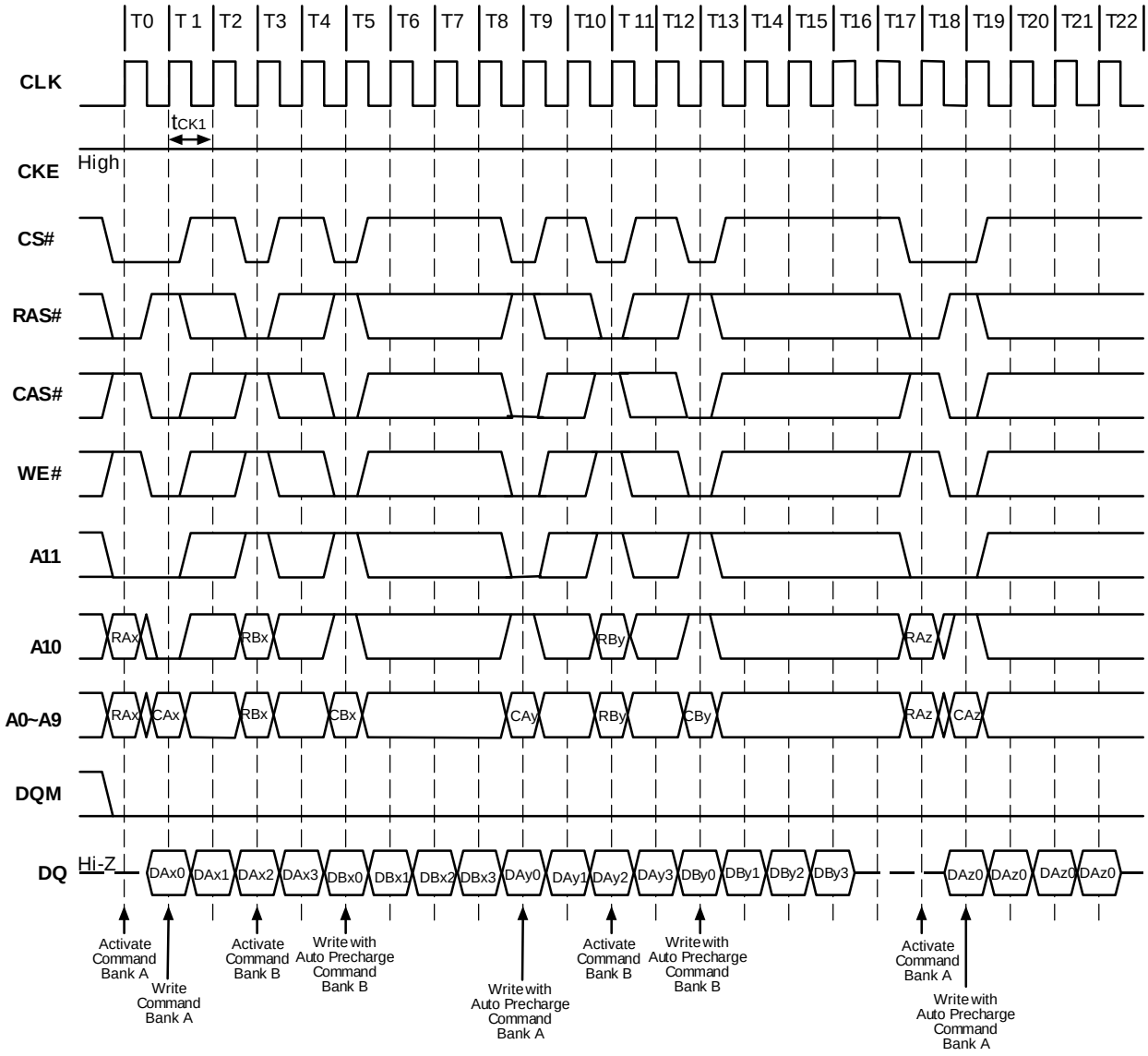


Figure 17.2. Auto Precharge after Write Burst (Burst Length=4, CAS# Latency=2)

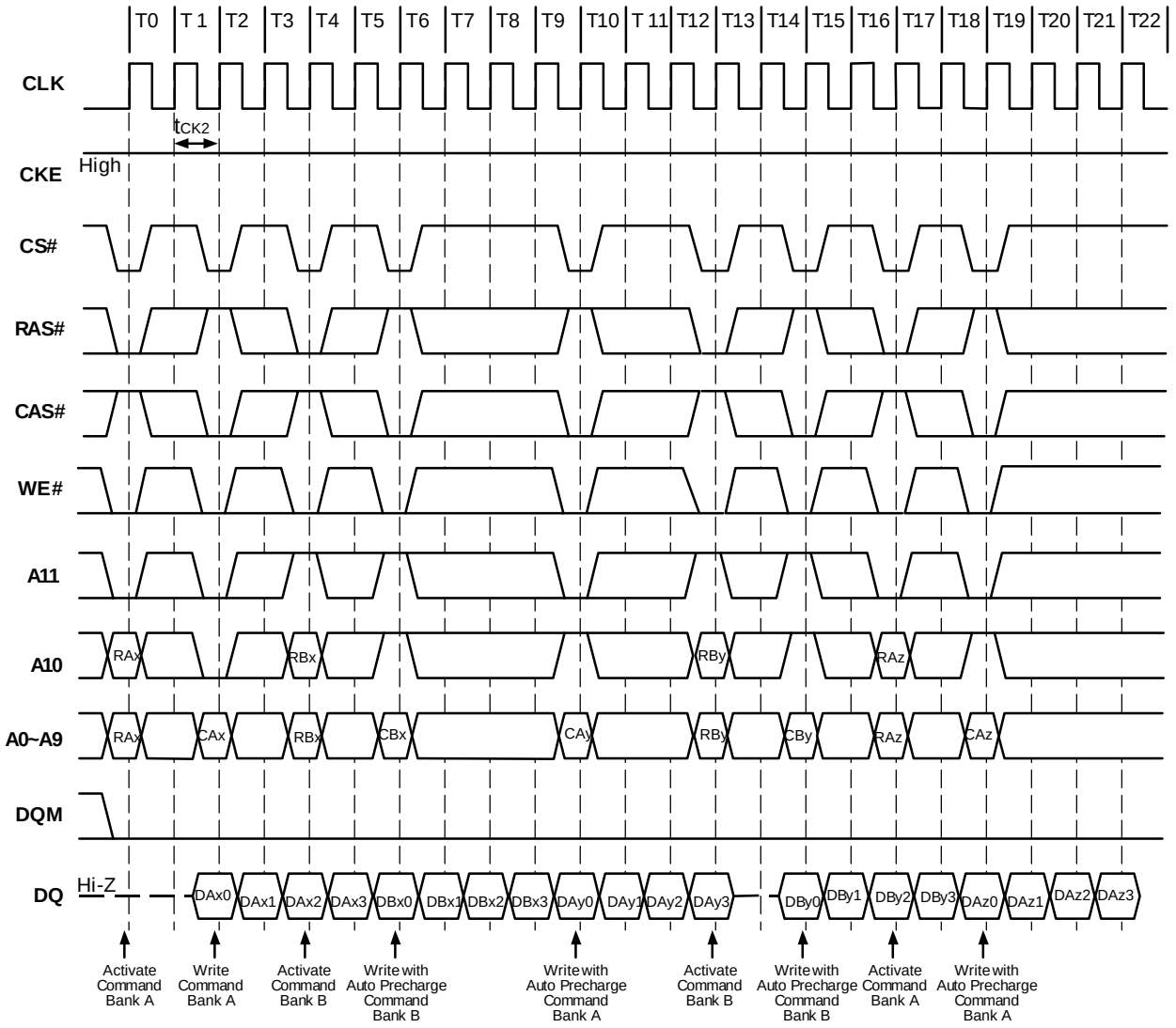


Figure 17.3. Auto Precharge after Write Burst (Burst Length=4, CAS# Latency=3)

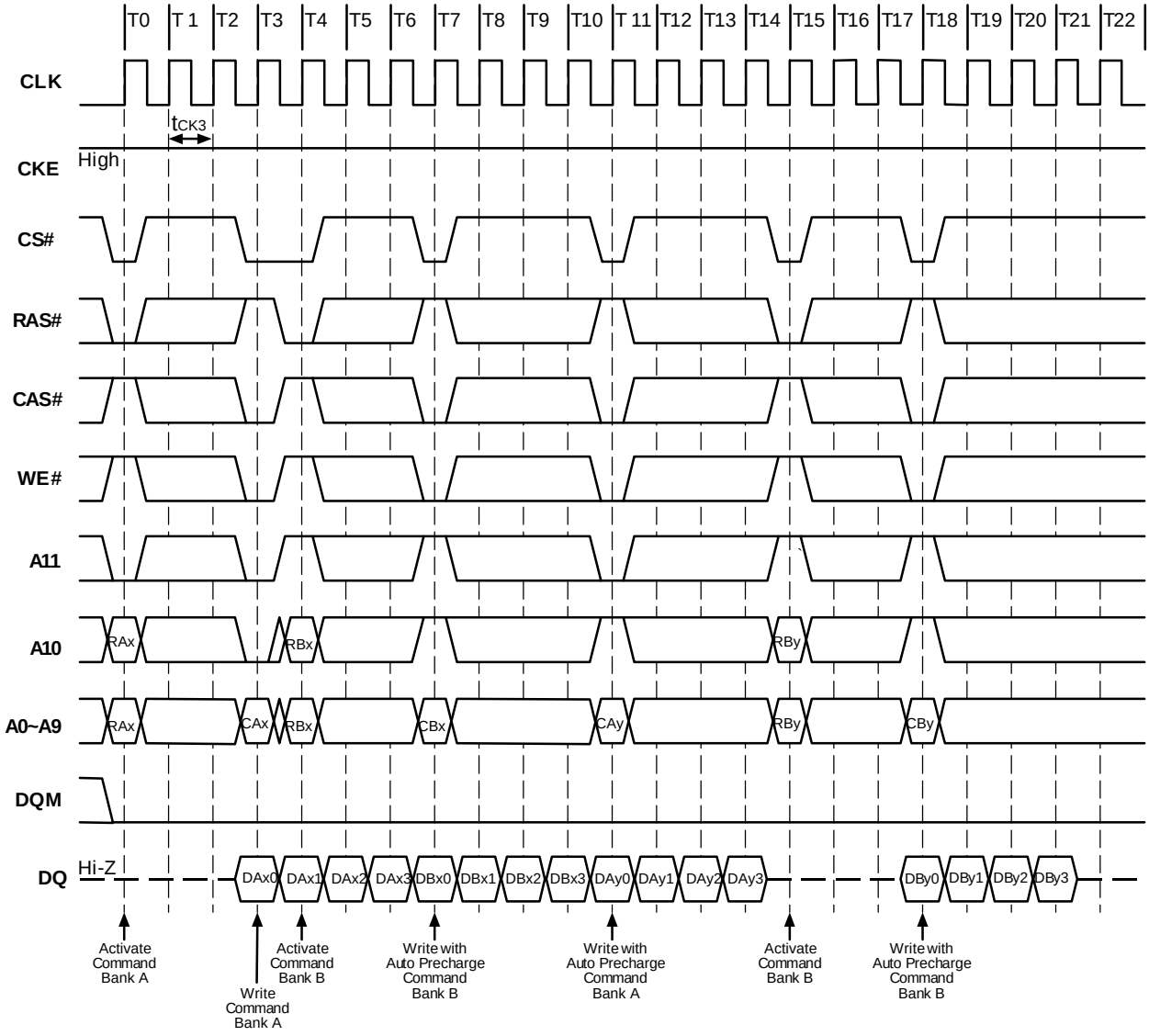


Figure 18.1. Full Page Read Cycle (Burst Length=Full Page, CAS# Latency=1)

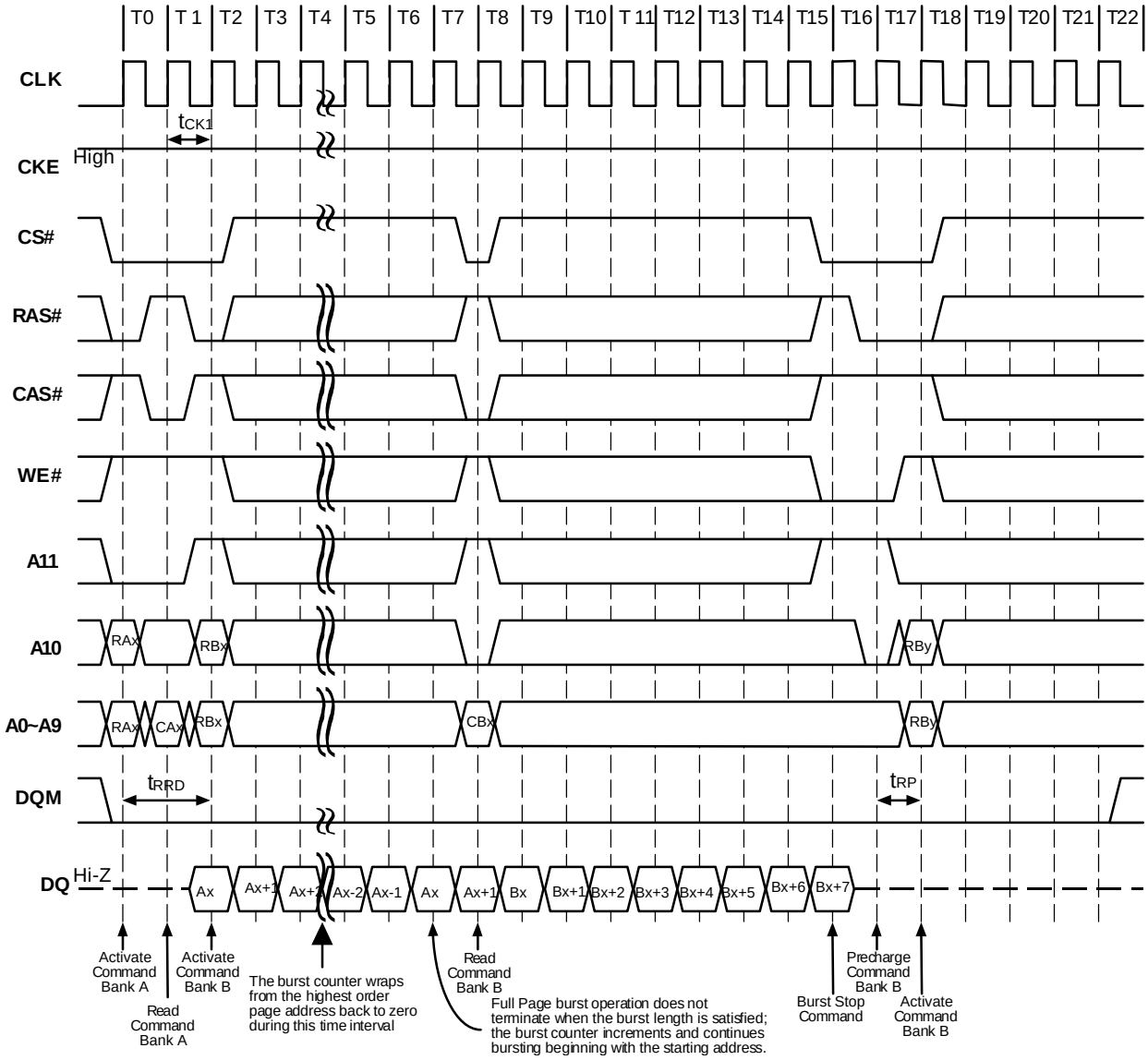


Figure 18.2. Full Page Read Cycle (Burst Length=Full Page, CAS# Latency=2)

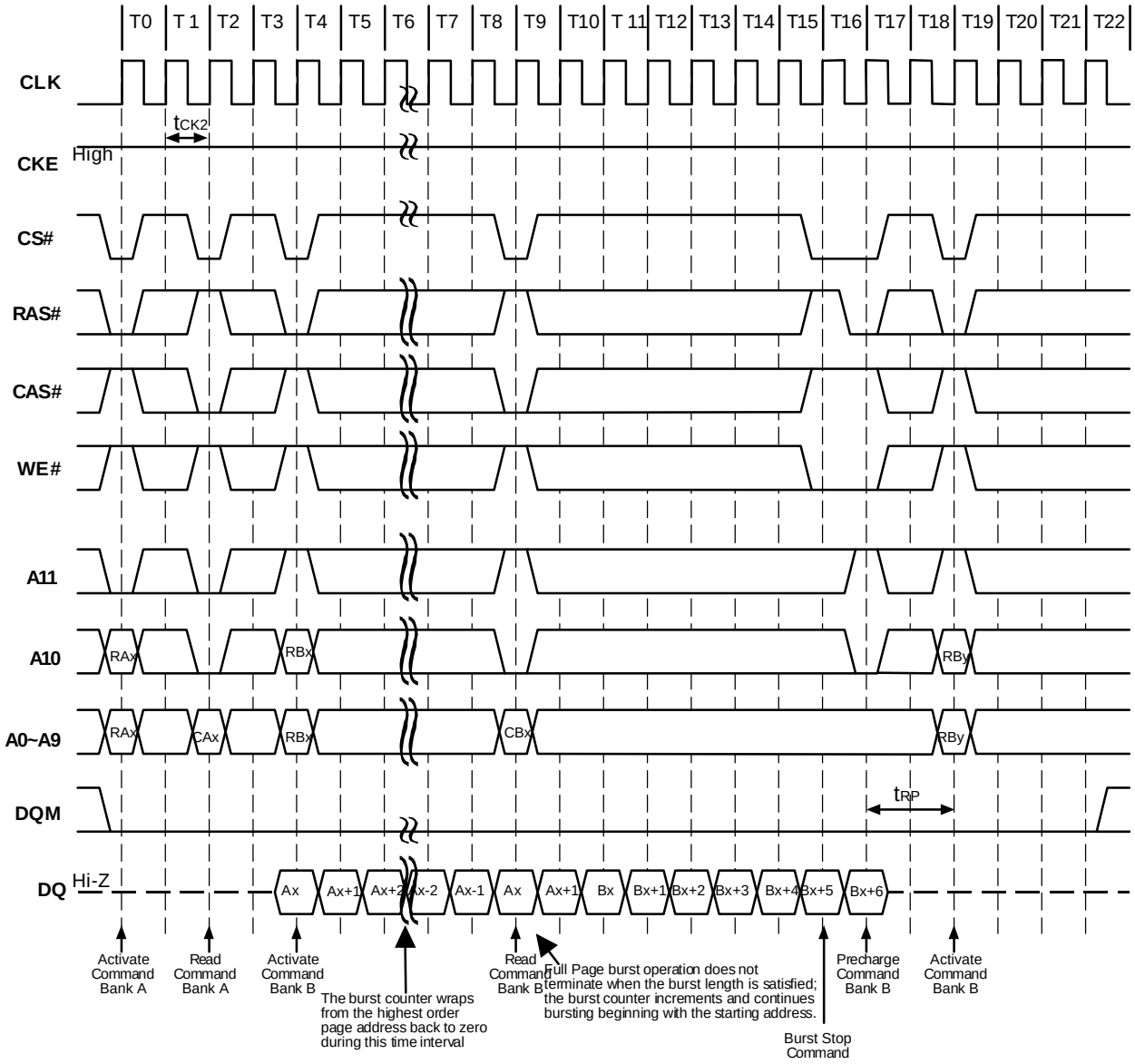


Figure 18.3. Full Page Read Cycle (Burst Length=Full Page, CAS# Latency=3)

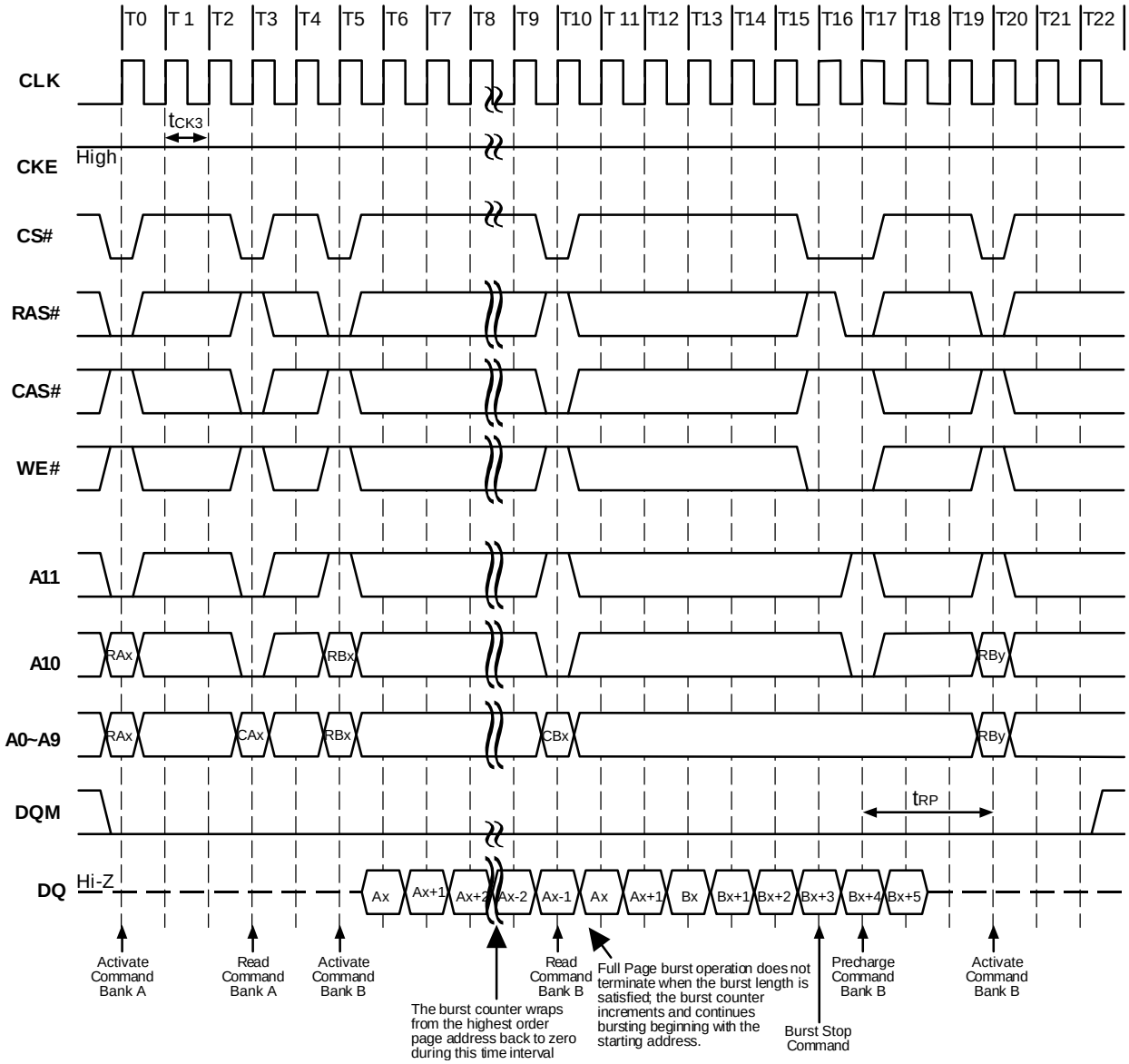


Figure 19.1. Full Page Write Cycle (Burst Length=Full Page, CAS# Latency=1)

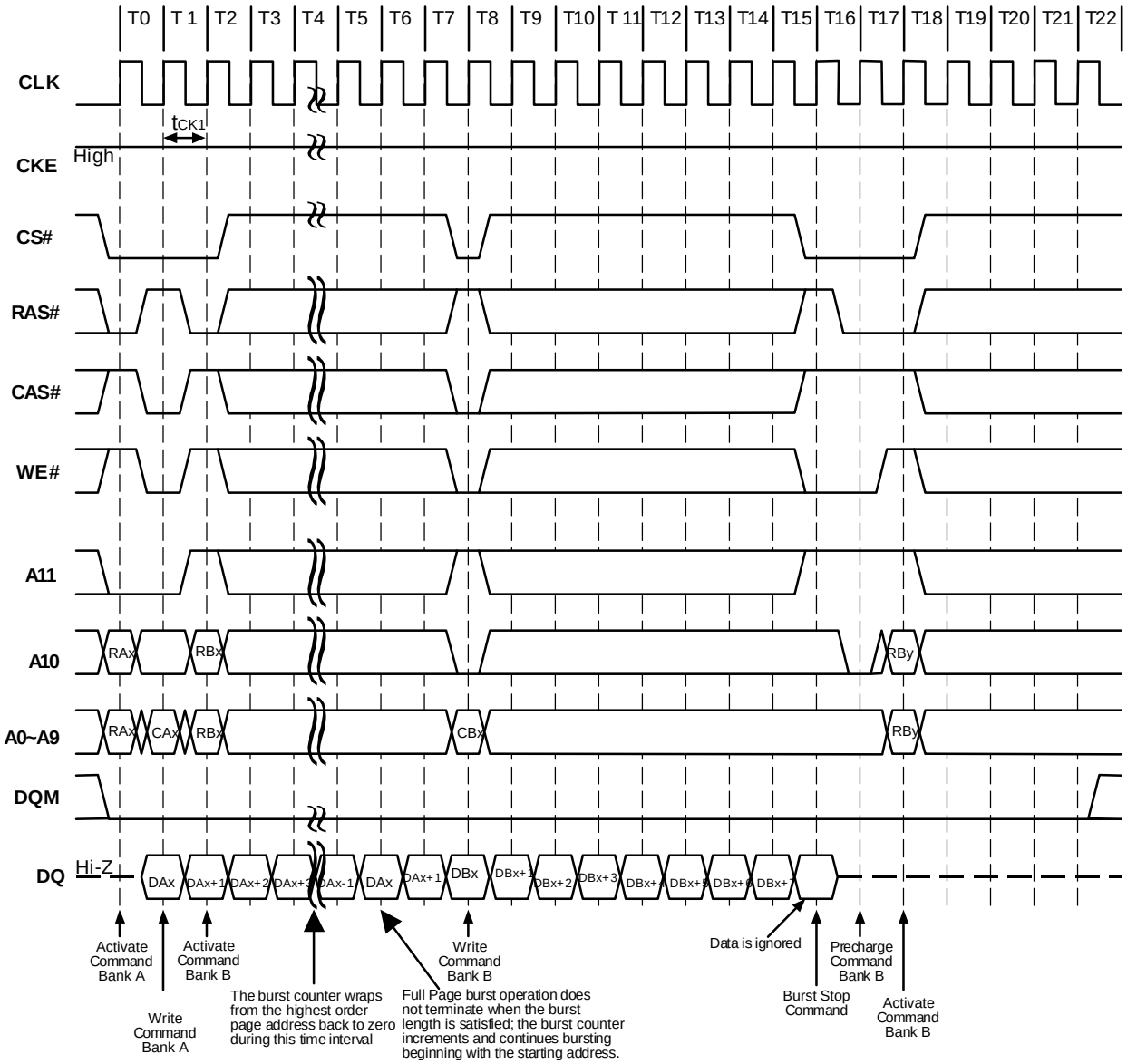


Figure 19.2. Full Page Write Cycle (Burst Length=Full Page, CAS# Latency=2)

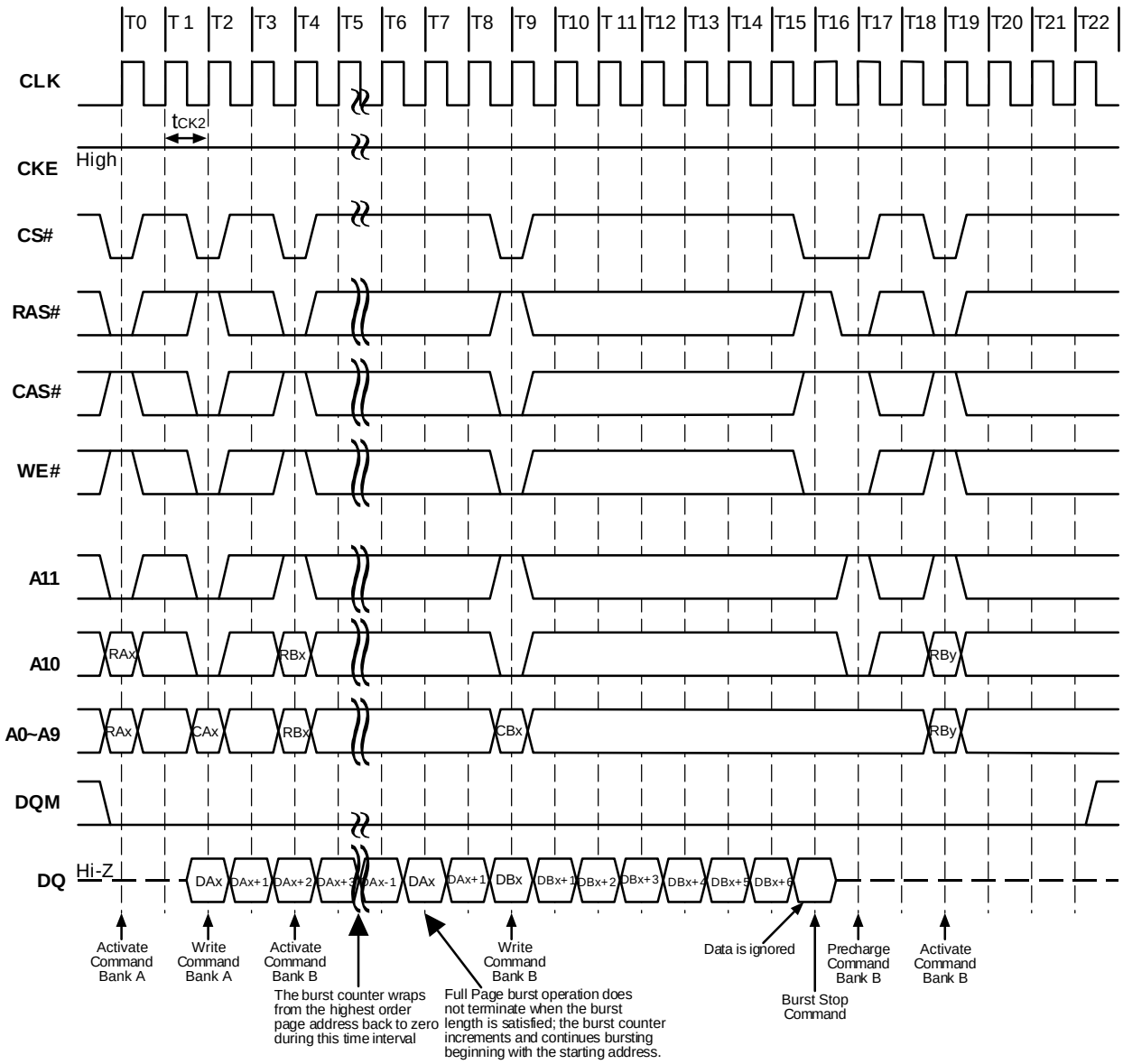


Figure 19.3. Full Page Write Cycle (Burst Length=Full Page, CAS# Latency=3)

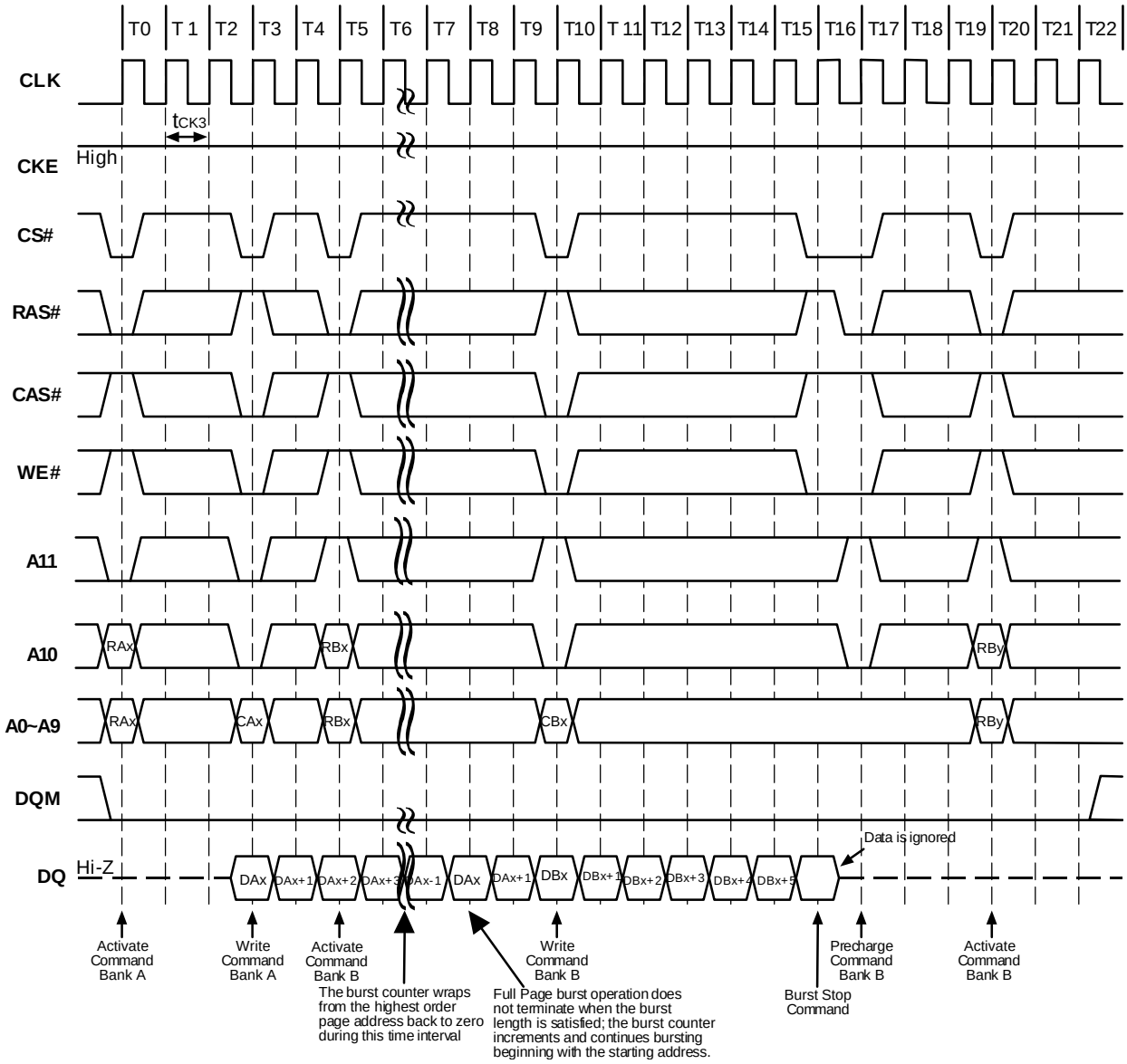


Figure 20. Byte Write Operation (Burst Length=4, CAS# Latency=2)

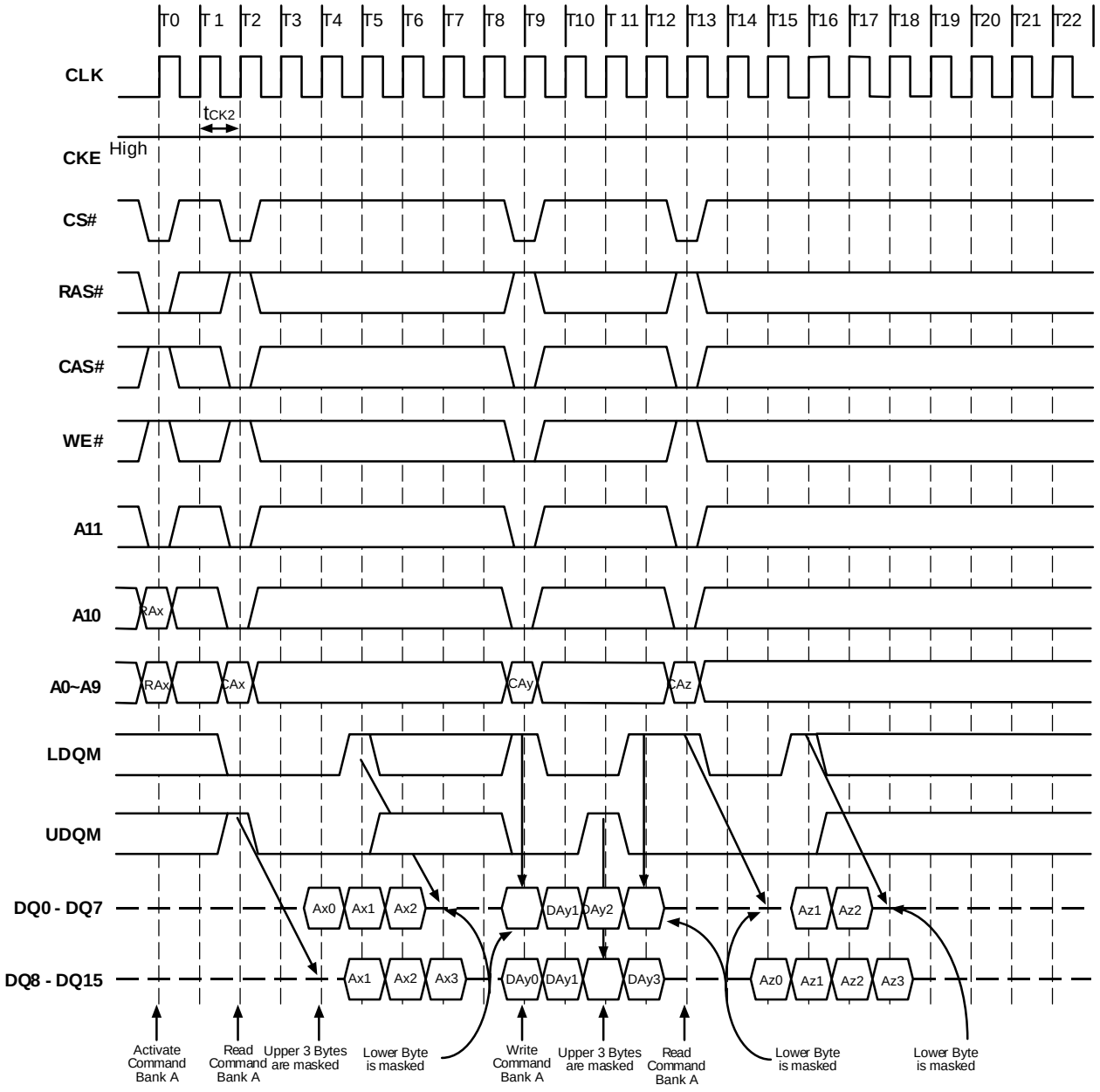


Figure 21. Random Row Read (Interleaving Banks)

(Burst Length=2, CAS# Latency=1)

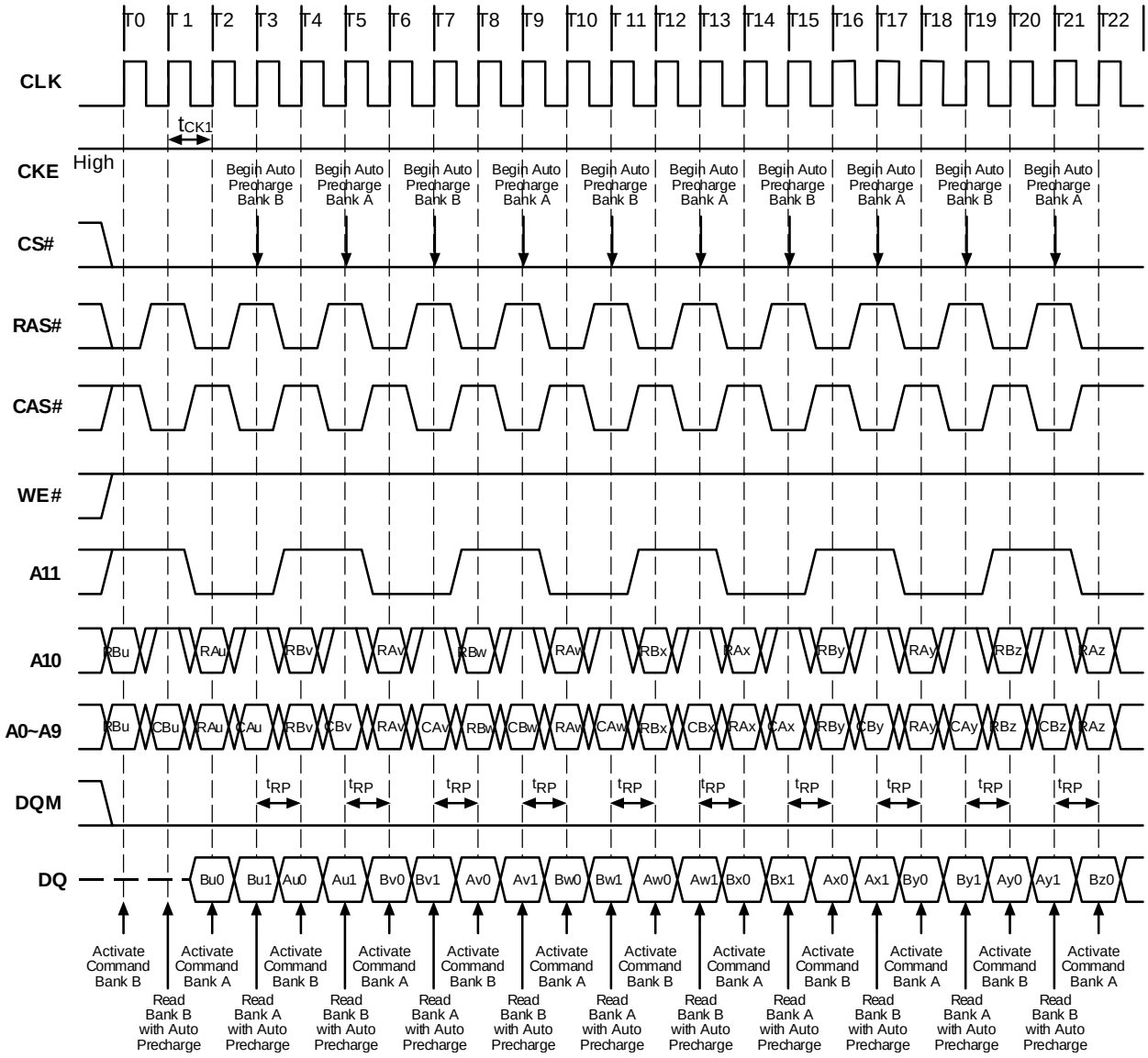


Figure 22. Full Page Random Column Read (Burst Length=Full Page, CAS# Latency=2)

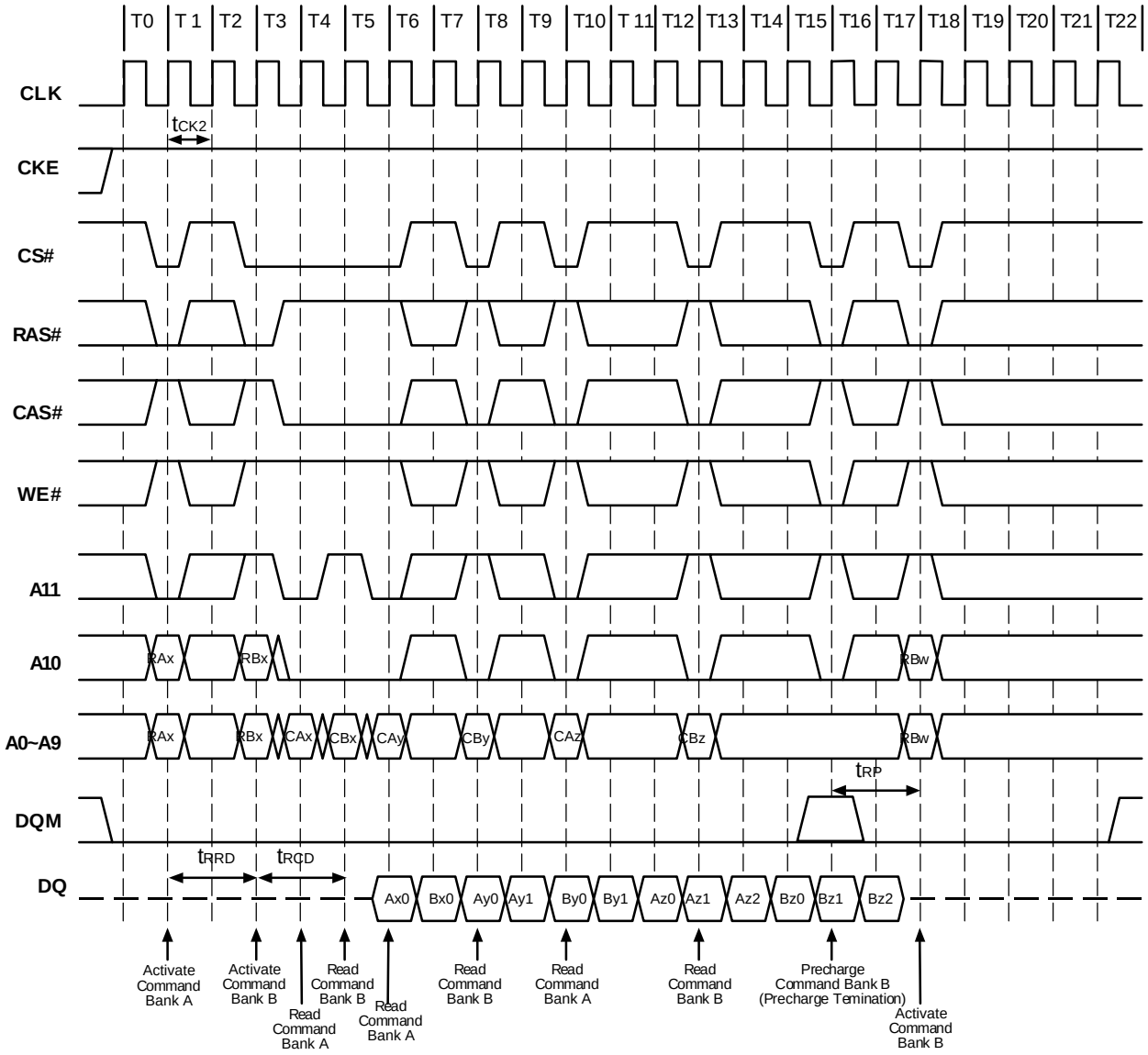


Figure 23. Full Page Random Column Write (Burst Length=Full Page, CAS# Latency=2)

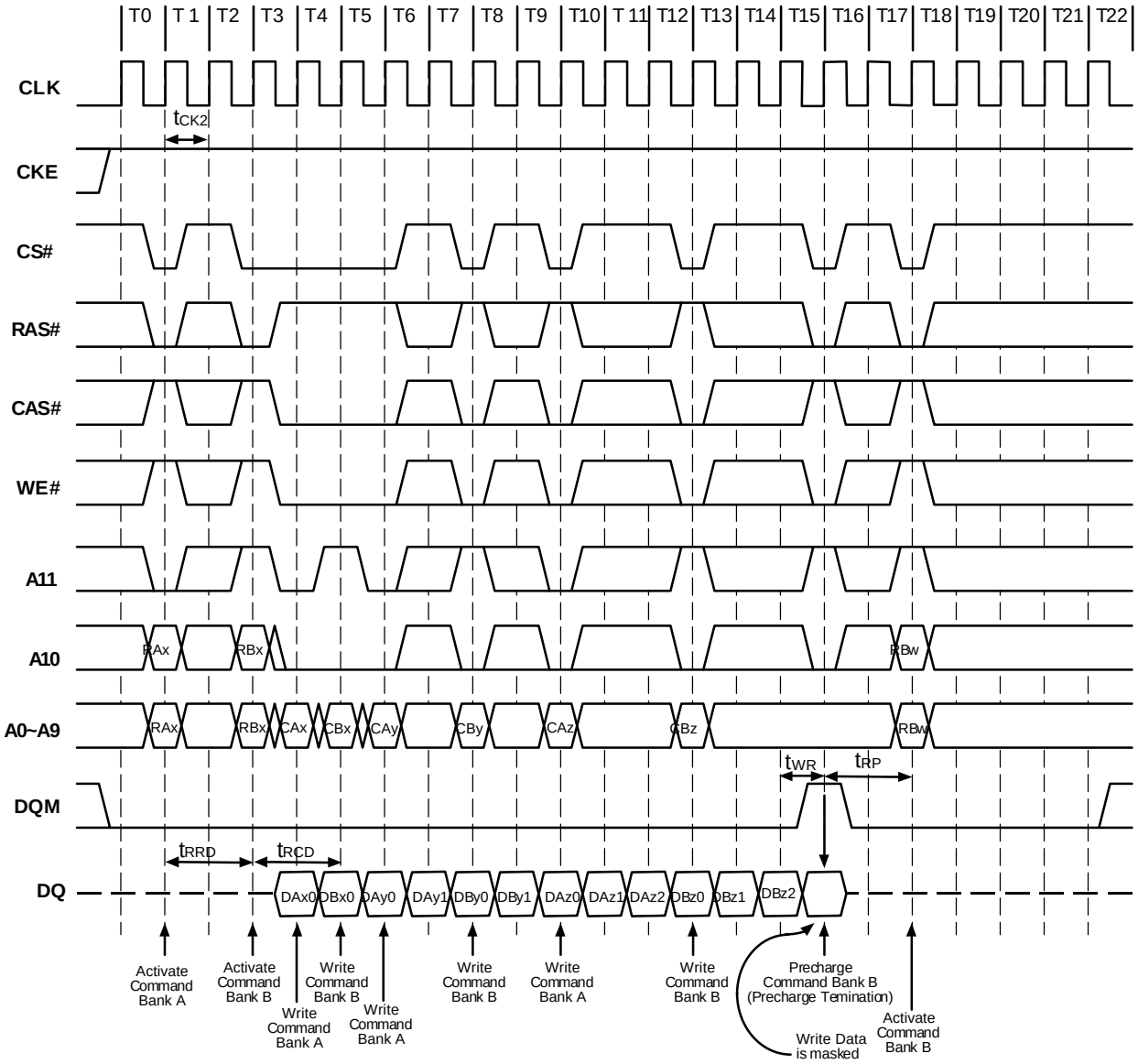


Figure 24.1. Precharge Termination of a Burst (Burst Length=Full Page, CAS# Latency=1)

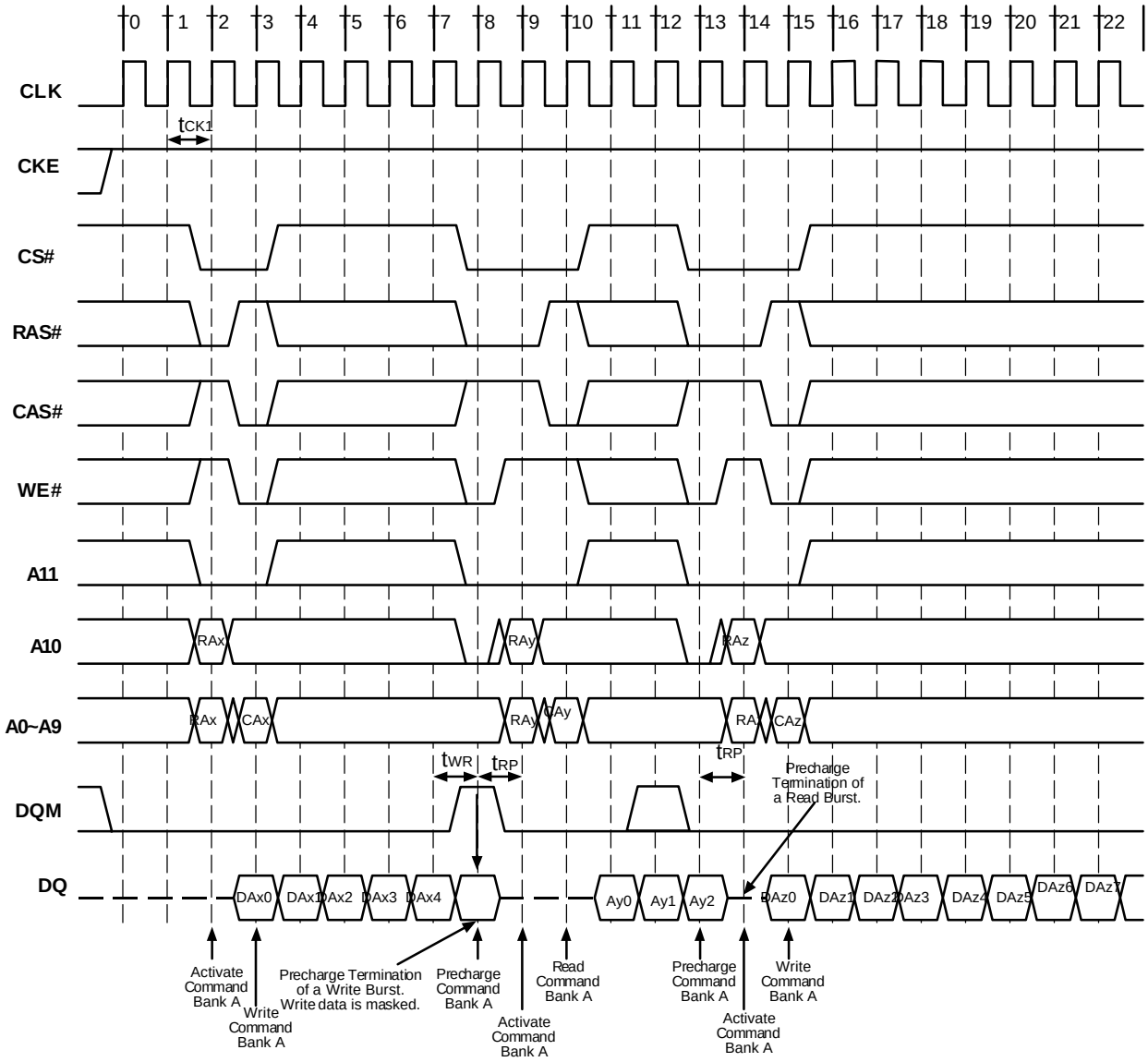


Figure 24.2. Precharge Termination of a Burst
(Burst Length=8 or Full Page, CAS# Latency=2)

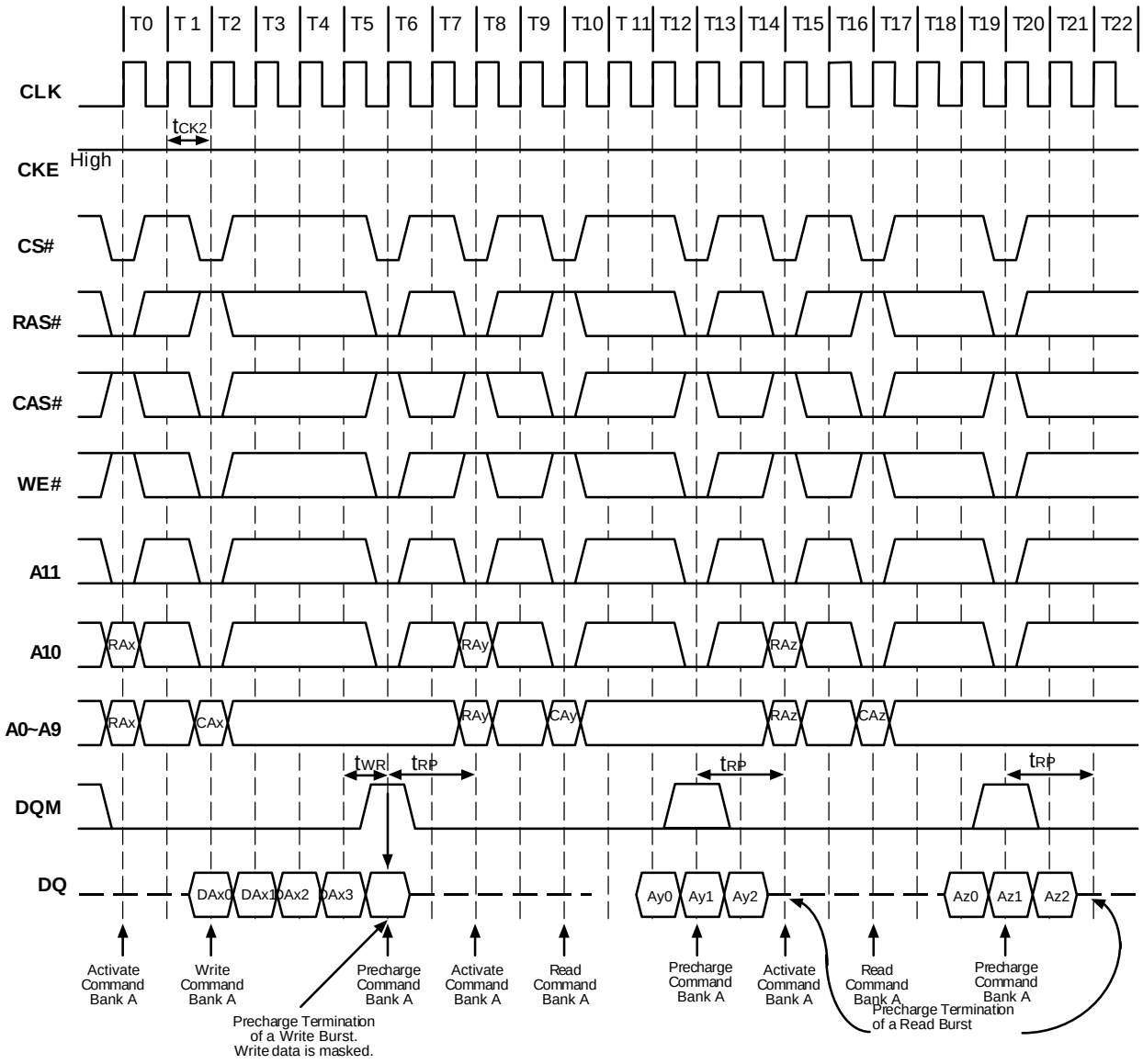
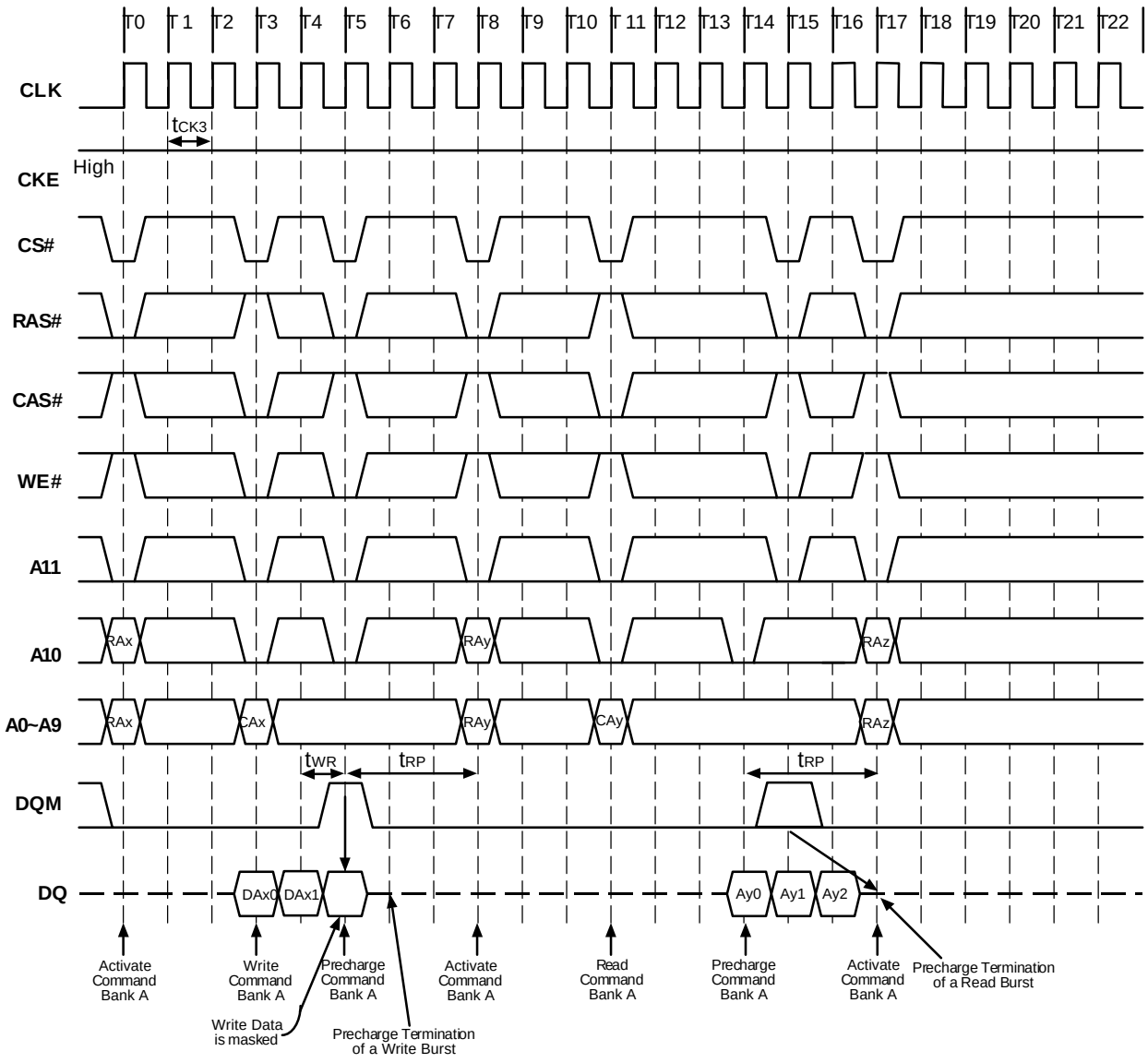
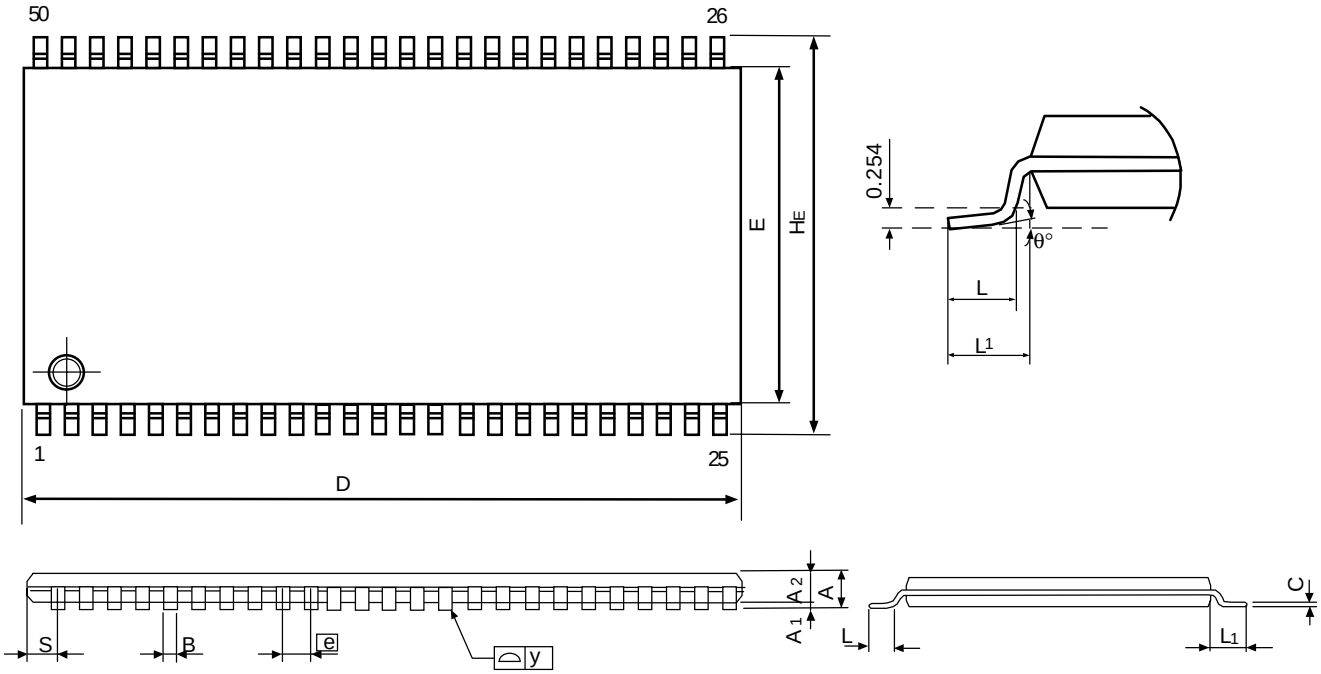


Figure 24.3. Precharge Termination of a Burst
(Burst Length=4, 8 or Full Page, CAS# Latency=3)



50 Pin TSOP II Package Outline Drawing Information



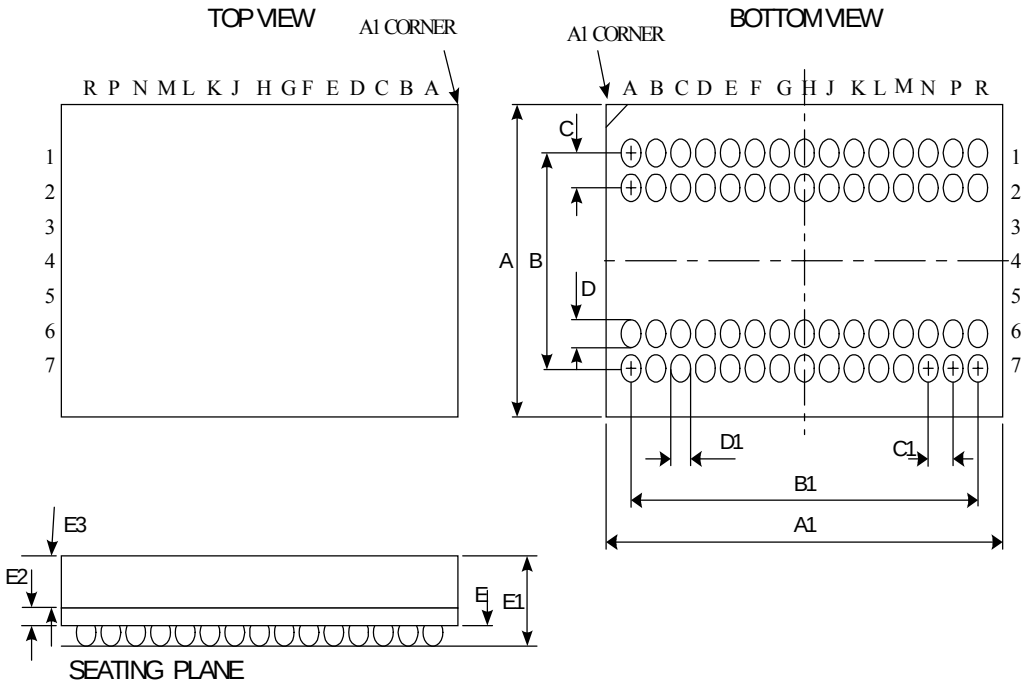
.

Symbol	Dimension in inch			Dimension in mm		
	Min	Normal	Max	Min	Normal	Max
A	-	-	0.047	-	-	1.20
A1	0.002	0.005	0.008	0.05	0.125	0.20
A2	-	-	0.039	-	-	1
B	0.012	0.015	0.018	0.3	0.375	0.45
c	-	0.006	-	-	0.155	-
D	0.82	0.825	0.83	20.82	20.95	21.08
E	0.398	0.400	0.402	10.11	10.16	10.21
e	-	0.031	-	-	0.80	-
HE	0.459	0.463	0.467	11.66	11.76	11.86
L	0.016	0.020	0.024	0.40	0.50	0.60
L1	-	0.0315	-	-	0.80	-
S	-	0.035	-	-	0.88	-
y	-	-	0.004	-	-	0.10
θ	0°	-	5°	0°	-	5°

Notes :

1. Dimension D&E do not include interiead flash.
2. Dimension B does not include dambar protrusion/intrusion.
3. Dimension S includes end flash.
4. Controlling dimension : mm

60-Ball (6.4mm x 10.1mm)VFBGA
Units in mm



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	6.30	6.40	6.50	0.248	2.52	2.56
A1	10.00	10.10	10.20	0.394	0.398	0.402
B	-	3.90(typ)	-	-	0.154(typ)	-
B1	-	9.10(typ)	-	-	0.358(typ)	-
C	-	0.65(typ)	-	-	0.026(typ)	-
C1		0.65(typ)	-	-	0.026(typ)	-
D	0.35	0.4	0.45	0.014	0.016	0.018
D1	0.35	0.4	0.45	0.014	0.016	0.018
E	0.22	0.27	0.32	0.009	0.11	0.13
E1	-	-	1.00*	-	-	0.039
E2	-	0.21	-	-	0.008	-
E3	0.42	0.45	0.48	0.017	0.018	0.019

Note : * if lead free package "E1" max.=1.2mm(0.047 inch)