




Helping Customers Innovate, Improve & Grow



### Description

Vectron's VL-821 Crystal Oscillator (XO) is a quartz stabilized square wave generator with a CMOS output, operating off either a 1.8, 2.5, or 3.3 volt supply. The VL-821 utilizes a high performance, low frequency quartz resonator followed by a custom ASIC to synthesize the output frequency.

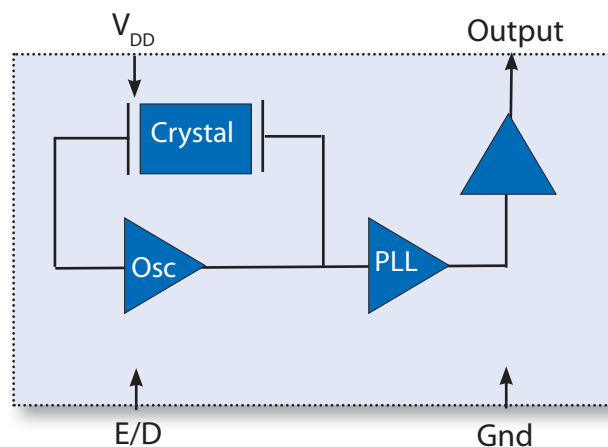
### Features

- Quick delivery
- CMOS Output
- 3.2mm x 2.5mm x 1.2mm
- Output frequencies to 200.00 MHz
- Tri-state output for the board test and debug
- -10/70°C or -40/85°C operating temperature
- Gold over nickel contact pads
- Product is compliant to RoHS directive  and fully compatible with lead free assembly

### Applications

- SONET/SDH/DWDM
- Ethernet, GE, SynchE
- Storage Area Networking
- Digital Video
- Broadband Access
- Microprocessors/DSP/FPGA

### Block Diagram

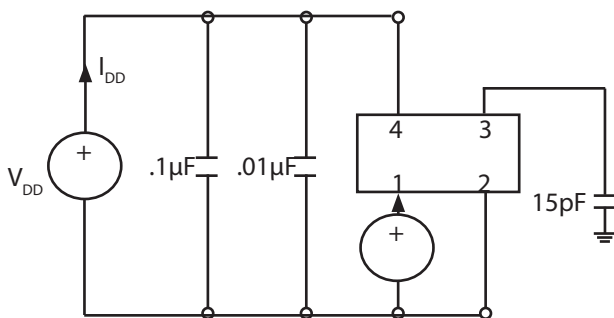


# Performance Specifications

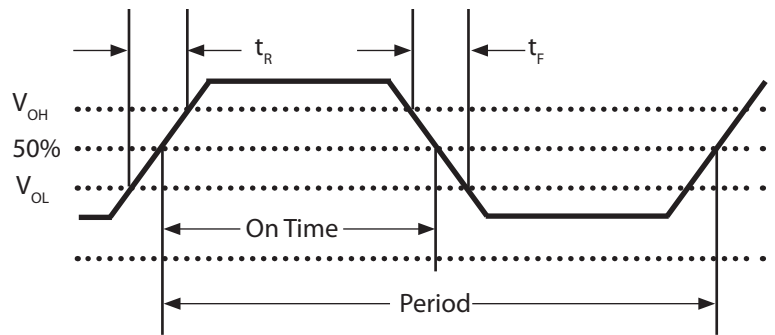
**Table 1. Electrical Performance, 3.3V Option**

Parameter	Symbol	Min	Typical	Maximum	Units
<b>Supply</b>					
Operating Supply Voltage <sup>1</sup>	$V_{DD}$	2.97	3.3	3.63	V
Absolute Maximum Operating Voltage		-0.05		5.0	V
Supply Current, Output Enabled <30 MHz 30.01 to 75 MHz 75.01 to 133 MHz 133.01 to 200 MHz	$I_{DD}$			10 15 20 25	mA
Supply Current, Output disable	$I_{DD}$			15	uA
<b>Frequency</b>					
Frequency	$f_o$	1.000		200.00	MHz
Stability <sup>4</sup> , (Ordering Option)		±25, ±50, ±100			ppm
<b>Outputs</b>					
Output Logic Levels Output Logic High <sup>2</sup> Output Logic Low <sup>2</sup> Output Logic High Drive Output Logic Low Drive	$V_{OH}$ $V_{OL}$ $I_{OH}$ $I_{OL}$	$0.9 \cdot V_{DD}$  8 8		$0.1 \cdot V_{DD}$	V V mA mA
Output Rise /Fall Time <sup>2</sup> , $f_o \leq 10\text{MHz}$ $f_o > 10\text{MHz}$	$t_R/t_F$			3 2	ns ns
Duty Cycle <sup>3</sup>	SYM	45	50	55	%
<b>Enable/Disable</b>					
Output Enable/Disable <sup>5</sup> Output Enable Output Disable	$V_{IH}$ $V_{IL}$	$0.7 \cdot V_{DD}$		$0.3V_{DD}$	V V
Start-Up Time	$t_{SU}$			2	ms
Operating Temp, (Ordering Option)	$T_{OP}$	-10/70 or -40/85			°C

- 1] A 0.01 uF and a 0.1uF capacitor should be located as close to the supply as possible (to ground).  $V_{DD}$  supply ramp should be <100 msec.
- 2] Figure 2 defines these parameters. Figure 1 illustrates the operating conditions under which these parameters are tested and specified.
- 3] Symmetry is measured defined as On Time/Period.
- 4] Includes calibration tolerance, operating temperature, supply voltage variations, aging and shock and vibration (not under operation).
- 5] Output will be enabled if the Enable/Disable is left open. E/D should be powered up after  $V_{DD}$ .



**Fig 1: Test Circuit**



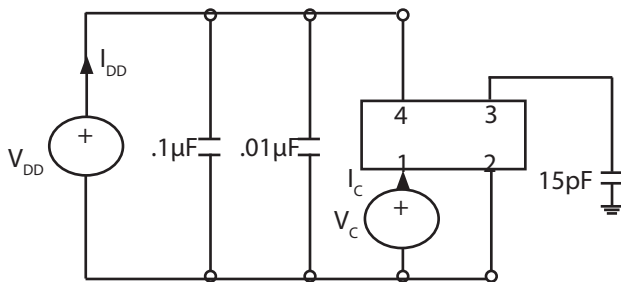
**Fig 2: Waveform**

# Performance Specifications

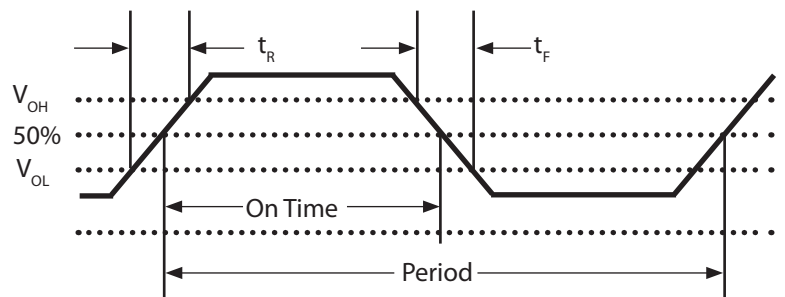
**Table 2. Electrical Performance, 2.5V Option**

Parameter	Symbol	Min	Typical	Maximum	Units
<b>Supply</b>					
Operating Supply Voltage <sup>1</sup>	$V_{DD}$	2.25	2.5	2.75	V
Absolute Maximum Operating Voltage		-0.5		5	V
Supply Current, Output Enable <30 MHz 30.01 to 75 MHz 75.01 to 166 MHz	$I_{DD}$			8.0 10.0 15.0	mA
Supply Current, Output Disabled $0.7V_{DD}$	$I_{DD}$			15	uA
<b>Frequency</b>					
Frequency	$f_o$	1.000		166.000	MHz
Stability <sup>4</sup> , (Ordering Option)		$\pm 25, \pm 50, \pm 100$			ppm
<b>Outputs</b>					
Output Logic Levels Output Logic High <sup>2</sup> Output Logic Low <sup>2</sup> Output Logic High Drive Output Logic Low Drive	$V_{OH}$ $V_{OL}$ $I_{OH}$ $I_{OL}$	$0.9*V_{DD}$  8 8		$0.1*V_{DD}$	V V mA mA
Output Rise /Fall Time <sup>2</sup> , $f_o \leq 10\text{MHz}$ $f_o > 10\text{MHz}$	$t_R/t_F$			4 3	ns ns
Duty Cycle <sup>3</sup>	SYM	45	50	55	%
<b>Enable/Disable</b>					
Output Enable/Disable <sup>5</sup> Output Enable Output Disable	$V_{IH}$ $V_{IL}$	$0.7*V_{DD}$		$0.3*V_{DD}$	V
Start-Up Time	$t_{SU}$			2	ms
Operating Temp, (Ordering Option)	$T_{OP}$	$-10/70$ or $-40/85$			°C

- 1] A 0.01 uF and a 0.1uF capacitor should be located as close to the supply as possible (to ground).  $V_{DD}$  supply ramp should be <100 msec.
- 2] Figure 2 defines these parameters. Figure 1 illustrates the operating conditions under which these parameters are tested and specified.
- 3] Symmetry is measured defined as On Time/Period.
- 4] Includes calibration tolerance, operating temperature, supply voltage variations, aging and shock and vibration (not under operation).
- 5] Output will be enabled if the Enable/Disable is left open. E/D should be powered up after  $V_{DD}$ .



**Fig 1: Test Circuit**



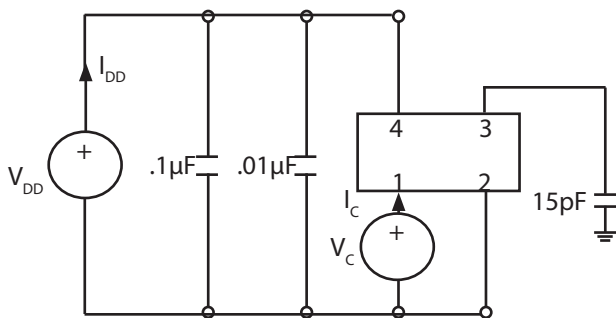
**Fig 2: Waveform**

# Performance Specifications

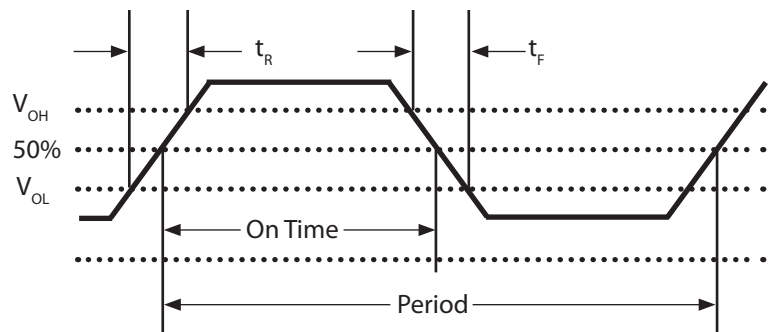
**Table 3. Electrical Performance, 1.8V Option**

Parameter	Symbol	Min	Typical	Maximum	Units
<b>Supply</b>					
Operating Supply Voltage <sup>1</sup>	$V_{DD}$	1.62	1.8	1.98	V
Absolute Maximum Voltage		-0.5		3.6	V
Supply Current, Output Enabled <30 MHz 30.01 to 75 MHz 75.01 to 133 MHz	$I_{DD}$			6 8 12	mA
Supply Current, Output Disabled	$I_{DD}$			15	uA
<b>Frequency</b>					
Frequency	$f_o$	1.000		133.00	MHz
Stability <sup>4</sup> , (Ordering Option)		±25, ±50, ±100			ppm
<b>Outputs</b>					
Output Logic Levels Output Logic High <sup>2</sup> Output Logic Low <sup>2</sup> Output Logic High Drive Output Logic Low Drive	$V_{OH}$ $V_{OL}$ $I_{OH}$ $I_{OL}$	$0.9*V_{DD}$  8 8		$0.1*V_{DD}$	V V mA mA
Output Rise /Fall Time <sup>2</sup> , $f_o \leq 10\text{MHz}$ $f_o > 10\text{MHz}$	$t_R/t_F$			5 4	ns ns
Duty Cycle <sup>3</sup>	SYM	45	50	55	%
<b>Enable/Disable</b>					
Output Enable/Disable <sup>5</sup> Output Enable Output Disable	$V_{IH}$ $V_{IL}$	$0.7*V_{DD}$		$0.3*V_{DD}$	V V
Start-Up Time	$t_{SU}$			2	ms
Operating Temp, (Ordering Option)	$T_{OP}$	-10/70 or -40/85			°C

- 1] A 0.01 uF and a 0.1uF capacitor should be located as close to the supply as possible (to ground).  $V_{DD}$  supply ramp should be <100 msec.
- 2] Figure 2 defines these parameters. Figure 1 illustrates the operating conditions under which these parameters are tested and specified.
- 3] Symmetry is measured defined as On Time/Period.
- 4] Includes calibration tolerance, operating temperature, supply voltage variations, aging and shock and vibration (not under operation).
- 5] Output will be enabled if the Enable/Disable is left open. E/D should be powered up after  $V_{DD}$ .

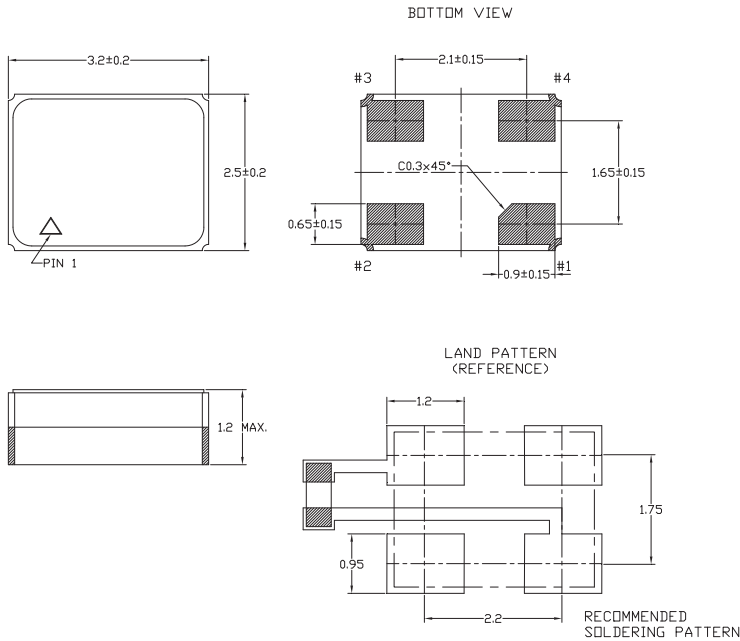


**Fig 1: Test Circuit**



**Fig 2: Waveform**

# Outline Drawing & Pad Layout



**Table 4. Pin Out**

Pin	Symbol	Function
1	E/D	Enable Disable
2	GND	Case and Electrical Ground
3	$f_o$	Output Frequency
4	$V_{DD}$	Power Supply Voltage

## Reliability

VI qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VL-821 family is capable of meeting the following qualification tests:

**Table 5. Environmental Compliance**

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Temperature Cycle	MIL-STD-883, Method 1010
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2015
Moisture Sensitivity Level	MSL 1
Contact Pads	Gold over Nickel

Although ESD protection circuitry has been designed into the VL-821 proper precautions should be taken when handling and mounting. VI employs a human body model (HBM) and a charged device model (CDM) for ESD susceptibility testing and design protection evaluation.

**Table 6. ESD Ratings**

Model	Minimum	Conditions
Human Body Model	1500V	MIL-STD-883, Method 3115
Charged Device Model	1000V	JESD 22-C101

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this datasheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability. Permanent damage is also possible if E/D is applied before  $V_{DD}$ .

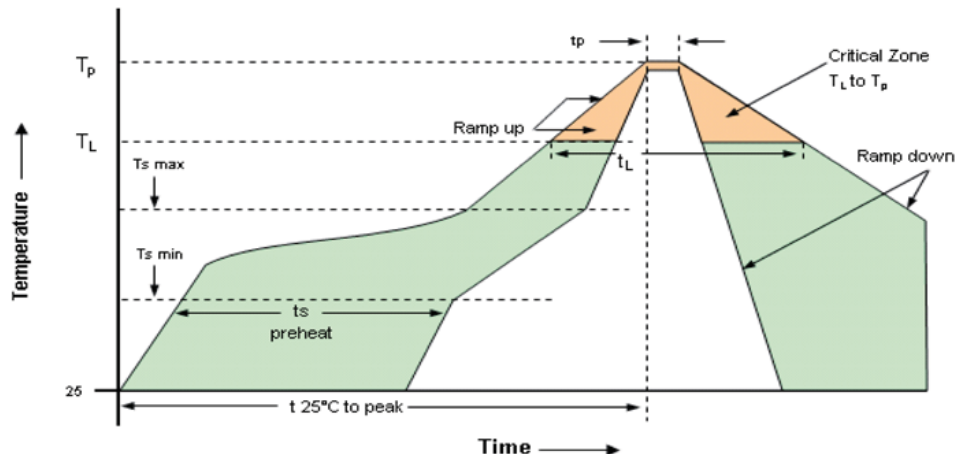
**Table 7. Absolute Maximum Ratings**

Parameter	Symbol	Ratings	Unit
Storage Temperature	$T_S$	-55 to 125	°C
Soldering Temp/Time	$T_{LS}$	260 / 20	°C / sec

# IR Reflow

## Solderprofile:

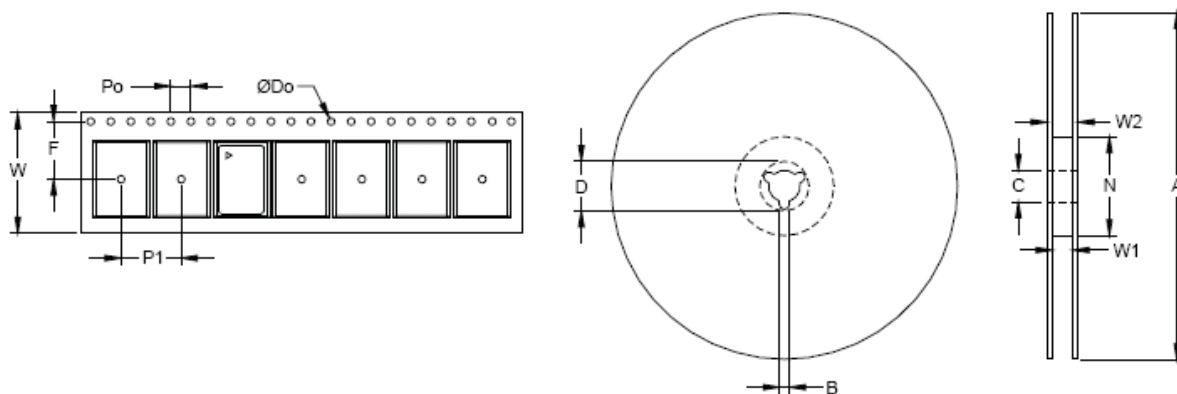
The VL-821 is qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The VL-821 device is hermetically sealed so an aqueous wash is not an issue.



**Table 8. Reflow Profile**

Parameter	Symbol	Value
PreHeat Time Ts-min Ts-max	$t_s$	60 sec Min, 260 sec Max 150°C 200°C
Ramp Up	$R_{UP}$	3 °C/sec Max
Time Above 217 °C	$t_L$	60 sec Min, 150 sec Max
Time To Peak Temperature	$T_{AMB-P}$	480 sec Max
Time at 260 °C	$t_p$	10 sec Max
Ramp Down	$R_{DN}$	6 °C/sec Max

## Tape and Reel



**Table 9. Tape and Reel Information**

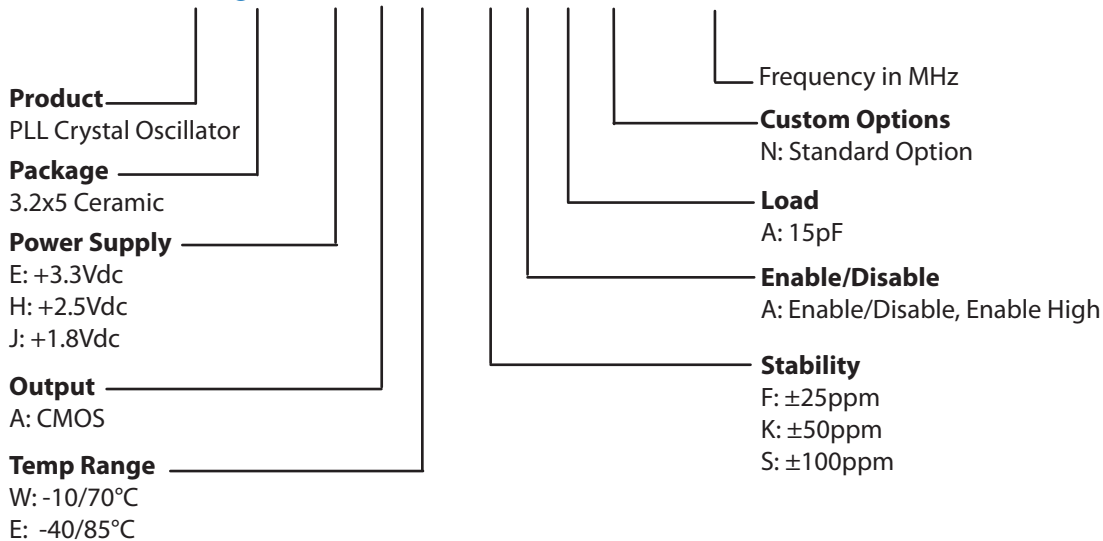
Dimension	Tape Dimensions (mm)					Reel Dimensions (mm)							# Per Reel
	W	F	Do	Po	P1	A	B	C	D	N	W1	W2	
Tolerance	Typ	Typ	Typ	Typ	Typ	Typ	Min	Typ	Min	Min	Typ	Typ	
VL-821	8	3.5	1.5	4	4	180	2	13		60	8	12	1000

**Table 10. Standard Output Frequencies (MHz)**

1.000	1.544	2.048	2.176	7.3728	8.000	10.000	11.0592
14.746	19.6608	24.49219	24.576	25.000	26.660	27.000	30.000
33.000	33.333	33.554	36.000	37.056	40.000	42.660	43.000
44.000	45.000	48.000	49.152	50.000	61.440	65.000	66.666
80.000	98.5382	106.25	110.00	124.444	125.000	133.000	135.000
150.000	155.520	156.000	156.250	160.000	162.000	170.000	200.000

## Ordering Information

### VL-821- E A W- K A A N- xxMxxxxxxx



*\*Note: not all combination of options are available.  
Other specifications may be available upon request.*

**Example: VL-821-EAW-KAAN-125M000000**

## For Additional Information, Please Contact

### USA:

Vectron International  
267 Lowell Road  
Hudson, NH 03051  
Tel: 1.888.328.7661  
Fax: 1.888.329.8328

### Europe:

Vectron International  
Landstrasse, D-74924  
Neckarbischofsheim, Germany  
Tel: +49 (0) 3328.4784.17  
Fax: +49 (0) 3328.4784.30

### Asia:

Vectron International  
1F-2F, No 8 Workshop, No 308 Fenju Road  
WaiGaoQiao Free Trade Zone  
Pudong, Shanghai, China 200131  
Tel: 86.21.5048.0777  
Fax: 86.21.5048.1881

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