19-4753; Rev 1; 9/09

EVALUATION KIT AVAILABLE

High-Efficiency, 1.5MHz Op Amps with RRIO

General Description

The MAX9617/MAX9618 are low-power, zero-drift operational amplifiers, designed for use in portable consumer, medical, and industrial applications.

The MAX9617/MAX9618 feature rail-to-rail CMOS inputs and outputs, a 1.5MHz GBW at just 59µA supply current and 10µV (max) zero-drift input offset voltage over time and temperature. The zero-drift feature of the MAX9617/MAX9618 reduces the high 1/f noise typically found in CMOS input operational amplifiers, making it useful for a wide variety of low-frequency measurement applications.

The MAX9617 is available in a space-saving, 2mm x 2mm, 6-pin SC70 package. The MAX9618 is available in a 2mm x 2mm, 8-pin SC70 package. All devices are specified over the -40°C to +125°C automotive operating temperature range.

Applications

Sensor Interfaces

Loop-Powered Systems

Portable Medical Devices

Battery-Powered Devices

Cardiac Monitors

Features

- **Low 59µA Quiescent Current**
- **Very-Low 10µV (max) Input Offset Voltage**
- **Low Input Noise**
  42nV/√Hz at 1kHz
  1µVP-P from 0.1Hz to 10Hz
- **Rail-to-Rail Inputs and Outputs**
- **1.5MHz GBW**
- **Ultra-Low 10pA Input Bias Current**
- **Single 1.8V to 5.5V Supply Voltage Range**
- **Unity-Gain Stable**
- **Available in Tiny 6-Pin SC70 (MAX9617) and 8-Pin SC70 (MAX9618) Packages**

Ordering Information

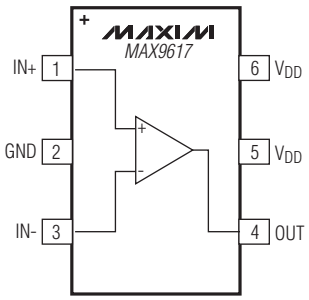
PART	TEMP RANGE	PIN-PACKAGE
MAX9617AXT+	-40°C to +125°C	6 SC70
MAX9618AXA+*	-40°C to +125°C	8 SC70

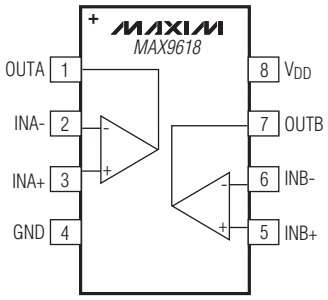
+Denotes a lead(Pb)-free/RoHS-compliant package.

**Future product—contact factory for availability.*

Functional Diagrams

TOP VIEW





High-Efficiency, 1.5MHz Op Amps with RRIO

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD} to GND).....-0.3V to +6V
All Other Pins, IN+ to IN- .....(GND - 0.3V) to (V_{DD} + 0.3V)
Short-Circuit Duration to Either Supply Rail,
OUT, OUTA, OUTB..... 10s
Continuous Input Current (any pins)..... ±20mA

Continuous Power Dissipation (T_A = +70°C)
6-Pin SC70 (derate 3.1mW/°C above +70°C).....245.4mW
8-Pin SC70 (derate 3.1mW/°C above +70°C).....245mW
Operating Temperature Range..... -40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +3.3V, V_{GND} = 0V, V_{IN+} = V_{IN-} = V_{DD}/2, R_L = 100kΩ to V_{DD}/2, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Supply Voltage Range	V_{DD}	Guaranteed by PSRR, 0°C ≤ T_A ≤ +70°C		1.6		5.5	V
		Guaranteed by PSRR, -40°C ≤ T_A ≤ +125°C		1.8		5.5	
Supply Current (per Amplifier)	I_{DD}	T_A = +25°C			59	78	µA
		-40°C ≤ T_A ≤ +125°C				111	
Power-Supply Rejection Ratio (Note 2)	PSRR	V_{DD} = 1.8V to 5.5V	T_A = +25°C	119	135		dB
			-40°C ≤ T_A ≤ +125°C	107			
		0°C ≤ T_A ≤ +70°C, V_{DD} = 1.6V to 5.5V		116	135		
Power-Up Time	t_{ON}	V_{DD} = 0 to 3V step, A_V = 1V/V			20		µs
DC SPECIFICATIONS							
Input Offset Voltage (Note 2)	V_{OS}	T_A = +25°C			0.8	10	µV
		-40°C ≤ T_A ≤ +125°C				25	
Input Offset Voltage Drift (Note 2)	ΔV_{OS}				5	120	nV/°C
Input Bias Current (Note 2)	I_B	T_A =+25°C			0.01	0.14	nA
		-40°C ≤ T_A ≤ +125°C				3.5	
Input Offset Current	I_{OS}				0.005		
Input Common-Mode Range	V_{CM}	Guaranteed by CMRR test	T_A = +25°C	-0.1		V_{DD} + 0.1	V
			-40°C ≤ T_A ≤ +125°C	-0.1		V_{DD} + 0.05	
Common-Mode Rejection Ratio (Note 2)	CMRR	-0.1V ≤ V_{CM} ≤ V_{DD} + 0.1V, T_A = +25°C		122	135		dB
		-0.1V ≤ V_{CM} ≤ V_{DD} + 0.05V, -40°C ≤ T_A ≤ +125°C		116			
Open-Loop Gain (Note 2)	AV_{OL}	20mV ≤ V_{OUT} ≤ V_{DD} - 20mV, R_L = 100kΩ to V_{DD}/2		120	138		dB
		150mV ≤ V_{OUT} ≤ V_{DD} - 150mV, R_L = 5kΩ to V_{DD}/2		123	160		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3.3V, V_{GND} = 0V, V_{IN+} = V_{IN-} = V_{DD}/2, R_L = 100kΩ to V_{DD}/2, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at +25°C.) (Note 1)

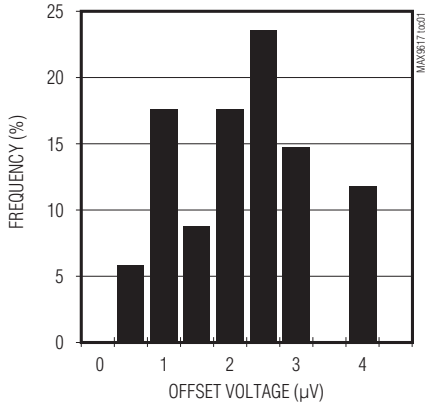
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Resistance	R_{IN}	Differential			50		MΩ
		Common mode			200		
Output-Voltage Swing	V_{OH}	V_{DD} - V_{OUT}	R_L = 100kΩ to V_{DD}/2			12	mV
			R_L = 5kΩ to V_{DD}/2			22	
			R_L = 600Ω to V_{DD}/2		50		
	V_{OL}	V_{OUT}	R_L = 100kΩ to V_{DD}/2			11	
			R_L = 5kΩ to V_{DD}/2			18	
			R_L = 600Ω to V_{DD}/2		50		
Short-Circuit Current	I_{SC}				150		mA
AC SPECIFICATIONS							
Gain-Bandwidth Product	GBWP				1.5		MHz
Slew Rate	SR	0V ≤ V_{OUT} ≤ 2V			0.7		V/µs
Input Voltage-Noise Density	e_n	f = 1kHz			42		nV/√Hz
Input Voltage Noise		0.1Hz ≤ f ≤ 10Hz			1		$µV_{P-P}$
Input Current-Noise Density	i_n	f = 1kHz			100		fA/√Hz
Phase Margin		C_L = 20pF			60		Degrees
Capacitive Loading	C_L	No sustained oscillation, A_V = 1V/V			400		pF
Crosstalk		f = 10kHz (MAX9618)			-100		dB

Note 1: Specifications are 100% tested at T_A = +25°C (exceptions noted). All temperature limits are guaranteed by design.
Note 2: Guaranteed by design.

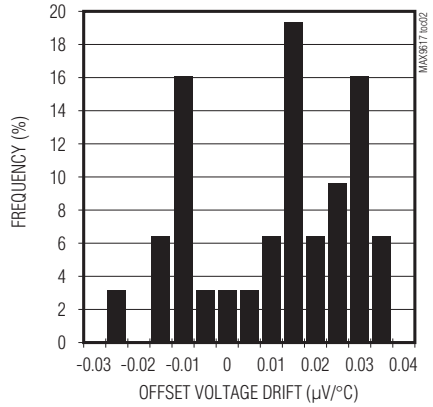
Typical Operating Characteristics

(V_{DD} = +3.3V, V_{GND} = 0V, outputs have R_L = 100kΩ connected to V_{DD}/2. T_A = +25°C, unless otherwise specified.)

OFFSET VOLTAGE HISTOGRAM



INPUT OFFSET VOLTAGE DRIFT HISTOGRAM

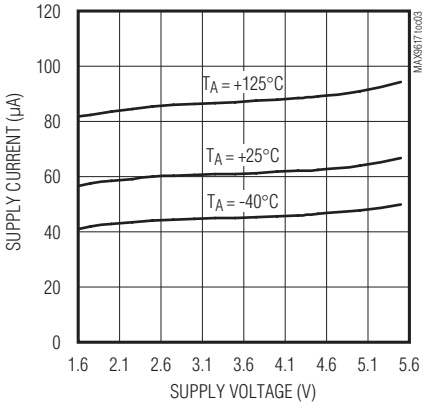


High-Efficiency, 1.5MHz Op Amps with RRIO

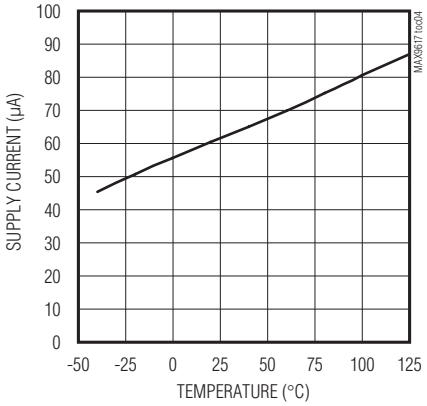
Typical Operating Characteristics (continued)

(V_{DD} = +3.3V, V_{GND} = 0V, outputs have R_L = 100kΩ connected to $V_{DD}/2$. T_A = +25°C, unless otherwise specified.)

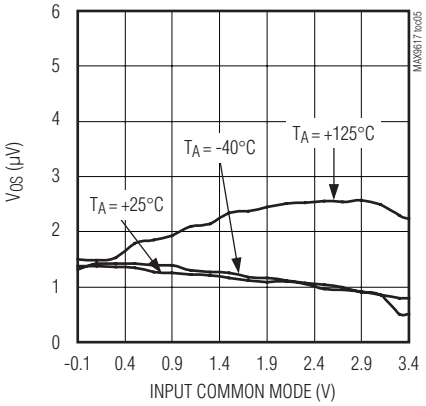
SUPPLY CURRENT vs. SUPPLY VOLTAGE



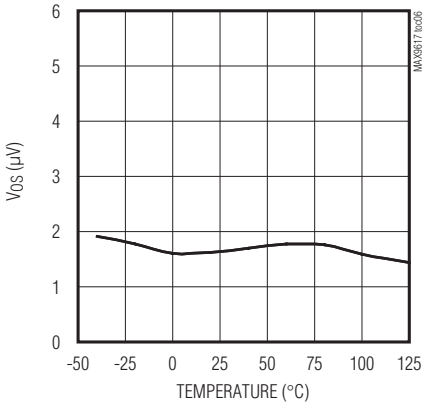
SUPPLY CURRENT vs. TEMPERATURE



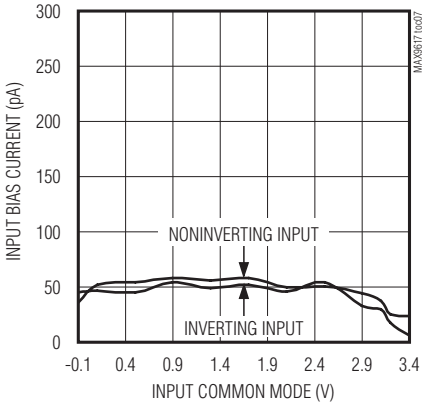
INPUT OFFSET VOLTAGE vs. INPUT COMMON MODE



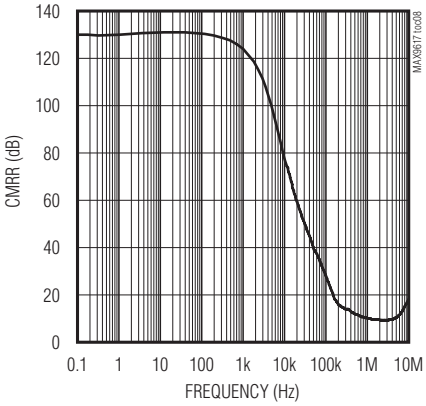
INPUT OFFSET VOLTAGE vs. TEMPERATURE



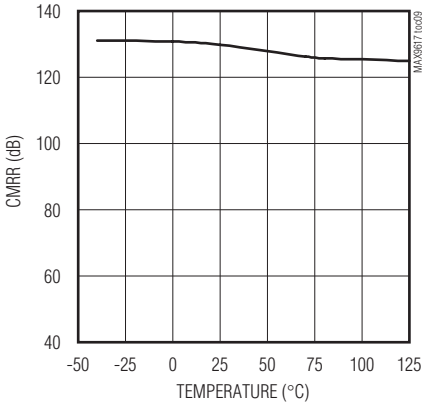
INPUT BIAS CURRENT vs. INPUT COMMON MODE



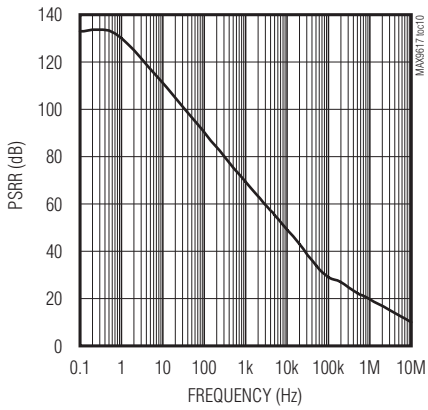
COMMON-MODE REJECTION RATIO vs. FREQUENCY



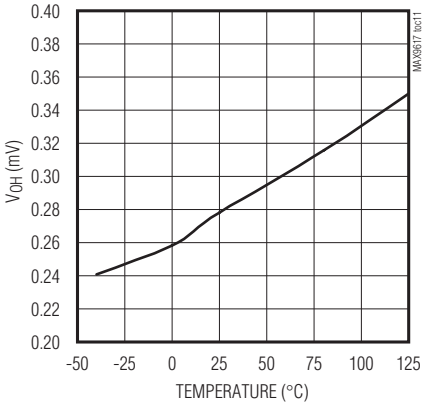
COMMON-MODE REJECTION RATIO vs. TEMPERATURE



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



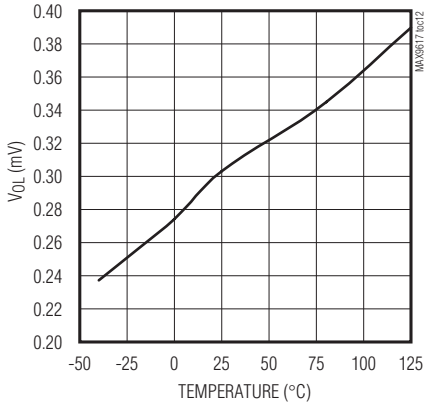
OUTPUT-VOLTAGE SWING HIGH vs. TEMPERATURE



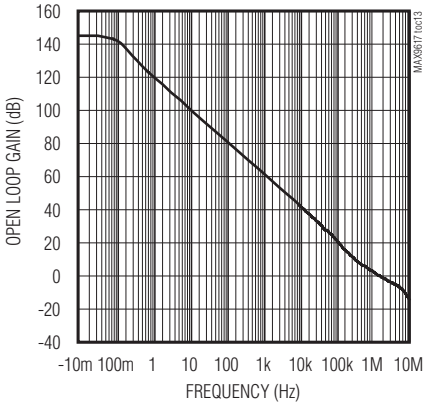
Typical Operating Characteristics (continued)

(V_{DD} = +3.3V, V_{GND} = 0V, outputs have R_L = 100kΩ connected to $V_{DD}/2$. T_A = +25°C, unless otherwise specified.)

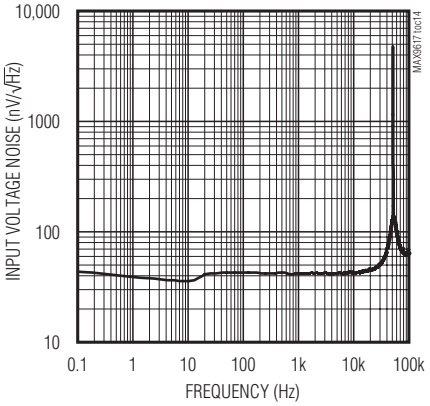
OUTPUT-VOLTAGE SWING LOW vs. TEMPERATURE



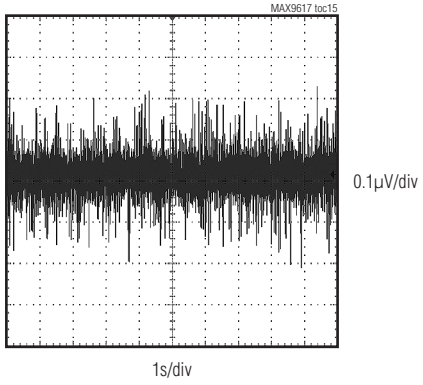
OPEN-LOOP GAIN vs. FREQUENCY



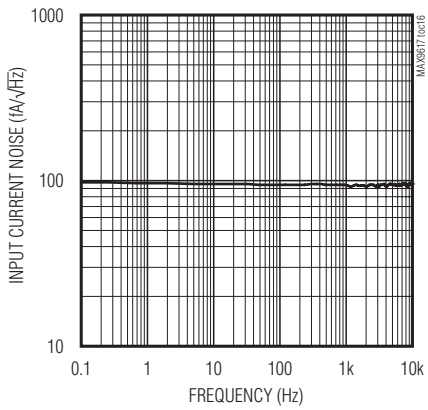
INPUT VOLTAGE NOISE vs. FREQUENCY



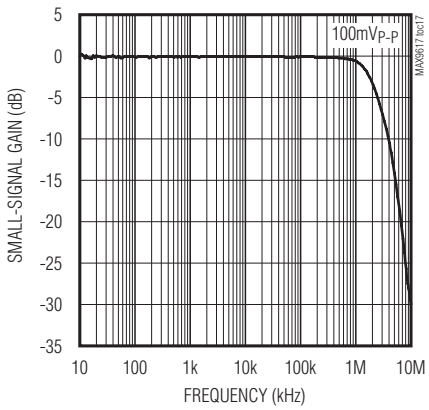
INPUT VOLTAGE 0.1Hz TO 10Hz NOISE



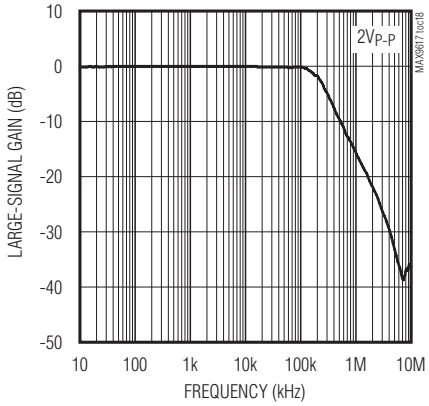
INPUT CURRENT NOISE vs. FREQUENCY



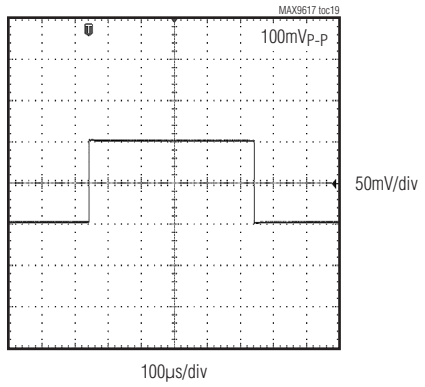
SMALL-SIGNAL GAIN vs. FREQUENCY



LARGE-SIGNAL GAIN vs. FREQUENCY



SMALL-SIGNAL STEP RESPONSE vs. TIME

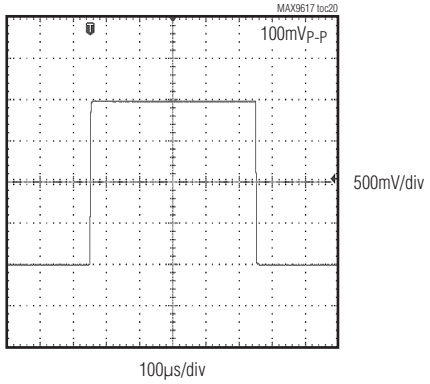


High-Efficiency, 1.5MHz Op Amps with RRIO

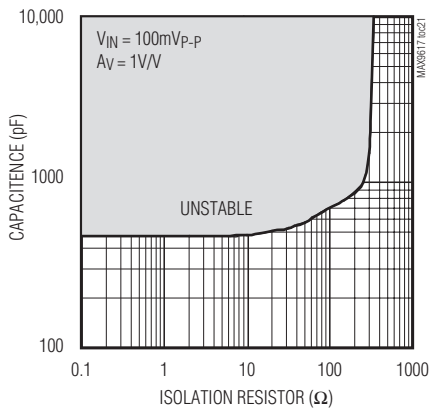
Typical Operating Characteristics (continued)

(V_{DD} = +3.3V, V_{GND} = 0V, outputs have R_L = 100kΩ connected to V_{DD}/2. T_A = +25°C, unless otherwise specified.)

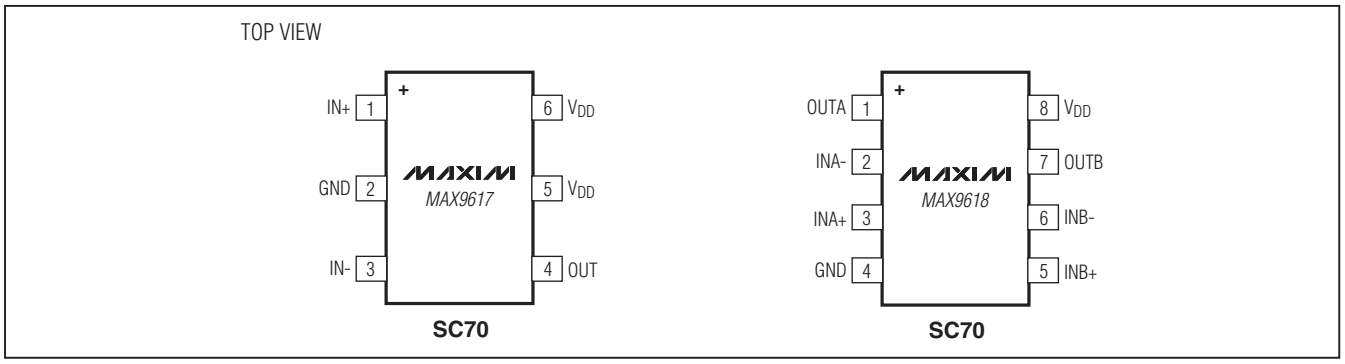
LARGE-SIGNAL STEP RESPONSE vs. TIME



CAPACITIVE LOAD vs. ISOLATION RESISTOR



Pin Configurations



Pin Description

PIN		NAME	FUNCTION
MAX9617	MAX9618		
1	—	IN+	Positive Input
2	4	GND	Ground
3	—	IN-	Negative Input
4	—	OUT	Output
5, 6	8	V_{DD}	Positive Supply Voltage. Bypass to GND with a 0.1µF capacitor.
—	1	OUTA	Channel A Output
—	2	INA-	Channel A Negative Input
—	3	INA+	Channel A Positive Input
—	5	INB+	Channel B Positive Input
—	6	INB-	Channel B Negative Input
—	7	OUTB	Channel B Output

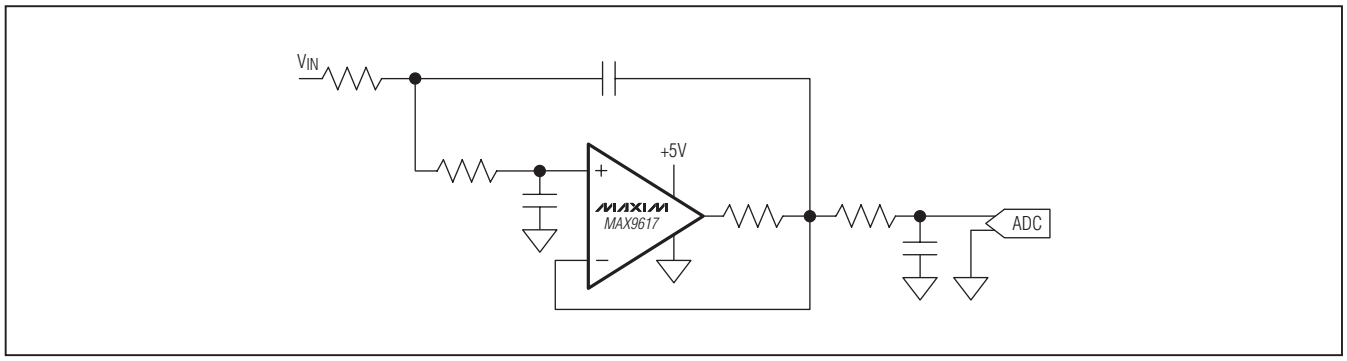


Figure 1. Typical Application Circuit: Sallen-Key Active Lowpass Filter

Detailed Description

The MAX9617 (single) and MAX9618 (dual) are precision, low-power op amps ideal for signal processing applications. These devices use an innovative autozero technique that allows precision and low noise with a minimum amount of power. The low input offset voltage, CMOS inputs, and the absence of 1/f noise allows for optimization of active filter designs.

The MAX9617/MAX9618 achieve rail-to-rail performance at the input through the use of a low-noise charge pump. This ensures a glitch-free, common-mode input voltage range extending from the negative supply rail up to the positive supply rail, eliminating crossover distortion common to traditional n-channel/p-channel CMOS pair inputs, reducing harmonic distortion at the output.

Autozero

The MAX9617/MAX9618 feature an autozero circuit that allows the device to achieve less than 10µV (max) of input offset voltage and eliminates the 1/f noise.

Internal Charge Pump

An internal charge pump provides an internal supply typically 1V beyond the upper rail. This internal rail allows the MAX9617/MAX9618 to achieve true rail-to-rail inputs and outputs, while providing excellent common-mode rejection, power-supply rejection ratios, and gain linearity.

The charge pump requires no external components, and in most applications is entirely transparent to the user. The operating frequency is well beyond the unity-gain frequency of the amplifier, avoiding aliasing or other signal integrity issues in sensitive applications.

Applications Information

The MAX9617/MAX9618 low-power, low-noise, and precision operational amplifiers are designed for applications in the portable medical, such as ECG and pulse oximetry, portable consumer, and industrial markets.

The MAX9617/MAX9618 are also ideal for loop-powered systems that interface with pressure sensors or strain gauges.

Capacitive-Load Stability

Driving large capacitive loads can cause instability in many op amps. The MAX9617/MAX9618 are stable with capacitive loads up to 400pF. Stability with higher capacitive loads can be improved by adding an isolation resistor in series with the op-amp output. This resistor improves the circuit's phase margin by isolating the load capacitor from the amplifier's output. The graph in the *Typical Operating Characteristics* gives the stable operation region for capacitive load versus isolation resistors.

Power Supplies and Layout

The MAX9617/MAX9618 operate either with a single supply from +1.6V to +5.5V with respect to ground or with dual supplies from ±0.8V to ±2.75V. When used with dual supplies, bypass both supplies with their own 0.1µF capacitor to ground. When used with a single supply, bypass V_{DD} with a 0.1µF capacitor to ground.

Careful layout technique helps optimize performance by decreasing the amount of stray capacitance at the op amp's inputs and outputs. To decrease stray capacitance, minimize trace lengths by placing external components close to the op amp's pins.

Chip Information

PROCESS: BiCMOS

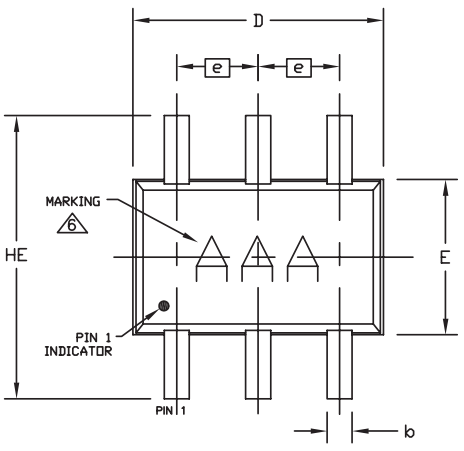
High-Efficiency, 1.5MHz Op Amps with RRIO

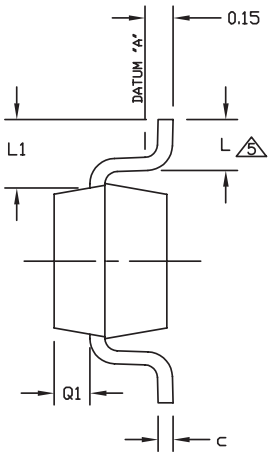
Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

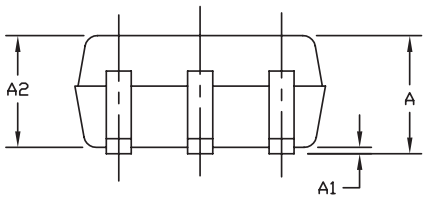
PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
6 SC70	X6SN-1	21-0077
8 SC70	X8C+1	21-0460

SC70, 6L.EPS





COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX
A	0.80	0.95	1.10
A1	0.00	0.07	0.10
A2	0.80	0.90	1.00
b	0.15	0.22	0.30
c	0.10	0.14	0.18
D	1.80	2.00	2.20
e	0.65 BSC.		
E	1.15	1.25	1.35
HE	1.80	2.20	2.40
L	0.26	0.34	0.46
L1	0.425 TYP.		
Q1	0.10	0.25	0.40
PKG. CODES	X6SN-1		



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. COPLANARITY 4 MILS. MAX.
5. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM "A" AND LEAD SURFACE.
6. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
7. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
8. ALL DIMENSIONS COMPLY TO JEDEC MO-203.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND LEAD FREE (+) PACKAGE CODES.

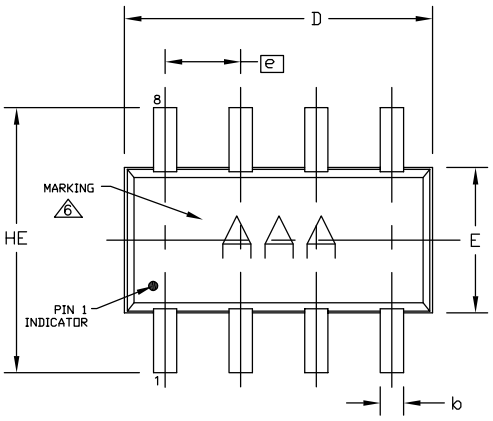
MAXIM

TITLE: PACKAGE OUTLINE, 6L SC70			
APPROVAL	DOCUMENT CONTROL NO. 21-0077	REV. G	1/1

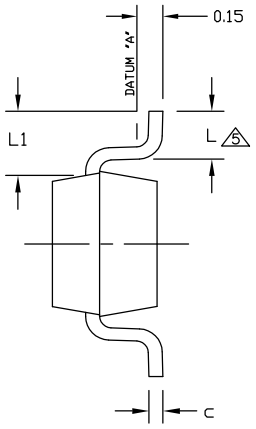
-DRAWING NOT TO SCALE-

Package Information (continued)

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

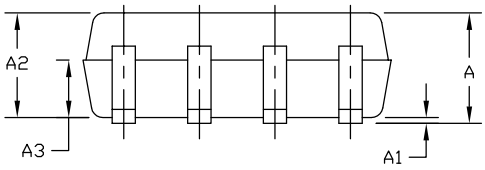


TOP VIEW



SIDE VIEW

COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX
A	0.80	0.95	1.10
A1	0.00	0.07	0.10
A2	0.80	0.90	1.00
A3	0.40	0.47	0.55
b	0.15	0.21	0.27
c	0.10	0.14	0.18
D	1.80	2.00	2.20
e	0.50 BSC.		
E	1.15	1.25	1.35
HE	1.80	2.20	2.40
L	0.26	0.34	0.46
L1	0.425 TYP.		
PKG. CODE	X8C-1		



SIDE VIEW

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. COPLANARITY 4 MILS. MAX.
5. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM "A" AND LEAD SURFACE.
6. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
7. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
8. ALL DIMENSIONS COMPLY TO JEDEC MO-203.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND LEAD FREE (+) PACKAGE CODES.

—DRAWING NOT TO SCALE—

MAXIM

TITLE:
PACKAGE OUTLINE,
8L SC70, COL PKG.

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0460	A	1/1

High-Efficiency, 1.5MHz Op Amps with RRIO

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/09	Initial release	—
1	9/09	Removed references to MAX9617 shutdown functionality	1, 2, 3, 6, 7