Product Specification

PE97022

3500 MHz UltraCMOS™ Integer-N PLL Rad Hard for Space Applications

Product Description

Peregrine's PE97022 is a high-performance integer-N PLL capable of frequency synthesis up to 3500 MHz. The device is designed for superior phase noise performance while providing an order of magnitude reduction in current consumption, when compared with existing commercial space PLLs.

The PE97022 features a 10/11 dual modulus prescaler, counters and a phase comparator as shown in Figure 1. Counter values are programmable through either a serial or parallel interface and can also be directly hard wired.

The PE97022 is optimized for commercial space applications. Single Event Latch up (SEL) is physically impossible and Single Event Upset (SEU) is better than 10^{-9} errors per bit / day. It is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering excellent RF performance and intrinsic radiation tolerance.

Features

- Low Power - 45 mA at 3.3V
- 3500 MHz operation
- ÷10/11 dual modulus prescaler
- Internal phase detector
- Serial, parallel or hardwired programmable
- Ultra-Low Phase Noise: -216 dBc/Hz
- SEU < 10^{-9} errors / bit-day
- 100 Krad (Si) total dose
- Pin compatible with the PE9702, packaged in a 44-lead CQFJ *(reference application note AN22 at www.psemi.com)*

Figure 1. Block Diagram

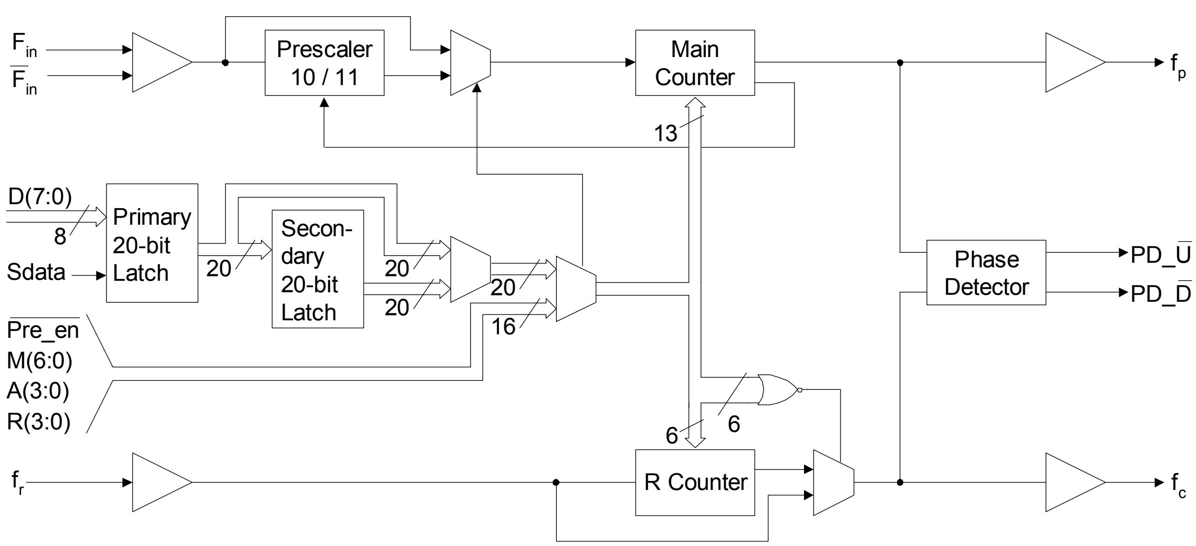


Figure 2. Pin Configurations (Top View)

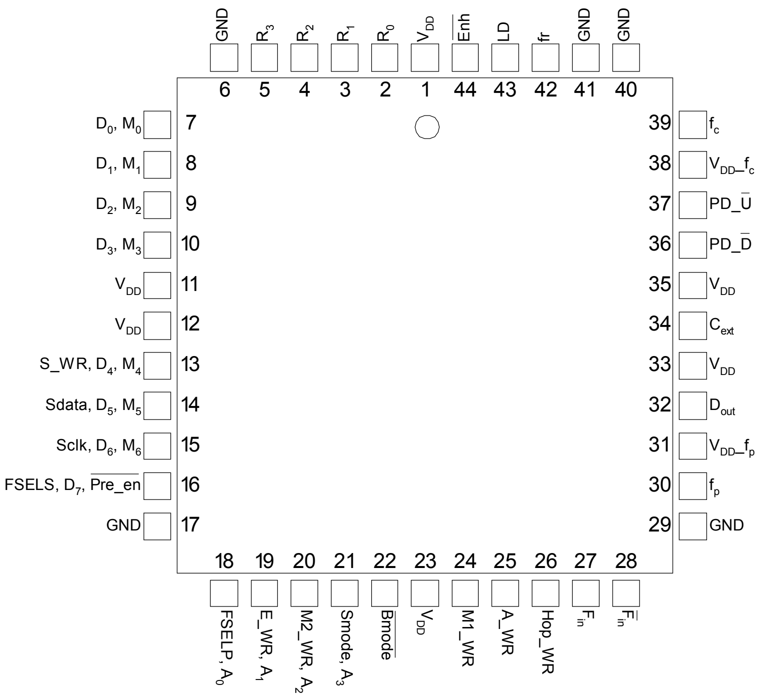


Figure 3. Package Type

44-lead CQFJ

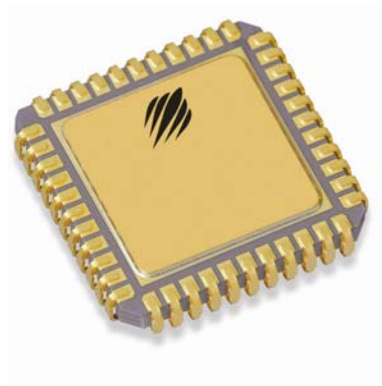


Table 1. Pin Descriptions

Pin No.	Pin Name	Interface Mode	Type	Description
1	V_{DD}	ALL	(Note 1)	Power supply input. Input may range from 2.85 V to 3.45 V. Bypassing recommended.
2	R_0	Direct	Input	R Counter bit0 (LSB).
3	R_1	Direct	Input	R Counter bit1.
4	R_2	Direct	Input	R Counter bit2.
5	R_3	Direct	Input	R Counter bit3.
6	GND	ALL	(Note 1)	Ground.
7	D_0	Parallel	Input	Parallel data bus bit0 (LSB).
	M_0	Direct	Input	M Counter bit0 (LSB).
8	D_1	Parallel	Input	Parallel data bus bit1.
	M_1	Direct	Input	M Counter bit1.
9	D_2	Parallel	Input	Parallel data bus bit2.
	M_2	Direct	Input	M Counter bit2.
10	D_3	Parallel	Input	Parallel data bus bit3.
	M_3	Direct	Input	M Counter bit3.
11	V_{DD}	ALL	(Note 1)	Same as pin 1.
12	V_{DD}	ALL	(Note 1)	Same as pin 1.
13	S_WR	Serial	Input	Serial load enable input. While S_WR is "low", Sdata can be serially clocked. Primary register data is transferred to the secondary register on S_WR or Hop_WR rising edge.
	D_4	Parallel	Input	Parallel data bus bit4
	M_4	Direct	Input	M Counter bit4

Table 1. Pin Descriptions (continued)

Pin No.	Pin Name	Interface Mode	Type	Description
14	Sdata	Serial	Input	Binary serial data input. Input data entered MSB first.
	D_5	Parallel	Input	Parallel data bus bit5.
	M_5	Direct	Input	M Counter bit5.
15	Sclk	Serial	Input	Serial clock input. Sdata is clocked serially into the 20-bit primary register (E_WR "low") or the 8-bit enhancement register (E_WR "high") on the rising edge of Sclk.
	D_6	Parallel	Input	Parallel data bus bit6.
	M_6	Direct	Input	M Counter bit6.
16	FSELS	Serial	Input	Selects contents of primary register (FSELS=1) or secondary register (FSELS=0) for programming of internal counters while in Serial Interface Mode.
	D_7	Parallel	Input	Parallel data bus bit7 (MSB).
	$\overline{\mathrm{Pre\_en}}$	Direct	Input	Prescaler enable, active "low". When "high", F_{in} bypasses the prescaler.
17	GND	ALL		Ground.
18	FSELP	Parallel	Input	Selects contents of primary register (FSELP=1) or secondary register (FSELP=0) for programming of internal counters while in Parallel Interface Mode.
	A_0	Direct	Input	A Counter bit0 (LSB).
19	E_WR	Serial	Input	Enhancement register write enable. While E_WR is "high", Sdata can be serially clocked into the enhancement register on the rising edge of Sclk.
		Parallel	Input	Enhancement register write. D[7:0] are latched into the enhancement register on the rising edge of E_WR.
	A_1	Direct	Input	A Counter bit1.
20	M2_WR	Parallel	Input	M2 write. D[3:0] are latched into the primary register (R[5:4], M[8:7]) on the rising edge of M2_WR.
	A_2	Direct	Input	A Counter bit2.
21	Smode	Serial, Parallel	Input	Selects serial bus interface mode ($\overline{\mathrm{Bmode}}$=0, Smode=1) or Parallel Interface Mode ($\overline{\mathrm{Bmode}}$=0, Smode=0).
	A_3	Direct	Input	A Counter bit3 (MSB).
22	$\overline{\mathrm{Bmode}}$	ALL	Input	Selects direct interface mode ($\overline{\mathrm{Bmode}}$=1).
23	V_{DD}	ALL	(Note 1)	Same as pin 1.
24	M1_WR	Parallel	Input	M1 write. D[7:0] are latched into the primary register ($\overline{\mathrm{Pre\_en}}$, M[6:0]) on the rising edge of M1_WR.
25	A_WR	Parallel	Input	A write. D[7:0] are latched into the primary register (R[3:0], A[3:0]) on the rising edge of A_WR.
26	Hop_WR	Serial, Parallel	Input	Hop write. The contents of the primary register are latched into the secondary register on the rising edge of Hop_WR.
27	F_{in}	ALL	Input	Prescaler input from the VCO. 3.5 GHz max frequency.
28	$\overline{F_{in}}$	ALL	Input	Prescaler complementary input. A bypass capacitor in series with a 51 Ω resistor should be placed as close as possible to this pin and be connected directly to the ground plane.
29	GND	ALL		Ground.
30	f_p	ALL	Output	Monitor pin for main divider output. Switching activity can be disabled through enhancement register programming or by floating or grounding V_{DD} pin 31.

Table 1. Pin Descriptions (continued)

Pin No.	Pin Name	Interface Mode	Type	Description
31	V_{DD}-f_p	ALL	(Note 1)	V_{DD} for f_p. Can be left floating or connected to GND to disable the f_p output.
32	Dout	Serial, Parallel	Output	Data Out. The MSEL signal and the raw prescaler output are available on Dout through enhancement register programming.
33	V_{DD}	ALL	(Note 1)	Same as pin 1.
34	Cext	ALL	Output	Logical “NAND” of PD_$\bar{U}$ and PD_$\bar{D}$ terminated through an on chip, 2 kΩ series resistor. Connecting Cext to an external capacitor will low pass filter the input to the inverting amplifier used for driving LD.
35	V_{DD}	ALL	(Note 1)	Same as pin 1.
36	PD_$\bar{D}$	ALL	Output	PD_$\bar{D}$ is pulse down when f_p leads f_c.
37	PD_$\bar{U}$	ALL		PD_$\bar{U}$ is pulse down when f_c leads f_p.
38	V_{DD}-f_c	ALL	(Note 1)	V_{DD} for f_c. Can be left floating or connected to GND to disable the f_c output.
39	f_c	ALL	Output	Monitor pin for reference divider output. Switching activity can be disabled through enhancement register programming or by floating or grounding V_{DD} pin 38.
40	GND	ALL		Ground.
41	GND	ALL		Ground.
42	f_r	ALL	Input	Reference frequency input.
43	LD	ALL	Output, OD	Lock detect and open drain logical inversion of CEXT. When the loop is in lock, LD is high impedance, otherwise LD is a logic low (“0”).
44	$\overline{\text{Enh}}$	Serial, Parallel	Input	Enhancement mode. When asserted low (“0”), enhancement register bits are functional.

Note 1: V_{DD} pins 1, 11, 12, 23, 31, 33, 35, and 38 are connected by diodes and must be supplied with the same positive voltage level. V_{DD} pins 31 and 38 are used to enable test modes and should be left floating.

Note 2: All digital input pins have 70 kΩ pull-down resistors to ground.

Table 2. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Supply voltage	-0.3	4.0	V
V_I	Voltage on any input	-0.3	V_{DD} + 0.3	V
I_I	DC into any input	-10	+10	mA
I_O	DC into any output	-10	+10	mA
T_{stg}	Storage temperature range	-65	150	°C

Table 3. Operating Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Supply voltage	2.85	3.45	V
T_A	Operating ambient temperature range	-40	85	°C

Table 4. ESD Ratings

Symbol	Parameter/Conditions	Level	Units
V_{ESD}	ESD voltage (Human Body Model) – Note 1	1000	V

Note 1: Periodically sampled, not 100% tested. Tested per MIL-STD-883, M3015 C2

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating in Table 4.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Table 5. DC Characteristics: V_{DD} = 3.3 V, -40° C < T_A < 85° C, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Operational supply current; Prescaler disabled Prescaler enabled	V_{DD} = 2.85 to 3.45 V		 15 45	 50	 mA mA
Digital Inputs: All except f_r, F_{in}, $\bar{F}_{in}$						
V_{IH}	High level input voltage	V_{DD} = 2.85 to 3.45 V	0.7 x V_{DD}			V
V_{IL}	Low level input voltage	V_{DD} = 2.85 to 3.45 V			0.3 x V_{DD}	V
I_{IH}	High level input current	V_{IH} = V_{DD} = 3.45 V			70	µA
I_{IL}	Low level input current	V_{IL} = 0, V_{DD} = 3.45 V	-1			µA
Reference Divider input: f_r						
I_{IHR}	High level input current	V_{IH} = V_{DD} = 3.45 V			100	µA
I_{ILR}	Low level input current	V_{IL} = 0, V_{DD} = 3.45 V	-100			µA
Counter and phase detector outputs: f_c, f_p.						
V_{OLD}	Output voltage LOW	I_{out} = 6 mA			0.4	V
V_{OHD}	Output voltage HIGH	I_{out} = -3 mA	V_{DD} - 0.4			V
Lock detect outputs: Cext, LD						
V_{OLC}	Output voltage LOW, Cext	I_{out} = 100 µA			0.4	V
V_{OHC}	Output voltage HIGH, Cext	I_{out} = -100 µA	V_{DD} - 0.4			V
V_{OLLD}	Output voltage LOW, LD	I_{out} = 1 mA			0.4	V

Table 6. AC Characteristics: V_{DD} = 3.3 V, -40° C < T_A < 85° C, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typical	Max	Units
Control Interface and Latches (see Figures 4, 5, 6)						
f_{Clk}	Serial data clock frequency	(Note 1)			10	MHz
t_{ClkH}	Serial clock HIGH time		30			ns
t_{ClkL}	Serial clock LOW time		30			ns
t_{DSU}	Sdata set-up time after Sclk rising edge, D[7:0] set-up time to M1_WR, M2_WR, A_WR, E_WR rising edge		10			ns
t_{DHLD}	Sdata hold time after Sclk rising edge, D[7:0] hold time to M1_WR, M2_WR, A_WR, E_WR rising edge		10			ns
t_{PW}	S_WR, M1_WR, M2_WR, A_WR, E_WR pulse width		30			ns
t_{CWR}	Sclk rising edge to S_WR rising edge. S_WR, M1_WR, M2_WR, A_WR falling edge to Hop_WR rising edge		30			ns
t_{CE}	Sclk falling edge to E_WR transition		30			ns
t_{WRC}	S_WR falling edge to Sclk rising edge. Hop_WR falling edge to S_WR, M1_WR, M2_WR, A_WR rising edge		30			ns
t_{EC}	E_WR transition to Sclk rising edge		30			ns
t_{MDO}	MSEL data out delay after Fin rising edge	C_L = 12 pf			8	ns
Main Divider (Including Prescaler) (Note 4)						
P_{Fin}	Input level range	External AC coupling 275 MHz ≤ Freq ≤ 3200MHz	-5		5	dBm
		External AC coupling 3.2 GHz < Freq ≤ 3.5 GHz 3.15 V ≤ VDD ≤ 3.45 V	0		5	dBm
Main Divider (Prescaler Bypassed) (Note 4)						
F_{in}	Operating frequency		50		300	MHz
P_{Fin}	Input level range	External AC coupling	-5		5	dBm
Reference Divider						
f_r	Operating frequency	(Note 3)			100	MHz
P_{fr}	Reference input power (Note 2)	Single-ended input	-2		10	dBm
Phase Detector						
f_c	Comparison frequency	(Note 3)			50	MHz
SSB Phase Noise (F_{in} = 1.9 GHz, f_r = 20 MHz, f_c = 20 MHz, LBW = 50 kHz, V_{DD} = 3.3 V, Temp = 25° C) (Note 4)						
Φ_N	Phase Noise	100 Hz Offset		-89		dBc/Hz
Φ_N	Phase Noise	1 kHz Offset		-95		dBc/Hz
Φ_N	Phase Noise	10 kHz Offset		-102		dBc/Hz
SSB Phase Noise (F_{in} = 1.9 GHz, f_r = 20 MHz, f_c = 20 MHz, LBW = 50 kHz, V_{DD} = 3.0 V, Temp = 25° C) (Note 4)						
Φ_N	Phase Noise	100 Hz Offset		-87		dBc/Hz
Φ_N	Phase Noise	1 kHz Offset		-94		dBc/Hz
Φ_N	Phase Noise	10 kHz Offset		-101		dBc/Hz

Note 1: Fclk is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify Fclk specification.

Note 2: CMOS logic levels can be used to drive reference input if DC coupled. Voltage input needs to be a minimum of 0.5Vp-p.

Note 3: Parameter is guaranteed through characterization only and is not tested.

Note 4: Parameters below are not tested for die sales. These parameters are verified during the element evaluation.

Figure 4. RF Sensitivity versus Frequency (typical device at temperature = 25° C)

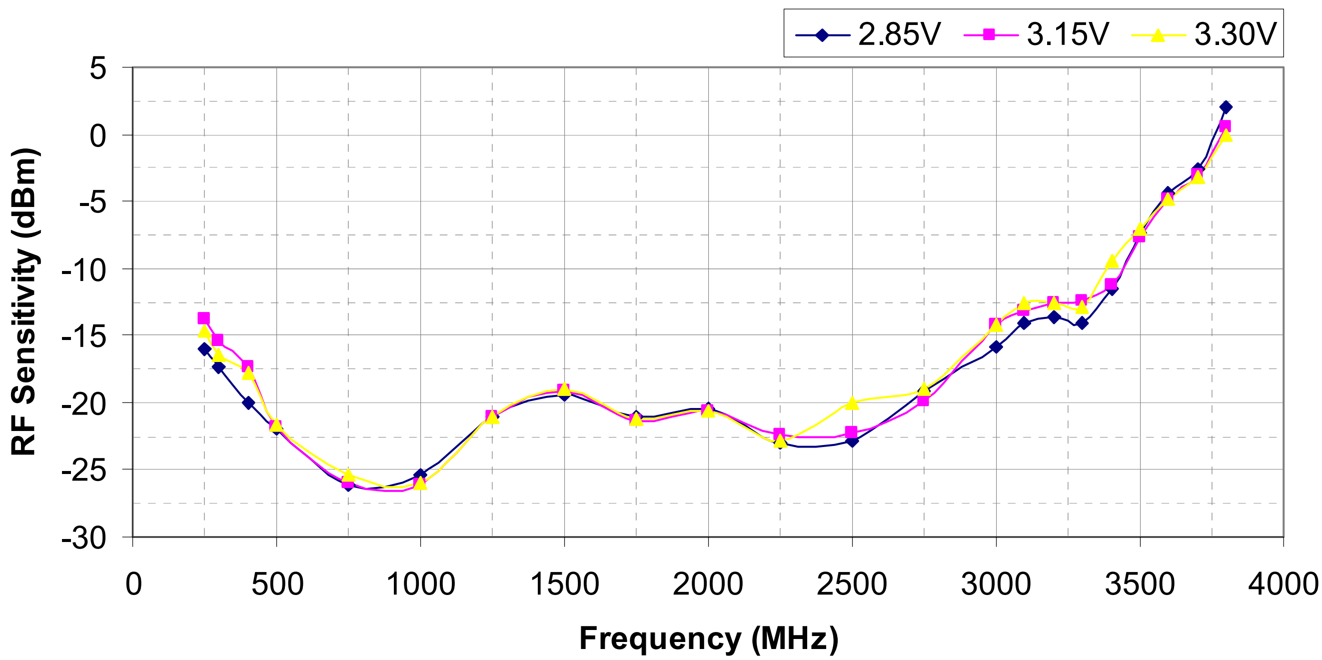
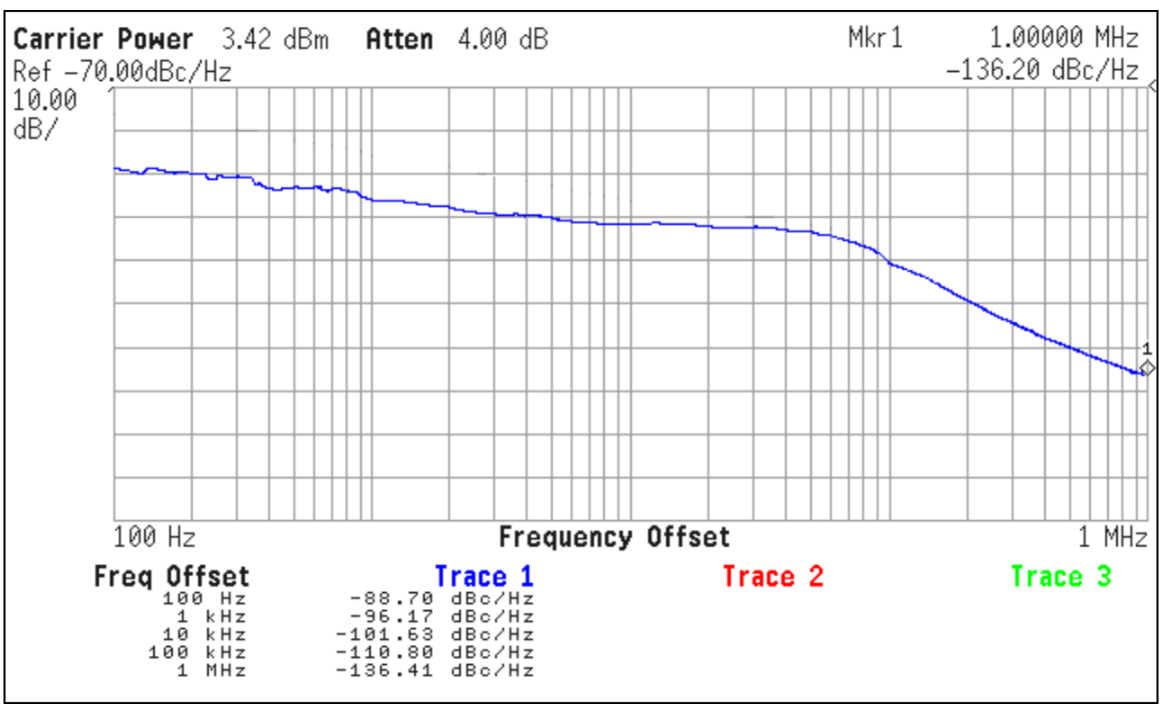


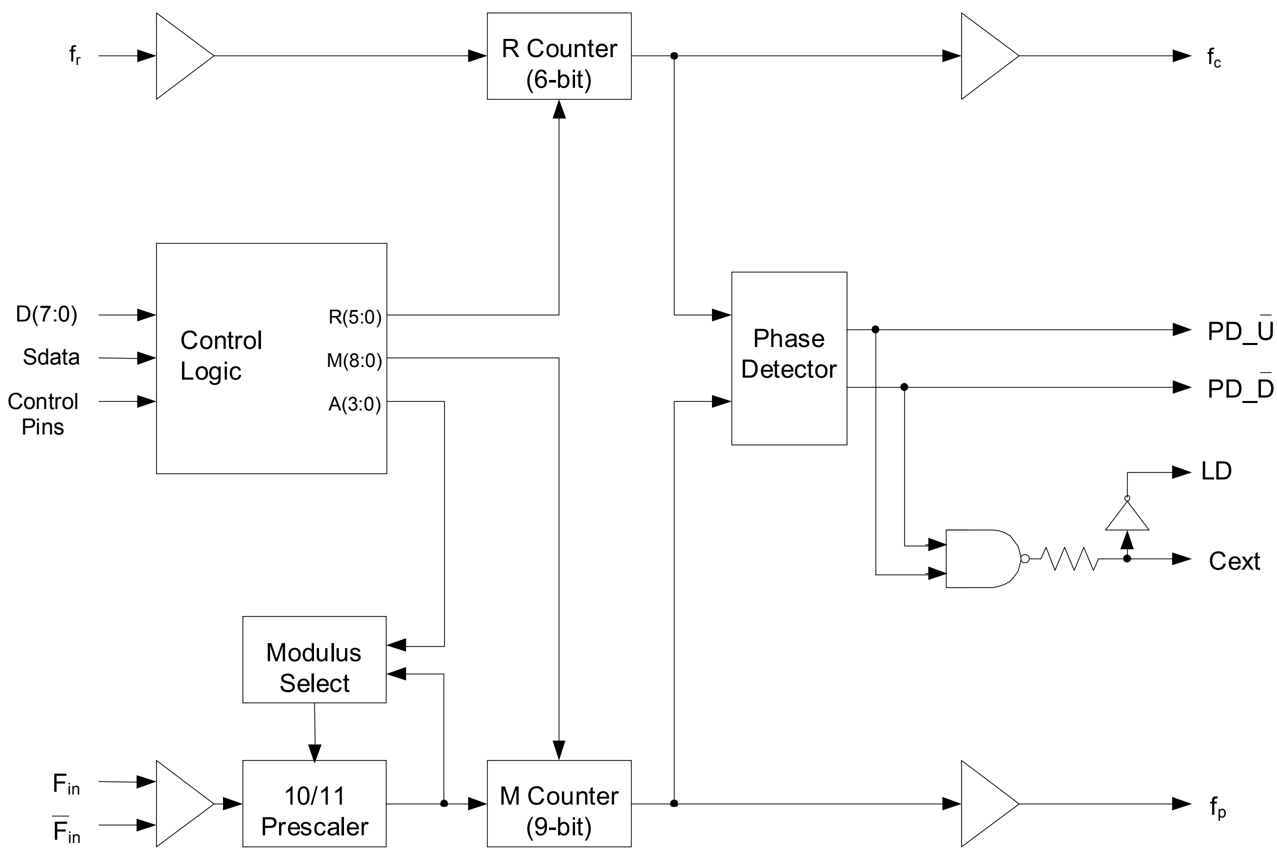
Figure 5. Typical Phase Noise for PE97022, VDD = 3.3 V, Temp = 25 C, Fvco = 1.92 GHz, Fcomp = 20 MHz, Loop Bandwidth = 50 kHz



Functional Description

The PE97022 consists of a prescaler, counters, a phase detector, and control logic. The dual modulus prescaler divides the VCO frequency by either 10 or 11, depending on the value of the modulus select. Counters "R" and "M" divide the reference and prescaler output, respectively, by integer values stored in a 20-bit register. An additional counter ("A") is used in the modulus select logic. The phase-frequency detector generates up and down frequency control signals. The control logic includes a selectable chip interface. Data can be written via serial bus, parallel bus, or hardwired directly to the pins. There are also various operational and test modes and a lock detect output.

Figure 6. Functional Block Diagram



Main Counter Chain

Normal Operating Mode

The main counter chain divides the RF input frequency, F_{in}, by an integer derived from the user-defined values in the "M" and "A" counters. It is composed of the 10/11 dual modulus prescaler, modulus select logic, and 9-bit M counter. Setting $\overline{\text{Pre\_en}}$ "low" enables the 10/11 prescaler. Setting $\overline{\text{Pre\_en}}$ "high" allows F_{in} to bypass the prescaler and powers down the prescaler.

The output from the main counter chain, f_p, is related to the VCO frequency, F_{in}, by the following equation:

$$f_p = F_{in} / [10 \times (M + 1) + A] \qquad (1)$$
$$\text{where } A \leq M + 1,\ 1 \leq M \leq 511$$

When the loop is locked, F_{in} is related to the reference frequency, f_r, by the following equation:

$$F_{in} = [10 \times (M + 1) + A] \times (f_r / (R+1)) \qquad (2)$$
$$\text{where } A \leq M + 1,\ 1 \leq M \leq 511$$

A consequence of the upper limit on A is that F_{in} must be greater than or equal to 90 x (f_r / (R+1)) to obtain contiguous channels. Programming the M Counter with the minimum value of "1" will result in a minimum M Counter divide ratio of "2".

In Direct Interface Mode, main counter inputs M_7 and M_8 are internally forced low. In this mode, the M value is limited to $1 \leq M \leq 127$.

Prescaler Bypass Mode

Setting $\overline{\text{Pre\_en}}$ "high" allows F_{in} to bypass and power down the prescaler. In this mode, the 10/11 prescaler and A register are not active, and the input VCO frequency is divided by the M counter directly. The following equation relates F_{in} to the reference frequency, f_r:

$$F_{in} = (M + 1) \times (f_r / (R+1))) \qquad (3)$$
$$\text{where } 1 \leq M \leq 511$$

In Direct Interface Mode, main counter inputs M_7 and M_8 are internally forced low. In this mode, the M value is limited to $1 \leq M \leq 127$.

Reference Counter

The reference counter chain divides the reference frequency, f_r, down to the phase detector comparison frequency, f_c.

The output frequency of the 6-bit R Counter is related to the reference frequency by the following equation:

$$f_c = f_r / (R + 1) \qquad (4)$$
$$\text{where } 0 \leq R \leq 63$$

Note that programming R with "0" will pass the reference frequency, f_r, directly to the phase detector.

In Direct Interface Mode, R Counter inputs R_4 and R_5 are internally forced low ("0"). In this mode, the R value is limited to $0 \leq R \leq 15$.

Register Programming

Parallel Interface Mode

Parallel Interface Mode is selected by setting the $\overline{\text{Bmode}}$ input "low" and the Smode input "low".

Parallel input data, D[7:0], are latched in a parallel fashion into one of three 8-bit primary register sections on the rising edge of M1_WR, M2_WR, or A_WR per the mapping shown in Table 7 on page 10. The contents of the primary register are transferred into a secondary register on the rising edge of Hop_WR according to the timing diagram shown in Figure 7. Data is transferred to the counters as shown in Table 7 on page 10.

The secondary register acts as a buffer to allow rapid changes to the VCO frequency. This double buffering for "ping-pong" counter control is programmed via the FSELP input. When FSELP is "high", the primary register contents set the counter inputs. When FSELP is "low", the secondary register contents are utilized.

Parallel input data, D[7:0], are latched into the enhancement register on the rising edge of E_WR according to the timing diagram shown in Figure 6. This data provides control bits as shown in Table 8 on page 10 with bit functionality enabled by asserting the $\overline{\text{Enh}}$ input "low".

Serial Interface Mode

Serial Interface Mode is selected by setting the $\overline{\text{Bmode}}$ input “low” and the Smode input “high”. While the E_WR input is “low” and the S_WR input is “low”, serial input data (Sdata input), B_0 to B_{19}, is clocked serially into the primary register on the rising edge of Sclk, MSB (B_0) first. The contents from the primary register are transferred into the secondary register on the rising edge of either S_WR or Hop_WR according to the timing diagram shown in Figure 7. Data is transferred to the counters as shown in Table 7.
The double buffering provided by the primary and secondary registers allows for “ping-pong” counter control using the FSELS input. When FSELS is “high”, the primary register contents set the counter inputs. When FSELS is “low”, the secondary register contents are utilized.
While the E_WR input is “high” and the S_WR input is “low”, serial input data (Sdata input), B_0 to B_7, is clocked serially into the enhancement register on the rising edge of Sclk, MSB (B_0) first. The enhancement register is double buffered to prevent inadvertent control changes during serial loading, with buffer capture of the serially-entered data performed on the falling edge of E_WR according to the timing diagram shown in Figure 6. After the falling edge of E_WR, the data provides control bits as shown in Table 8 with bit functionality enabled by asserting the $\overline{\text{Enh}}$ input “low”.

Direct Interface Mode

Direct Interface Mode is selected by setting the $\overline{\text{Bmode}}$ input “high”.

Counter control bits are set directly at the pins as shown in Table 7. In Direct Interface Mode, main counter inputs M_7 and M_8, and R Counter inputs R_4 and R_5 are internally forced low (“0”).

Table 7. Primary Register Programming

Interface Mode	$\overline{\text{Enh}}$	$\overline{\text{Bmode}}$	Smode	R_5	R_4	M_8	M_7	$\overline{\text{Pre\_en}}$	M_6	M_5	M_4	M_3	M_2	M_1	M_0	R_3	R_2	R_1	R_0	A_3	A_2	A_1	A_0
Parallel	1	0	0	M2_WR rising edge load				M1_WR rising edge load								A_WR rising edge load							
				D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Serial*	1	0	1	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9	B_{10}	B_{11}	B_{12}	B_{13}	B_{14}	B_{15}	B_{16}	B_{17}	B_{18}	B_{19}
Direct	1	1	X	0	0	0	0	$\overline{\text{Pre\_en}}$	M_6	M_5	M_4	M_3	M_2	M_1	M_0	R_3	R_2	R_1	R_0	A_3	A_2	A_1	A_0

*Serial data clocked serially on Sclk rising edge while E_WR “low” and captured in secondary register on S_WR rising edge.

MSB (first in) ↑ (last in) LSB ↑

Table 8. Enhancement Register Programming

Interface Mode	$\overline{\text{Enh}}$	$\overline{\text{Bmode}}$	Smode	Reserved	Reserved	Reserved	Power down	Counter load	MSEL output	Prescaler output	f_c, f_p OE
Parallel	0	0	0	E_WR rising edge load							
				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Serial*	0	0	1	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7

*Serial data clocked serially on Sclk rising edge while E_WR “high” and captured in the double buffer on E_WR falling edge.

MSB (first in) ↑ (last in) LSB ↑

Figure 7. Parallel Interface Mode Timing Diagram

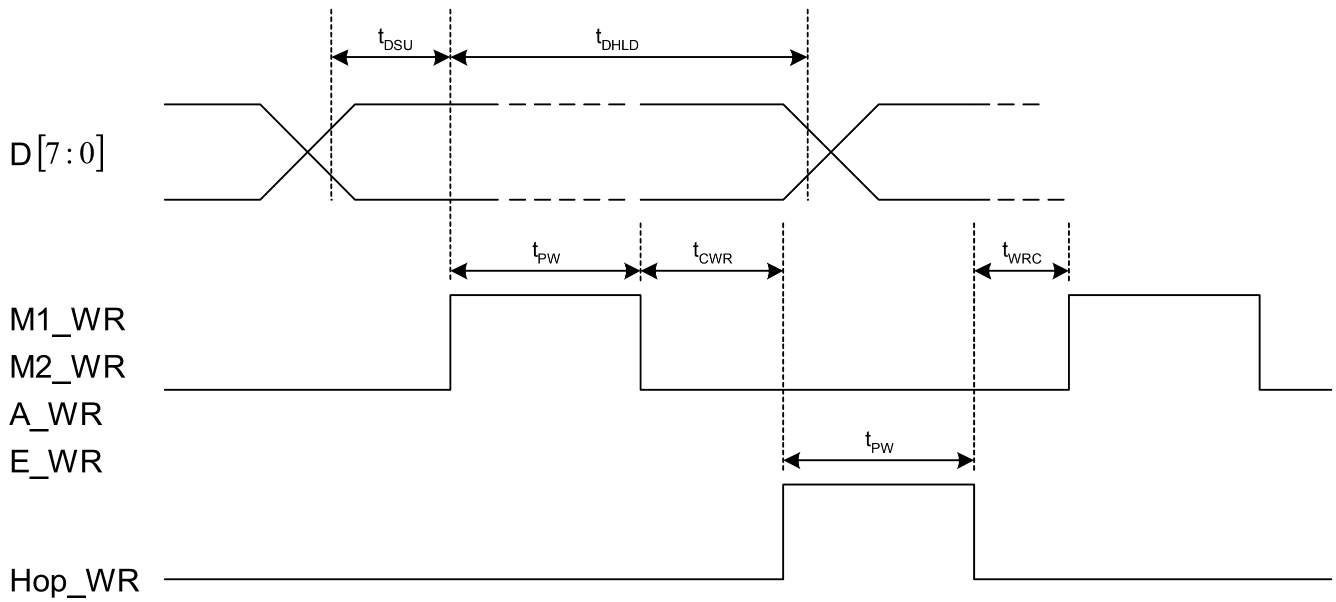
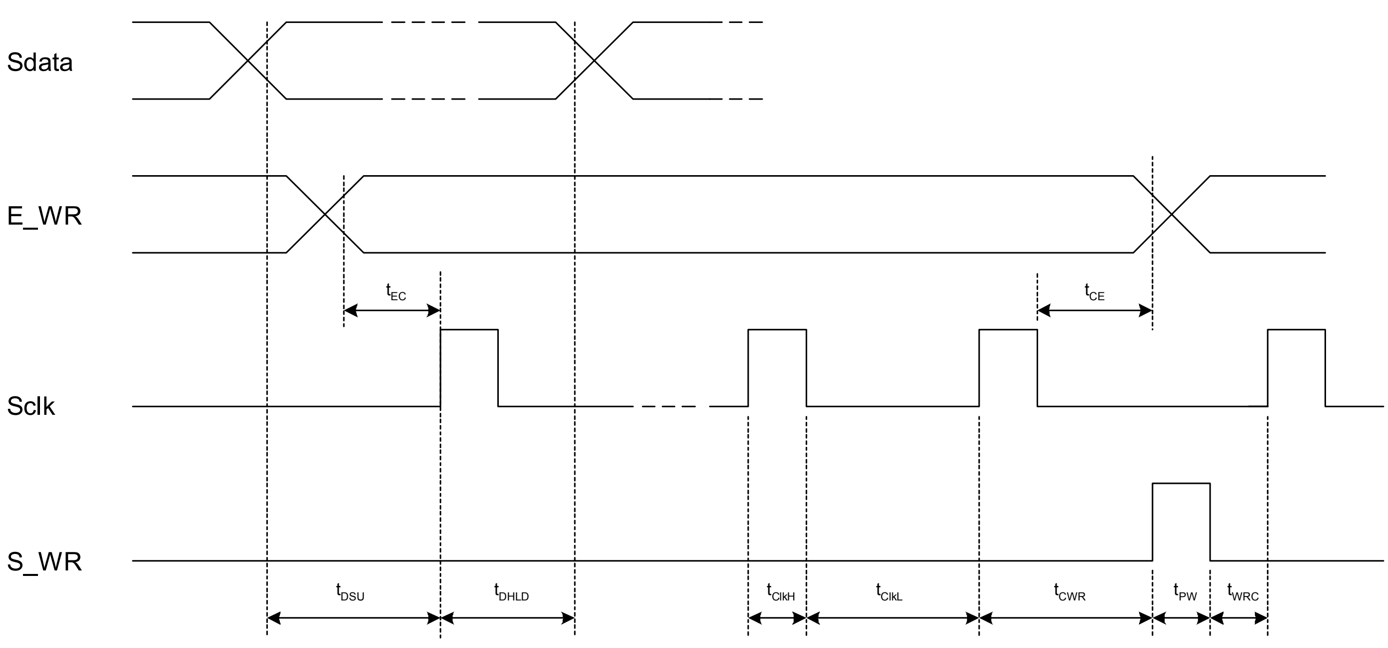


Figure 8. Serial Interface Mode Timing Diagram



Enhancement Register

The functions of the enhancement register bits are shown below with all bits active “high”.

Table 9. Enhancement Register Bit Functionality

Bit Function		Description
Bit 0	Reserved**	
Bit 1	Reserved**	
Bit 2	Reserved**	
Bit 3	Power down	Power down of all functions except programming interface.
Bit 4	Counter load	Immediate and continuous load of counter programming as directed by the $\overline{\text{Bmode}}$ and Smode inputs.
Bit 5	MSEL output	Drives the internal dual modulus prescaler modulus select (MSEL) onto the Dout output.
Bit 6	Prescaler output	Drives the raw internal prescaler output (fmain) onto the Dout output.
Bit 7	f_p, f_c OE	f_p, f_c outputs disabled.

** Program to 0

Phase Detector

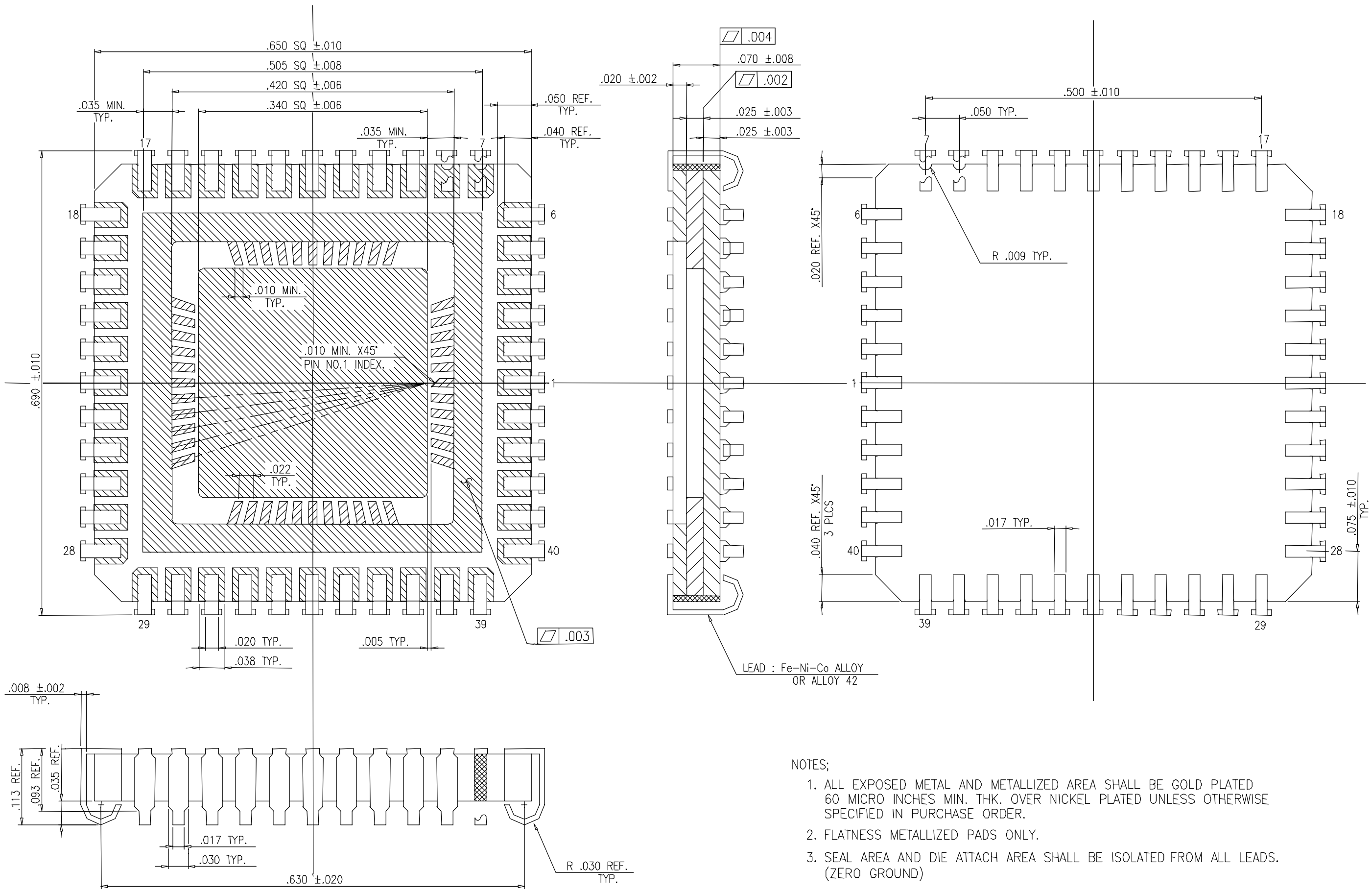
The phase detector is triggered by rising edges from the main Counter (f_p) and the reference counter (f_c). It has two outputs, namely PD_Ū, and PD_D̄. If the divided VCO leads the divided reference in phase or frequency (f_p leads f_c), PD_D̄ pulses “low”. If the divided reference leads the divided VCO in phase or frequency (f_r leads f_p), PD_Ū pulses “low”. The width of either pulse is directly proportional to phase offset between the two input signals, f_p and f_c. The phase detector gain is 430 mV / radian.

PD_Ū and PD_D̄ are designed to drive an active loop filter which controls the VCO tune voltage.

PD_Ū pulses result in an increase in VCO frequency and PD_D̄ results in a decrease in VCO frequency.

A lock detect output, LD is also provided, via the pin Cext. Cext is the logical “NAND” of PD_Ū and PD_D̄ waveforms, which is driven through a series 2k ohm resistor. Connecting Cext to an external shunt capacitor provides integration. Cext also drives the input of an internal inverting comparator with an open drain output. Thus LD is an “AND” function of PD_Ū and PD_D̄. See Figure 4 for a schematic of this circuit.

Figure 9. Package Drawing
44-lead CQFJ



All dimensions are in inches

Table 10. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
97022-01	PE97022 ES	Engineering Samples	44-pin CQFJ	40 units / Tray
97022-11	PE97022	Flight Units	44-pin CQFJ	40 units / Tray
97022-99	FA97022	Die Production Units	Die	100 units / waffle pack
97022-00	PE97022 EK	Evaluation Kit		1 / Box

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Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a DCN (Document Change Notice).

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