Actel POWER MATTERS

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CoreAPB3

DirectCore

Product Summary

Intended Use

- Intended for Use in Processor-Based Systems to Implement the AMBA APB Bus Fabric
- Allows Connection of either AMBA, APB2, or APB3 Peripherals to an APB3 Master
- Configured for Easy and Automatic System Design with CoreConsole
- To Be Used Only with APB Masters that Do Not Have Built-In APB Address Decoding

Key Features

- Up to 16 Slave Devices (APB2 or APB3) Supported
- Automatic Connection to AHB Bridge (CoreAHBtoAPB3) and APB Slaves, as well as APB3 Slaves
- Provides Configurable Address Decoding for APB Slots

Benefits

- Allows Easy Connection of APB Devices to a CoreMP7 or Cortex™-M1 Subsystem
- Auto Stitch in CoreConsole for Rapid Development
- Compatible with AMBA, CoreMP7, and Cortex-M1

Supported Device Families

- Fusion
- IGLOO™
- IGLOOe
- ProASIC®3L
- ProASIC3
- ProASIC3E

Synthesis and Simulation Support

- Supported in the Actel Libero® Integrated Design Environment (IDE)

Verification and Compliance

- Compliant with AMBA

Contents

General Description

Along with CoreAHBtoAPB3, the CoreAPB3 bus component provides an AMBA APB fabric that supports up to 16 APB slaves. CoreAHBtoAPB3 provides APB address decoding in the form of select signals. CoreAPB3 is concerned with multiplexing the read data busses, PREADY signals, and PSLVERR signals to send to CoreAHBtoAPB3. Figure 1 gives an illustration of CoreAPB3.

There is one APB master, which sends out a PSEL signal to CoreAPB3. This is used by CoreAPB3, along with appropriate bits from the PADDR bus, to decode the appropriate PSELS signal. This address decoding is dependent on the RangeSize hardware parameter/generic. All 16 APB slots are always of equal size. However, this size may be configured as any value from 256 locations to 1 M locations by setting RangeSize appropriately (via CoreConsole).

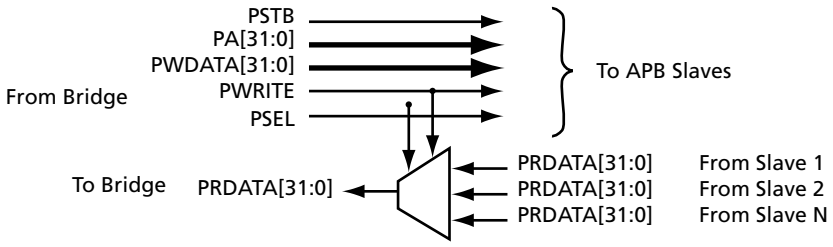

Figure 1 • **CoreAPB3**

Pinout

The pinout of CoreAPB3 is shown in Figure 2.

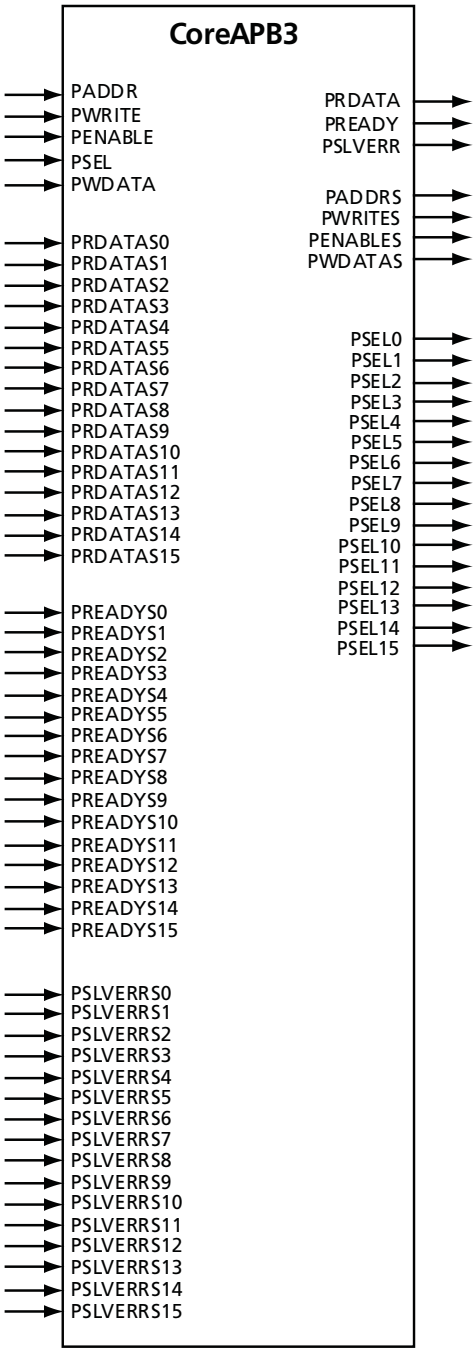

Figure 2 • **CoreAPB3 Pinout**

Connecting CoreAPB3 in CoreConsole

Table 1 lists the ports present on the APB bus and describes how to connect these in CoreConsole.

Table 1 • **APB Bus Connections**

Connection	CoreConsole Label	Description
Required Connections		
APB3 mirrored master interface	APB3mmaster	This interface connects to the APB3master interface of CoreAHBtoAPB3.
Optional Connections		
	APBmslave0	APB mirrored slave 0 interface
	APBmslave1	APB mirrored slave 1 interface
	APBmslave2	APB mirrored slave 2 interface
	APBmslave3	APB mirrored slave 3 interface
	APBmslave4	APB mirrored slave 4 interface
	APBmslave5	APB mirrored slave 5 interface
	APBmslave6	APB mirrored slave 6 interface
	APBmslave7	APB mirrored slave 7 interface
	APBmslave8	APB mirrored slave 8 interface
	APBmslave9	APB mirrored slave 9 interface
	APBmslave10	APB mirrored slave 10 interface
	APBmslave11	APB mirrored slave 11 interface
	APBmslave12	APB mirrored slave 12 interface
	APBmslave13	APB mirrored slave 13 interface
	APBmslave14	APB mirrored slave 14 interface
	APBmslave15	APB mirrored slave 15 interface

Utilization

The utilization for CoreAPB3 in a Fusion, IGLOO, ProASIC3L, ProASIC3, or ProASIC3E device is 580 tiles when attached to 16 APB slave devices. The utilization in a ProASIC^{PLUS} device is 640 tiles for the same configuration. Both these numbers assume the use of typical synthesis conditions.

Ordering Information

The obfuscated RTL version of SysBASIC (SysBASIC-OC) is available for free with CoreConsole. The source RTL version of SysBASIC (SysBASIC-RM) can be ordered through your local Actel sales representative. CoreAPB3 cannot be ordered separately from the SysBASIC core bundle.

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v2.1)	Page
v2.0	The "Supported Device Families" section was updated to include ProASIC3L.	1
	The "Utilization" section was updated to include ProASIC3L.	3
Advanced v0.1	The "Product Summary" section and "Utilization" section were updated to add Cortex-M1 and IGLOO/e information.	1, 3
	The "Ordering Information" section was updated to state that CoreAPB3 cannot be ordered separately from the SysBASIC core bundle.	3

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," and "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of an advanced or production datasheet containing general product information. This brief summarizes specific device and family information for unreleased products.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

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