Features

- **Contactless Read/Write Data Transmission**
- **Radio Frequency f_{RF} from 100 kHz to 150 kHz**
- **e5550, e5551, T5557 Binary Compatible**
- **Extended Mode**
- **Small Size, Configurable for ISO/IEC 11784/785 Compatibility**
- **75 pF On-chip Resonant Capacitor (Mask Option)**
- **7 × 32-bit EEPROM Data Memory Including 32-bit Password**
- **Separate 64-bit Memory for Traceability Data**
- **32-bit Configuration Register in EEPROM to Setup:**
  - **Data Rate**
    - **RF/2 to RF/128, Binary Selectable, or**
    - **Fixed e5550 Data Rates**
  - **Modulation/Coding**
    - **FSK, PSK, Manchester, Bi-phase, NRZ**
  - **Other Options**
    - **Password Mode**
    - **Max Block Feature**
    - **Answer-On-Request (AOR) Mode**
    - **Inverse Data Output**
    - **Direct Access Mode**
    - **Sequence Terminator(s)**
    - **Write Protection (Through Lock-bit per Block)**
    - **Fast Write Method (5 Kbps versus 2 Kbps)**
    - **OTP Functionality**
    - **POR Delay up to 67 ms**

Multifunctional 330-bit Read/Write RF Identification IC

ATA5567

1. Description

The ATA5567 is a contactless R/W IDentification IC (IDIC®) for applications in the 125-kHz frequency range. A single coil, connected to the chip, serves as the IC's power supply and bi-directional communication interface. The antenna and chip together form a transponder or tag.

The on-chip 330-bit EEPROM (10 blocks, 33 bits each) can be read and written block-wise from a reader. Block 0 is reserved for setting the operation modes of the ATA5567 tag. Block 7 may contain a password to prevent unauthorized writing.

Data is transmitted from the IDIC using load modulation. This is achieved by damping the RF field with a resistive load between the two terminals Coil 1 and Coil 2. The IC receives and decodes 100% amplitude-modulated (OOK) pulse-interval-encoded bit streams from the base station or reader.
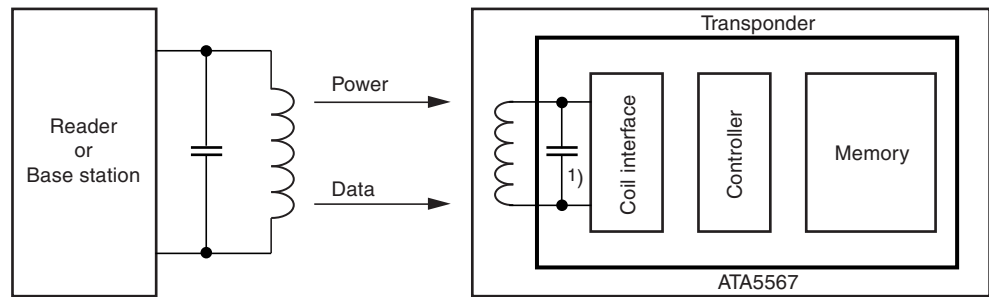
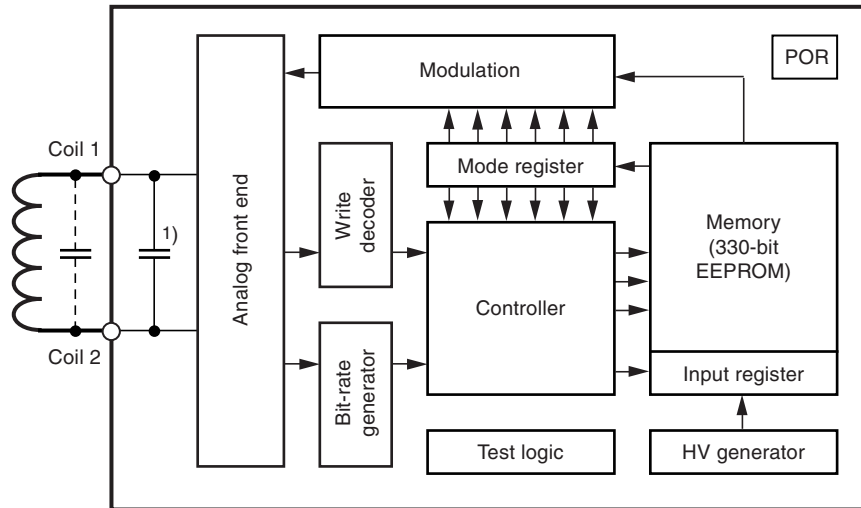## 2. System Block Diagram

Figure 2-1. RFID System Using ATA5567 Tag

1) Mask option

3. ATA5567 – Building Blocks

Figure 3-1. Block Diagram

1) Mask option

3.1 Analog Front End (AFE)

The AFE includes all circuits which are directly connected to the coil. It generates the IC's power supply and handles the bi-directional data communication with the reader. It consists of the following blocks:

- Rectifier to generate a DC supply voltage from the AC coil voltage
- Clock extractor
- Switchable load between Coil 1 and Coil 2 for data transmission from the tag to the reader
- Field gap detector for data transmission from the base station to the tag
- ESD protection circuitry

3.2 Data-rate Generator

The data rate is binary programmable to operate at any data rate between RF/2 and RF/128 or equal to any of the fixed e5550/e5551 and T5554 bit rates (RF/8, RF/16, RF/32, RF/40, RF/50, RF/64, RF/100, and RF/128).

3.3 Write Decoder

This function decodes the write gaps and verifies the validity of the data stream according to the Atmel e555x write method (pulse interval encoding).

3.4 HV Generator

This on-chip charge pump circuit generates the high voltage required for programming of the EEPROM.

3.5 DC Supply

Power is externally supplied to the IDIC via the two coil connections. The IC rectifies and regulates this RF source and uses it to generate its supply voltage.

3.6 Power-On Reset (POR)

This circuit delays the IDIC functionality until an acceptable voltage threshold has been reached.

3.7 Clock Extraction

The clock extraction circuit uses the external RF signal as its internal clock source.

3.8 Controller

The control-logic module executes the following functions:

- Loads mode register with configuration data from EEPROM block 0 after power-on and also during reading
- Controls memory access (read, write)
- Handles write data transmission and write error modes

The first two bits of the reader to tag data stream are the opcode, for example, write, direct access, or reset.

In password mode, the 32 bits received after the opcode are compared with the password stored in memory block 7.

3.9 Mode Register

The mode register stores the configuration data from the EEPROM block 0. It is continually refreshed at the start of every block read and (re-)loaded after any POR event or reset command. On delivery, the mode register is preprogrammed with the value 0014 8000h which corresponds to continuous read of block 0, Manchester coded, RF/64.

Figure 3-2. Block 0 Configuration Mapping – e5550 Compatibility Mode

L	1 2 3 4	5 6 7 8	9 10 11 12	13 14 15 16	17 18 19 20	21 22 23 24	25 26 27 28	29 30 31 32
	0 1 1 0	0 0 0 0	0 0 0	0		0		0 0

Field labels:
- **L**: Lock Bit — 0 = Unlocked, 1 = Locked
- **1 2 3 4**: Master Key (Note 1), 2))
- **Data Bit Rate** (bits 9–12 region):
  - RF/8 = 0 0 0
  - RF/16 = 0 0 1
  - RF/32 = 0 1 0
  - RF/40 = 0 1 1
  - RF/50 = 1 0 0
  - RF/64 = 1 0 1
  - RF/100 = 1 1 0
  - RF/128 = 1 1 1
- **Modulation** (bits 17–20 region):
  - 0 0 0 0 0 = Direct
  - 0 0 0 0 1 = PSK1
  - 0 0 0 1 0 = PSK2
  - 0 0 0 1 1 = PSK3
  - 0 0 1 0 0 = FSK1
  - 0 0 1 0 1 = FSK2
  - 0 0 1 1 0 = FSK1a
  - 0 0 1 1 1 = FSK2a
  - 0 1 0 0 0 = Manchester
  - 1 0 0 0 0 = Bi-phase ('50)
  - 1 1 0 0 0 = Reserved
- **PSK CF** (bits 21–24 region):
  - 0 0 = RF/2
  - 0 1 = RF/4
  - 1 0 = RF/8
  - 1 1 = Res
- **AOR**
- **Max Block** (bits 25–28)
- **PWD**
- **ST-sequence Terminator**
- **POR delay** (bits 29–32)

1) If Master Key = 6 then test mode write commands are ignored
2) If Master Key < > 6 or 9 then extended function mode is disabled

3.10 Modulator

The modulator consists of data encoders for the following basic types of modulation:

Table 3-1. Types of e5550-compatible Modulation Modes

Mode	Direct Data Output		
FSK1a[1]	FSK/8-/5	0 = RF/8;	1 = RF/5
FSK2a[1]	FSK/8-/10	0 = RF/8;	1 = RF/10
FSK1[1]	FSK/5-/8	0 = RF/5;	1 = RF/8
FSK2[1]	FSK/10-/8	0 = RF/10;	1 = RF/8
PSK1[2]	Phase change when input changes		
PSK2[2]	Phase change on bit clock if input high		
PSK3[2]	Phase change on rising edge of input		
Manchester	0 = falling edge, 1 = rising edge		
Bi-phase	1 creates an additional mid-bit change		
NRZ	1 = damping on, 0 = damping off		

Notes: 1. A common multiple of bit rate and FSK frequencies is recommended.
2. In PSK mode the selected data rate has to be an integer multiple of the PSK sub-carrier frequency.

3.11 Memory

The memory is a 330-bit EEPROM, which is arranged in 10 blocks of 33 bits each. All 33 bits of a block, including the lock bit, are programmed simultaneously.

Block 0 of page 0 contains the mode/configuration data, which is not transmitted during regular-read operations. Block 7 of page 0 may be used as a write protection password.

Bit 0 of every block is the lock bit for that block. Once locked, the block (including the lock bit itself) is not re-programmable through the RF field.

Blocks 1 and 2 of page 1 contain traceability data and are transmitted with the modulation parameters defined in the configuration register after the opcode "11" is issued by the reader (see). These traceability data blocks are programmed and locked by Atmel.

Figure 3-3.   Memory Map
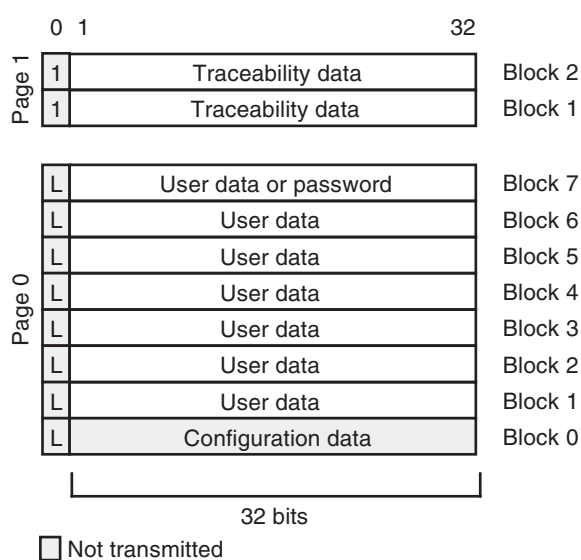

3.12 Traceability Data Structure

Blocks 1 and 2 of page 1 contain the traceability data and are programmed and locked by Atmel during production testing[1]. The most significant byte of block 1 is fixed to E0h, the allocation class (ACL) as defined in ISO/IEC 15963-1. The second byte is therefore defined as Atmel®'s manufacturer ID (15h). The following 8 bits are used as IC reference byte (ICR bits 47 to 40). The 3 most significant bits define the IC version of the ATA5567, the foundry version, or both. The lower 5 bits are by default reset (00) as the Atmel standard value. Other values may be assigned, by request, to high volume customers as tag issuer identification.

The lower 40 bits of the data encode Atmel's traceability information, and conform to a unique numbering system. These 40 data bits are divided in two sub-groups, a 5-digit lot ID number, and the binary wafer number (5 bits) concatenated with the sequential die number per wafer.

Note: 1. This is only valid for sawn wafer "DDB, DDT" delivery.

Figure 3-4. ATA5567 Traceability Data Structure
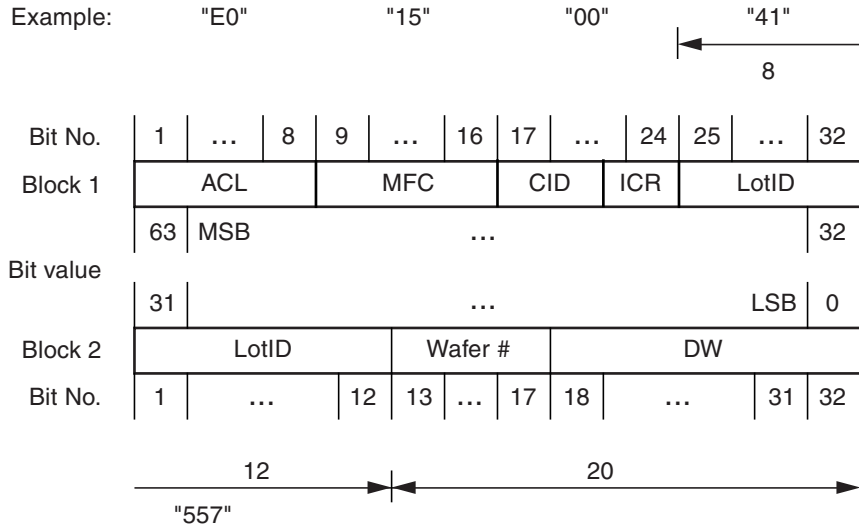
ACL   Allocation class as defined in ISO/IEC 15963-1 = E0h
MFC   Manufacturer code of Atmel Corporation as defined in ISO/IEC 7816-6 = 15h
UID   UID issuer identifier on request (respectively 5 bit CID and 3 bit ICR)
    CID   Customer ID on request
    ICR   IC revision
LotID   5-digit lot number, e.g., "41557"
Wafer#   5 bits for wafer#
DW   15 bits encoded as sequential die on wafer number

4. Operating the ATA5567

4.1 Initialization and POR Delay

The Power-On-Reset (POR) circuit remains active until an adequate voltage threshold has been reached. This threshold will be reached also if the coil voltage ramps up in terms of a few volts per second. It means that the tag can be moved slowly towards the reader without performance loss. This in turn triggers the default start-up delay sequence. During this configuration period of about 192 field clocks, the ATA5567 is initialized with the configuration data stored in EEPROM block 0. During initialization of the configuration block 0, for all ATA55670x variants the load damping is active permanently (see Figure 4-5 on page 10). The ATA55671x types (without damping option) achieve a longer read range based on the lower activation field strength.

If the POR-delay bit is reset, no additional delay is observed after the configuration period. Tag modulation in regular-read mode will be observed about 3 ms after entering the RF field. If the POR delay bit is set, the ATA5567 remains in a permanent damping state until 8190 internal field clocks have elapsed.

$$T_{INIT} = (192 + 8190 \times POR\ delay) \times T_C \approx 67\ ms; T_C = 8\ \mu s\ at\ 125\ kHz$$

Any field gap occurring during this initialization phase will restart the complete sequence. After this initialization time the ATA5567 enters regular-read mode and modulation starts automatically using the parameters defined in the configuration register.

## 4.2 Tag to Reader Communication

During normal operation, the data stored within the EEPROM is cycled and the Coil 1 and Coil 2 terminals are load modulated. This resistive load modulation can be detected at the reader module.

4.3 Regular-read Mode

In regular-read mode, data from the memory is transmitted serially, starting with block 1, bit 1, up to the last block (for example, 7), bit 32. The last block which will be read is defined by the mode parameter field MAXBLK in EEPROM block 0. When the data block addressed by MAX-BLK has been read, data transmission restarts with block 1, bit 1.

The user may limit the cyclic data stream in regular-read mode by setting the MAXBLK between 0 and 7 (representing each of the 8 data blocks). If set to 7, blocks 1 through 7 can be read. If set to 1, only block 1 is transmitted continuously. If set to 0, the contents of the configuration block (normally not transmitted) can be read. In the case of MAXBLK = 0 or 1, regular-read mode can not be distinguished from block-read mode.

Figure 4-1. Examples for Different MAXBLK Settings
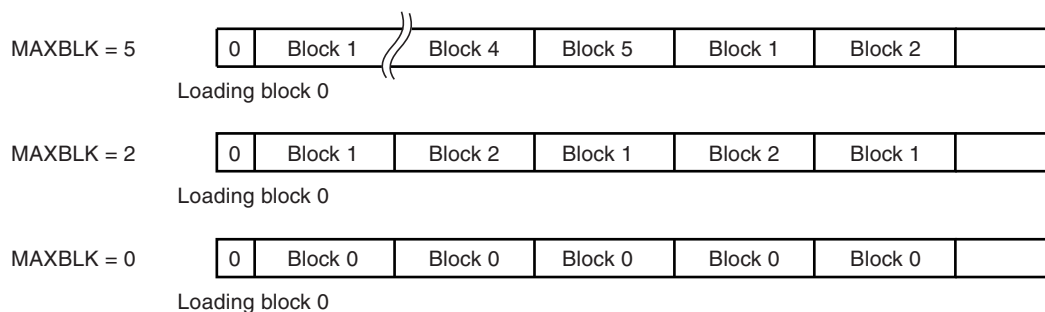
Every time the ATA5567 enters regular-read or block-read mode, the first bit transmitted is a logical 0. The data stream starts with block 1, bit 1, continues through MAXBLK, bit 32, and cycles continuously if in regular-read mode.

Note: This behavior is different from the original e555x and helps to decode PSK-modulated data.

4.4 Block-read Mode

With the direct access command, only the addressed block is repetitively read. This mode is called block-read mode. Direct access is entered by transmitting the page access opcode ("10" or "11"), a single "0" bit and the requested 3-bit block address when the tag is in normal mode.

In password mode (PWD bit set), the direct access to a single block needs the valid 32-bit password to be transmitted after the page access opcode, whereas a "0" bit and the 3-bit block address follow afterwards. In case the transmitted password does not match with the contents of block 7, the ATA5567 tag returns to the regular-read mode.

Note: A direct access to block 0 of page 1 will read the configuration data of block 0, page 0.
A direct access to blocks 3 to 7 of page 1 reads all data bits as zero.

4.5 e5550 Sequence Terminator

The sequence terminator ST is a special damping pattern which is inserted before the first block and may be used to synchronize the reader. This e5550-compatible sequence terminator consists of 4 bit periods with underlaying data values of "1". During the second and the fourth bit periods, modulation is switched off (Manchester encoding – switched on). Bi-phase modulated data blocks need fixed leading and trailing bits in combination with the sequence terminator to be identified reliably.

The sequence terminator may be individually enabled by setting mode bit 29 (ST = 1) in the e5550-compatibility mode (X-mode = 0).

In the regular-read mode, the sequence terminator is inserted at the start of each MAXBLK-limited read data stream.

In block-read mode – after any block-write or direct access command – or if MAXBLK was set to 0 or 1, the sequence terminator is inserted before the transmission of the selected block.

This behavior is especially different from former e5550-compatible ICs (T5551, T5554).

Figure 4-2. Read Data Stream with Sequence Terminator
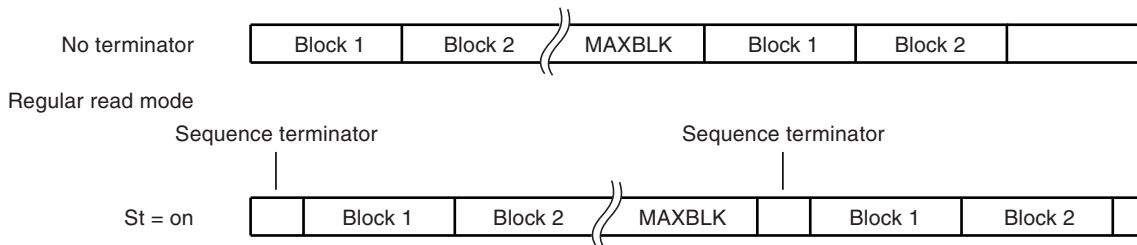
Figure 4-3. e5550-compatible Sequence Terminator Waveforms
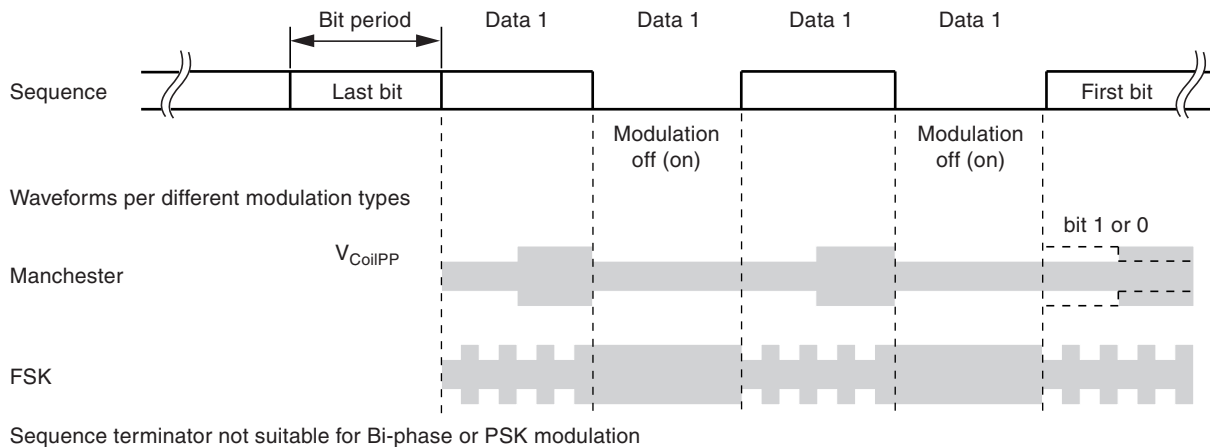
4.6   Reader to Tag Communication

Data is written to the tag by interrupting the RF field with short field gaps (on-off keying) in accordance with the e5550 write method. The time between two gaps encodes the "0" or "1" information to be transmitted (pulse interval encoding). The duration of the gaps is usually 50 μs to 150 μs. The time between two gaps is nominally 24 field clocks for a "0" and 54 field clocks for a "1". When there is no gap for more than 64 field clocks after a previous gap, the ATA5567 exits the write mode. The tag starts with the command execution if the correct number of bits were received. If a failure is detected, the ATA5567 does not continue and will enter regular-read mode.

4.7   Start Gap

The initial gap is referred to as the start gap. This triggers the reader to tag communication. During this mode of operation, the receive damping is permanently enabled to ease gap detection. The start gap may need to be longer than subsequent gaps in order to be detected reliably.

A start gap will be accepted at any time after the mode register has been loaded ($\geq$ 3 ms). A single gap will not change the previously selected page (by former opcode "10" or "11").

Figure 4-4.   Start of Reader to Tag Communication
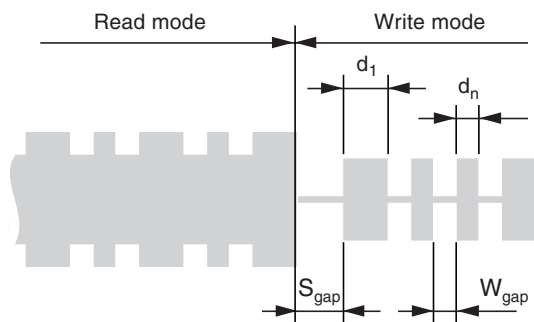
Table 4-1.   Write Data Decoding Scheme

Parameters	Remark	Symbol	Min.	Max.	Unit
Start gap		S_{gap}	10	50	FC
Write gap	Normal write mode	W_{gap}	8	30	FC
Write data in normal mode	"0" data	d_0	16	31	FC
	"1" data	d_1	48	63	FC

4.8 Write Data Protocol

The ATA5567 expects to receive a dual bit opcode as the first two bits of a reader command sequence. There are three valid opcodes:

- The opcodes "10" and "11" precede all block write and direct access operations for page 0 and page 1
- The RESET opcode "00" initiates a POR cycle
- The opcode "01" precedes all test mode write operations. Any test mode access is ignored after the master key (bits 1 to 4) in block 0 has been set to "6". Any further modifications of the master key are prohibited by setting the lock bit of block 0 or the OTP bit

Writing must follow these rules:

- Standard write needs the opcode, the lock bit, 32 data bits, and the 3-bit address (38 bits total)
- Protected write (PWD bit set) requires a valid 32-bit password between the opcode and data bits or address bits
- For the AOR wake-up command, an opcode and a valid password are necessary to select and activate a specific tag

Note: The data bits are read in the same order as written.

If the transmitted command sequence is invalid, the ATA5567 enters regular-read mode with the previously selected page (by former opcode "10" or "11").

Figure 4-5. Complete Writing Sequence
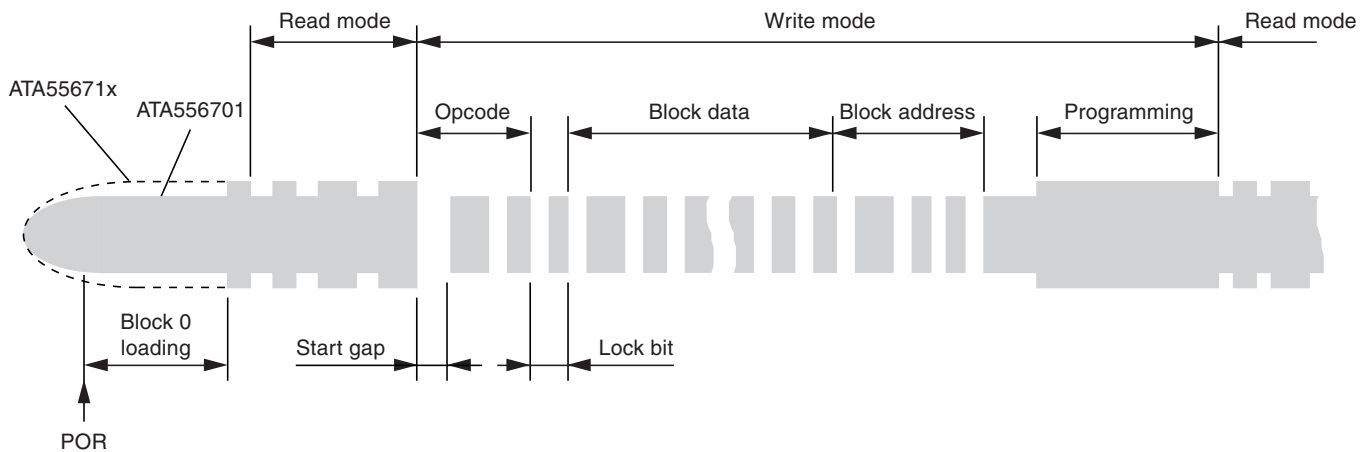
Figure 4-6. ATA5567 Command Formats
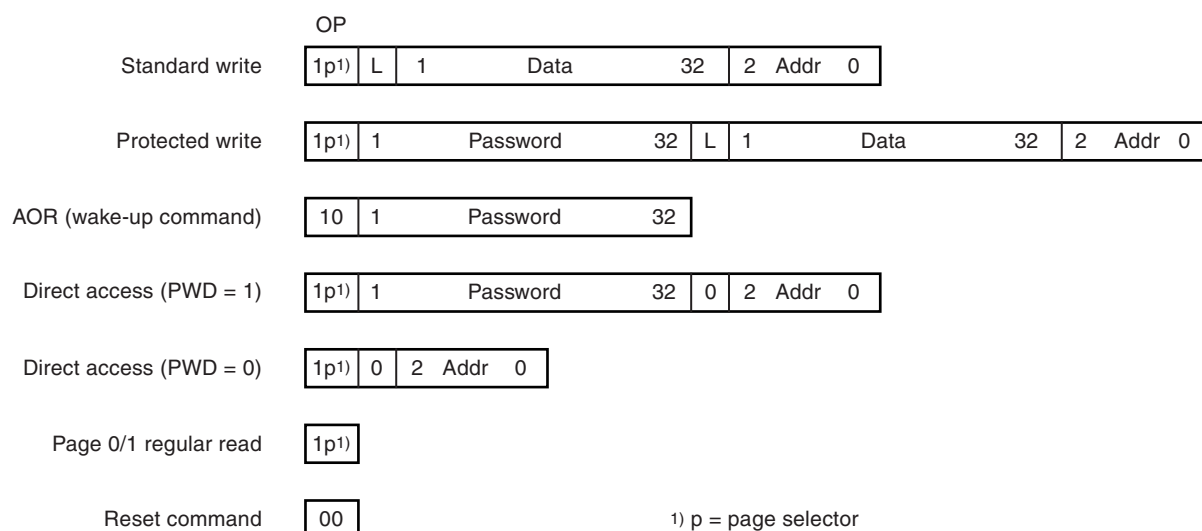
4.9 Password

When password mode is active (PWD = 1), the first 32 bits after the opcode are regarded as the password. They are compared bit by bit with the contents of block 7, starting at bit 1. If the comparison fails, the ATA5567 will not program the memory, instead it will restart in regular-read mode once the command transmission is finished.

Note: In password mode, MAXBLK should be set to a value below 7 to prevent the password from being transmitted by the ATA5567.

Each transmission of the direct access command (two opcode bits, 32-bit password, "0" bit plus 3 address bits = 38 bits) needs about 18 ms. Testing all possible combinations (about 4.3 billion) would take about two years.

4.10 Answer-On-Request (AOR) Mode

When the AOR bit is set, the ATA5567 does not start modulation in the regular-read mode after loading configuration block 0. The tag waits for a valid AOR data stream (wake-up command) from the reader before modulation is enabled. The wake-up command consists of the opcode ("10") followed by a valid password. The selected tag will remain active until the RF field is turned off or a new command with a different password is transmitted which may address another tag in the RF field.

Table 4-2. ATA5567 — Modes of Operation

PWD	AOR	Behavior of Tag after Reset Command or POR	De-activate Function
1	1	Answer-On-Request (AOR) mode: • Modulation starts after wake-up with a matching password • Programming needs valid password	Command with non-matching password deactivates the selected tag
1	0	Password mode: • Modulation in regular-read mode starts after reset • Programming and direct access needs valid password	
0	--	Normal mode: • Modulation in regular-read mode starts after reset • Programming and direct access without password	

Figure 4-7. Answer-On-Request (AOR) Mode

ATA55671x

ATA556701

$V_{Coil1 - Coil2}$

Modulation

Block 0
loading

POR

No modulation
because AOR = 1

AOR wake-up command
(with valid PWD)
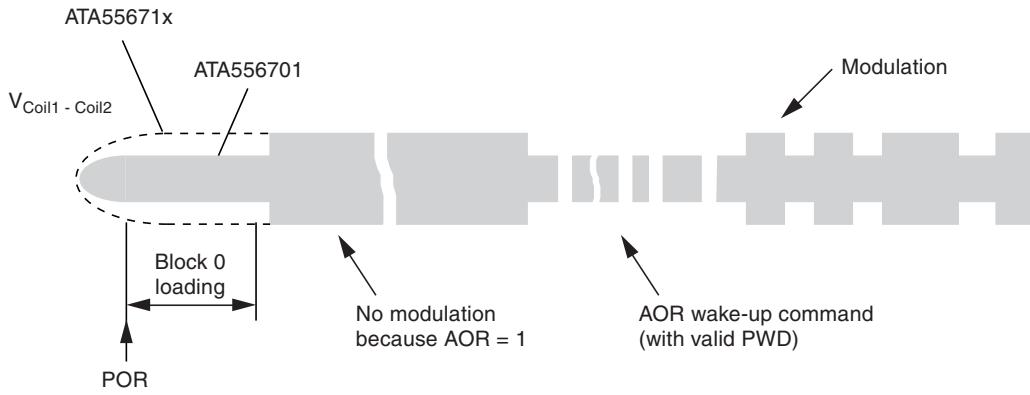
Figure 4-8. Coil Voltage after Programming of a Memory Block

$V_{Coil 1 - Coil 2}$

Write data to tag	5.6 ms	Read programmed memory block	POR or	Read block 1 to MAXBLK
	Programming and data verification	(Block-read mode)	Single gap	(Regular-read mode)
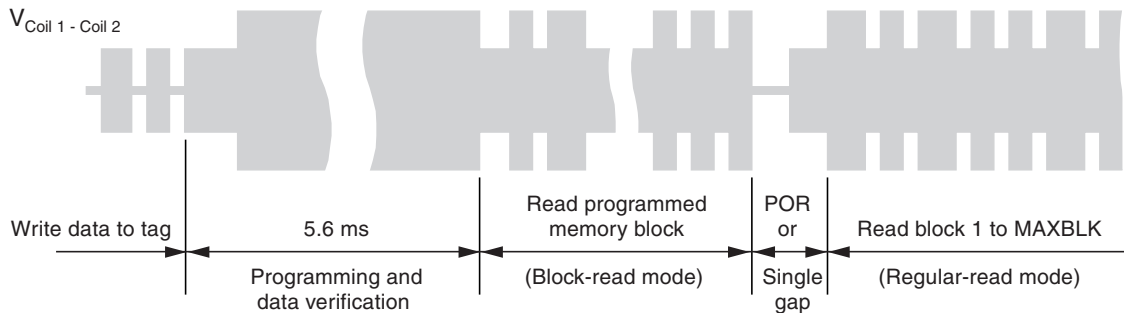
Figure 4-9. Anticollision Procedure Using AOR Mode
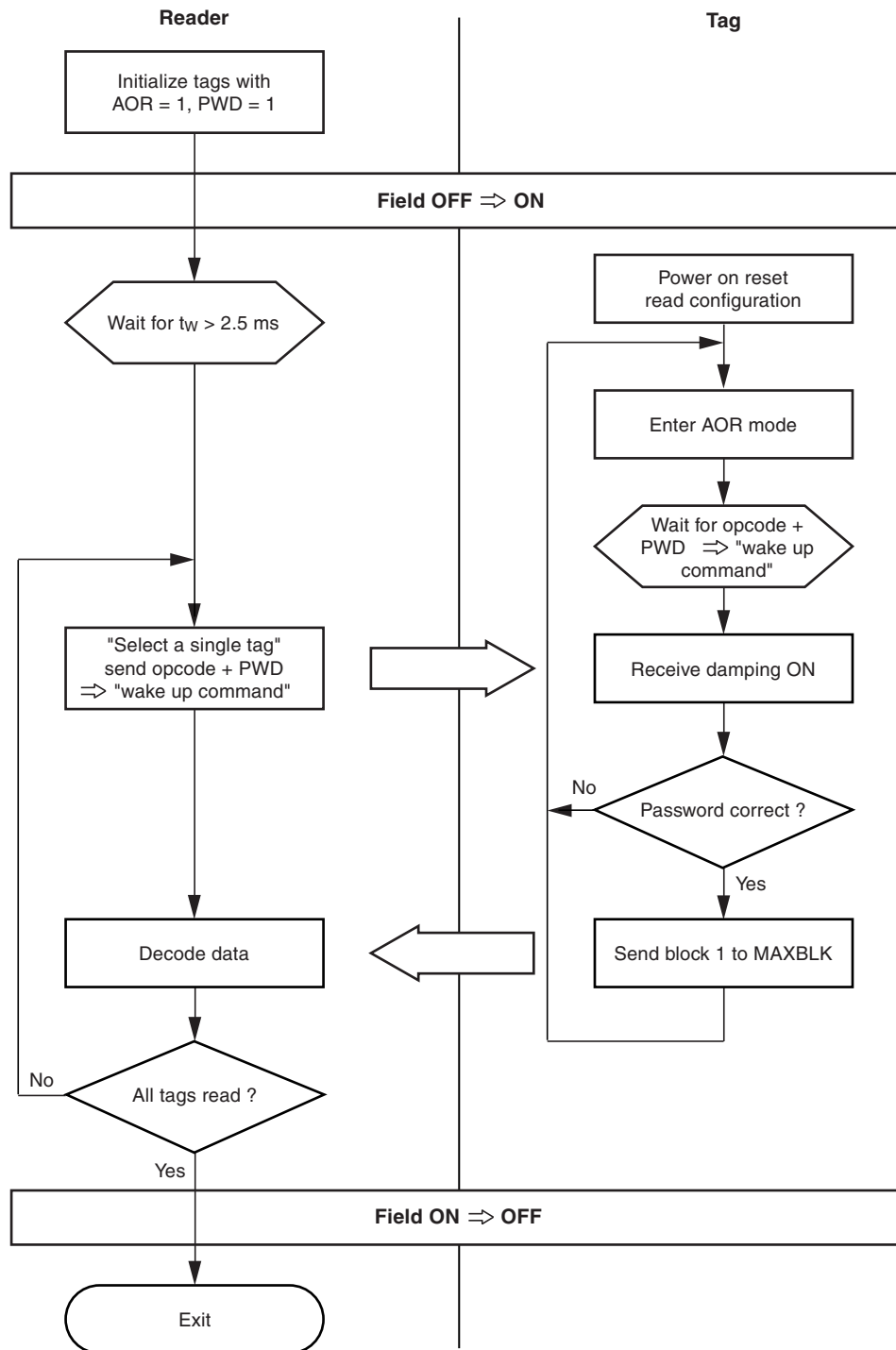
4.11 Programming

When all necessary information has been received by the ATA5567, programming may proceed. There is a clock delay between the end of the writing sequence and the start of programming.

Typical programming time is 5.6 ms. This cycle includes a data verification read to grant secure and correct programming. After programming was executed successfully, the ATA5567 enters block-read mode transmitting the block just programmed (see Figure 4-8 on page 12).

Note: This timing and behavior is different from the e555x-family predecessors.

5. Error Handling

Several error conditions can be detected to ensure that only valid bits are programmed into the EEPROM. There are two error types, which lead to two different actions.

5.1 Errors During Writing

The following detectable errors could occur during writing data to the ATA5567:

- Wrong number of field clocks between two gaps (that is, not a valid "1" or "0" pulse stream)
- Password mode is activated and the password does not match the contents of block 7
- The number of bits received in the command sequence is incorrect

Valid bit counts accepted by the ATA5567 are:

Password write	70 bits	(PWD = 1)
Standard write	38 bits	(PWD = 0)
AOR wake up	34 bits	(PWD = 1)
Direct access with PWD	38 bits	(PWD = 1)
Direct access	6 bits	(PWD = 0)
Reset command	2 bits	
Page 0/1 regular-read	2 bits	

If any of these erroneous conditions were detected, the ATA5567 enters regular-read mode, starting with block 1 of the page defined in the command sequence.

5.2 Errors Before or During Programming

If the command sequence was received successfully, the following error could still prevent programming:

- The lock bit of the addressed block is set already

In case of a locked block, programming mode will not be entered. The ATA5567 reverts to block-read mode, continuously transmitting the currently addressed block.

If the command sequence is validated and the addressed block is not write protected, the new data will be programmed into the EEPROM memory. The new state of the block write protection bit (lock bit) will be programmed at the same time accordingly.

Each programming cycle consists of 4 consecutive steps: erase block, erase verification (data = 0), programming, write verification (corresponding data bits = 1).

- If a data verification error is detected after an executed data block programming, the tag will stop modulation (modulation defeat) until a new command is transmitted.

Figure 5-1. ATA5567 Functional Diagram
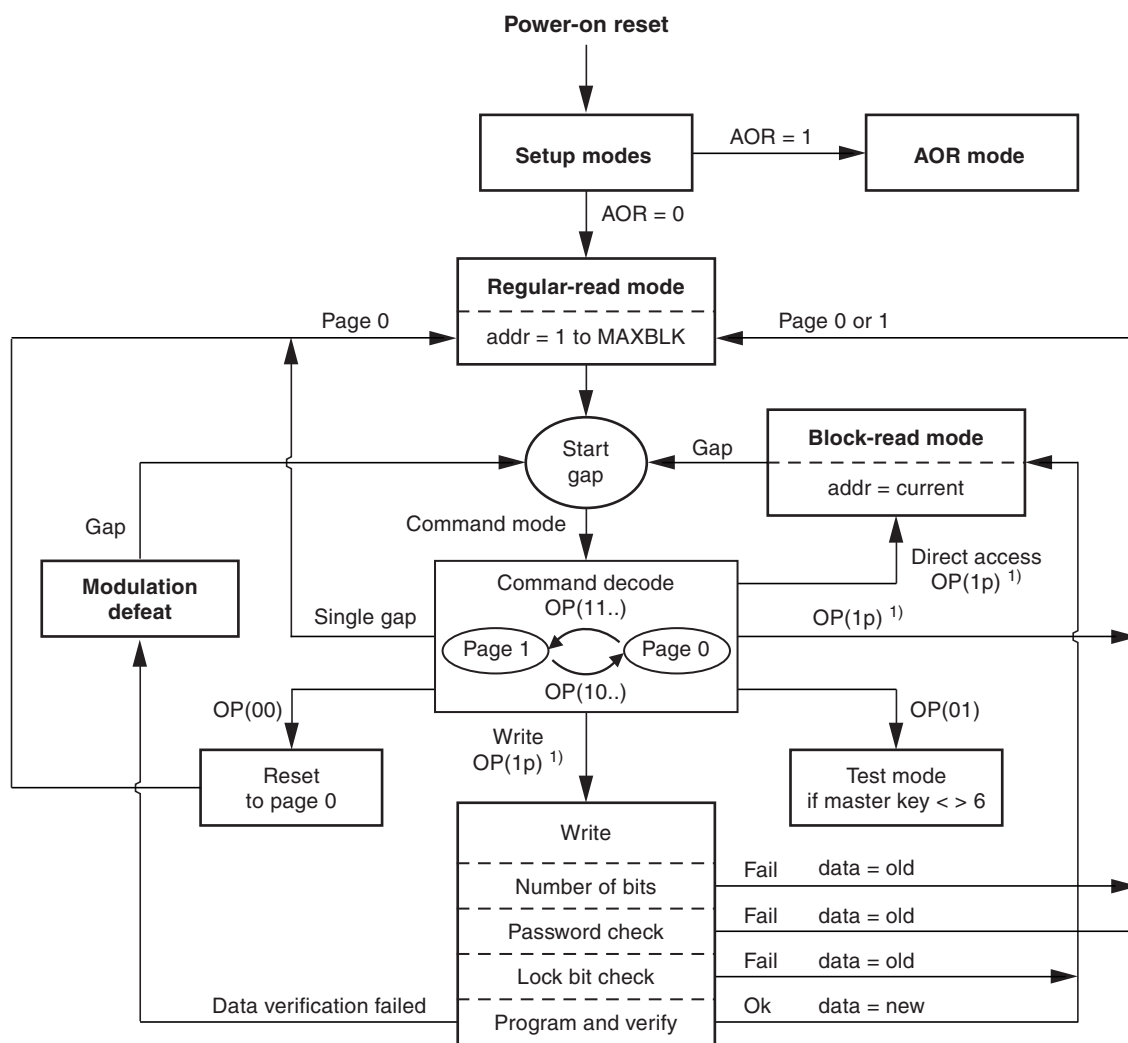
$^{1)}$ p = page selector

6. ATA5567 in Extended Mode (X-mode)

In general, the block 0 setting of the master key (bits 1 to 4) to the value "6" or "9" together with the X-mode bit will enable the extended mode functions.

- Master key = 9: Test mode access and extended mode are both enabled.
- Master key = 6: Any test mode access will be denied but the extended mode is still enabled.

Any other master key setting will prevent the activation of the ATA5567 extended mode options, even when the X-mode bit is set.

6.1 Binary Bit-rate Generator

In extended mode the data rate is binary programmable to operate at any data rate between RF/2 and RF/128 as given in the formula below.

Data rate = RF / (2n + 2)

6.2 OTP Functionality

If the OTP bit is set to "1", all memory blocks are write protected and behave as if all lock bits are set to 1. If the master key is set to "6" additionally, the ATA5567 mode of operation is locked forever (= OTP functionality).

If the master key is set to "9", the test-mode access allows the re-configuration of the tag again.

Figure 6-1. Block 0 — Configuration Map in Extended Mode (X-mode)

1) If Master Key = 6 and bit 15 is set, then test mode access is disabled and extended mode is active
2) If Master Key = 9 and bit 15 is set, then extended mode is enabled

Table 6-1. ATA5567 Types of Modulation in Extended Mode

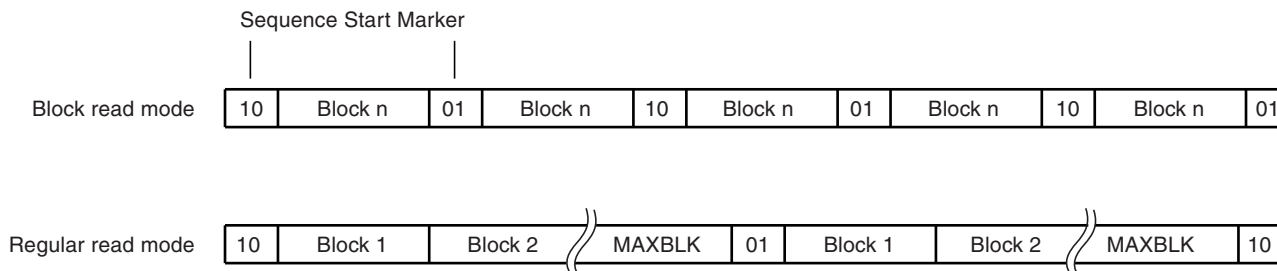| Mode	Direct Data Output Encoding	Inverse Data Output Encoding	
FSK1[1]	FSK/5-/8 0 = RF/5; 1 = RF/8	FSK/8-/5 0 = RF/8; 1 = RF/5	(= FSK1a)
FSK2[1]	FSK/10-/8 0 = RF/10; 1 = RF/8	FSK/8-/10 0 = RF/8; 1 = RF/10	(= FSK2a)
PSK1[2]	Phase change when input changes	Phase change when input changes	
PSK2[2]	Phase change on bit clock if input high	Phase change on bit clock if input low	
PSK3[2]	Phase change on rising edge of input	Phase change on falling edge of input	
Manchester	0 = falling edge, 1 = rising edge on mid-bit	1 = falling edge, 0 = rising edge on mid-bit	
Bi-phase 1 ('50)	"1" creates an additional mid-bit change	"0" creates an additional mid-bit change	
Bi-phase 2 ('57)	"0" creates an additional mid-bit change	"1" creates an additional mid-bit change	
NRZ	1 = damping on, 0 = damping off	0 = damping on, 1 = damping off	

Notes: 1.   A common multiple of bit rate and FSK frequencies is recommended.

2.   In PSK mode the selected data rate has to be an integer multiple of the PSK sub-carrier frequency.

6.3 Sequence Start Marker

**Figure 6-2.** ATA5567 Sequence Start Marker in Extended Mode

Sequence Start Marker

Block read mode	10	Block n	01	Block n	10	Block n	01	Block n	10	Block n	01

Regular read mode	10	Block 1	Block 2	MAXBLK	01	Block 1	Block 2	MAXBLK	10

The ATA5567 sequence start marker is a special damping pattern, which may be used to synchronize the reader. The sequence start marker consists of two bits ("01" or "10") which are inserted as a header before the first block to be transmitted if bit 29 in extended mode is set. At the start of a new block sequence, the value of the two bits is inverted.

6.4 Inverse Data Output

The ATA5567 supports in its extended mode (X-mode) an inverse data output option. If inverse data is enabled, the modulator as shown in Figure 6-3 works on inverted data (see Table 6-1 on page 16). This function is supported for all basic types of encoding.

Figure 6-3. Data Encoder for Inverse Data Output
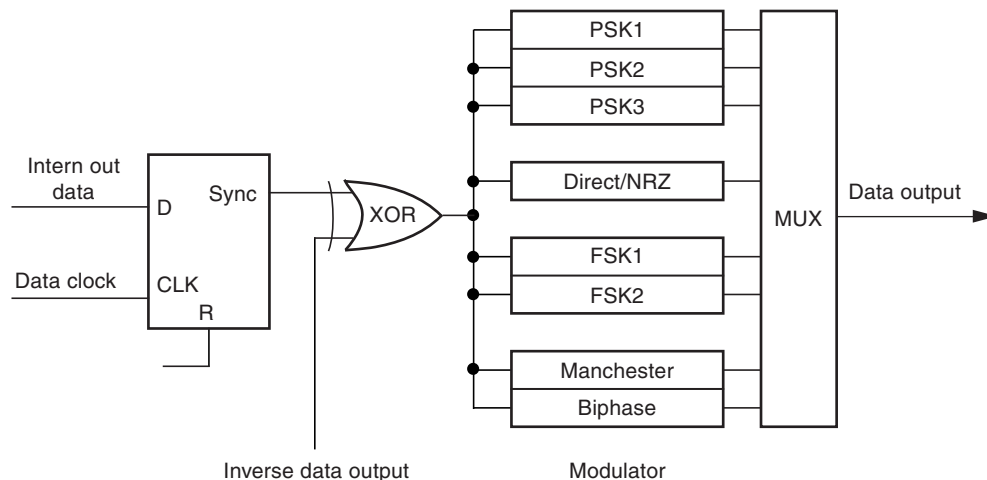
6.5 Fast Write

In the optional fast write mode, the time between two gaps is nominally 12 field clocks for a "0" and 27 field clocks for a "1". When there is no gap for more than 32 field clocks after a previous gap, the ATA5567 will exit the write mode. Please refer to .

Table 6-2. Fast Write Data Decoding Schemes

Parameters	Remark	Symbol	Min.	Max.	Unit
Start gap	–	S_{gap}	10	50	FC
Write gap	Normal write mode	Wn_{gap}	8	30	FC
	Fast write mode	Wf_{gap}	8	20	FC
Write data in normal mode	"0" data	d_0	16	31	FC
	"1" data	d_1	48	63	FC
Write data in fast mode	"0" data	d_0	8	15	FC
	"1" data	d_1	24	31	FC

Figure 6-4. Example of Manchester Coding with Data Rate RF/16
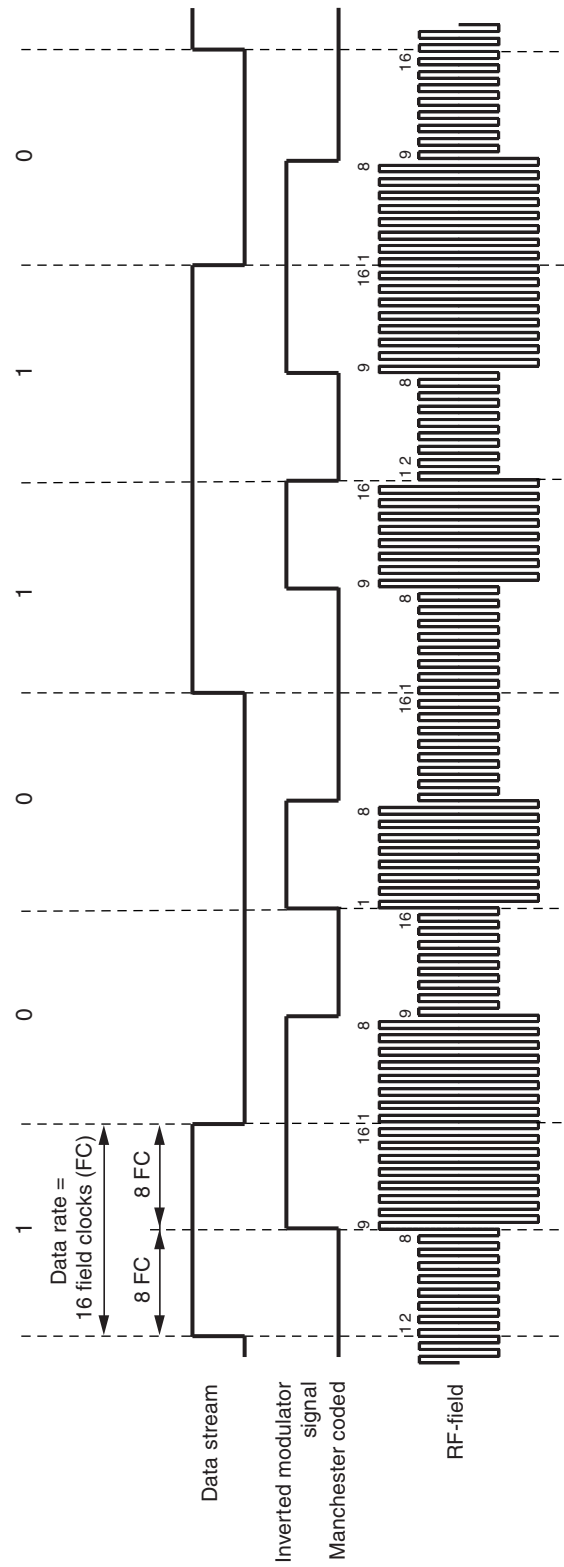
Figure 6-5. Example of Bi-phase Coding with Data Rate RF/16
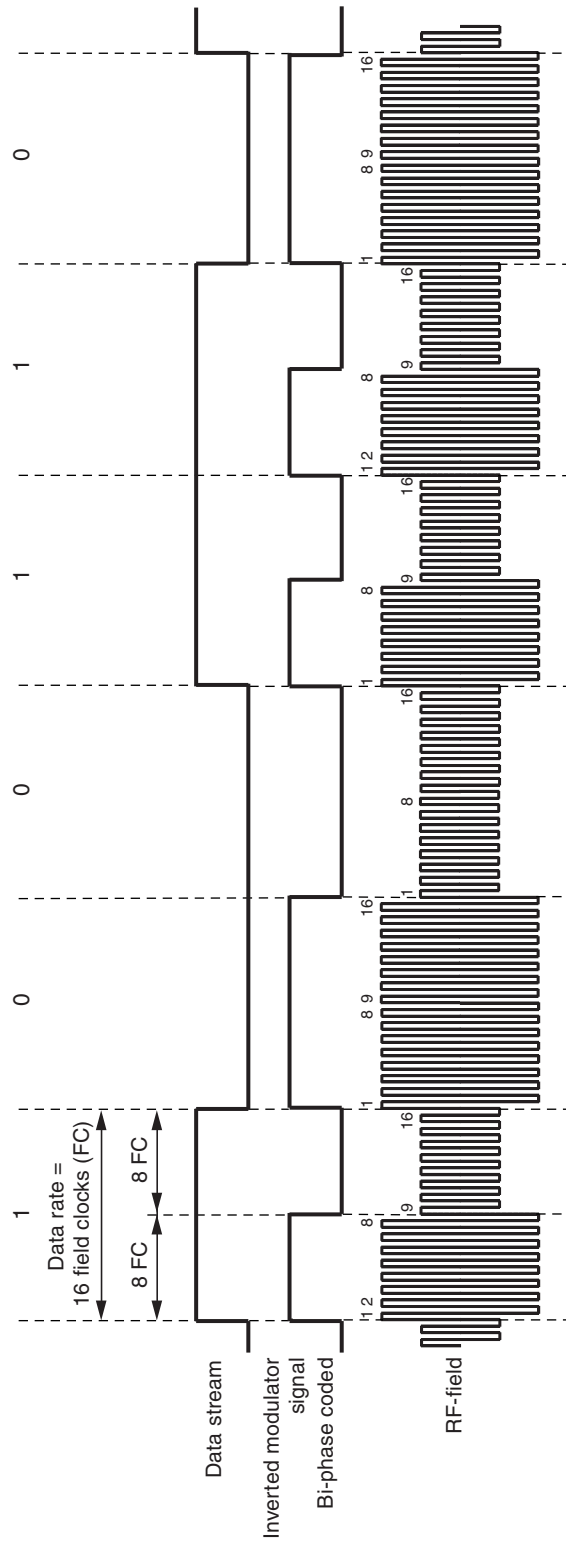
Figure 6-6. Example: FSK1a Coding with Data Rate RF/40, Subcarrier f_0 = RF/8, f_1 = RF/5
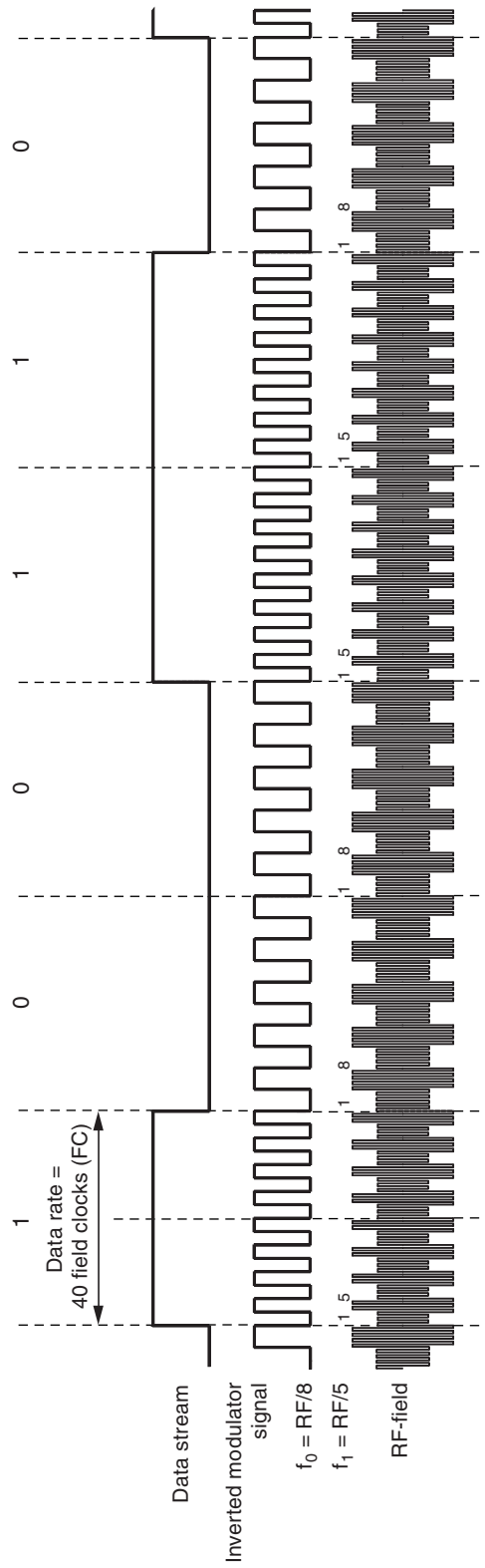
Figure 6-7. Example of PSK1 Coding with Data Rate RF/16
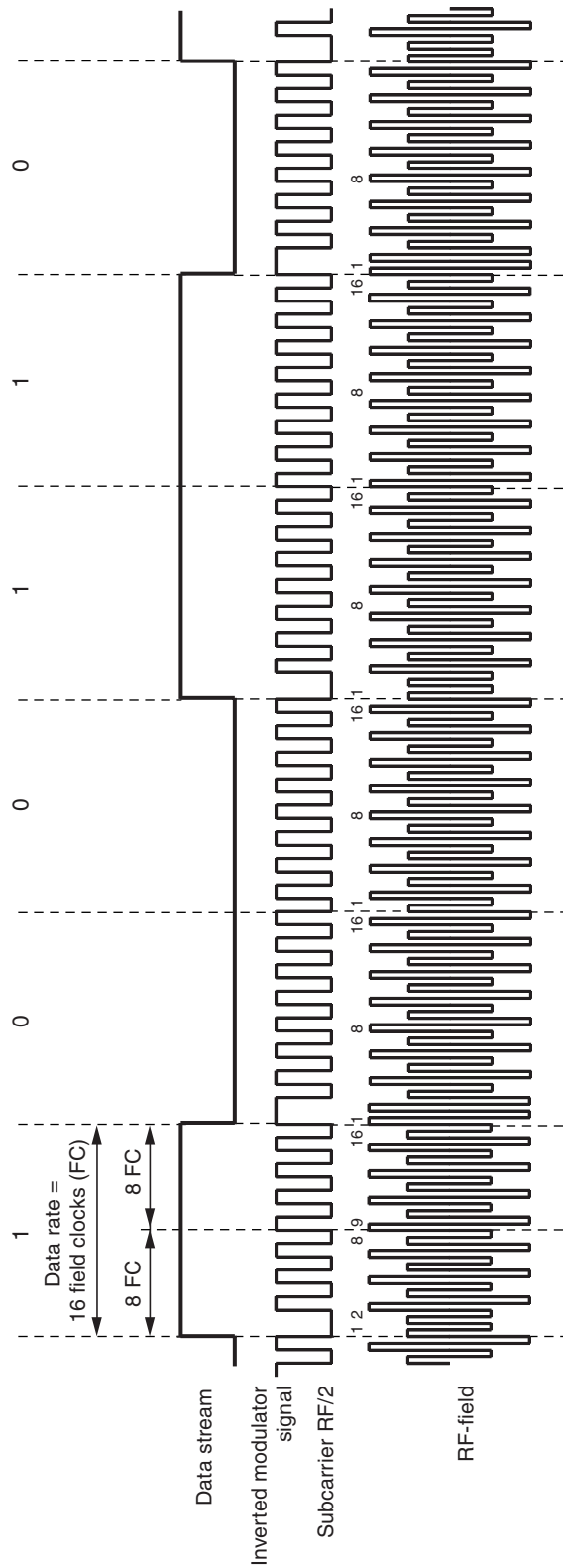
Figure 6-8. Example of PSK2 Coding with Data Rate RF/16

4874F–RFID–07/08
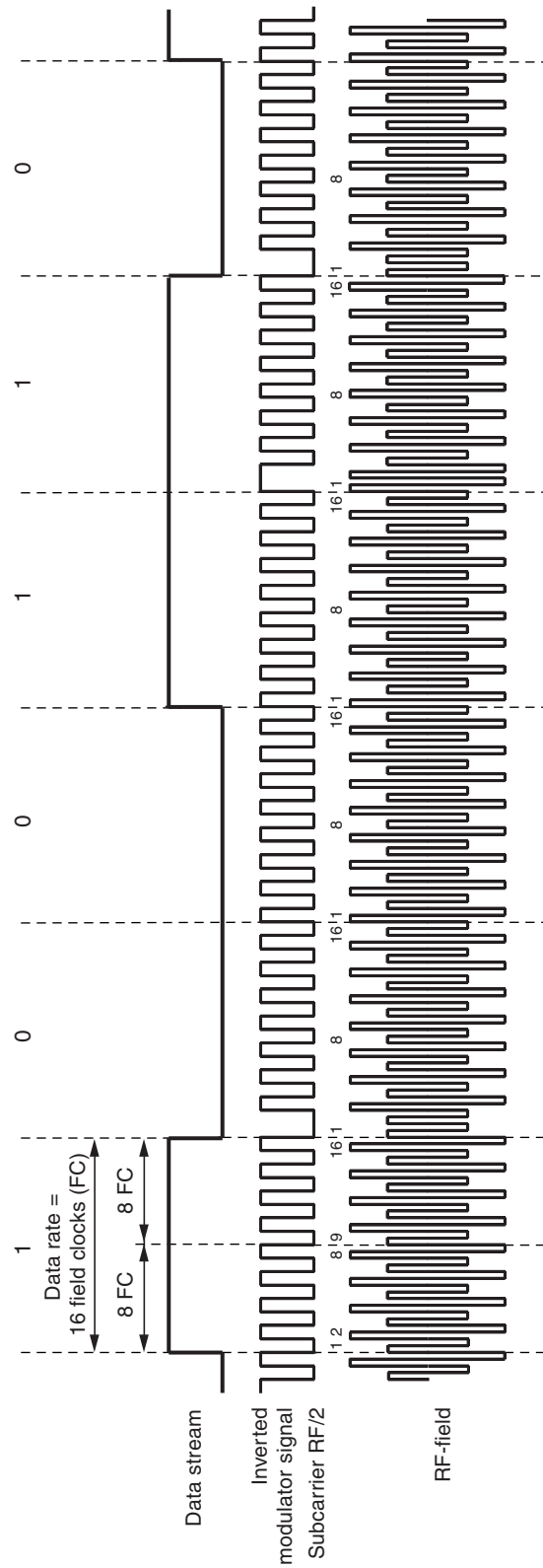
Figure 6-9. Example of PSK3 Coding with Data Rate RF/16
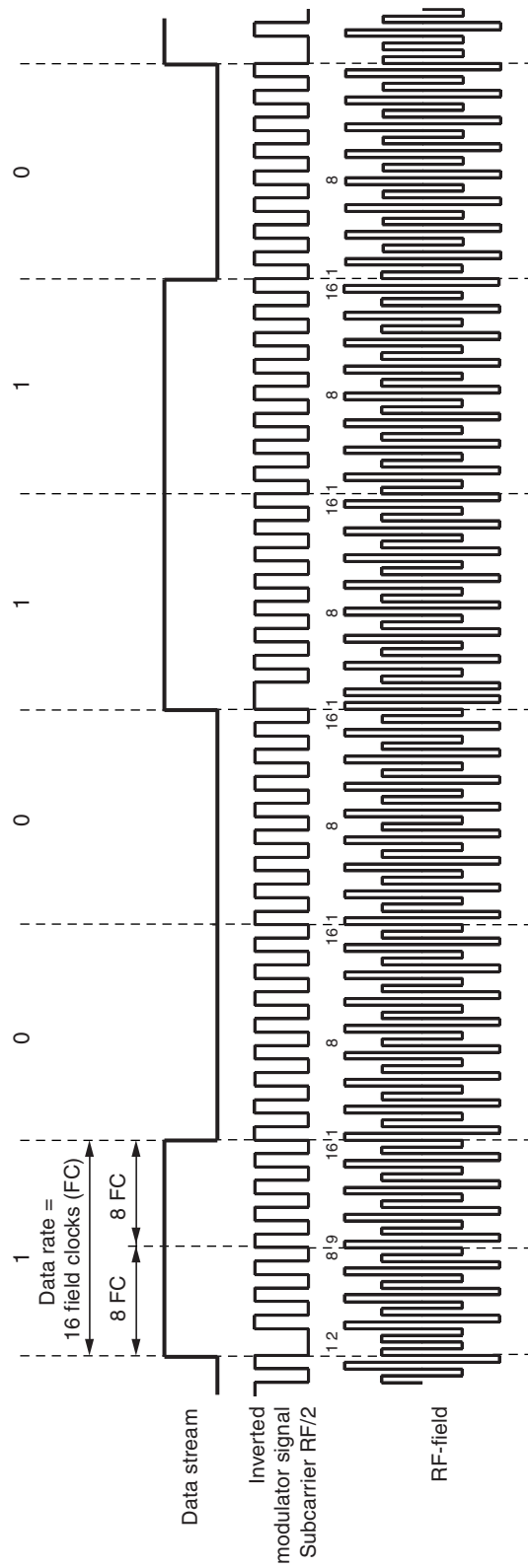
7. Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Value	Unit
Maximum DC current into Coil 1/Coil 2	I_{coil}	20	mA
Maximum AC current into Coil 1/Coil 2 f = 125 kHz	$I_{coil\ p}$	20	mA
Power dissipation (die) (free-air condition, time of application: 1s)	P_{tot}	100	mW
Electrostatic discharge maximum to MIL-Standard 883 C method 3015	V_{max}	4000	V
Operating ambient temperature range	T_{amb}	−40 to +85	°C
Storage temperature range (data retention reduced)	T_{stg}	−40 to +150	°C

8. Electrical Characteristics

T_{amb} = +25°C; f_{coil} = 125 kHz; unless otherwise specified

No.	Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit	Type*
1	RF frequency range		f_{RF}	100	125	150	kHz	
2.1	Supply current (without current consumed by the external LC tank circuit)	T_{amb} = 25°C[1] (see Figure 6-9 on page 24)	I_{DD}		1.5	3	µA	T
2.2		Read – full temperature range			2	4	µA	Q
2.3		Programming – full temperature range			25	40	µA	Q
3.1	Coil voltage (AC supply)	POR threshold (50 mV hysteresis)	$V_{coil\ pp}$	3.2	3.6	4.0	V	Q
3.2		Read mode and write command[2]		6		V_{clamp}	V	Q
3.3		Program EEPROM[2]		8		V_{clamp}	V	Q
4.1	Start-up time	$V_{coil\ pp}$ = 6V	$t_{startup}$		2.5	3	ms	Q
4.2	Start-up voltage ramp	$V_{coil\ pp}$ = 0 to 6V	t_{max}			1	s	Q
5	Clamp voltage	10 mA current into Coil 1/Coil 2	V_{clamp}	17		23	V	T

*) Type means: T: directly or indirectly tested during production; Q: guaranteed based on initial product qualification data

Notes: 1. I_{DD} measurement setup R = 100 kΩ; V_{CLK} = V_{coil} = 5V: EEPROM programmed to 00 ... 000 (erase all); chip in modulation defeat. I_{DD} = (V_{OUTmax} − V_{CLK}) / R

2. Current into Coil 1/Coil 2 is limited to 10 mA. The damping circuitry has the same structure as the e5550. The damping characteristics are defined by the internally limited supply voltage (= minimum AC coil voltage)

3. V_{mod} measurement setup: R = 2.3 kΩ; V_{CLK} = 3V; setup with modulation enabled (see Figure 8-1 on page 26).

4. Since EEPROM performance is influenced by assembly processes, Atmel confirms the parameters for DOW (tested die on uncut wafer) delivery.

5. The tolerance of the on-chip resonance capacitor C_r is ±10% at 3σ over whole production. The capacitor tolerance is ±3% at 3σ on a wafer basis.

6. The tolerance of the micromodule resonance capacitor C_r is ±5% at 3σ over whole production.

8. Electrical Characteristics (Continued)

T_{amb} = +25°C; f_{coil} = 125 kHz; unless otherwise specified

No.	Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit	Type*
6.1	Modulation parameters	V_{coilpp} = 6V on test circuit generator and modulation ON[3]	$V_{mod\,pp}$		4.2	4.8	V	T
6.2			$I_{mod\,pp}$	400	600		µA	T
6.3		Thermal stability	V_{mod}/T_{amb}		–6		mV/°C	Q
7	Programming time	From last command gap to re-enter read mode (64 + 648 internal clocks)	T_{prog}	5	5.7	6	ms	T
8	Endurance	Erase all/Write all[4]	n_{cycle}	100,000			Cycles	Q
9.1	Data retention	Top = 55°C[4]	$t_{retention}$	10	20	50	Years	
9.2		Top = 150°C[4]	$t_{retention}$	96			hrs	T
9.3		Top = 250°C[4]	$t_{retention}$	24			hrs	Q
10	Resonance capacitor	Mask option[5]	C_r	70	78	86	pF	T
11.1	Micromodule capacitor parameters	Capacitance tolerance T_{amb}	C_r	313.5	330	346.5	pF	T
11.2		Temperature coefficient	TBD	TBD	TBD	TBD	TBD	TBD
11.3			TBD	TBD	TBD	TBD	TBD	TBD

*) Type means: T: directly or indirectly tested during production; Q: guaranteed based on initial product qualification data

Notes:
1. I_{DD} measurement setup R = 100 kΩ, V_{CLK} = V_{coil} = 5V: EEPROM programmed to 00 ... 000 (erase all); chip in modulation defeat. I_{DD} = (V_{OUTmax} – V_{CLK}) / R
2. Current into Coil 1/Coil 2 is limited to 10 mA. The damping circuitry has the same structure as the e5550. The damping characteristics are defined by the internally limited supply voltage (= minimum AC coil voltage)
3. V_{mod} measurement setup: R = 2.3 kΩ, V_{CLK} = 3V; setup with modulation enabled (see).
4. Since EEPROM performance is influenced by assembly processes, Atmel confirms the parameters for DOW (tested die on uncut wafer) delivery.
5. The tolerance of the on-chip resonance capacitor C_r is ±10% at 3σ over whole production. The capacitor tolerance is ±3% at 3σ on a wafer basis.
6. The tolerance of the micromodule resonance capacitor C_r is ±5% at 3σ over whole production.

Figure 8-1. Measurement Setup for I_{DD} and V_{mod}
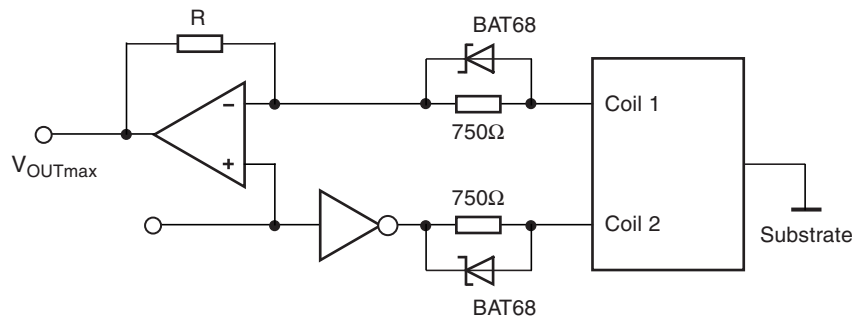
9. Ordering Information[1]

ATA5567	a b	- x x x	Package		Drawing
		- DDW	- Die on wafer, 6" unsawn wafer, thickness 300 µm (on request)		
		- DDT 1	- Die in tray (waffle pack), thickness 300 µm		
		- DDB	- Die on foil, 6" sawn wafer with ring, thickness 150 µm		Figure 10-3 on page 30
		11N	- 2 pads without on-chip capacitor		Figure 10-1 on page 28
		14N	- 4 pads with on-chip 75 pF capacitor		Figure 10-2 on page 29
		01N	- 2 pads without capacitor, damping during initialization		Figure 10-1 on page 28

Note: 1. For available order codes, contact your local Atmel Sales/Marketing office.

ATA556711	- x x x	Package	Drawing
	- TASY	- SO8 package (lead-free)	Figure 10-7 on page 34

ATA556715	- x x x	Package	Drawing
	- PAE	- NOA3 micromodule (lead-free)	Figure 10-5 on page 32 and Figure 10-6 on page 33

9.1   Ordering Examples

ATA556714N-DDB   Tested die on sawn 6" wafer on foil with ring, thickness 150 µm, 75 pF on-chip capacitor, no damping during POR initialization; especially for ISO 11784/785 and access control applications

9.2   Available Order Codes

ATA556711N-DDT 1
ATA556711N-DDB
ATA556714N-DDB
ATA556715-PAE
ATA556711-TASY

New order codes will be created by customer request if order quantities are over 250k pieces.

10. Package Information

Figure 10-1. 2-pad Layout

Dimensions in µm
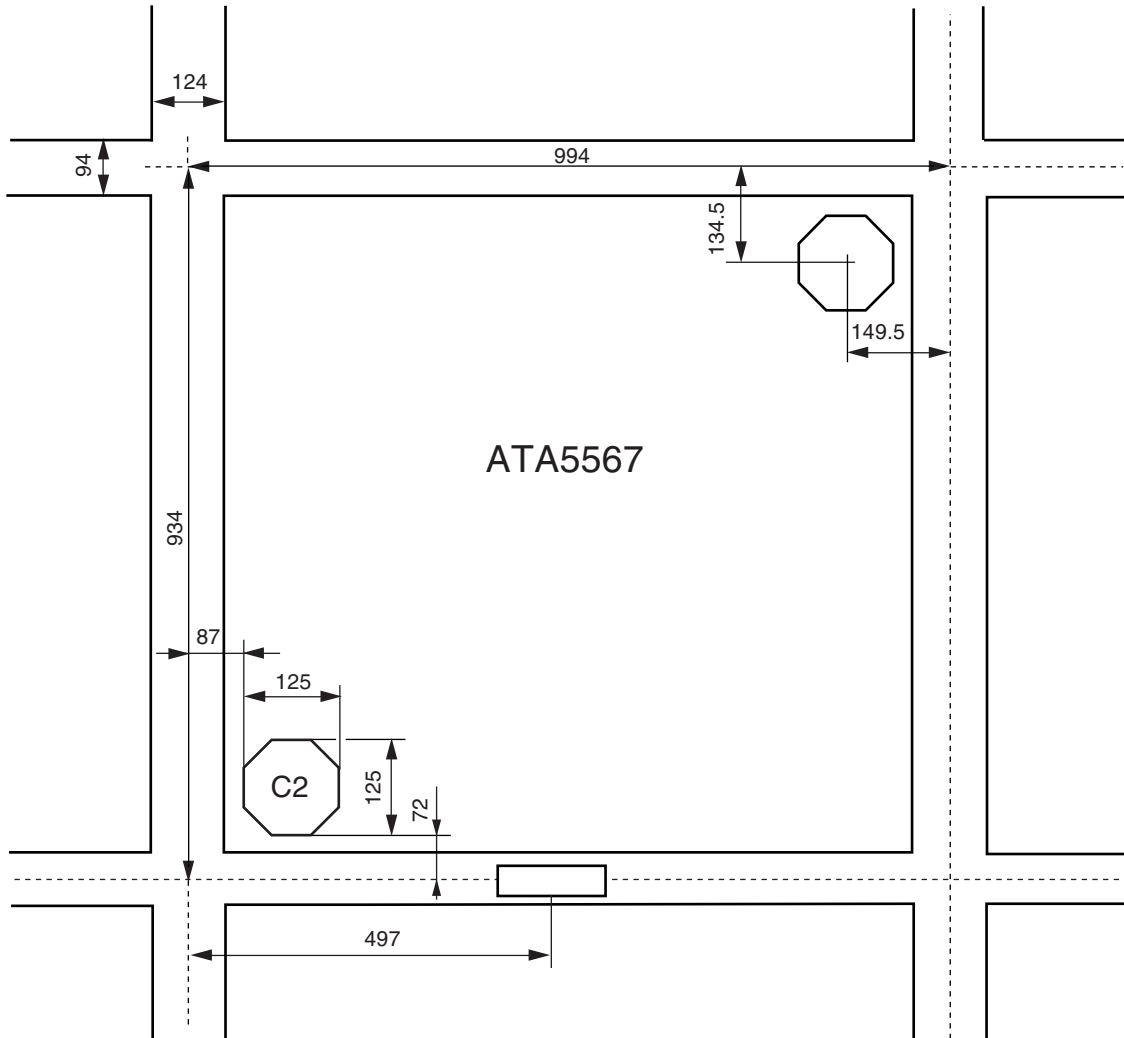
Figure 10-2. 4-pad Layout

Dimensions in µm
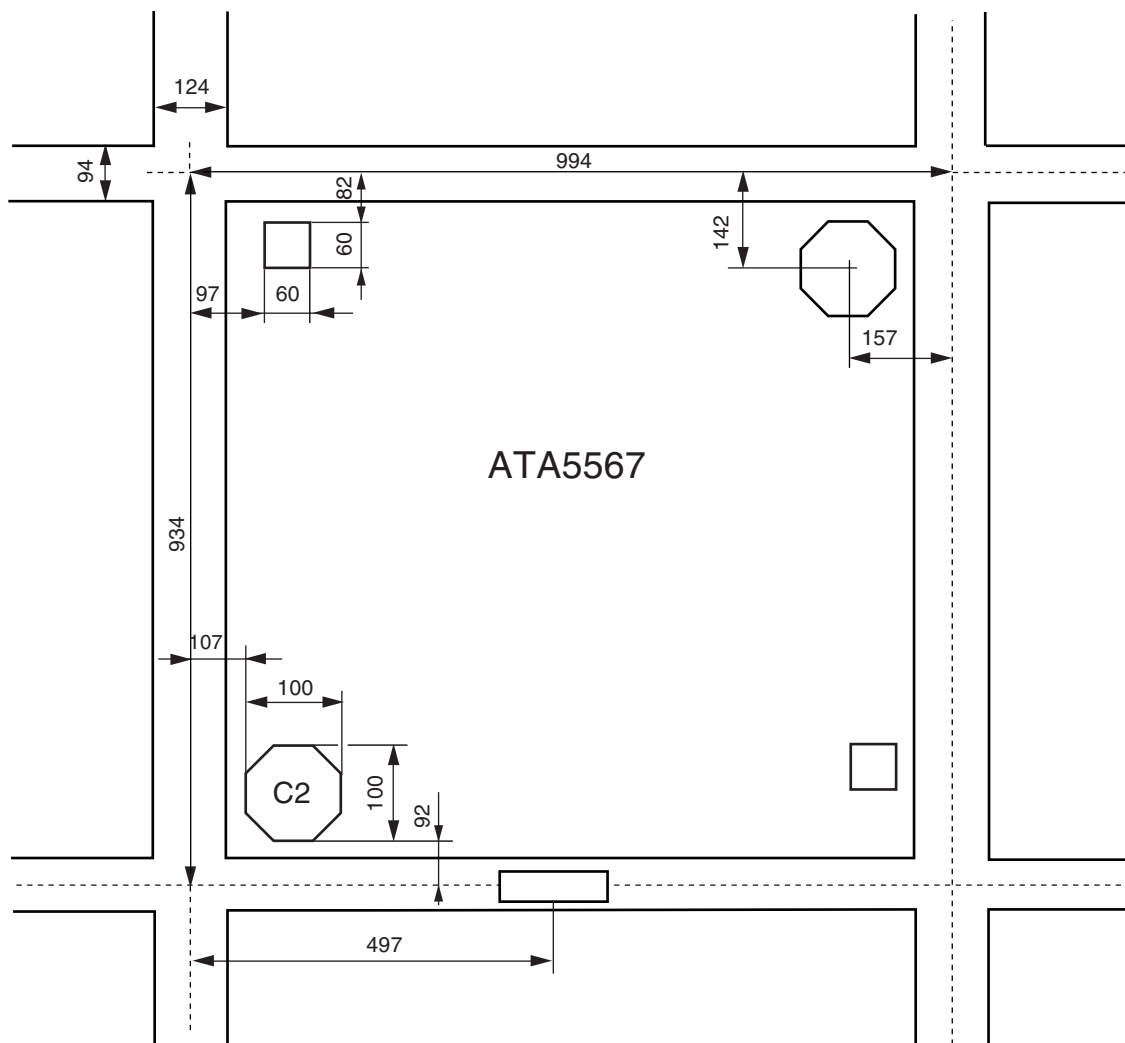
Figure 10-3. 6" Sawn Wafer with Ring, Thickness 150 µm
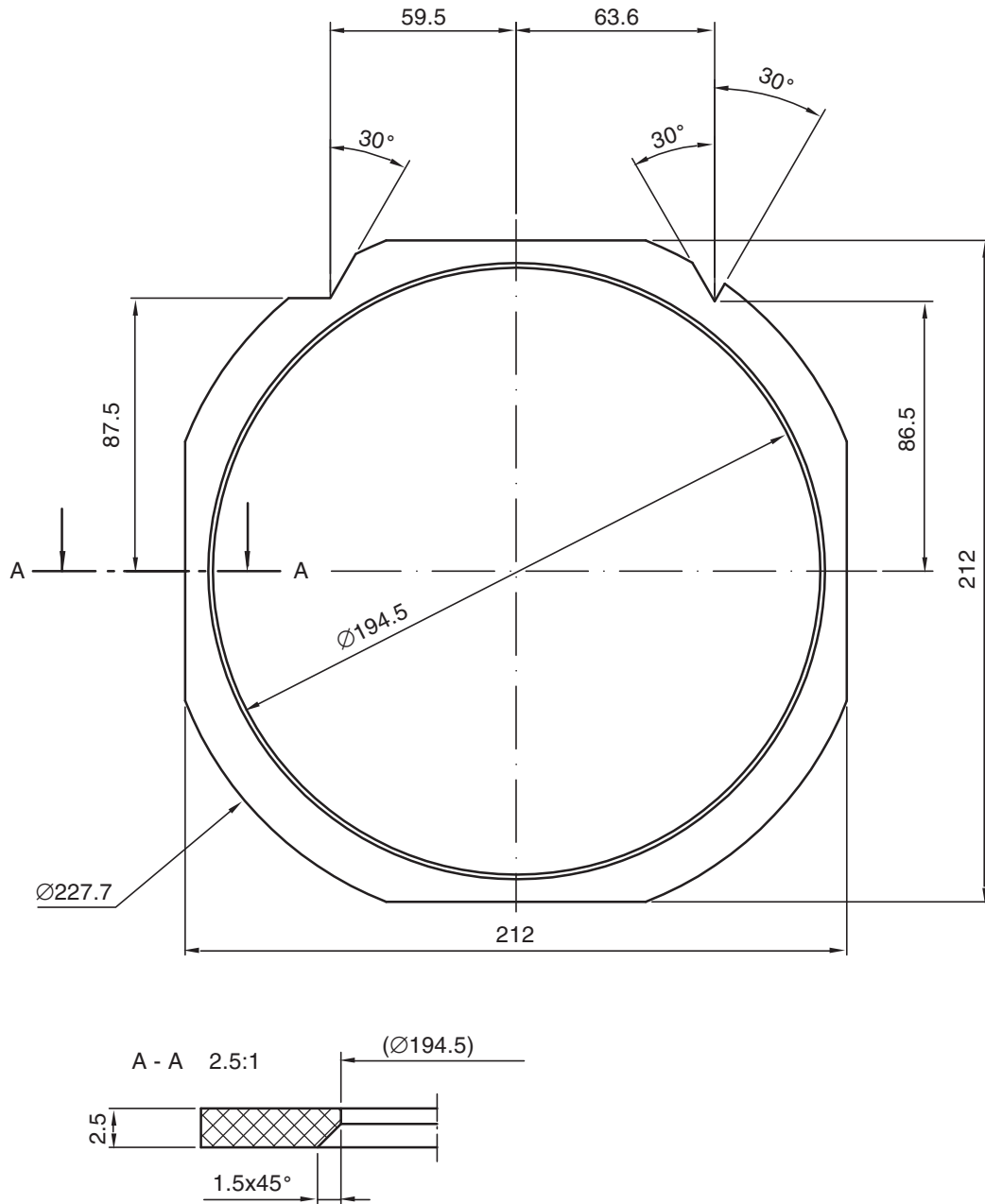
Figure 10-4. Wafer Map

Flat Edge
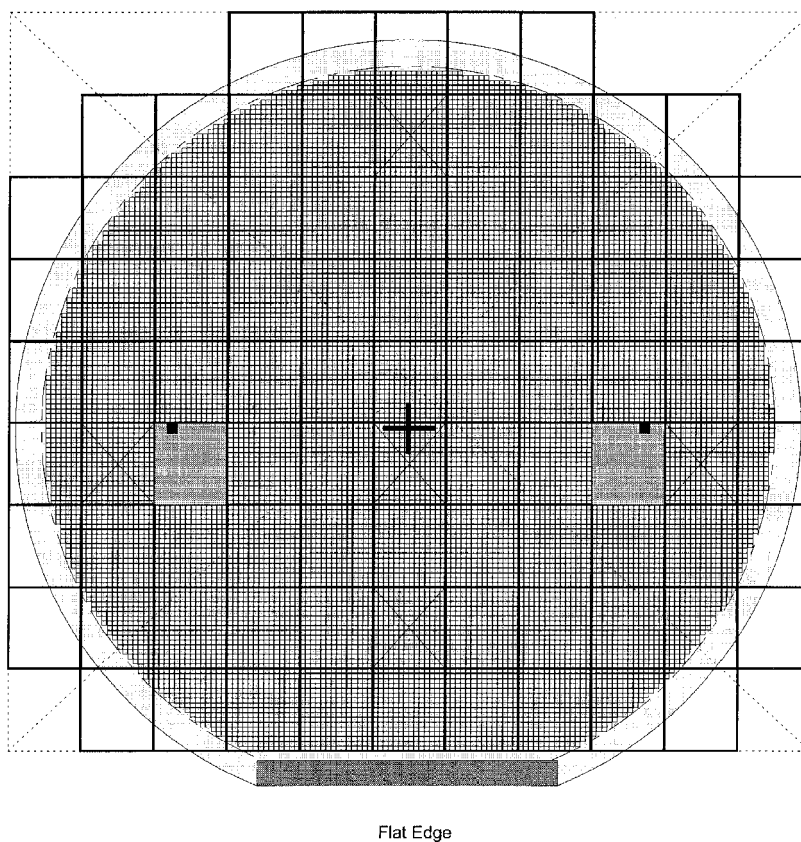
Die: 0.894 × 0.864, Step: 0.994 × 0.934, N: 14 × 7, Frame Step: 13.916 × 15.878
> Shift-ASML = [0.3; –6.9]: 15539 dice, 87 shots (11 columns × 9 rows)
> Shift-CANON/ALARM/SEM = [0.3; –6.9] – W2 = [–13.152; 6.9] – W1 = [–6.648; 6.9]

10.1 Failed Die Identification

Every die on the wafer not passing Atmel's test sequence is marked with ink.
The ink dot specification:

- Dot size: 200 μm
- Position: center of die
- Color: black

Figure 10-5. NOA3 Micromodule

technical drawings
according to DIN
specifications

Dimensions in mm

X

X5:1

Note:
1. Reject hole by testing device
2. Punching cutline
   recommendation for singulation
3. Total package thickness
   exclusive punching burr
4. Module dimension
   after electrical disconnection

Drawing-No.: 6.549-5035.01-4

Issue: 1; 28.04.06

Subcontractor: NedCard

Drawing refers to following types: Micromodule NOA-3

Figure 10-6. Shipping Reel
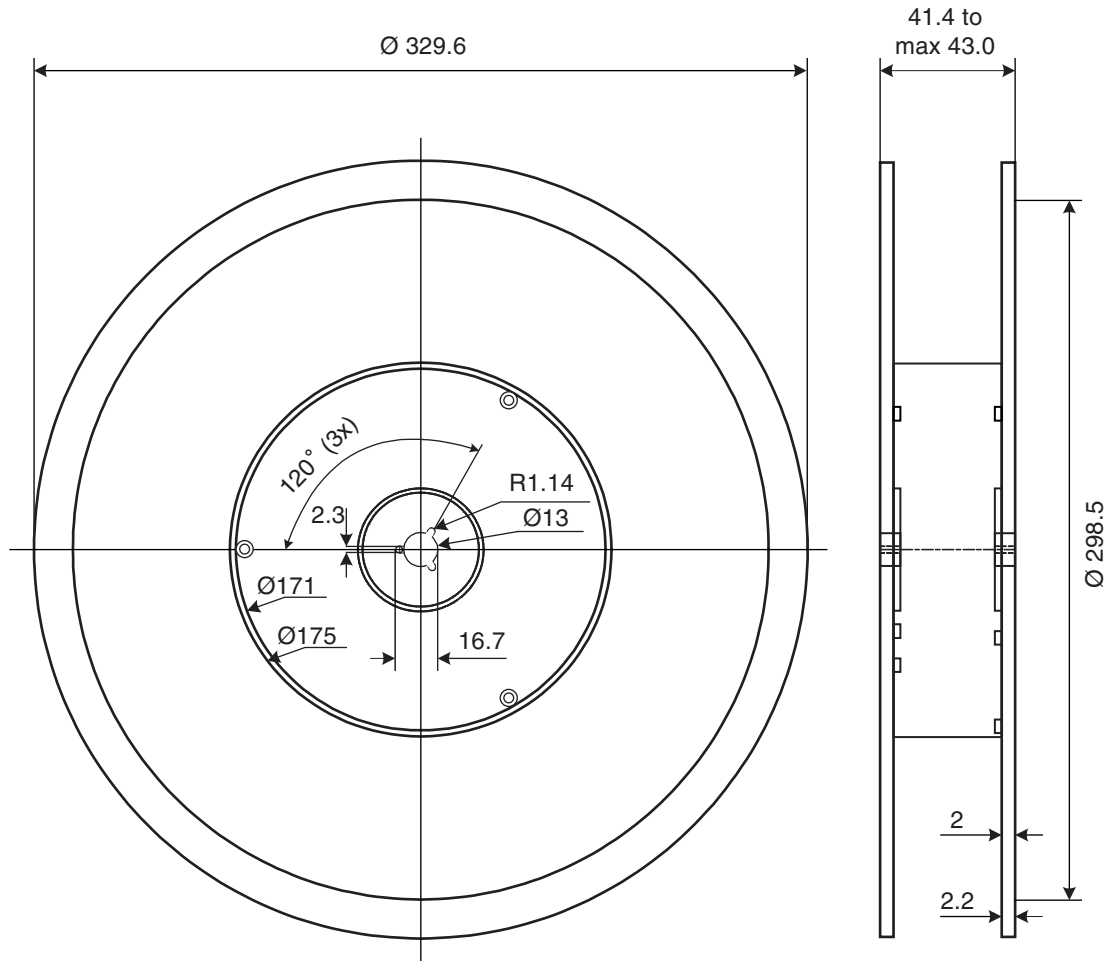
Figure 10-7. SO8 Package

Package: SO 8

Dimensions in mm
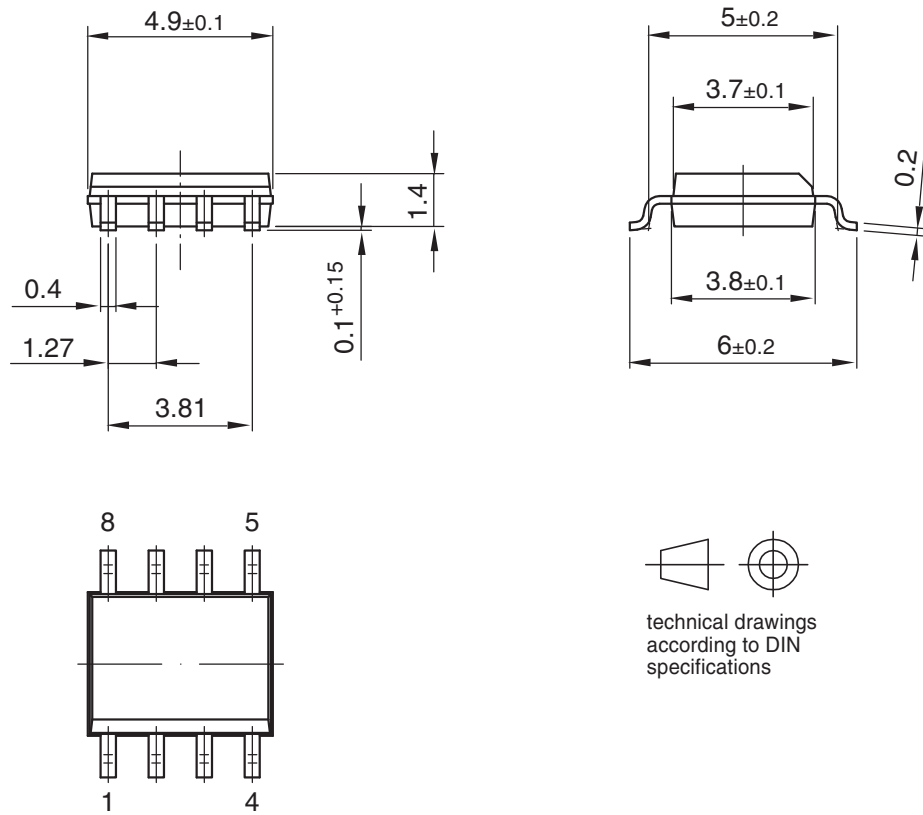
Drawing-No.: 6.541-5031.01-4

Issue: 1; 15.08.06

Figure 10-8. Pinning SO8

COIL2	1	8	COIL1
NC	2	7	NC
NC	3	6	NC
NC	4	5	NC
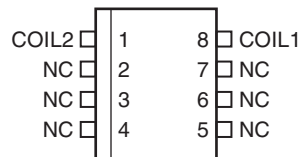
11. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4874F-RFID-07/08	• Section 3.12 "Traceability Data Structure" on page 5 changed • Section 6 "ATA5567 in Extended Mode (X-mode) on page 15 changed • Section 9 "Ordering Information" on page 27 changed
4874E-RFID-10/07	• Put datasheet in a new template • Section 9 "Ordering Information" on page 27 changed • Old Figure 10-3 "Solder Bump on NiAu" replaced with new Figure 10-3 "6" Sawn Wafer with Ring, Thickness 150 µm"

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054
Saint-Quentin-en-Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
rfid@atmel.com

Sales Contact
www.atmel.com/contacts

Literature Requests
www.atmel.com/literature