M66591GP

ASSP (USB2.0 Peripheral Controller)

REJ03F0101-0100Z
Rev.1.00
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1 Overview

1.1 Overview

The M66591 is a general-purpose USB (Universal Serial Bus) device controller compliant with the Universal Serial Bus Specification Revision 2.0 and supports both Hi-Speed and Full-Speed transfer.

The USB Hi-Speed and Full-Speed transceiver are built-in, and the M66591 meets control, bulk and interrupt transfer types which are defined in the Universal Serial Bus Specification Revision 2.0.

The M66591 has a 3.5K byte FIFO and 7 endpoints (maximum) for data transfer.

Further, being equipped with the split bus (DMA interface) which is independent from the CPU bus interface, the M66591 is suitable for use in systems that require large capacity data transfer at Hi-Speed.

1.2 Features

- Universal Serial Bus Specification Revision 2.0 compliant
- Built-in USB transceiver
- Supports both Hi-Speed (480M bps) and Full-Speed (12M bps)
- USB protocol layer by hardware
  - Bit stuffing encoding and decoding
  - CRC (Cyclic Redundancy Check) generation and checking
  - NRZI (Non Return Zero Invert) encoding and decoding
  - Packet detection
  - USB address checking
- Hi-Speed and Full-Speed detection by hardware
- Supports the following USB transfer types
  - Control transfer (PIPE0)
  - Bulk transfer (PIPE1~PIPE4)
  - Interrupt transfer (PIPE5~PIPE6)
- Built-in FIFO buffer (3.5K bytes) for endpoints
- Up to 7 endpoints selectable
- Data transfer condition selectable for each PIPE
  - Hi-Speed
    - PIPE0: Control transfer, continuous transfer mode, 256-byte FIFO
    - PIPE1~2: Bulk in or bulk out transfer, 512-byte FIFO, double buffer
    - PIPE3~4: Bulk in or bulk out transfer, 512-byte FIFO, single buffer
    - PIPE5~6: Interrupt in transfer, 64-byte FIFO, single buffer
  - Full-Speed
    - PIPE0: Control transfer, continuous transfer mode, 256-byte FIFO
    - PIPE1~2: Bulk in or bulk out transfer, continuous transfer mode, 512-byte FIFO, double buffer
    - PIPE3~4: Bulk in or bulk out transfer, continuous transfer mode, 512-byte FIFO, single buffer
    - PIPE5~6: Interrupt in transfer, 64-byte FIFO, single buffer
- Automatic response for Set Address request
- Supports the following input frequency
  - 12 / 24 / 48MHz
- Supports 16-bit CPU I/F and 8/16-bit DMA transfer
- Supports separate/multiplex bus
  - 16-bit separate/multiplex bus
- Supports 8-bit split bus (DMA interface)
- USB status output for power management
- 1.8V/3.3V interface power supply
- Application
  - Digital camera, printer, external storage device and all Hi-Speed USB PC peripheral device

1.3 Pin Configuration

The pin configuration (top view) of the M66591 is shown in Figure 1.1.

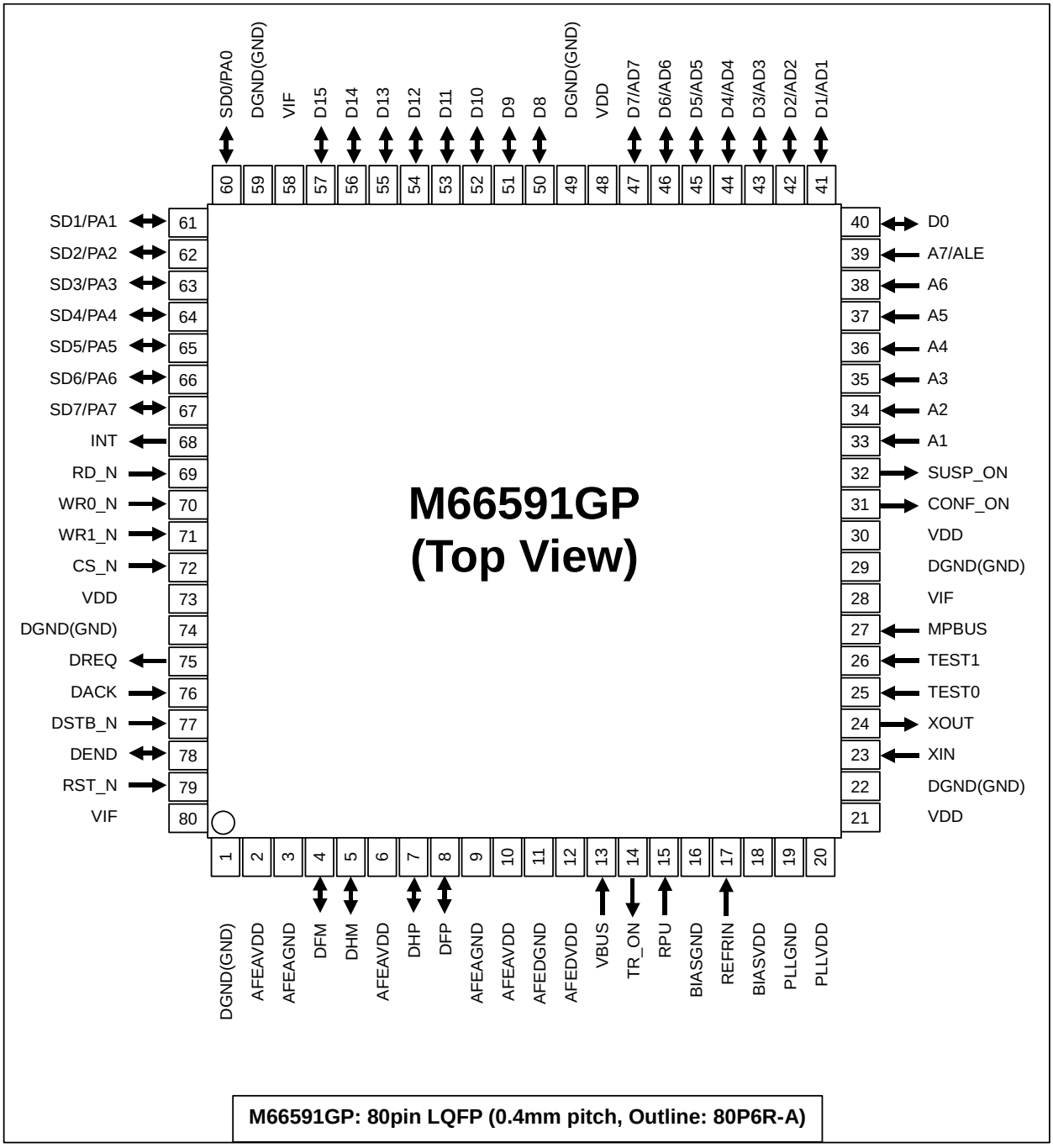


Figure 1.1 Pin Configuration of M66591

The pin functions of the M66591 are shown in Table 1.1.

Table 1.1 Pin Functions of M66591

Item	Pin Name	Input/Output	Name / Function	Pin Count
CPU interface	D15-D8	Input/Output	**Data Bus** These are data bus to access the registers from the CPU.	8
	D7/AD7-D1/AD1, D0	Input/Output	**Data Bus / Address Bus** When select to 16-bit separate bus, these pins are used as D7-D0 of data bus. When select to 16-bit multiplex bus, D7-D0 input/output and AD7-AD1 input are performed at time-sharing. In this case, AD0 is not used.	8
	A7/ALE, A6-A1	Input	**Address Bus / Address Latch Enable** When select to 16-bit separate bus, these pins are address bus to access the registers from the CPU. When select to 16-bit multiplex bus, A7 becomes the ALE pin, latching addresses at the falling edge. A6-A1 are not used.	7
	CS_N	Input	**Chip Select** When this pin is low level, M66591 is selected.	1
	RD_N	Input	**Read Strobe** Data are read from registers at low level.	1
	WR1_N	Input	**D15-D8 Byte Write Strobe** The data (D15-D8) are written to the registers at the rising edge.	1
	WR0_N	Input	**D7-0 Byte Write Strobe** The data (D7-D0) are written to the registers at the rising edge.	1
	MPBUS	Input	**Bus Mode Select** The 16-bit separate bus is selected at low level. The 16-bit multiplex bus is selected at high level. This pin should not be switched after H/W reset.	1
Interrupt interface	INT	Output	**Interrupt** Interrupts are requested to the CPU. Polarity of this pin can be selected by register setting.	1
DMA interface	SD7/PA7-SD0/PA0	Input/Output	**Split Bus / General-purpose Port** These pins are used to select either split bus (DMA Interface) or general-purpose port (GPIO).	8
	DREQ	Output	**DMA Request** This pin is used to request DMA transfer of the D0_FIFO port. Polarity of this pin can be selected by register setting.	1
	DACK	Input	**DMA Acknowledge** DMA transfer of the D0_FIFO port is enabled in either low or high level. Polarity of this pin can be selected by register setting.	1
	DSTB_N	Input	**Split Bus Strobe** This pin is used as data strobe signal when the D0_FIFO port has been set to the split bus (DMA Interface). When the RWstb bit of the Data Pin & FIFO/DMA Control Pin Configuration Register 2 is set to “1” (RD/WR strobe mode), this pin is used as data strobe signal.	1
	DEND	Input/Output	**Transfer Terminal** When the PIPE direction is “IN”, this pin receives transfer complete signal as an input signal from any other peripheral chip or the CPU. When the PIPE direction is “OUT”, this pin indicates the last data transferred as the output signal. Polarity of this pin can be set by a register.	1
USB interface	DHP	Input/Output	**USB Hi-Speed Data** Connect the D+ signal of USB bus.	1
	DHM	Input/Output	**USB Hi-Speed Data** Connect the D- signal of USB bus.	1
	DFP	Input/Output	**USB Full-Speed Data** Connect this pin to DHP via a 43Ω 1% resistance.	1
	DFM	Input/Output	**USB Full-Speed Data** Connect this pin to DHM via a 43Ω 1% resistance.	1

Item	Pin Name	Input/Output	Name / Function	Pin Count
	RPU	Input	**Pull-up Control** Connect this pin to TR_ON pin via a 1.5KΩ 5% resistance.	1
	TR_ON	Output	**Pull-up Power Supply Output** 3.3V power supply output for pull-up. This supply internally converts VBUS input from 5V to 3.3V and outputs it.	1
	VBUS	Input	**VBUS Input** Connect to the Vbus of USB bus. Connection or shutdown of the Vbus can be detected.	1
	REFRIN	Input	**Reference Input** Connect this pin to BIASGND via a 1.2KΩ 1% resistance.	1
USB status output	CONF_ON	Output	**USB Configured Output** This pin is used to indicate the transition to configured state. This pin is N-ch open drain output.	1
	SUSP_ON	Output	**USB Suspend Output** This pin is used to indicate the transition to suspend state. This pin is N-ch open drain output.	1
Clock	XIN	Input	**Oscillator Input** These pins are used to input/output the signals of internal clock oscillation circuits. Connect a crystal unit between Xin and Xout pins.	1
	XOUT	Output	**Oscillator Output** If an external clock signal is used, input it to the Xin pin. Leave Xout open.	1
System control	RST_N	Input	**Reset** This pin is used to initialize the values of the internal register or the counter at low level.	1
	TEST1-0	Input	**Test** These pins are input for the test. Fix to low level or keep open.	2
Power supply	AFEAVDD	Input	**Analog Power Supply** Connect to the 3.3V power supply.	3
	AFEAGND	Input	**Analog Ground**	2
	AFEDVDD	Input	**USB Transceiver Digital Power Supply** Connect to the 3.3V power supply.	1
	AFEDGND	Input	**USB Transceiver Digital Power Ground**	1
	BIASVDD	Input	**BIAS Power Supply** Connect to the 3.3V power supply.	1
	BIASGND	Input	**BIASGND**	1
	PLLVDD	Input	**PLL Power Supply** Connect to the 3.3V power supply.	1
	PLLGND	Input	**PLLGND**	1
	VDD	Input	**Core Power Supply** Connect to the 3.3V power supply.	4
	VIF	Input	**IO Power Supply** Connect to the 1.8V or 3.3V power supply.	3
	DGND	Input	**Digital Ground**	6

The care method of non-used pin of M66591are shown in Table 1.2.

Table 1.2 The care method of non-used pin of M66591

Item	Pin Name	Care Method
CPU interface	A6-A1	Open
DMA interface	SD7/PA7-SD0/PA0	Pull-up or pull-down or setting to output port
	DREQ	Open
	DACK, DEND	Pull-up or pull-down or connect to VIF
	DSTB_N	Pull-up or connect to VIF
System control	TEST1-0	Open or connect to GND
USB status output	CONF_ON, SUSP_ON	Open

1.4 Pin Functions

The pin functions of the M66591are shown in Figure 1.2.

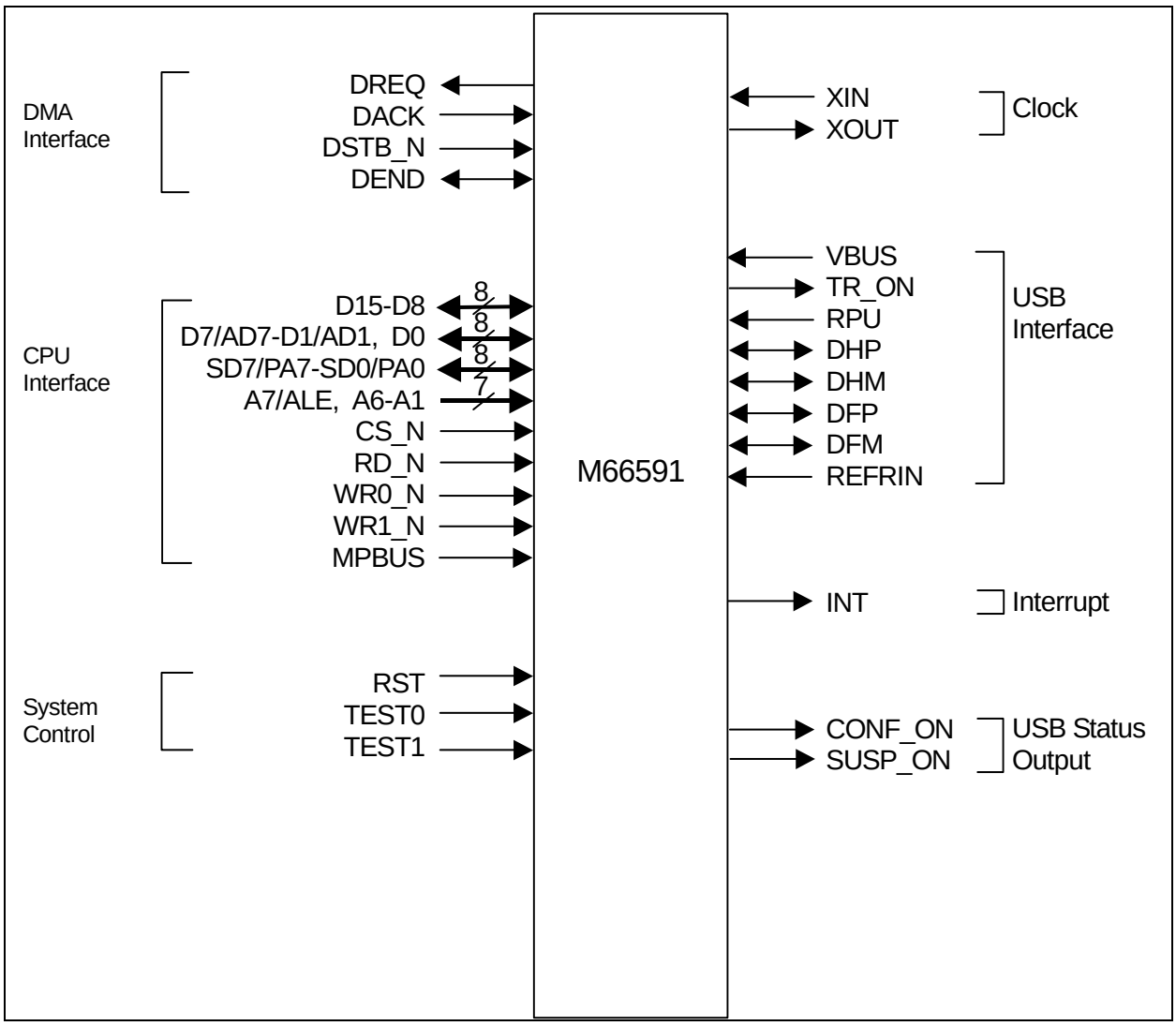


Figure 1.2 Pin Function Diagram of M66591

1.5 Block Diagram

M66591 contains four blocks, SIE (Serial Interface Engine) side block and CPU side block and bus interface unit (BIU) and FIFO memory. SIE side block includes USB transceiver (UTM), protocol engine (Prtcl_Eng), PIPE controller (PIPE_Ctrl), and interrupt controller (Int_Ctrl). CPU side block includes FIFO port (FIFO_Port), and register block (USB_Reg).

The block diagram of M66591 is shown in Figure 1.3.

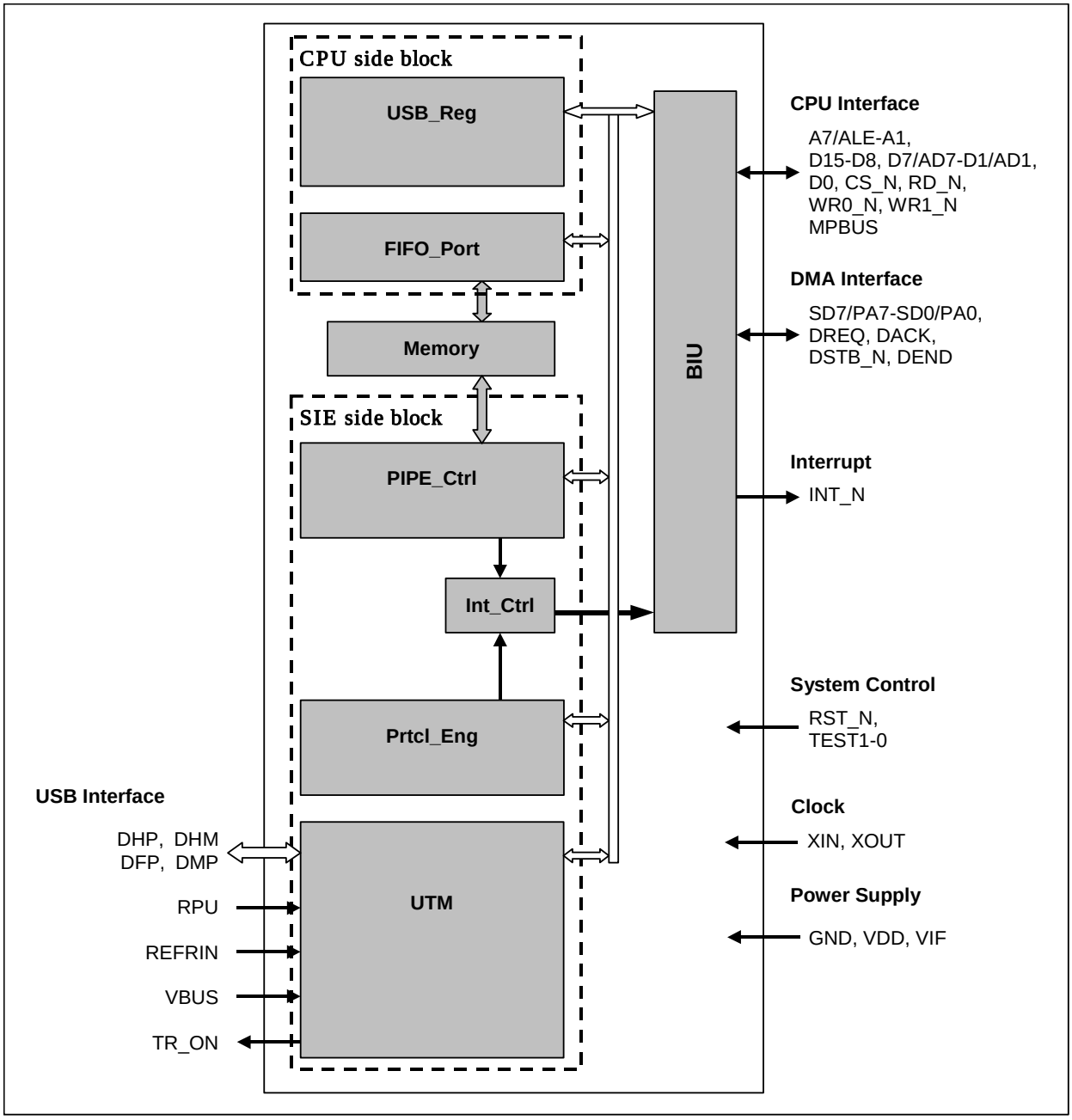


Figure 1.3 Block Diagram of M66591

2 Registers

How to Read Register Tables

① Bit Numbers: Each register is connected with an internal bus of 16-bit wide, so the bit numbers of the registers located at odd addresses are b15-b8, and those at even addresses are b7-b0.

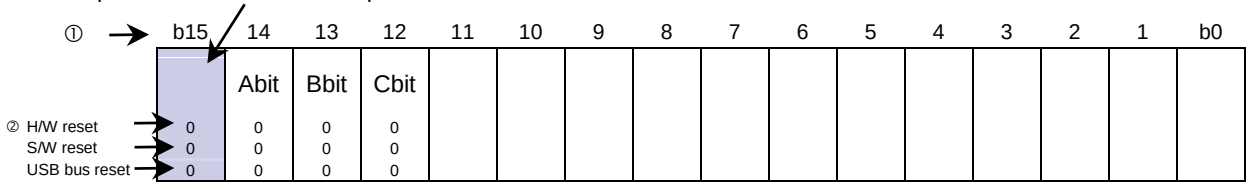
② State of Register at Reset:
Represents the initial state of each register immediately after reset with hexadecimal numbers. The “H/W reset” is the reset by an external reset signal; the “S/W reset” is the reset by the USBE bit of the USB Operation Enable Register.

③ At Read:
○ ... Read enabled
? ... Read disabled (Read value invalid)
0 ... Read always as 0
1 ... Read always as 1

④ At Write:
○ ... Write enabled
Δ ... Write enable conditionally (includes some conditions at write)
— ... Write disabled (Don’t care “0” and “1” at write)
X ··· Write disabled

<Example of representation>

Not implemented in the shaded portion.



②

<H/W reset: H’0000>

<S/W reset: ->

<USB bus reset: ->

b	Bit name	Function	R	W
15	Reserved.		0	-
14	A bit (----------)	0: ---------- 1: ----------	0	0
13	B bit (----------)	0: ---------- 1: ----------	0	0
12	C bit (----------)	0: ---------- 1: ----------	0	0
			③	④

2.1 Register Mapping

M66591 register mapping is shown in Figure 2.1, Figure 2.2 and Figure 2.3, each register is described below.

Address	+1 address b15 – b8	+0 address b7 – b0	Reset state H/W	Reset state S/W	Reset state USB bus
H'00	USB Transceiver Control Register 0		0000h	-	-
H'02	USB Transceiver Control Register 1		0000 0000 0100 00??b	---- ---- ---- --??b	---- ---- ---- --00b
H'04	HS/FS Mode Register		0000h	-000 0000 0000 0000b	-000 0000 0000 00--b
H'06	Test Mode Register		0000h	0000h	00-- ---- ---- ----b
H'08	Data Pin & FIFO/DMA Control Pin Configuration Register 0		00??h	-	-
H'0A	Data Pin & FIFO/DMA Control Pin Configuration Register 1		0000h	-	-
H'0C	Data Pin & FIFO/DMA Control Pin Configuration Register 2		0000h	-	-
H'0E					
H'10					
H'12					
H'14	C_FIFO Port Register 0		0000h	????h	-
H'16					
H'18	D0_FIFO Port Register 0		0000h	????h	-
H'1A					
H'1C					
H'1E					
H'20					
H'22					
H'24					
H'26	DCP Continuous Transmit Data Length Register		0000h	0000h	-
H'28	C_FIFO Port Control Register 0		0000h	0000h	-
H'2A					
H'2C	C_FIFO Port Control Register 1		0000h	0000h	-
H'2E	C_FIFO Port Control Register 2		0000h	0000h	-
H'30	D0_FIFO Port Control Register 0		0000h	0000h	-
H'32					
H'34	D0_FIFO Port Control Register 2		0000h	0000h	-
H'36	D0_FIFO Port Control Register 3		0000h	0000h	-
H'38					
H'3A					
H'3C					
H'3E					
H'40	INT Pin Configuration Register 0		0000h	0000h	-
H'42	INT Pin Configuration Register 1		0000h	-	-
H'44	INT Pin Configuration Register 2		0000h	0000h	-
H'46					

Note: Refer to each register described below.

Figure 2.1 Register Mapping (1)

Address	+1 address b15 – b8	+0 address b7 – b0	Reset state H/W	Reset state S/W	Reset state USB bus
H'48	INT Pin Configuration Register 3		0000h	0000h	-
H'4A					
H'4C	INT Pin Configuration Register 4		0000h	0000h	-
H'4E					
H'50					
H'52					
H'54					
H'56					
H'58					
H'5A					
H'5C					
H'5E					
H'60	Interrupt Status Register 0		0000 0000 ?000 0000b	0000 0000 ?000 0000b	---1 ---- -001 ----b
H'62					
H'64	Interrupt Status Register 1		0000h	0000h	-
H'66					
H'68	Interrupt Status Register 2		0000h	0000h	-
H'6A					
H'6C	Interrupt Status Register 3		0000h	0000h	-
H'6E					
H'70					
H'72					
H'74	USB Address Register		0000h	0000h	0000h
H'76					
H'78	USB Request Register 0		0000h	0000h	0000h
H'7A	USB Request Register 1		0000h	0000h	0000h
H'7C	USB Request Register 2		0000h	0000h	0000h
H'7E	USB Request Register 3		0000h	0000h	0000h
H'80					
H'82	DCP Configuration Register 1		0000h	0000h	-
H'84	DCP Configuration Register 2		0000h	0000h	-
H'86					
H'88	DCP Control Register		0000h	0000h	---- ---- ---- -000b
H'8A					
H'8C	PIPE Configuration Select Register		0000h	0000h	-
H'8E					
H'90	PIPE Configuration Window Register 0		0000h	0000h	00-- ---- ---- ----b
H'92					
H'94					
H'96					
H'98					

Note: Refer to each register described below.

Figure 2.2 Register Mapping (2)

Address	+1 address		+0 address		Reset state		
	b15	b8	b7	b0	H/W	S/W	USB bus
H'9A							
H'9C							
H'9E							
H'A0	PIPE1 Control Register				0000h	0000h	---- ---- ---- --00b
H'A2	PIPE2 Control Register				0000h	0000h	---- ---- ---- --00b
H'A4	PIPE3 Control Register				0000h	0000h	---- ---- ---- --00b
H'A6	PIPE4 Control Register				0000h	0000h	---- ---- ---- --00b
H'A8	PIPE5 Control Register				0000h	0000h	---- ---- ---- --00b
H'AA	PIPE6 Control Register				0000h	0000h	---- ---- ---- --00b

Note: Refer to each register described below.

Figure 2.3 Register Mapping (3)

2.2 Register Bit Map

	Odd number address (001h)								Even number address (000h)							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USB Transceiver Control Register 0 (USBTrnsCtrl0)																
0 0	XTAL [1:0]		XCKE	RCKE	PLLC	SCKE			HSE			RpuE				USBE
USB Transceiver Control Register 1 (USBTrnsCtrl1)																
0 2															LNST [1:0]	
HS/FS Mode Register (HSFSMode)																
0 4								WKUP							RHST [1:0]	
Test Mode Register (TestMd)																
0 6	SUSPEN	CONFEN												TST [2:0]		
Data Pin & FIFO/DMA Control Pin Configuration Register 0 (PinCtrlCfg0)																
0 8									PA [7:0]							
Data Pin & FIFO/DMA Control Pin Configuration Register 1 (PinCtrlCfg1)																
0 A	LDRV							big_end						PAdir		DB_Cfg
Data Pin & FIFO/DMA Control Pin Configuration Register 2 (PinCtrlCfg2)																
0 C		DreqA	Burst	DreqE		DackA	RWstb	DackE		DendA	Pktmd	DendE		Obus		
0 E																
1 0																
1 2																
C_FIFO Port Register 0 (C_FIFOPort0)																
1 4	C_FIFO_Port [15:0]															
1 6																
D0_FIFO Port Register 0 (D0_FIFOPort0)																
1 8	D0_FIFO_Port [15:0]															
1 A																
1 C																
1 E																
2 0																
2 2																
2 4																
DCP Continuous Transmit Data Length Register (DCPSdln)																
2 6								SDLN [8:0]								
C_FIFO Port Control Register 0 (C_FIFOPortCtrl0)																
2 8	RCNT	REW				MBW					ISEL			Current_PIPE [2:0]		
2 A																
C_FIFO Port Control Register 1 (C_FIFOPortCtrl1)																
2 C	BVAL	BCLR	FRDY				CPU_DTLN [9:0]									
C_FIFO Port Control Register 2 (C_FIFOPortCtrl2)																
2 E	TGL	SCLR	SBUSY													

	Odd number address (001h)								Even number address (000h)							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D0_FIFO Port Control Register 0 (D0_FIFOPortCtrl0)																
3 0	RCNT	REW	ABCR			MBW	TREnb	TRclr						Current_PIPE [2:0]		
3 2																
D0_FIFO Port Control Register 2 (D0_FIFOPortCtrl2)																
3 4	BVAL	BCLR	FRDY				DMA_DTLN [9:0]									
D0_FIFO Port Control Register 3 (D0_FIFOPortCtrl3)																
3 6	TRNCNT [15:0]															
3 8																
3 A																
3 C																
3 E																
INT Pin Configuration Register 0 (INTPinCfg0)																
4 0	VBSE	RSME		DVSE	CTRE	BEMPE	INTNE	INTRE	URST	SADR	SCFG	SUSP	WDST	RDST	CMPL	SERR
INT Pin Configuration Register 1 (INTPinCfg1)																
4 2															INTL	INTA
INT Pin Configuration Register 2 (INTPinCfg2)																
4 4										PIPEB_RE6	PIPEB_RE5	PIPEB_RE4	PIPEB_RE3	PIPEB_RE2	PIPEB_RE1	DCP_RE
4 6																
INT Pin Configuration Register 3 (INTPinCfg3)																
4 8										PIPEB_NRE6	PIPEB_NRE5	PIPEB_NRE4	PIPEB_NRE3	PIPEB_NRE2	PIPEB_NRE1	DCP_NRE
4 A																
INT Pin Configuration Register 4 (INTPinCfg4)																
4 C										PIPEB_EMPE6	PIPEB_EMPE5	PIPEB_EMPE4	PIPEB_EMPE3	PIPEB_EMPE2	PIPEB_EMPE1	DCP_EMPE
4 E																
5 0																
5 2																
5 4																
5 6																
5 8																
5 A																
5 C																
5 E																
Interrupt Status Register 0 (INTStatus0)																
6 0	VBUSINT	RESM		DVST	CTRT	BEMP	INTN	INTR	VBUSSTS	DVSQ [2:0]			VALID	CTSQ [2:0]		
6 2																
Interrupt Status Register 1 (INTStatus1)																
6 4										PIPEB_RDY6	PIPEB_RDY5	PIPEB_RDY4	PIPEB_RDY3	PIPEB_RDY2	PIPEB_RDY1	DCP_RDY
6 6																
Interrupt Status Register 2 (INTStatus2)																
6 8										PIPEB_NRDY6	PIPEB_NRDY5	PIPEB_NRDY4	PIPEB_NRDY3	PIPEB_NRDY2	PIPEB_NRDY1	DCP_NRDY
6 A																

	Odd number address (001h)								Even number address (000h)							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Interrupt Status Register 3 (INTStatus3)

6 C										PIPEB_EMP_OVR6	PIPEB_EMP_OVR5	PIPEB_EMP_OVR4	PIPEB_EMP_OVR3	PIPEB_EMP_OVR2	PIPEB_EMP_OVR1	DCP_EMP_OVR
6 E																
7 0																
7 2																

USB Address Register (USBAddress)

7 4										USB_Addr [6:0]						
7 6																

USB Request Register 0 (USBReq0)

7 8	bRequest [7:0]	bmRequestType [7:0]

USB Request Register 1 (USBReq1)

7 A	wValue [15:0]

USB Request Register 2 (USBReq2)

7 C	wIndex [15:0]

USB Request Register 3 (USBReq3)

7 E	wLength [15:0]
8 0	

DCP Configuration Register 1 (DCPCfg1)

8 2								CNTMD								

DCP Configuration Register 2 (DCPCfg2)

8 4										DCP_MXPS [6:0]						
8 6																

DCP Control Register (DCPCtrl)

8 8	BSTS							SQCLR				NYETMD		CCPL	PID [1:0]	
8 A																

PIPE Configuration Select Register (PipeCfgSel)

8 C														PIPE_SEL [2:0]		
8 E																

PIPE Configuration Window Register 0 (PipeCfgWin0)

9 0	PEN		ITMD			BFRE	DBLB	CNTMD				DIR		EP_NUM [2:0]		
9 2																
9 4																
9 6																
9 8																
9 A																
9 C																
9 E																

PIPE i Control Register (i=1~6) (PipeiCtrl(i=1-6))

A 0	BSTS						ACLR	SQCLR				NYETMD			PID [1:0]
A 2	BSTS						ACLR	SQCLR				NYETMD			PID [1:0]
A 4	BSTS						ACLR	SQCLR				NYETMD			PID [1:0]
A 6	BSTS						ACLR	SQCLR				NYETMD			PID [1:0]
A 8	BSTS						ACLR	SQCLR							PID [1:0]
A A	BSTS						ACLR	SQCLR							PID [1:0]

2.3 USB Transceiver Control Register 0

■ USB Transceiver Control Register 0 (USBTrnsCtrl0) <Address: H'00>

B15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
Xtal [1:0]		XCKE	RCKE	PLLC	SCKE			HSE			RpuE				USBE
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset: H'0000>
<S/W reset: ->
<USB bus reset: ->

b	Bit name	Function	R	W
15~14	Xtal [1:0] Clock Select	00: External clock frequency: 12MHz 01: External clock frequency: 24MHz 10: External clock frequency: 48MHz 11: Reserved	○	○
13	XCKE Oscillation Buffer Enable	0: Disable oscillation buffer 1: Enable oscillation buffer	○	○
12	RCKE Internal Reference Clock Supply Enable	0: Disable reference clock (RCK) supply 1: Enable reference clock (RCK) supply	○	○
11	PLLC PLL Operation Enable	0: Disable PLL 1: Enable PLL	○	○
10	SCKE USB Clock Supply Enable	0: Disable internal clock supply 1: Enable internal clock supply	○	○
9~8	Reserved. Set it to "0".		"0"	"0"
7	HSE Hi-Speed Enable	0: Disable Hi-Speed mode 1: Enable Hi-Speed mode	○	○
6~5	Reserved. Set it to "0".		"0"	"0"
4	RpuE Pull-up Control	0: Disable D+ pull-up 1: Enable D+ pull-up	○	○
3~1	Reserved. Set it to "0".		"0"	"0"
0	USBE USB Module Operation Enable	0: USB module reset state (S/W reset) 1: USB module operation enable (S/W reset state release)	○	○

(1) Xtal [1:0] (Clock Select) Bits (b15-b14)

These bits set the multiplication factor of the external clock into PLL.

(2) XCKE (Oscillation Buffer Enable) Bit (b13)

This bit sets enable/disable of the oscillation buffer.
This bit is set to "1" by H/W after resume from suspend state.

(3) RCKE (Internal Reference Clock Supply Enable) Bit (b12)

This bit sets enable/disable of the internal reference clock supply. Do not set this bit to "1" until the clock oscillation becomes stable.

(4) PLLC (PLL Operation Enable) Bit (b11)

This bit sets enable/disable of the PLL. Do not set this bit to "1" until the clock oscillation becomes stable.

(5) SCKE (USB Clock Supply Enable) Bit (b10)

This bit sets enable/disable of the internal clock supply. Do not set this bit to "1" until the PLL clock oscillation becomes stable.

(6) HSE (Hi-Speed Enable) Bit (b7)

This bit sets enable/disable of the Hi-Speed mode.
When the Hi-Speed mode is disabled, M66591 is used as the Full-Speed only device. When the Hi-Speed mode is enabled, M66591 is used either as the Hi-Speed or the Full-Speed device.

Note: It is necessary to set this bit before enabling internal clock.

(7) RpuE (Pull-up Control) Bit (b4)

This bit sets enable/disable of the D+ line pull-up.

(8) USBE (USB Module Operation Enable) Bit (b0)

This bit sets enable/reset state of the USB module operation.
While this bit is kept at “0”, the register initialized by the software reset cannot be accessed for write.

Note: As for the program sequence and clock oscillation waiting time for setting this register, refer to “3.1 System Control”.

2.4 USB Transceiver Control Register 1

■ USB Transceiver Control Register 1 (USBTrnsCtrl1) <Address: H'02>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
														LNST [1:0]	
0	0	0	0	0	0	0	0	0	1	0	0	0	0	?	?
-	-	-	-	-	-	-	-	-	-	-	-	-	-	?	?
-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0

<H/W reset: B'0000 0000 0100 00??>
<S/W reset: B'---- ---- ---- --??>
<USB bus reset: B'---- ---- ---- --00>

b	Bit name	Function	R	W
15~7	Reserved.		"?"	×
6	Reserved. Set it to "1".		"1"	×
5~2	Reserved.		"?"	×
1~0	LNST [1:0] Line Status	• Read USB bus state • Write Invalid (Ignored when written)	○	×

(1) LNST [1:0] (Line Status) Bits (b1-b0)

These bits indicate USB bus (D+/D-) status. The relationships between statuses of USB bus and these bits are shown in the table below:

LNST [1:0]		FS	HS	Chirp
0	0	SE0	Squelch	Squelch
0	1	J State	UnSquelch	Chirp J
1	0	K State	-	Chirp K
1	1	SE1	-	-

Explanation of Terms:

FS:	In operation in Full-Speed mode
HS:	In operation in Hi-Speed mode
Chirp:	In execution of reset handshake protocol in Hi-Speed mode enable state (HSE="1")
Squelch:	Squelch state (SE0 state or idle state)
Unsquelch:	Hi-Speed J state or Hi-Speed K state
Chirp J:	Chirp J state or Hi-Speed J state
Chirp K:	Chirp K state or Hi-Speed K state

2.5 HS/FS Mode Register

■ HS/FS Mode Register (HSFSMode) <Address: H'04>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
							WKUP							RHST [1:0]	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	0	0	0	0	0	0	0	0	0	0	0	0	0	-	-

<H/W reset: H'0000>
<S/W reset: B'-000 0000 0000 0000>
<USB bus reset: B'-000 0000 0000 00-->

b	Bit name	Function	R	W
15~9	Reserved. Set it to "0".		"0"	"0"
8	WKUP Remote Wakeup	• Read 0: Do not output the remote wakeup signal 1: Output the remote wakeup signal • Write 0: Invalid (Ignored when written) 1: Output the remote wakeup signal	○	○
7~2	Reserved. Set it to "0".		"0"	"0"
1~0	RHST [1:0] Reset Handshake Status	• Read Indicate the reset handshake status • Write Invalid	○	-

(1) WKUP (Remote Wakeup) Bit (b8)

When "1" is written to this bit, K state is output for 10ms before returning to bus idling state (Remote wakeup signal) and then this bit is cleared to "0" automatically.

The USB bus idle state of minimum 5ms needs to be retained until remote wake up signal is transmitted in the Universal Serial Bus Specification Revision 2.0. Therefore, even if "1" is written to this bit immediately after suspend state is detected, K state can be output after 2ms of waiting.

K state is not output even if "1" is written to this bit while it is not in suspend state.

Note: When a permission of remote wakeup has not been issued from the host, do not set this bit to "1".

(2) RHST (Reset Handshake Status) Bits (b1-b0)

These bits indicate state of reset handshake protocol.

00: Reset detection wait state.
01: Reset handshake in process.
10: Reset handshake completed, Full-Speed mode.
11: Reset handshake completed, Hi-Speed mode.

2.6 Test Mode Register

■ Test Register (TestMd) <Address: H'06>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
SUSPEN	CONFEN												TST [2:0]		
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: ->

b	Bit name	Function	R	W
15	SUSPEN SUSP_ON Pin Output Enable	0: Disable SUSP_ON pin output 1: Enable SUSP_ON pin output	○	○
14	CONFEN CONF_ON Pin Output Enable	0: Disable CONF_ON pin output 1: Enable CONF_ON pin output	○	○
13~3	Reserved. Set it to "0".		"0"	"0"
2~0	TST [2:0] Test Mode Select	Set to test mode	○	○

(1) SUSPEN (SUSP_ON Pin Output Enable) Bit (b15)

This bit sets enable/disable of the SUSP_ON pin output.
0: Disable SUSP_ON pin output.
1: Enable SUSP_ON pin output. When the DVSQ [2:0] bits of the Interrupt Status Register 0 are set to "1XX", low level is output to the SUSP_ON pin.

(2) CONFEN (USB Configured Output Enable) Bit (b14)

This bit sets enable/disable of the CONF_ON pin output.
0: Disable CONF_ON pin output.
1: Enable CONF_ON pin output. When the DVSQ [2:0] bits of the Interrupt Status Register 0 are set to "X11", low level is output to the CONF_ON pin.

(3) TST (Test Mode Select) Bits (b2-b0)

These bits are used to select test mode. These bits are valid only in Hi-Speed mode. During operation in Full-Speed mode, set these bits to "000".
000: Standard operation mode
001: Test_J
010: Test_K
011: Test_SE0_NAK
100: Test_Packet
101-111: Reserved

2.7 Data Pin & FIFO/DMA Control Pin Configuration Register 0

■ Data Pin & FIFO/DMA Control Pin Configuration Register 0 (PinCtrlCfg0) <Address: H'08>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
								PA [7:0]							
0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset: H'00??>
<S/W reset: ->
<USB bus reset: ->

b	Bit name	Function	R	W
15~8	Reserved. Set it to "0".		"0"	"0"
7~0	PA [7:0] General port A	0: Low level 1: High level The port number corresponds to the bit number. b0: PA0 pin b1: PA1 pin b2: PA2 pin b3: PA3 pin b4: PA4 pin b5: PA5 pin b6: PA6 pin b7: PA7 pin	○	○

(1) PA [7:0] (General Port A) Bits (b7-b0)

When the DB_Cfg bit of the Data Pin & FIFO/DMA Control Pin Configuration Register 1 is set to "0" (GPIO), the SD7-SD0 pins are assigned to general purpose port PA [7:0].

Since general purpose port has a separate buffer for input and output, when the port is set to input, the read data is always the state of input pins even if any data is written to these bits.

The output buffer of general purpose port is undefined after H/W reset. It is necessary to write initial value before change direction to output, when using as output port. And, the value is undefined when reading from output port.

2.8 Data Pin & FIFO/DMA Control Pin Configuration Register 1

■ Data Pin & FIFO/DMA Control Pin Configuration Register 1 (PinCtrlCfg1) <Address: H'0A>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
LDRV							big_end						PAdir		DB_Cfg
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset: H'0000>
<S/W reset: ->
<USB bus reset: ->

b	Bit name	Function	R	W
15	LDRV Drive Current Adjust	0: When VIF=1.7~2.0V 1: When VIF=2.7~3.6V	○	○
14~9	Reserved. Set it to "0".		"0"	"0"
8	big_end Big Endian Mode	0: Little endian 1: Big endian	○	○
7~3	Reserved. Set it to "0".		"0"	"0"
2	PAdir Port A Direction	0: Input 1: Output	○	○
1	Reserved. Set it to "0".		"0"	"0"
0	DB_Cfg Data Bus Configuration	0: SD7-SD0/PA7-PA0 are set as the general-purpose port 1: SD7- SD0/PA7-PA0 are set as the split bus	○	○

(1) LDRV (Drive Current Adjust) Bit (b15)

This bit is used to adjust the drive current of the output pins.
The output pins here refer to SD7-0, D15-0, INT, DREQ, DEND, SUSP_ON and CONF_ON pins.

(2) big_end (Big Endian Mode) Bit (b8)

This bit sets the endian of the C_FIFO port and the D0_FIFO port.
When this bit is set to "0", the C_FIFO port and the D0_FIFO port becomes little endian.
When this bit is set to "1", the C_FIFO port and the D0_FIFO port becomes big endian.

	b15~b8	b7~b0
Little Endian	Odd number address	Even number address
Big Endian	Even number address	Odd number address

(3) PAdir (Port A Direction) Bit (b2)

This bit sets the port A direction. This bit is valid only when the DB_Cfg bit is set to "0".
General purpose port PA7-PA0 is input port when this bit is set to "0".
General purpose port PA7-PA0 is output port when this bit is set to "1".

(4) DB_Cfg (Data Bus Configuration) Bit (b0)

This bit sets the operations of SD7-SD0/PA7-PA0.
When this bit is set to "0", SD7-SD0/PA7-PA0 becomes the general-purpose port (GPIO).
When this bit is set to "1", SD7-SD0/PA7-PA0 becomes the split bus for the D0_FIFO port. In this case, CPU access to the D0_FIFO Port Register is invalid.

2.9 Data Pin & FIFO/DMA Control Pin Configuration Register 2

■ Data Pin & FIFO/DMA Control Pin Configuration Register 2 (PinCtrlCfg2) <Address: H'0C>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
0 - -	DreqA 0 - -	Burst 0 - -	DreqE 0 - -	0 - -	DackA 0 - -	RWstb 0 - -	DackE 0 - -	0 - -	DendA 0 - -	Pktmd 0 - -	DendE 0 - -	0 - -	Obus 0 - -	0 - -	0 - -

<H/W reset: H'0000>
<S/W reset: ->
<USB bus reset: ->

b	Bit name	Function	R	W
15	Reserved. Set it to "0".		"0"	"0"
14	DreqA DREQ Polarity Select	0: Low active 1: High active	○	○
13	Burst Burst Mode	0: Normal mode (Cycle steal mode) 1: Burst mode	○	○
12	DreqE DREQ Output Enable	0: Disable DREQ signal output 1: Enable DREQ signal output	○	○
11	Reserved. Set it to "0".		"0"	"0"
10	DackA DACK Polarity Select	0: Low active 1: High active	○	○
9	RWstb RD/WR Strobe Mode	0: WRn_N and RD_N pins are used as the strobe signal 1: DSTB_N pin is used as the strobe signal	○	○
8	DackE DACK Pin Select	0: Address, WRn_N, RD_N and CS_N pins are selected as the handshake signal 1: DACK pin is selected as the handshake signal	○	○
7	Reserved. Set it to "0".		"0"	"0"
6	DendA DEND Polarity Select	0: Low active 1: High active	○	○
5	Pktmd Packet Mode	0: Transaction completion output mode 1: Buffer completion output mode	○	○
4	DendE DEND Pin Enable	0: Disable DEND pin 1: Enable DEND pin	○	○
3	Reserved. Set it to "0".		"0"	"0"
2	Obus OUT Bus Mode	0: Hi-Speed drive mode 1: Normal mode	○	○
1~0	Reserved. Set it to "0".		"0"	"0"

(1) DreqA (DREQ Polarity Select) Bit (b14)

This bit sets the DREQ pin polarity.

(2) Burst (Burst Mode) Bit (b13)

This bit selects the DREQ pin timing.

When the normal mode (cycle steal mode) is set, the DREQ pin is asserted on every transfer (8 bits or 16 bits) and is negated every time a DACK pin is input.

When the burst mode is set, the DREQ pin is continuously asserted during data transfer and is negated on completion of all data transfer.

(3) DreqE (DREQ Output Enable) Bit (b12)

This bit sets the enable of DREQ pin output.

(4) DackA (DACK Polarity Select) Bit (b10)

This bit sets the DACK pin polarity.

(5) RWstb (RD/WR Strobe Mode) Bit (b9)

This bit selects the read/write strobe signal for DMA data transfer. Set this bit to "1" in order to use DMA transfer in split bus (DMA Interface).

This bit is valid only when the DackE bit is set to "1".

(6) DackE (DACK Pin Select) Bit (b8)

This bit selects the handshake signal for DMA transfer. When this bit is set to "0", DMA transfer is performed in the CPU bus, where access to the split bus (DMA Interface) is disabled.

(7) DendA (DEND Polarity Select) Bit (b6)

This bit sets the DEND pin polarity.

(8) Pktmd (Packet Mode) Bit (b5)

This bit is used to determine the operation of the DEND pin which indicates the last data transfer of DMA data transfer in the OUT direction data transfer.

When this bit is set to "0", the DEND pin is asserted on completion of the packet count transfer specified by the TRNCNT [15:0] bits of D0_FIFO Port Control Register 3, or a short packet transfer.

When this bit is set to "1", the DEND pin is asserted on completion of buffer size transfer preset in PIPE.

During the IN direction data transfer this bit is invalid, because the DEND pin is kept in input direction.

(9) DendE (DEND Pin Enable) Bit (b4)

This bit sets the enable of DEND signal input/output.

When the input/output of the DEND pin is disabled, the DEND pin becomes Hi-Z output.

When the PIPE direction is OUT by setting to the Current_PIPE [2:0] bits of the D0_FIFO Port Control Register 0, the DEND pin is kept in output direction. When the PIPE direction is IN, the DEND pin becomes in input direction.

(10) Obus (OUT Bus Mode) Bit (b2)

This bit selects a driving method of the split bus (DMA Interface) data pin and DEND pin.

When this bit is set to "0" and the PIPE direction is OUT by setting to the Current_PIPE [2:0] bits of the D0_FIFO Port Control Register 0, the data pin and the DEND pin are always driven. And, when it is set to IN, these pins are kept always ready for input.

When this bit is set to "1" and the PIPE direction is OUT by setting to the Current_PIPE [2:0] bits of the D0_FIFO Port Control Register 0, the data pin and the DEND pin are driven "High" or "Low" during the period both the DACK pin and the DSTB_N pin are asserted. And, when it is set to IN, these pins are kept always ready for input only during the period the DACK pin is asserted.

2.10 C_FIFO Port Register 0

■ C_FIFO Port Register 0 (C_FIFOPort0) <Address: H'14>

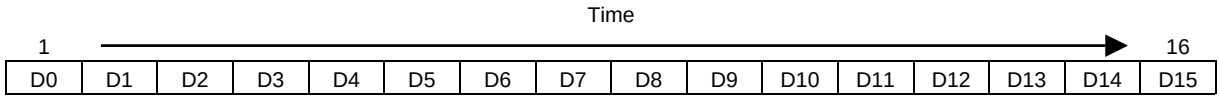
b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
C_FIFO_Port [15:0]															
0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -

<H/W reset: H'0000>
<S/W reset: H'????>
<USB bus reset: ->

b	Bit name	Function	R	W
15~0	C_FIFO_Port [15:0] C_FIFO Port	<When PIPE direction is set to OUT> • Read Reads receive data <When PIPE direction is set to IN> • Write Writes transmit data	○	○

(1) C_FIFO_Port [15:0] (C_FIFO Port) Bits (b15-b0)

This register is a data port for FIFO buffer reading and writing by CPU access. The data written in the FIFO buffer is sent out to USB bus in order of LSB first. The data received from the USB bus is stored in FIFO buffer in the same order. (in the case of a 16-bit little endian)



(The order of the data sent to USB bus)

When the PIPE direction is OUT by setting to the Current_PIPE [2:0] bits of the C_FIFO Port Control Register 0 (DIR bit of PIPE Configuration Window Register 0 is set to "0".), it is set to receive FIFO data register.

When the PIPE direction is IN (DIR bit of PIPE Configuration Window Register 0 is set to "1".), it is set to transmit FIFO data register.

Further, the direction is determined by the ISEL bit of the C_FIFO Port Control Register 0 when the DCP ("000") is assigned to the Current_PIPE [2:0] bits. When the ISEL bit is set to "0", it becomes the receive FIFO data register, and when the ISEL bit is set to "1", it becomes the transmit FIFO data register.

The corresponding bits become as follows according to the big_end bit of the Data Pin & FIFO/DMA Control Pin Configuration Register 1:

big_end = "0" (Little endian)

When MBW bit of C_FIFO Port Control Register 0 is set to "0" (8-bit width), C_FIFO_Port [7:0] are valid.

When MBW bit of C_FIFO Port Control Register 0 is set to "1" (16-bit width), C_FIFO_Port [15:0] are valid. C_FIFO_Port [15:8] are upper 8 bits, C_FIFO_Port [7:0] are lower 8 bits.

big_end = "1" (Big endian)

When MBW bit of C_FIFO Port Control Register 0 is set to "0"(8-bit width), C_FIFO_Port [15:8] are valid.

When MBW bit of C_FIFO Port Control Register 0 is set to "1" (16-bit width), C_FIFO_Port [15:0] are valid. C_FIFO_Port [15:8] are lower 8 bits, C_FIFO_Port [7:0] are upper 8 bits.

Note: Only by this register can be used to access DCP FIFO buffer.

2.11 D0_FIFO Port Register 0

■ D0_FIFO Port Register 0 (D0_FIFOPort0) <Address: H'18>

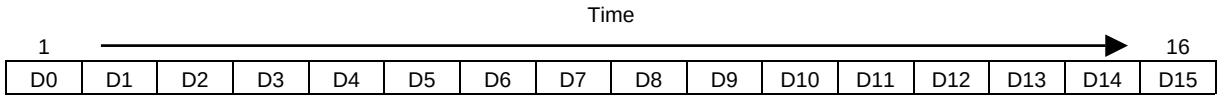
b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
D0_FIFO_Port [15:0]															
0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -

<H/W reset: H'0000 0000>
<S/W reset: ->
<USB bus reset: ->

b	Bit name	Function	R	W
15~0	D0_FIFO_Port [15:0] D0_FIFO Port	<When PIPE direction is set to OUT> • Read Reads receive data <When PIPE direction set to IN> • Write Writes transmit data	○	○

(1) D0_FIFO_Port [15:0] (D0_FIFO Port) Bits (b15-b0)

This register is a data port for FIFO buffer reading and writing by DMA access. The data written in the FIFO buffer is sent out to USB bus in order of LSB first. The data received from the USB bus is stored in FIFO buffer in the same order. (in the case of a 16-bit little endian)



(The order of the data sent to USB bus)

When the PIPE direction is OUT by setting to the Current_PIPE [2:0] bits of the D0_FIFO Port Control Register 0 (DIR bit of PIPE Configuration Window Register 0 is set to "0".), it is set to receive FIFO data register.

When the PIPE direction is IN (DIR bit of PIPE Configuration Window Register 0 is set to "1".), it is set to transmit FIFO data register.

Further, when "000" is assigned to the Current_PIPE [2:0] bits and the DB_Cfg bit of the Data Pin & FIFO/DMA Control Pin Configuration Register 1 is set to "1", this register is invalid for CPU access.

The corresponding bits become as follows according to the big_end bit of the Data Pin & FIFO/DMA Control Pin Configuration Register 1:

big_end = "0" (Little endian)

When MBW bit of D0_FIFO Port Control Register 0 is set to "0" (8-bit width), D0_FIFO_Port [7:0] are valid.

When MBW bit of D0_FIFO Port Control Register 0 is set to "1" (16-bit width), D0_FIFO_Port [15:0] are valid. D0_FIFO_Port [15:8] are upper 8 bits, D0_FIFO_Port [7:0] are lower 8 bits.

big_end = "1" (Big endian)

When MBW bit of D0_FIFO Port Control Register 0 is set to "0"(8-bit width), D0_FIFO_Port [15:8] are valid.

When MBW bit of D0_FIFO Port Control Register 0 is set to "1" (16-bit width), D0_FIFO_Port [15:0] are valid. D0_FIFO_Port [15:8] are lower 8 bits, D0_FIFO_Port [7:0] are upper 8 bits.

2.12 DCP Continuous Transmit Data Length Register

■ DCP Continuous Transmit Data Length Register (DCPSdln) <Address: H'26>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
							SDLN [8:0]								
0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: ->

b	Bit name	Function	R	W
15~9	Reserved. Set it to "0".		"0"	"0"
8~0	SDLN [8:0] Control Read Continuous Transmit Data Length	Control read continuous transmit data length	○	○

(1) SDLN [8:0] (Control Read Continuous Transmit Data Length) Bits (b8-b0)

These bits set the transmit data length (byte count) of the control read in continuous transfer mode. The set value includes maximum "H'100" (256 bytes). When control read continuous transfer mode is set, set this register before writing transmit data into the C_FIFO Port Register.

This bit is valid only when follows condition 1 and condition 2 are met.

Condition 1: The Current_PIPE [2:0] bits = "000" and the ISEL = "1" of the C_FIFO Port Control Register 0.

Condition 2: The CNTMD="1" of the DCP Configuration Register 1 (Control continuous transfer mode).

The operations in control read transfer set by these bits is as follows:

(1) When the SDLN value is equal to an integral multiple (excluding 256) of MaxPacketSize:
M66591, after the number of data assigned by the data SDLN bits is written in the FIFO buffer, automatically starts data transmission and, following completion of this transmission, automatically transmits the zero-length packet to the next IN token.

(2) When the SDLN value is equal to "256" (H'100):
In this case, M66591 starts data transmission in the same way as the above (1), however, does not transmit the zero-length packet.

(3) When the SDLN value is equal to "0":
After transmission data are written in the FIFO buffer and the BVAL bit is set, M66591 starts data transmission. When the number of data written in FIFO is equal to the FIFO buffer size having been set, there is no need for setting to the BVAL bit. Also, the zero-length packet is not automatically transmitted on completion of data transmission. In order to transmit the zero-length packet, it is necessary to set the BVAL bit without writing data in the FIFO buffer after setting the SDLN bits to "0".

(4) When the SDLN value is other than the above:
M66591, after the number of data assigned in the data SDLN is written in the FIFO buffer, automatically starts data transmission. In this case, the short packet follows the transmit data, the zero-length packet is not transmit. (When the IN token is received after transmit of the short packet,M66591 responds with NAK, generating an INTN interrupt.)

Note: It is necessary to clear buffer (BCLR="1") after setting the SDLN [8:0] bits.

2.13 C_FIFO Port Control Register 0

■ C_FIFO Port Control Register 0 (C_FIFOPortCtrl0) <Address: H'28>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
RCNT	REW				MBW					ISEL			Current_PIPE [2:0]		
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: ->

b	Bit name	Function	R	W
15	RCNT Read Count Mode	0: The CPU_DTLN bits are cleared by reading all receive data 1: The CPU_DTLN bits are counted down by reading receive data	○	○
14	REW Buffer Rewind	<When set to OUT buffer> • Write 0: Invalid (Ignored when written) 1: Clears the buffer reading pointer <When set to IN buffer> • Write 0: Invalid (Ignored when written) 1: Clears the buffer writing pointer	"0"	○
13~11	Reserved. Set it to "0".		"0"	"0"
10	MBW FIFO Access Maximum Bit Width	0: 8-bit width 1: 16-bit width	○	○
9~6	Reserved. Set it to "0".		"0"	"0"
5	ISEL DCP Access Direction Select	0: Select FIFO buffer read (control write) 1: Select FIFO buffer write (control read)	○	○
4~3	Reserved. Set it to "0".		"0"	"0"
2~0	Current_PIPE [2:0] C_FIFO Port Access PIPE Select	"000" DCP "001" PIPE1 "010" PIPE2 "011" PIPE3 "100" PIPE4 "101" PIPE5 "110" PIPE6 "111" Invalid	○	○

(1) RCNT (Read Count Mode) Bit (b15)

This bit sets the count down mode of the CPU_DTLN [9:0] bits of the C_FIFO Port Control Register 1.

When this bit is set to "0", the CPU_DTLN [9:0] bits do not change by reading the data from the C_FIFO Port Register 0, and are cleared when all data is read out.

When this bit is set to "1", the CPU_DTLN [9:0] bits are decremented every time the data is read from the C_FIFO Port Register 0.

(2) REW (Buffer Rewind) Bit (b14)

This bit rewinds the reading/writing pointer of the FIFO buffer by writing "1" to this bit.

Writing "0" to this bit is invalid.

When the PIPE direction having been set to the Current_PIPE [2:0] bits is OUT, buffer data can be read out again from the beginning after the rewind operation.

When the PIPE direction having been set to the Current_PIPE [2:0] bits is IN, all data having been written so far are made invalid after the rewind operation and buffer data can be written again from the beginning.

When the FRDY bit of the C_FIFO Port Control Register 1 is "1", rewind operation is executable. When "1" is written to the REW bit concurrently with renewal of the Current_PIPE [2:0] bits, the rewind operation is executed to the FIFO buffer of the renewed PIPE.

(3) MBW (FIFO Access Maximum Bit Width) Bit (b10)

This bit selects the bit width of the C_FIFO port access.
0: 8-bit width
1: 16-bit width

When changing the MBW setting, the following should be noted:
(1) When the PIPE having been set to the Current_PIPE [2:0] is OUT:
The MBW is disabled to change setting after the Current_PIPE [2:0] has been set.
Be sure to set the MBW concurrently with or before setting of the Current_PIPE [2:0].

(2) When the PIPE having been set to the Current_PIPE [2:0] is IN:
The MBW is disabled to change the following setting after the Current_PIPE [2:0] has been set.
* Changing from the MBW="1" (8-bit width) to "1" (16-bit width)
Changes other than the above are possible. An example of changes in the MBW setting is shown below:
<Example of enable changes in the MBW setting: To write the short packet data of 131 bytes>
(1) To set PIPE which has a buffer area of 512 bytes. (To set the MBW="1" concurrently with setting of the Current_PIPE [2:0].)
(2) To write up to 130 bytes with 16-bit width.
(3) To change the MBW setting to "0".
(4) To write 1 byte with 8-bit width. (131 bytes in total)
(5) To write "1" to the BVAL bit. (Short packet data transmission)

(4) ISEL (DCP Access Direction Select) Bit (b5)

This bit selects the access direction of DCP. This bit is valid only when DCP is set to the Current_PIPE [2:0] bits.

(5) Current_PIPE [2:0] (C_FIFO Port Access PIPE Select) Bits (b2-b0)

These bits designate the access PIPE to the C_FIFO port.
Each configuration register (max. packet size, etc.) of the PIPE having been set to the Current_PIPE [2:0] should not be changed.
When changing each configuration register of the PIPE, either change the Current_PIPE [2:0] once or clear buffer by setting "1" to the BCLR bit of the C_FIFO Port Control Register 1 after changing each configuration register.
Further, when DCP has been set to the Current_PIPE [2:0], neither each configuration register nor the SDLN can be changed. If it is changed, buffer must be cleared.
Also, this setting while accessing the C_FIFO Port Register 0 should not be changed.

Note: Do not set these bits to the same value as the Current_PIPE [2:0] bits of the D0_FIFO Port Control Register 0. (Do not set one PIPE simultaneously to both the C_FIFO port and the D0_FIFO port.)

2.14 C_FIFO Port Control Register 1

■ C_FIFO Port Control Register 1 (C_FIFOPortCtrl1) <Address: H'2C>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
BVAL	BCLR	FRDY				CPU_DTLN [9:0]									
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: ->

b	Bit name	Function	R	W
15	BVAL Buffer Valid Flag	<When set to OUT buffer> • Read 0: Disables to read the data of buffer 1: Enables to read the data of buffer • Write Invalid (Ignored when written) <When set to IN buffer> • Read 0: Incomplete to write the data to buffer 1: Complete to write the data to buffer • Write 0: Invalid (Ignored when written) 1: Enable to transmit short packet	○	○
14	BCLR Buffer Clear	<When set to OUT buffer> • Write 0: Invalid (Ignored when written) 1: Buffer clear (When the BVAL bit is set to "1") <When set to IN buffer> • Write 0: Invalid (Ignored when written) 1: Buffer clear (When the BVAL bit is set to "0")	"0"	○
13	FRDY C_FIFO Port Ready	0: Disables to access the C_FIFO Port Register 0 1: Enables to access the C_FIFO Port Register 0	○	-
12~10	Reserved. Set it to "0".		"0"	"0"
9~0	CPU_DTLN [9:0] C_FIFO Receive Data Length	Stores the receive data length (byte count)	○	-

(1) BVAL (Buffer Valid Flag) Bit (b15)

This bit indicates status of whether or not the PIPE buffer set to the Current_PIPE [2:0] bits of the C_FIFO Port Control Register 0 is accessible.

When the PIPE having been set to the Current_PIPE [2:0] bits of the C_FIFO Port Control Register 0 is OUT, this bit indicates whether or not data exist in the buffer.

This bit is changed from "0" to "1" in the following conditions:

(1) When the buffer has become full with a received data packet or when it has received a short packet in continuous transfer mode.

(2) When "1" is written to the TGL bit of the C_FIFO Port Control Register 2 in continuous transfer mode.

(3) When 1 packet data have been received in non-continuous transfer mode.

This bit is cleared when data are read out from the buffer, making the buffer empty. However, when the zero-length packet is received while the buffer is empty, this bit is not cleared. In this case, it is cleared by writing "1" to the BCLR bit.

When the PIPE having been set to the Current_PIPE [2:0] bits is IN, setting "1" to this bit enables transmit of the short packet. Further, it enables transmit of the zero-length packet by setting "1" simultaneously to this bit and to the BCLR bit.

This bit is changed from "0" to "1" in the following conditions:

(1) When data have been written until the buffer becomes full in continuous transfer mode.

(2) When data have been written up to the MaxPacketSize in non-continuous transfer mode.
When the buffer becomes empty, this bit is cleared. Writing “0” to this bit is invalid.
Further, the PIPE having been set to the Current_PIPE [2:0] is DCP, the IN/OUT direction is determined by the ISEL bit.

Note: When the PIPE having been set to the Current_PIPE [2:0] bits is IN and this bit is “1”, writing “1” to this bit is prohibited.

(2) BCLR (Buffer Clear) Bit (b14)

When “1” is written to this bit, the buffer of the PIPE having been set to the Current_PIPE [2:0] bits is cleared. Refer to “3.6.2.3 Buffer Clear” for detail.
While the FRDY bit of the C_FIFO Port Control Register 1 is “1”, it enables writing “1” to this bit.
However, the PIPE having been set to the Current_PIPE [2:0] bits of the C_FIFO Port Control Register 0 is DCP, the buffer having been selected by the ISEL bit is cleared irrespective of the FRDY bit. To clear the buffer of DCP, set the PID [1:0] bits of DCP Control Register to the NAK before writing “1” to this bit.
Writing “0” to this bit is invalid.

(3) FRDY (C_FIFO Port Ready) Bit (b13)

The C_FIFO Port Register 0 can be accessed while “1” is set to this bit.

(4) CPU_DTLN [9:0] (C_FIFO Receive Data Length) Bits (b9-b0)

These bits indicate the receive data length.
When the RCNT bit of the C_FIFO Port Control Register 0 is “1”, every time the C_FIFO Port Register is read out, these bits count down at -1 for 8-bit width and -2 for 16-bit width.
When the RCNT bit is “0”, the receive data length is retained also during reading data and these bits are cleared after all the receive data are read out.
When the PIPE having been set to the Current_PIPE [2:0] bits of the C_FIFO Port Control Register 0 is IN direction, these bits are invalid.
Further, when the PIPE having been set to the Current_PIPE [2:0] bits is DCP, these bits are valid only when the ISEL bit is “1”.

Note: It is necessary to do polling FDRY and confirm FRDY = 1 before read these bits. Refer to “3.6 Buffer Memory” for reading timing.

2.15 C_FIFO Port Control Register 2

■ C_FIFO Port Control Register 2 (C_FIFOPortCtrl2) <Address: H'2E>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
TGL	SCLR	SBUSY													
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: ->

b	Bit name	Function	R	W
15	TGL Buffer Toggle	<When set to OUT buffer> • Write 0: Invalid (Ignored when written) 1: Toggles access buffer <When set to IN buffer> • Write Set it to "0"	"0"	○
14	SCLR Buffer Clear	<When set to OUT buffer> • Write 0: Invalid (Ignored when written) 1: Inhibited <When set to IN buffer> • Write 0: Invalid (Ignored when written) 1: Clear the SIE side buffer	"0"	○
13	SBUSY SIE side Buffer Busy	0: SIE no access state 1: SIE access state	○	-
12~0	Reserved. Set it to "0".		"0"	"0"

(1) TGL (Buffer Toggle) Bit (b15)

The SIE side buffer is changed over to the CPU side buffer by writing "1" to this bit while the FIFO buffer is not full in continuous transfer mode. At this time, the buffer ready interrupt occurs. This bit is valid only for the PIPE of OUT direction. Further, when the PIPE which has been set to the Current_PIPE [2:0] bits of the C_FIFO Port Control Register 0 is DCP, writing "1" to this bit is invalid.

Writing "0" to this bit is invalid.

Explanation of Terms: Refer to "1.5 Block Diagram" about "SIE side" and "CPU side".

(2) SCLR (Buffer Clear) Bit (b14)

The SIE side buffer is cleared and the SIE side buffer is changed over to the CPU side buffer by writing "1" to this bit. This bit is valid only for the PIPE of IN direction. Further, when the PIPE which has been set to the Current_PIPE [2:0] bits of the C_FIFO Port Control Register 0 is DCP, writing "1" to this bit is invalid.

Please set according to the following procedures in order to use this bit:

(1) Set the PID [1:0] bits of the PIPE i Control Register corresponding to the PIPE having been set to the Current_PIPE [2:0] bits of the C_FIFO Port Control Register 0 to the NAK so that it does not respond to the IN transaction.

(2) Confirm that the SBUSY bit is "0". (Confirm that no buffer access exists.)

(3) Clear the SIE-side buffer by writing "1" to the SCLR bit.

Writing "0" to this bit is invalid.

(3) SBUSY (SIE side Buffer Busy) Bit (b13)

This bit indicates that SIE is accessing the buffer of the PIPE having been set to the Current_PIPE [2:0] bits of the C_FIFO Port Control Register 0. Further, when the PIPE which has been set to the Current_PIPE [2:0] bits is DCP, reading of this bit is invalid.

2.16 D0_FIFO Port Control Register 0

■ D0_FIFO Port Control Register 0 (D0_FIFOPortCtrl0) <Address: H'30>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
RCNT	REW	ABCR			MBW	TREnb	TRclr						Current_PIPE [2:0]		
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: ->

b	Bit name	Function	R	W
15	RCNT Read Count Mode	0: The DMA_DTLN bits are cleared by reading all receive data 1: The DMA_DTLN bits are counted down by reading receive data	○	○
14	REW Buffer Rewind	<When set to OUT buffer> • Write 0: Invalid (Ignored when written) 1: Clears the buffer reading pointer <When set to IN buffer> • Write 0: Invalid (Ignored when written) 1: Clears the buffer writing pointer	"0"	○
13	ABCR Automatic Buffer Clear Mode	0: Disable automatic buffer clear 1: Enable automatic buffer clear	○	○
12~11	Reserved. Set it to "0".		"0"	"0"
10	MBW FIFO Port Access Bit Width	0: 8-bit width 1: 16-bit width	○	○
9	TREnb Transaction Counter Enable	0: Disable transaction counter function 1: Enable transaction counter function	○	○
8	TRclr Transaction Counter Clear	0: Invalid 1: Clears the transaction counter	○	○
7~3	Reserved. Set it to "0".		"0"	"0"
2~0	Current_PIPE [2:0] D0_FIFO Port Access PIPE Designate	"000" Disable use of D0_FIFO port "001" PIPE1 "010" PIPE2 "011" PIPE3 "100" PIPE4 "101" PIPE5 "110" PIPE6 "111" Invalid	○	○

(1) RCNT (Read Count Mode) Bit (b15)

This bit sets the count down mode of the DMA_DTLN [9:0] bits of the D0_FIFO Port Control Register 2.

When this bit is set to "0", the DMA_DTLN [9:0] bits do not change by reading the data from the D0_FIFO Port Register 0, and are cleared when all data is read out.

When this bit is set to "1", the DMA_DTLN [9:0] bits is decremented every time the data is read from the D0_FIFO Port Register 0.

(2) REW (Buffer Rewind) Bit (b14)

This bit rewinds the reading/writing pointer of the FIFO buffer by writing "1" to this bit.

Writing "0" to this bit is invalid.

When the PIPE direction having been set to the Current_PIPE [2:0] bits is OUT, buffer data can be read out again from the beginning after the rewind operation.

When the PIPE direction having been set to the Current_PIPE [2:0] bits is IN, all data having been written so far are made invalid after the rewind operation and buffer data can be written again from the beginning.

When the FRDY bit of the D0_FIFO Port Control Register 2 is "1", rewind operation is executable. When "1" is

written to the REW bit concurrently with renewal of the Current_PIPE [2:0] bits, the rewind operation is executed to the FIFO buffer of the renewed PIPE.

(3) ABCR (Automatic Buffer Clear Mode) Bit (b13)

This bit is valid only when the PIPE direction having been set to the Current_PIPE [2:0] bits is OUT.
It is selected whether the FIFO is cleared by software or by hardware at the time of (1) or (2) mentioned below:
(1) When the zero-length packet has been received while the buffer is kept empty.
(2) When the short packet is received (including, also, the zero-length packet) or when a packet for the transaction counter has been received, where the BFRE bit of the PIPE Configuration Window Register 0 corresponding to the PIPE having been set to the Current_PIPE [2:0] is "1".

0: Disable automatic buffer clear mode.
In the above (1) or (2), buffer status is not cleared by reading out all the buffer data (with the BVAL bit of the D0_FIFO Port Control Register 2 = "1"). Therefore, following completion of reading out by the DMA transfer, the byte count of the last transfer can be confirmed by reading out the DMA_DTLN [9:0] bits (RCNT="0") of the D0_FIFO Port Control Register 2. Please set "1" to the BCLR bit the D0_FIFO Port Control Register 2 in order to clear the buffer.
1: Enable automatic buffer clear mode.
When all the buffer data have been read out, the buffer is automatically cleared and becomes to state ready for receiving the next data.

(4) MBW (FIFO Port Access Bit Width) Bit (b10)

This bit selects the bit width of the D0_FIFO port access.
0: 8-bit width
1: 16-bit width

When changing the MBW setting, the following should be noted:
(1) When the PIPE having been set to the Current_PIPE [2:0] is OUT:
The MBW is disabled to change setting after the Current_PIPE [2:0] has been set.
Be sure to set the MBW concurrently at the time or before setting of the Current_PIPE [2:0].

(2) When the PIPE having been set to the Current_PIPE [2:0] is IN:
The MBW is disabled to change the following setting after the Current_PIPE [2:0] has been set. When setting has been changed, output of the DREQ pin does not function properly.
When the short packet is transmitted and no byte write function exists in the external DMAC, it is enable to write data as follows:
<Example to write the last byte of the short packet to the DMA port PIPE by the CPU access >
(1) Set PIPE which has a buffer area of 512 bytes. (To set the MBW="1" concurrently with setting of the Current_PIPE [2:0].)
(2) Write up to 130 bytes in 16-bit width by DREQ/DACK pins in DMA, and to stop the external DMAC.
(3) Disable DREQ output by writing "0" to the DreqE bit.
(4) Change the MBW bit setting to "0".
(5) Write 1 byte with 8-bit width by the CPU access. (131 bytes in total)
(6) Write "1" to the BVAL bit. (Short packet data transmission)

(5) TREnb (Transaction Counter Enable) Bit (b9)

This bit sets the enable/disable of transaction counter function.
0: Disable transaction counter function
1: Enable transaction counter function
This bit is valid only when the PIPE direction having been set to the Current_PIPE [2:0] bits is OUT.
For details of transaction counter function, refer to the TRNCNT [15:0] bits of the D0_FIFO Port Control Register 3.
Before setting this bit, be sure to set the PID [1:0] bits of the PIPE i Control Register (i=1~6) to "00" (NAK).

(6) TRclr (Transaction Counter Clear) Bit (b8)

Writing "1" to this bit clears the counter of transaction counter function.
Writing "0" to this bit is invalid.
Before setting this bit, be sure to set the PID [1:0] bits of the PIPE i Control Register (i=1~6) to "00" (NAK).

(7) Current_PIPE [2:0] (D0_FIFO Port Access PIPE Designate) Bits (b2-b0)

These bits designate the access PIPE to the D0_FIFO port.

Do not change each configuration register (max. packet size, etc.) of the PIPE having been set to the Current_PIPE [2:0].

When changing each configuration register of the PIPE, either change the Current_PIPE [2:0] once or clear buffer by setting “1” to the BCLR bit of the D0_FIFO Port Control Register 2 after changing each configuration register.

Also, this setting should not be changed while accessing the D0_FIFO Port Register 0.

Note: Do not set these bits to the same value as the Current_PIPE [2:0] bits of the C_FIFO Port Control Register 0. (Do not set one PIPE simultaneously to both the C_FIFO port and the D0_FIFO port.)

2.17 D0_FIFO Port Control Register 2

■ D0_FIFO Port Control Register 2 (D0_FIFOPortCtrl2) <Address: H'34>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
BVAL	BCLR	FRDY				DMA_DTLN [9:0]									
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: ->

b	Bit name	Function	R	W
15	BVAL Buffer Valid Flag	<When set to OUT buffer> • Read 0: Disables to read the data of buffer 1: Enables to read the data of buffer • Write Invalid (Ignored when written) <When set to IN buffer> • Read 0: Incomplete to write the data to buffer 1: Complete to write the data to buffer • Write 0: Invalid (Ignored when written) 1: Enable to transmits short packet	○	○
14	BCLR Buffer Clear	<When set to OUT buffer> • Write 0: Invalid (Ignored when written) 1: Buffer clear (When the BVAL bit is set to "1") <When set to IN buffer> • Write 0: Invalid (Ignored when written) 1: Buffer clear (When the BVAL bit is set to "0")	"0"	○
13	FRDY D0_FIFO Port Ready	0: Disables to access the D0_FIFO Port Register 0 1: Enables to access the D0_FIFO Port Register 0	○	-
12~10	Reserved. Set it to "0".		"0"	"0"
9~0	DMA_DTLN [9:0] D0_FIFO Receive Data	Stores the receive data length (byte count)	○	-

(1) BVAL (Buffer Valid Flag) Bit (b15)

This bit indicates status whether or not the PIPE buffer set to the Current_PIPE [2:0] bits of the D0_FIFO Port Control Register 0 is accessible.

When the PIPE which has been set to the Current_PIPE [2:0] bits of the D0_FIFO Port Control Register 0 is OUT, this bit indicates whether or not data exist in the buffer.

This bit is changed from "0" to "1" in the following conditions:

(1) When the buffer has become full with a received data packet or when it has received a short packet in continuous transfer mode.

(2) When a packet has been received up to the value preset to the TRNCNT [15:0] bits of the D0_FIFO Port Control Register 3 with the TREnb bit of the D0_FIFO Port Control Register 0 set to "1".

(3) When 1 packet data have been received in non-continuous transfer mode.

This bit is cleared when data are read out from the buffer, making the buffer empty. This bit may not be automatically cleared depending on setting of the BFRE bit of the PIPE Configuration Window Register 0 corresponding to the setting PIPE having been set to the ABCR bit or the Current_PIPE [2:0] bits of the D0_FIFO Port Control Register 0. For details, refer to the ABCR bit.

When the PIPE having been set to the Current_PIPE [2:0] bits is IN, setting "1" to this bit enables transmit of the short packet. Further, it enables transmit of the zero-length packet by setting "1" simultaneously to this bit and to

the BCLR bit.
This bit is changed from “0” to “1” on the following conditions:
(1) When data have been written until the buffer becomes full in continuous transfer mode.
(2) When data have been written up to the MaxPacketSize in non-continuous transfer mode.
(3) When the DEND pin has been asserted during the DMA transfer:
When the buffer becomes empty, this bit is cleared. Writing “0” to this bit is invalid.

Note: When the PIPE which has been set to the Current_PIPE [2:0] bits is IN and this bit is “1”, do not write “1” to this bit.

(2) BCLR (Buffer Clear) Bit (b14)

When “1” is written to this bit, the buffer of the PIPE having been set to the Current_PIPE [2:0] bits is cleared. Refer to “3.6.2.3 Buffer Clear” for detail.
While the FRDY bit of the D0_FIFO Port Control Register 2 is “1”, it enables writing “1” to this bit.
Writing “0” to this bit is invalid.

(3) FRDY (D0_FIFO Port Ready) Bit (b13)

The D0_FIFO Port Register 0 can be accessed while “1” is set to this bit.

(4) DMA_DTLN [9:0] (D0_FIFO Receive Data) Bits (b9-b0)

These bits indicate the receive data length.
When the RCNT bit of the D0_FIFO Port Control Register 0 is “1”, every time the D0_FIFO Port Register 0 is read out, these bits count down at -1 for 8-bit width and -2 for 16-bit width.
When the RCNT bit is “0”, the receive data length is retained also during data reading and this bits are cleared after all the received data are read out.
When the PIPE which has been set to the Current_PIPE [2:0] bits of the D0_FIFO Port Control Register 0 is IN direction, this bit is invalid.

Note: It is necessary to do polling FDRY and confirm FRDY = 1 before read these bits. Refer to “3.6 Buffer Memory” for reading timing.

2.18 D0_FIFO Port Control Register 3

■ D0_FIFO Port Control Register 3 (D0_FIFOPortCtrl3) <Address: H'36>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
TRNCNT [15:0]															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: ->

b	Bit name	Function	R	W
15~0	TRNCNT [15:0] Transaction Counter	<When TREnb bit is set to "0"> Packet count that completes the receiving <When TREnb bit is set to "1"> Received packet count	○	○

(1) TRNCNT [15:0] (Transaction Counter) Bits (b15-b0)

These bits are valid only when the PIPE direction having been set to the Current_PIPE [2:0] bits of the D0_FIFO Port Control Register 0 is OUT.

The transaction counter uses the two internal registers:
a) Current counter register
b) Upper limit register

Writing to these bits means writing to the upper limit register. Reading of these bits consists of the following:
When the TREnb bit of D0_FIFO Port Control Register 0 is "0", the upper limit register is read out.
When the TREnb bit of D0_FIFO Port Control Register 0 is "1", the current counter register is read out.

When TREnb bit of D0_FIFO Port Control Register 0 is set to "1", every time the OUT transaction is received, the current counter register is incremented.
The current counter register is cleared in the following event:
(1) When a short packet has been received in an executed OUT transaction.
(2) When the current counter register has reached the upper limit register of the above b).
(3) When "1" has been written to the TRclr bit of the D0_FIFO Port Control Register 0.

Note:

(1) Before setting these bits, be sure to set the PID [1:0] bits of the PIPE i Control Register (i=1~6) to "00" (NAK).

(2) When the TREnb bit is set to "1", be sure not to change this register.

2.19 INT Pin Configuration Register 0

■ INT Pin Configuration Register 0 (INTPinCfg0) <Address: H'40>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
VBSE	RSME		DVSE	CTRE	BEMPE	INTNE	INTRE	URST	SADR	SCFG	SUSP	WDST	RDST	CMPL	SERR
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: ->

b	Bit name	Function	R	W
15	VBSE VBUS Interrupt Enable	0: Disable interrupt 1: Enable interrupt (Interrupt occurs when the VBUSINT bit of the Interrupt Status Register 0 is set to "1")	O	O
14	RSME Resume Interrupt Enable	0: Disable interrupt 1: Enable interrupt (Interrupt occurs when the RESM bit of the Interrupt Status Register 0 is set to "1")	O	O
13	Reserved. Set it to "0".		"0"	"0"
12	DVSE Device State Transition Interrupt Enable	0: Disable interrupt 1: Enable interrupt (Interrupt occurs when the DVST bit of the Interrupt Status Register 0 is set to "1")	O	O
11	CTRE Control Transfer Stage Transition Interrupt Enable	0: Disable interrupt 1: Enable interrupt (Interrupt occurs when the CTRT bit of the Interrupt Status Register 0 is set to "1")	O	O
10	BEMPE PIPE Buffer Empty/Size Error Interrupt Enable	0: Disable interrupt 1: Enable interrupt (Interrupt occurs when the BEMP bit of the Interrupt Status Register 0 is set to "1")	O	O
9	INTNE PIPE Buffer Not Ready Interrupt Enable	0: Disable interrupt 1: Enable interrupt (Interrupt occurs when the INTN bit of the Interrupt Status Register 0 is set to "1")	O	O
8	INTRE PIPE Buffer Ready Interrupt Enable	0: Disable interrupt 1: Enable interrupt (Interrupt occurs when the INTR bit of the Interrupt Status Register 0 is set to "1")	O	O
7	URST USB Reset Detect	0: Disable the DVST bit set 1: Enable the DVST bit set	O	O
6	SADR SetAddress Execute	0: Disable the DVST bit set 1: Enable the DVST bit set	O	O
5	SCFG SetConfiguration Execute	0: Disable the DVST bit set 1: Enable the DVST bit set	O	O
4	SUSP Suspend Detect	0: Disable the DVST bit set 1: Enable the DVST bit set	O	O
3	WDST Control Write Transfer Data Stage Complete	0: Disable the CTRT bit set 1: Enable the CTRT bit set	O	O
2	RDST Control Read Transfer Data Stage Complete	0: Disable the CTRT bit set 1: Enable the CTRT bit set	O	O
1	CMPL Control Transfer Complete	0: Disable the CTRT bit set 1: Enable the CTRT bit set	O	O
0	SERR Control Transfer Sequence Error	0: Disable the CTRT bit set 1: Enable the CTRT bit set	O	O

(1) VBSE (VBUS Interrupt Enable) Bit (b15)

This bit sets enable/disable of the VBUS interrupt.
When this bit is set to "1", the interrupt is occurs if the VBUS bit of Interrupt Status Register 0 is set to "1".
This bit is capable of writing/reading even if the clock is not supplied (SCKE bit or XCKE bit of USB Transceiver Control Register 0 is set to 0.).

(2) RSME (Resume Interrupt Enable) Bit (b14)

This bit sets enable/disable of the resume interrupt.
When this bit is set to "1", the interrupt is occurs if the RESM bit is set to "1".
This bit is capable of writing/reading even if the clock is not supplied (SCKE bit or XCKE bit of USB Transceiver Control Register 0 is set to 0.).

(3) DVSE (Device State Transition Interrupt Enable) Bit (b12)

This bit sets enable/disable of the device state transition interrupt.
When this bit is set to "1", the interrupt occurs if the DVST bit is set to "1".
The conditions of setting "1" to the DVST bit depend on the URST, SADR, SCFG or SUSP bits.

(4) CTRE (Control Transfer Stage Transition Interrupt Enable) Bit (b11)

This bit sets enable/disable of the control transfer stage transition interrupt.
When this bit is set to "1", the interrupt occurs if the CTRT bit is set to "1".
The conditions of setting "1" to the CTRT bit depend on the WDST, RDST, CMPL or SERR bits.
The complete of setup stage cannot set enable/disable to set "1" to the CTRT bit.

(5) BEMPE (PIPE Buffer Empty/Size Error Interrupt Enable) Bit (b10)

This bit sets enable/disable of the PIPE buffer empty/size error interrupt.
When this bit is set to "1", the interrupt occurs if the BEMP bit is set to "1".

(6) INTNE (PIPE Buffer Not Ready Interrupt Enable) Bit (b9)

This bit sets enable/disable of the PIPE buffer not ready interrupt.
When this bit is set to "1", the interrupt occurs if the INTN bit is set to "1".

(7) INTRE (PIPE Buffer Ready Interrupt Enable) Bit (b8)

This bit sets enable/disable of the PIPE buffer ready interrupt.
When this bit is set to "1", the interrupt occurs if the INTR bit is set to "1".

(8) URST (USB Reset Detect) Bit (b7)

This bit selects whether to set the DVST bit to "1" or not at the USB bus reset detection.
The register is initialized by the USB reset detection, irrespective of the value of this bit.

(9) SADR (SetAddress Execute) Bit (b6)

This bit selects whether to set the DVST bit to "1" or not at the SetAddress execution.
For details, refer to the DVST bit.

(10) SCFG (SetConfiguration Execute) Bit (b5)

This bit selects whether to set the DVST bit to "1" or not at the SetConfiguration execution.
For details, refer to the DVST bit.

(11) SUSP (Suspend Detect) Bit (b4)

This bit selects whether to set the DVST bit to "1" or not at the suspend detection.

(12) WDST (Control Write Transfer Data Stage Complete) Bit (b3)

This bit selects whether to set the CTRT bit to "1" or not when transited to status stage after data stage during the control write transfer.

(13) RDST (Control Read Transfer Data Stage Complete) Bit (b2)

This bit selects whether to set the CTRT bit to "1" or not when transited to status stage after data stage during the control read transfer.

(14) CMPL (Control Transfer Complete) Bit (b1)

This bit selects whether to set the CTRT bit to "1" or not when the status stage completes during the control transfer.

(15) SERR (Control Transfer Sequence Error) Bit (b0)

This bit selects whether to set the CTRT bit to "1" or not when the sequence error is detected during the control transfer.

Note: Refer to "3.3 Interrupt" for detail.

2.20 INT Pin Configuration Register 1

■ INT Pin Configuration Register 1 (INTPinCfg1) <Address: H'42>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	0 - -	INTL 0 - -	INTA 0 - -

<H/W reset: H'0000>
<S/W reset: ->
<USB bus reset: ->

b	Bit name	Function	R	W
15~2	Reserved. Set it to "0".		"0"	"0"
1	INTL Interrupt Output Sense	0: Edge sense 1: Level sense	○	○
0	INTA Interrupt Output Polarity	0: Low Active 1: High Active	○	○

(1) INTL (Interrupt Output Sense) Bit (b1)

This bit selects the interrupt signal output type.

When edge sense is selected, the interrupt signal is negated when the interrupt factors have been cleared. However, when any other interrupt factor is not still cleared, the signal is asserted once again. The duration of negation is 650ns.

When level sense is selected, the signal is kept in asserted until all the interrupt factors are cleared.

(2) INTA (Interrupt Output Polarity) Bit (b0)

This bit sets the interrupt signal output polarity.

2.21 INT Pin Configuration Register 2

■ INT Pin Configuration Register 2 (INTPinCfg2) <Address: H'44>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	PIPEB_RE6 0 0 -	PIPEB_RE5 0 0 -	PIPEB_RE4 0 0 -	PIPEB_RE3 0 0 -	PIPEB_RE2 0 0 -	PIPEB_RE1 0 0 -	DCP_RE 0 0 -

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: ->

b	Bit name	Function	R	W
15~7	Reserved. Set it to "0".		"0"	"0"
6	PIPEB_RE6 PIPE6 Buffer Ready Interrupt Enable	0: Disable the INTR bit set 1: Enable the INTR bit set	○	○
5	PIPEB_RE5 PIPE5 Buffer Ready Interrupt Enable	0: Disable the INTR bit set 1: Enable the INTR bit set	○	○
4	PIPEB_RE4 PIPE4 Buffer Ready Interrupt Enable	0: Disable the INTR bit set 1: Enable the INTR bit set	○	○
3	PIPEB_RE3 PIPE3 Buffer Ready Interrupt Enable	0: Disable the INTR bit set 1: Enable the INTR bit set	○	○
2	PIPEB_RE2 PIPE2 Buffer Ready Interrupt Enable	0: Disable the INTR bit set 1: Enable the INTR bit set	○	○
1	PIPEB_RE1 PIPE1 Buffer Ready Interrupt Enable	0: Disable the INTR bit set 1: Enable the INTR bit set	○	○
0	DCP_RE DCP_FIFO Buffer Ready Interrupt Enable	0: Disable the INTR bit set 1: Enable the INTR bit set	○	○

(1) PIPEB_RE6 (PIPE6 Buffer Ready Interrupt Enable) Bits (b6)

This bit select whether to set the INTR bit of Interrupt Status Register 0 to "1" or not when the PIPEB_RDY6 bit of the Interrupt Status Register 1 is set to "1".

(2) PIPEB_RE5 (PIPE5 Buffer Ready Interrupt Enable) Bits (b5)

This bit select whether to set the INTR bit of Interrupt Status Register 0 to "1" or not when the PIPEB_RDY5 bit of the Interrupt Status Register 1 is set to "1".

(3) PIPEB_RE4 (PIPE4 Buffer Ready Interrupt Enable) Bits (b4)

This bit select whether to set the INTR bit of Interrupt Status Register 0 to "1" or not when the PIPEB_RDY4 bit of the Interrupt Status Register 1 is set to "1".

(4) PIPEB_RE3 (PIPE3 Buffer Ready Interrupt Enable) Bits (b3)

This bit select whether to set the INTR bit of Interrupt Status Register 0 to "1" or not when the PIPEB_RDY3 bit of the Interrupt Status Register 1 is set to "1".

(5) PIPEB_RE2 (PIPE2 Buffer Ready Interrupt Enable) Bits (b2)

This bit select whether to set the INTR bit of Interrupt Status Register 0 to "1" or not when the PIPEB_RDY2 bit of the Interrupt Status Register 1 is set to "1".

(6) PIPEB_RE1 (PIPE1 Buffer Ready Interrupt Enable) Bits (b1)

This bit select whether to set the INTR bit of Interrupt Status Register 0 to "1" or not when the PIPEB_RDY1 bit of the Interrupt Status Register 1 is set to "1".

(7) DCP_RE (DCP_FIFO Buffer Ready Interrupt Enable) Bit (b0)

This bit selects whether to set the INTR bit of Interrupt Status Register 0 to "1" or not when the DCP_RDY bit of the Interrupt Status Register 1 is set to "1".

2.22 INT Pin Configuration Register 3

■ INT Pin Configuration Register 3 (INTPinCfg3) <Address: H'48>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	PIPEB_NRE6 0 0 -	PIPEB_NRE5 0 0 -	PIPEB_NRE4 0 0 -	PIPEB_NRE3 0 0 -	PIPEB_NRE2 0 0 -	PIPEB_NRE1 0 0 -	DCP_NRE 0 0 -

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: ->

b	Bit name	Function	R	W
15~7	Reserved. Set it to "0".		"0"	"0"
6	PIPEB_NRE6 PIPE6 Buffer Not Ready Interrupt Enable	0: Disable the INTN bit set 1: Enable the INTN bit set	O	O
5	PIPEB_NRE5 PIPE5 Buffer Not Ready Interrupt Enable	0: Disable the INTN bit set 1: Enable the INTN bit set	O	O
4	PIPEB_NRE4 PIPE4 Buffer Not Ready Interrupt Enable	0: Disable the INTN bit set 1: Enable the INTN bit set	O	O
3	PIPEB_NRE3 PIPE3 Buffer Not Ready Interrupt Enable	0: Disable the INTN bit set 1: Enable the INTN bit set	O	O
2	PIPEB_NRE2 PIPE2 Buffer Not Ready Interrupt Enable	0: Disable the INTN bit set 1: Enable the INTN bit set	O	O
1	PIPEB_NRE1 PIPE1 Buffer Not Ready Interrupt Enable	0: Disable the INTN bit set 1: Enable the INTN bit set	O	O
0	DCP_NRE DCP_FIFO Buffer Not Ready Interrupt Enable	0: Disable the INTN bit set 1: Enable the INTN bit set	O	O

(1) PIPEB_NRE6 (PIPE6 Buffer Not Ready Interrupt Enable) Bits (b6)

These bits select whether to set the INTN bit of Interrupt Status Register 0 to "1" or not when the PIPEB_NRDY6 bit of the Interrupt Status Register 2 is set to "1".

(2) PIPEB_NRE5 (PIPE5 Buffer Not Ready Interrupt Enable) Bits (b5)

These bits select whether to set the INTN bit of Interrupt Status Register 0 to "1" or not when the PIPEB_NRDY5 bit of the Interrupt Status Register 2 is set to "1".

(3) PIPEB_NRE4 (PIPE4 Buffer Not Ready Interrupt Enable) Bits (b4)

These bits select whether to set the INTN bit of Interrupt Status Register 0 to "1" or not when the PIPEB_NRDY4 bit of the Interrupt Status Register 2 is set to "1".

(4) PIPEB_NRE3 (PIPE3 Buffer Not Ready Interrupt Enable) Bits (b3)

These bits select whether to set the INTN bit of Interrupt Status Register 0 to "1" or not when the PIPEB_NRDY3 bit of the Interrupt Status Register 2 is set to "1".

(5) PIPEB_NRE2 (PIPE2 Buffer Not Ready Interrupt Enable) Bits (b2)

These bits select whether to set the INTN bit of Interrupt Status Register 0 to "1" or not when the PIPEB_NRDY2 bit of the Interrupt Status Register 2 is set to "1".

(6) PIPEB_NRE1 (PIPE1 Buffer Not Ready Interrupt Enable) Bits (b1)

These bits select whether to set the INTN bit of Interrupt Status Register 0 to "1" or not when the PIPEB_NRDY1 bit of the Interrupt Status Register 2 is set to "1".

(7) DCP_NRE (DCP_FIFO Buffer Not Ready Interrupt Enable) Bit (b0)

This bit selects whether to set the INTN bit of Interrupt Status Register 0 to "1" or not when the DCP _NRDY bit of the Interrupt Status Register 2 is set to "1".

2.23 INT Pin Configuration Register 4

■ INT Pin Configuration Register 4 (INTPinCfg4) <Address: H'4C>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	PIPEB_EMPE6 0 0 -	PIPEB_EMPE5 0 0 -	PIPEB_EMPE4 0 0 -	PIPEB_EMPE3 0 0 -	PIPEB_EMPE2 0 0 -	PIPEB_EMPE1 0 0 -	DCP_EMPE 0 0 -

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: ->

b	Bit name	Function	R	W
15~7	Reserved. Set it to "0".		"0"	"0"
6	PIPEB_EMPE6 PIPE6 Buffer Empty/Size-Error Interrupt Enable	0: Disable the BEMP bit set 1: Enable the BEMP bit set	O	O
5	PIPEB_EMPE5 PIPE5 Buffer Empty/Size-Error Interrupt Enable	0: Disable the BEMP bit set 1: Enable the BEMP bit set	O	O
4	PIPEB_EMPE4 PIPE4 Buffer Empty/Size-Error Interrupt Enable	0: Disable the BEMP bit set 1: Enable the BEMP bit set	O	O
3	PIPEB_EMPE3 PIPE3 Buffer Empty/Size-Error Interrupt Enable	0: Disable the BEMP bit set 1: Enable the BEMP bit set	O	O
2	PIPEB_EMPE2 PIPE2 Buffer Empty/Size-Error Interrupt Enable	0: Disable the BEMP bit set 1: Enable the BEMP bit set	O	O
1	PIPEB_EMPE1 PIPE1 Buffer Empty/Size-Error Interrupt Enable	0: Disable the BEMP bit set 1: Enable the BEMP bit set	O	O
0	DCP_EMPE DCP_FIFO Buffer Empty/Size-Error Interrupt Enable	0: Disable the BEMP bit set 1: Enable the BEMP bit set	O	O

(1) PIPEB_EMPE6 (PIPE6 Buffer Empty/Size Error Interrupt Enable) Bits (b6)

These bits select whether to set the BEMP bit of Interrupt Status Register 0 to "1" or not when the PIPEB_EMP_OVR6 bit of the Interrupt Status Register 3 is set to "1".

(2) PIPEB_EMPE5 (PIPE5 Buffer Empty/Size Error Interrupt Enable) Bits (b5)

These bits select whether to set the BEMP bit of Interrupt Status Register 0 to "1" or not when the PIPEB_EMP_OVR5 bit of the Interrupt Status Register 3 is set to "1".

(3) PIPEB_EMPE4 (PIPE4 Buffer Empty/Size Error Interrupt Enable) Bits (b4)

These bits select whether to set the BEMP bit of Interrupt Status Register 0 to "1" or not when the PIPEB_EMP_OVR4 bit of the Interrupt Status Register 3 is set to "1".

(4) PIPEB_EMPE3 (PIPE3 Buffer Empty/Size Error Interrupt Enable) Bits (b3)

These bits select whether to set the BEMP bit of Interrupt Status Register 0 to "1" or not when the PIPEB_EMP_OVR3 bit of the Interrupt Status Register 3 is set to "1".

(5) PIPEB_EMPE2 (PIPE2 Buffer Empty/Size Error Interrupt Enable) Bits (b2)

These bits select whether to set the BEMP bit of Interrupt Status Register 0 to "1" or not when the PIPEB_EMP_OVR2 bit of the Interrupt Status Register 3 is set to "1".

(6) PIPEB_EMPE1 (PIPE1 Buffer Empty/Size Error Interrupt Enable) Bits (b1)

These bits select whether to set the BEMP bit of Interrupt Status Register 0 to "1" or not when the PIPEB_EMP_OVR1 bit of the Interrupt Status Register 3 is set to "1".

(7) DCP_EMPE (DCP_FIFO Buffer Empty/Size Error Interrupt Enable) Bit (b0)

This bit selects whether to set the BEMP bit of Interrupt Status Register 0 to "1" or not when the DCP_EMP_OVR bit of the Interrupt Status Register 3 is set to "1".

2.24 Interrupt Status Register 0

■ Interrupt Status Register 0 (INTStatus0) <Address: H'60>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
VBUSINT	RESM		DVST	CTRT	BEMP	INTN	INTR	VBUSSTS	DVSQ [2:0]			VALID	CTSQ [2:0]		
0	0	0	0	0	0	0	0	?	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	?	0	0	0	0	0	0	0
-	-	-	1	-	-	-	-	-	0	0	1	-	-	-	-

<H/W reset: B'0000 0000 ?000 0000>
<S/W reset: B'0000 0000 ?000 0000>
<USB bus reset: B'---1 ---- -001 ---->

b	Bit name	Function	R	W
15	VBUSINT VBUS Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid when internal clock is supplied (Ignored when written) Cancel interrupt clear status when internal clock is not supplied	○	○
14	RESM Resume Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid when internal clock is supplied (Ignored when written) Cancel interrupt clear status when internal clock is not supplied	○	○
13	Reserved. Set it to "0".		"0"	"0"
12	DVST Device State Transition Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○
11	CTRT Control Transfer Stage Transition Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○
10	BEMP PIPE Buffer Empty/Size Error Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write Invalid (Ignored when written)	○	-
9	INTN PIPE Buffer Not Ready Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write Invalid (Ignored when written)	○	-
8	INTR PIPE Buffer Ready Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write Invalid (Ignored when written)	○	-

b	Bit name	Function	R	W
7	VBUSSTS VBUS Level Port	• Read 0: Low input 1: High input • Write Invalid (Ignored when written)	○	-
6~4	DVSQ [2:0] Device State	• Read 000: Powered state 001: Default state 010: Address state 011: Configured state 1xx: Suspended state • Write Invalid (Ignored when written)	○	-
3	VALID Setup Packet Detect	• Read 0: No detection 1: Receiving the setup packet • Write 0: Clear this VALID bit 1: Invalid (Ignored when written)	○	○
2~0	CTSQ [2:0] Control Transfer Stage	• Read 000: Idle or setup stage 001: Control read transfer data stage 010: Control read transfer status stage 011: Control write transfer data stage 100: Control write transfer status stage 101: Control write no data transfer status stage 110: Control transfer sequence error 111: Reserved • Write Invalid (Ignored when written)	○	○

Note: x is an optional value.

(1) VBUSINT (VBUS Interrupt) Bit (b15)

This bit indicates the change of the VBUS input.

This bit is set to "1" when the VBUS input changes (from Low to High or from High to Low). This bit can be set even while the internal clock is not supplied (SCLK bit of USB Transceiver Control Register 0 is "0".).

This bit is cleared to "0" by writing "0". In case the internal clock is not supplied (when the SCKE bit of USB Transceiver Control Register 0 is "0"), it is necessary to write "1" after writing "0".

(2) RESM (Resume Interrupt) Bit (b14)

This bit is set to "1" when the USB bus state is changed from suspended (DVST bits = "1xx") to J state->K state or J State->"SE0". This bit can be set even while the internal clock is not supplied (SCLK bit of USB Transceiver Control Register 0 is "0".).

This bit is cleared to "0" by writing "0". In case the internal clock is not supplied (when the SCKE bit of USB Transceiver Control Register 0 is set to "0"), it is necessary to write "1" after writing "0".

(3) DVST (Device State Transition Interrupt) Bit (b12)

This bit indicates the transition of the device state.

The device state transition interrupt includes the following four factors:

USB reset detect

SET_ADDRESS execute

SET_CONFIGURATION execute

Suspend detect

These four factors can be individually enable/disable.

This bit is cleared to "0" by writing "0". This bit is not cleared when the internal clock (SCLK) is not supplied.

Writing "1" to this bit has no affect.

(4) CTRT (Control Transfer Stage Transition Interrupt) Bit (b11)

This bit indicates the transition of stage in control transfers.
The control transfer stage transition interrupt includes the following fifth factors:
Setup stage complete
Control write transfer status stage transition
Control read transfer status stage transition
Control transfer complete
Control transfer sequence error
These five factors can be individually enable/disable, excepting the setup stage complete.
This bit is cleared to "0" by writing "0". This bit is not cleared when the internal clock (SCLK) is not supplied.
Writing "1" to this bit has no affect.

(5) BEMP (PIPE Buffer Empty/Size Error Interrupt) Bit (b10)

This bit indicates the occurrence of buffer empty or buffer size over error.
When either the PIPEB_EMP_OVR [6:1] bits or the DCP_EMP_OVR bit of the Interrupt Status Register 3 is set to "1", this bit is set to "1".
This bit is cleared by clearing all the bits of the Interrupt Status Register 3.

(6) INTN (PIPE Buffer Not Ready Interrupt) Bit (b9)

This bit indicates the NAK has been responded to the host because of the buffer not ready state.
When either the PIPEB_ NRDY [6:1] bits or the DCP_ NRDY bit of the Interrupt Status Register 2 is set to "1", this bit is set to "1".
This bit is cleared by clearing all the bits of the Interrupt Status Register 2.

(7) INTR (PIPE Buffer Ready Interrupt) Bit (b8)

This bit indicates the buffer ready state (that can be read/write).
When either the PIPEB_ RDY [6:1] bits or the DCP_ RDY bit of the Interrupt Status Register 1 is set to "1", this bit is set to "1".
This bit is cleared by clearing all the bits of the Interrupt Status Register 1.

(8) VBUSSTS (VBUS Level Port) Bit (b7)

This bit indicates the VBUS pin state.
When this bit changes, the VBUSINT bit is set to "1". This bit is capable of reading the correct value even if the internal clock (SCLK) is not supplied.
As this bit directly reflects the status of the VBUS pin, the processing of reading this bit two or three times to filter the chattering is required when executing the USB attach/detach processing by using this bit value.

(9) DVSQ [2:0] (Device State) Bits (b6-b4)

These bits indicate the present device states.
The device state conforms to description concerning the device state in chapter 9 of the Universal Serial Bus Specification Revision 2.0.
The state after hardware resetting is the Powered state.
The state after software resetting is the Powered state.
The state after USB resetting is the Default state.
Execution of the SET_ADDRESS (Address !="0") brings transition into the address state, while execution of the SET_ADDRESS (Address="0") brings transition into the default state.
Execution of the SET_CONFIGURATION (Configuration !="0") brings transition into the configured state, while execution of the SET_CONFIGURATION (Configuration="0")" brings transition into the address state.
Detection of suspend brings transition into the suspend state.

(10) VALID (Setup Packet Detect) Bit (b3)

This bit indicates that the setup packet has been received.
When the setup packet is completely received, this bit is set to "1". The interrupt does not occur with this bit.
This bit is cleared to "0" by writing "0". This bit is not cleared when the internal clock (SCLK) is not supplied.
Writing "1" to this bit has no affect.
No writing is enabled to the PID [1:0] bits of the DCP Control Register while this bit is "1".

(11) CTSQ [2:0] (Control Transfer Stage) Bits (b2-b0)

These bits indicate the present stage in the control transfer.

Note for clearing the VBUSINT/RESM/SOFR/DVST/CTST status bits:

In order to continuously clear status bits while the VBUSINT/RESM/SOFR/DVST/CTST status bits are set to "1" by being multiplexed, the access cycle time of 100ns or more is required from clear to the next clear. For example, where both the DVST status bit and the CTST status bit are simultaneously set, the access cycle required from when "0" is written to the DVST bit to when "0" is written until the CTST bit is 100ns or more. Also at this time, it is able to clear the DVST bit and the CTST bit at the same time.

2.25 Interrupt Status Register 1

■ Interrupt Status Register 1 (INTStatus1) <Address: H'64>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	PIPEB_RDY6 0 0 -	PIPEB_RDY5 0 0 -	PIPEB_RDY4 0 0 -	PIPEB_RDY3 0 0 -	PIPEB_RDY2 0 0 -	PIPEB_RDY1 0 0 -	DCP_RDY 0 0 -

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: ->

b	Bit name	Function	R	W
15~7	Reserved. Set it to "0".		"0"	"0"
6	PIPEB_RDY6 PIPE6 Buffer Ready Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○
5	PIPEB_RDY5 PIPE5 Buffer Ready Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○
4	PIPEB_RDY4 PIPE4 Buffer Ready Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○
3	PIPEB_RDY3 PIPE3 Buffer Ready Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○
2	PIPEB_RDY2 PIPE2 Buffer Ready Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○
1	PIPEB_RDY1 PIPE1 Buffer Ready Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○
0	DCP_RDY Default Control PIPE Buffer Ready Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○

(1) PIPEB_RDY6 (PIPE6 Buffer Ready Interrupt) Bits (b6)

This bit indicates that PIPE6 buffer is kept in read ready state.
This bit is cleared to "0" by writing "0". This bit is not cleared when the internal clock is not supplied (SCLK bit of USB Transceiver Control Register 0 is "0".).
Writing "1" to this bit has no affect.

(2) PIPEB_RDY5 (PIPE5 Buffer Ready Interrupt) Bits (b5)

This bit indicates that PIPE5 buffer is kept in read ready state.
This bit is cleared to "0" by writing "0". This bit is not cleared when the internal clock is not supplied (SCLK bit of USB Transceiver Control Register 0 is "0".).
Writing "1" to this bit has no affect.

(3) PIPEB_RDY4 (PIPE4 Buffer Ready Interrupt) Bits (b4)

This bit indicates that PIPE4 buffer is kept in read ready state.
This bit is cleared to "0" by writing "0". This bit is not cleared when the internal clock is not supplied (SCLK bit of USB Transceiver Control Register 0 is "0".).
Writing "1" to this bit has no affect.

(4) PIPEB_RDY3 (PIPE3 Buffer Ready Interrupt) Bits (b3)

This bit indicates that PIPE3 buffer is kept in read ready state.
This bit is cleared to "0" by writing "0". This bit is not cleared when the internal clock is not supplied (SCLK bit of USB Transceiver Control Register 0 is "0".).
Writing "1" to this bit has no affect.

(5) PIPEB_RDY2 (PIPE2 Buffer Ready Interrupt) Bits (b2)

This bit indicates that PIPE2 buffer is kept in read ready state.
This bit is cleared to "0" by writing "0". This bit is not cleared when the internal clock is not supplied (SCLK bit of USB Transceiver Control Register 0 is "0".).
Writing "1" to this bit has no affect.

(6) PIPEB_RDY1 (PIPE1 Buffer Ready Interrupt) Bits (b1)

This bit indicates that PIPE1 buffer is kept in read ready state.
This bit is cleared to "0" by writing "0". This bit is not cleared when the internal clock is not supplied (SCLK bit of USB Transceiver Control Register 0 is "0".).
Writing "1" to this bit has no affect.

(7) DCP_RDY (Default Control PIPE Buffer Ready Interrupt) Bit (b0)

This bit indicates that the default control PIPE buffer is kept in read ready state.
When the data packet has been received properly in the control write transfer, this bit is set to "1". When the transmission FIFO buffer is kept in write ready state in the control read transfer, this bit is not set to "1". Use default control PIPE buffer empty/size-error interrupt to confirm the completion of the control read transfer.
This bit is cleared to "0" by writing "0". This bit is not cleared when the internal clock is not supplied (SCLK bit of USB Transceiver Control Register 0 is "0".).
Writing "1" to this bit has no affect.

Note for clearing the buffer ready interrupt (PIPEB_RDY6-PIPEB_RDY1/DCP_RDY) status bits:

In order to continuously clear status bits while the PIPEB_RDY6-PIPEB_RDY1/DCP_RDY status bits are set to "1" by being multiplexed, the access cycle time of 100ns or more is required from clear to the next clear. For example, where both the PIPEB_RDY1 status bit and the PIPEB_RDY2 status bit are simultaneously set, the access cycle required from when "0" is written to the PIPEB_RDY1 bit until when "0" is written to the PIPEB_RDY2 bit is 100ns or more. Also at this time, it is able to clear the PIPEB_RDY1 bit and the PIPEB_RDY2 bit at the same time.

2.26 Interrupt Status Register 2

■ Interrupt Status Register 2 (INTStatus2) <Address: H'68>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	PIPEB_NRDY6 0 0 -	PIPEB_NRDY5 0 0 -	PIPEB_NRDY4 0 0 -	PIPEB_NRDY3 0 0 -	PIPEB_NRDY2 0 0 -	PIPEB_NRDY1 0 0 -	DCP_NRDY 0 0 -

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: ->

b	Bit name	Function	R	W
15~7	Reserved. Set it to "0".		"0"	"0"
6	PIPEB_NRDY6 PIPE6 Buffer Not Ready Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○
5	PIPEB_NRDY5 PIPE5 Buffer Not Ready Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○
4	PIPEB_NRDY4 PIPE4 Buffer Not Ready Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○
3	PIPEB_NRDY3 PIPE3 Buffer Not Ready Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○
2	PIPEB_NRDY2 PIPE2 Buffer Not Ready Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○
1	PIPEB_NRDY1 PIPE1 Buffer Not Ready Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○
0	DCP_NRDY Default Control PIPE Buffer Not Ready Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○

(1) PIPEB_NRDY6 (PIPE6 Buffer Not Ready Interrupt) Bits (b6)

This bit is set to “1” when IN token/OUT token is received with PIPE6 buffer at not ready state.
The not ready status means the state in which a NAK response has been issued to the host on disabling of transmit/receive while the PID [1:0] bits of PIPE 6 Control Register are set to “01”(BUF).
This bit is cleared to “0” by writing “0”. This bit is not cleared when the internal clock is not supplied (SCLK bit of USB Transceiver Control Register 0 is “0”.).
Writing “1” to these bits has no affect.

(2) PIPEB_NRDY5 (PIPE5 Buffer Not Ready Interrupt) Bits (b5)

This bit is set to “1” when IN token/OUT token is received with PIPE5 buffer at not ready state.
The not ready status means the state in which a NAK response has been issued to the host on disabling of transmit/receive while the PID [1:0] bits of PIPE 5 Control Register are set to “01”(BUF).
This bit is cleared to “0” by writing “0”. This bit is not cleared when the internal clock is not supplied (SCLK bit of USB Transceiver Control Register 0 is “0”.).
Writing “1” to these bits has no affect.

(3) PIPEB_NRDY4 (PIPE4 Buffer Not Ready Interrupt) Bits (b4)

This bit is set to “1” when IN token/OUT token is received with PIPE4 buffer at not ready state.
The not ready status means the state in which a NAK response has been issued to the host on disabling of transmit/receive while the PID [1:0] bits of PIPE4 Control Register are set to “01”(BUF).
This bit is cleared to “0” by writing “0”. This bit is not cleared when the internal clock is not supplied (SCLK bit of USB Transceiver Control Register 0 is “0”.).
Writing “1” to these bits has no affect.

(4) PIPEB_NRDY3 (PIPE3 Buffer Not Ready Interrupt) Bits (b3)

This bit is set to “1” when IN token/OUT token is received with PIPE3 buffer at not ready state.
The not ready status means the state in which a NAK response has been issued to the host on disabling of transmit/receive while the PID [1:0] bits of PIPE 3 Control Register are set to “01”(BUF).
This bit is cleared to “0” by writing “0”. This bit is not cleared when the internal clock is not supplied (SCLK bit of USB Transceiver Control Register 0 is “0”.).
Writing “1” to these bits has no affect.

(5) PIPEB_NRDY2 (PIPE2 Buffer Not Ready Interrupt) Bits (b2)

This bit is set to “1” when IN token/OUT token is received with PIPE2 buffer at not ready state.
The not ready status means the state in which a NAK response has been issued to the host on disabling of transmit/receive while the PID [1:0] bits of PIPE 2 Control Register are set to “01”(BUF).
This bit is cleared to “0” by writing “0”. This bit is not cleared when the internal clock is not supplied (SCLK bit of USB Transceiver Control Register 0 is “0”.).
Writing “1” to these bits has no affect.

(6) PIPEB_NRDY1 (PIPE1 Buffer Not Ready Interrupt) Bits (b1)

This bit is set to “1” when IN token/OUT token is received with PIPE1 buffer at not ready state.
The not ready status means the state in which a NAK response has been issued to the host on disabling of transmit/receive while the PID [1:0] bits of PIPE 1 Control Register are set to “01”(BUF).
This bit is cleared to “0” by writing “0”. This bit is not cleared when the internal clock is not supplied (SCLK bit of USB Transceiver Control Register 0 is “0”.).
Writing “1” to these bits has no affect.

(2) DCP_NRDY (Default Control PIPE Buffer Not Ready Interrupt) Bit (b0)

This bit is set to “1” when IN token/OUT token is received with DCP buffer at not ready state.
The not ready status means the state in which an NAK response has been issued to the host on disabling of transmit/receive while the PID [1:0] bits of DCP Control Register are set to “01” (BUF).
This bit is not set to “1” by the NAK response in the status stage of the control transfer.
This bit is cleared to “0” by writing “0”. This bit is not cleared when the internal clock is not supplied (SCLK bit of USB Transceiver Control Register 0 is “0”.).
Writing “1” to this bit has no affect.

Note for clearing the buffer not ready interrupt (PIPEB_NRDY6-PIPEB_NRDY1/DCP_NRDY) status bits:

In order to continuously clear status bits while the PIPEB_NRDY6-PIPEB_NRDY1/DCP_NRDY status bits are set to "1" by being multiplexed, the access cycle time of 100ns or more is required from clear to the next clear. For example, where both the PIPEB_NRDY1 status bit and the PIPEB_NRDY2 status bit are simultaneously set, the access cycle required from when "0" is written to the PIPEB_NRDY1 bit until when "0" is written to the PIPEB_NRDY2 bit is 100ns or more. Also at this time, it is enable to clear the PIPEB_NRDY1 bit and the PIPEB_NRDY2 bit at the same time.

2.27 Interrupt Status Register 3

■ Interrupt Status Register 3 (INTStatus3) <Address: H'6C>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	PIPEB_EMP _OVR6 0 0 -	PIPEB_EMP _OVR5 0 0 -	PIPEB_EMP _OVR4 0 0 -	PIPEB_EMP _OVR3 0 0 -	PIPEB_EMP _OVR2 0 0 -	PIPEB_EMP _OVR1 0 0 -	DCP_EMP_ OVR 0 0 -

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: ->

b	Bit name	Function	R	W
15~7	Reserved. Set it to "0".		"0"	"0"
6	PIPEB_EMP_OVR6 PIPE6 Buffer Empty/Size Error Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○
5	PIPEB_EMP_OVR5 PIPE5 Buffer Empty/Size Error Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○
4	PIPEB_EMP_OVR4 PIPE4 Buffer Empty/Size Error Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○
3	PIPEB_EMP_OVR3 PIPE3 Buffer Empty/Size Error Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○
2	PIPEB_EMP_OVR2 PIPE2 Buffer Empty/Size Error Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○
1	PIPEB_EMP_OVR1 PIPE1 Buffer Empty/Size Error Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○
0	DCP_EMP_OVR Default Control PIPE Buffer Empty/Size- Error Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○

(1) PIPEB_EMP_OVR6 (PIPE6 Buffer Empty/Size-Error Interrupt) Bits (b6)

This bit indicates that the received data size exceeds the maximum packet size or that the buffers of PIPE6 are empty.

(1) When the transfer direction IN:
When all data stored in the buffers of PIPE6 have been transmitted (buffer empty), this bit is set to "1".

(2) When the transfer direction OUT:
When the data packet size which has been received has exceeded max packet size of PIPE6 (size over detect), this bit is set to "1". The PID [1:0] bits of the PIPE 6 Control Register is set to "1X" (STALL).

This bit is cleared to "0" by writing "0". This bit is not cleared when the internal clock is not supplied (SCLK bit of USB Transceiver Control Register 0 is "0".).
Writing "1" to these bits has no affect.

(2) PIPEB_EMP_OVR5 (PIPE5 Buffer Empty/Size-Error Interrupt) Bits (b5)

This bit indicates that the received data size exceeds the maximum packet size or that the buffers of PIPE5 are empty.

(1) When the transfer direction IN:
When all data stored in the buffers of PIPE5 have been transmitted (buffer empty), this bit is set to "1".

(2) When the transfer direction OUT:
When the data packet size which has been received has exceeded max packet size of PIPE5 (size over detect), this bit is set to "1". The PID [1:0] bits of the PIPE 5 Control Register is set to "1X" (STALL).

This bit is cleared to "0" by writing "0". This bit is not cleared when the internal clock is not supplied (SCLK bit of USB Transceiver Control Register 0 is "0".).
Writing "1" to these bits has no affect.

(3) PIPEB_EMP_OVR4 (PIPE4 Buffer Empty/Size-Error Interrupt) Bits (b4)

This bit indicates that the received data size exceeds the maximum packet size or that the buffers of PIPE4 are empty.

(1) When the transfer direction IN:
When all data stored in the buffers of PIPE4 have been transmitted (buffer empty), this bit is set to "1".

(2) When the transfer direction OUT:
When the data packet size which has been received has exceeded max packet size of PIPE4 (size over detect), this bit is set to "1". The PID [1:0] bits of the PIPE 4 Control Register is set to "1X" (STALL).

This bit is cleared to "0" by writing "0". This bit is not cleared when the internal clock is not supplied (SCLK bit of USB Transceiver Control Register 0 is "0".).
Writing "1" to these bits has no affect.

(4) PIPEB_EMP_OVR3 (PIPE3 Buffer Empty/Size-Error Interrupt) Bits (b3)

This bit indicates that the received data size exceeds the maximum packet size or that the buffers of PIPE3 are empty.

(1) When the transfer direction IN:
When all data stored in the buffers of PIPE3 have been transmitted (buffer empty), this bit is set to "1".

(2) When the transfer direction OUT:
When the data packet size which has been received has exceeded max packet size of PIPE3 (size over detect), this bit is set to "1". The PID [1:0] bits of the PIPE 3 Control Register is set to "1X" (STALL).

This bit is cleared to "0" by writing "0". This bit is not cleared when the internal clock is not supplied (SCLK bit of USB Transceiver Control Register 0 is "0".).
Writing "1" to these bits has no affect.

(5) PIPEB_EMP_OVR2 (PIPE2 Buffer Empty/Size-Error Interrupt) Bits (b2)

This bit indicates that the received data size exceeds the maximum packet size or that the buffers of PIPE2 are empty.

(1) When the transfer direction IN:
When all data stored in the buffers of PIPE2 have been transmitted (buffer empty), this bit is set to "1".

(2) When the transfer direction OUT:
When the data packet size which has been received has exceeded max packet size of PIPE2 (size over detect), this bit is set to "1". The PID [1:0] bits of the PIPE 2 Control Register is set to "1X" (STALL).

This bit is cleared to "0" by writing "0". This bit is not cleared when the internal clock is not supplied (SCLK bit of USB Transceiver Control Register 0 is "0".).
Writing "1" to these bits has no affect.

(6) PIPEB_EMP_OVR1 (PIPE1 Buffer Empty/Size-Error Interrupt) Bits (b1)

This bit indicates that the received data size exceeds the maximum packet size or that the buffers of PIPE1 are empty.

(1) When the transfer direction IN:
When all data stored in the buffers of PIPE1 have been transmitted (buffer empty), this bit is set to "1".

(2) When the transfer direction OUT:
When the data packet size which has been received has exceeded max packet size of PIPE1 (size over detect), this bit is set to "1". The PID [1:0] bits of the PIPE 1 Control Register is set to "1X" (STALL).

This bit is cleared to "0" by writing "0". This bit is not cleared when the internal clock is not supplied (SCLK bit of USB Transceiver Control Register 0 is "0".).
Writing "1" to these bits has no affect.

(7) DCP_EMP_OVR (Default Control PIPE Buffer Empty/Size Error Interrupt) Bit (b0)

This bit indicates that the received data size exceeds the maximum packet size or that the transmit buffers of the DCP is empty.

(1) When the transfer direction IN:
When all data stored in the transmit buffers of the DCP have been transmitted (buffer empty), this bit is set to "1".

(2) When the transfer direction OUT:
When the data packet size having been received has exceeded the preset value of the DCP_MXPS [6:0] of the DCP Configuration Register 2 (size over detect), this bit is set to "1". At this time, the PID [1:0] bits of the DCP Control Register are set to "1X" (STALL).

This bit is cleared to "0" by writing "0". This bit is not cleared when the internal clock is not supplied (SCLK bit of USB Transceiver Control Register 0 is "0".).
Writing "1" to this bit has no affect.

Note for clearing the buffer empty interrupt (PIPEB_EMP_OVR6-PIPEB_EMP_OVR1/DCP_EMP_OVR) status bits:

In order to continuously clear status bits while the PIPEB_EMP_OVR6-PIPEB_EMP_OVR1/DCP_EMP_OVR status bits are set to "1" by being multiplexed, the access cycle time of 100ns or more is required from clear to the next clear.

For example, where both the PIPEB_EMP_OVR1 status bit and the PIPEB_EMP_OVR2 status bit are simultaneously set, the access cycle required from when "0" is written to the PIPEB_EMP_OVR1 bit until when "0" is written to the PIPEB_EMP_OVR2 bit is 100ns or more. Also at this time, it is able to clear the PIPEB_EMP_OVR1 bit and the PIPEB_EMP_OVR2 bit at the same time.

2.28 USB Address Register

■ USB Address Register (USBAddress) <Address: H'74>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
									USB_Addr [6:0]						
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: H'0000>

b	Bit name	Function	R	W
15~7	Reserved. Set it to "0".		"0"	"0"
6~0	USB_Addr [6:0] USB Address	• Read USB address assigned by the host • Write Invalid (Ignored when written)	○	-

(1) USB_Addr [6:0] (USB Address) Bits (b6-b0)

These bits store the USB address which has been assigned the SET_ADDRESS device request by the host.

These bits automatically respond to the SET_ADDRESS device request and they are renewed to the new USB address on completion of the control transfer status stage.

2.29 USB Request Register 0

■ USB Request Register 0 (USBReq0) <Address: H'78>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
bRequest [7:0]								bmRequestType [7:0]							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: H'0000>

b	Bit name	Function	R	W
15~8	bRequest [7:0] Request	• Read Request received in the setup stage • Write Invalid (Ignored when written)	○	-
7~0	bmRequestType [7:0] Request Type	• Read Request type received in the setup stage • Write Invalid (Ignored when written)	○	-

(1) bRequest [7:0] (Request) Bits (b15-b8)

These bits store the bRequest of the device request received in the setup stage of the control transfer.

(2) bmRequestType [7:0] (Request Type) Bits (b7-b0)

These bits store the bmRequestType of the device request received in the setup stage of the control transfer.

2.30 USB Request Register 1

■ USB Request Register 1 (USBReq1) <Address: H'7A>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
wValue [15:0]															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: H'0000>

b	Bit name	Function	R	W
15~0	wValue [15:0] Value	• Read Value received in the setup stage • Write Invalid (Ignored when written)	○	-

(1) wValue [15:0] (Value) Bits (b15-b0)

These bits store the wValue of the device request received in the setup stage of the control transfer.

2.31 USB Request Register 2

■ USB Request Register 2 (USBReq2) <Address: H'7C>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
wIndex [15:0]															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: H'0000>

b	Bit name	Function	R	W
15~0	wIndex [15:0] Index	• Read Index received in the setup stage • Write Invalid (Ignored when written)	○	-

(1) wIndex [15:0] (Index) Bits (b15-b0)

These bits store the wIndex of the device request received in the setup stage of the control transfer.

2.32 USB Request Register 3

■ USB Request Register 2 (USBReq3) <Address: H'7E>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
wLength [15:0]															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: H'0000>

b	Bit name	Function	R	W
15~0	wLength [15:0] Length	• Read Length received in the setup stage • Write Invalid (Ignored when written)	○	-

(1) wLength [15:0] (Length) Bits (b15-b0)

These bits store the wLength of the device request received in the setup stage of the control transfer.

2.33 DCP Configuration Register 1

■ DCP Configuration Register 1 (DCPCfg1) <Address: H'82>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
0	0	0	0	0	0	0	CNTMD	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: ->

b	Bit name	Function	R	W
15~9	Reserved. Set it to "0".		"0"	"0"
8	CNTMD Continuous Transmit/Receive Mode	0: Non-continuous transmit/receive mode 1: Continuous transmit/receive mode	○	○
7~0	Reserved. Set it to "0".		"0"	"0"

(1) CNTMD (Continuous Transmit/Receive Mode) Bits (b8)

These bits set the transmit/receive mode in data stage of the control read/write transfer.

In case of the control read transfer:
CNTMD = "0": Non-continuous transmit mode
The transmit completes under the conditions as follows:
- Transmits the data equivalent to the size set by the DCP_MXPS [6:0] bits of DCP Configuration Register 2 or transmits the short packet by setting the BVAL bit of C_FIFO Port Control Register 1 to "1".

The writing completes under the conditions as follows:
- Writes to the buffer the data equivalent to the size set by the DCP_MXPS [6:0] bits. (BVAL bit changes to "1").
- Writes "1" to the BVAL bit.

CNTMD = "1": Continuous transmit mode
The transmit completes under the conditions as follows:
- Transmits the data equivalent to the size set by the SDLN [8:0] bits of DCP Continuous Transmit Data Length Register or transmits the short packet by setting the BVAL bit to "1".

The writing completes under the conditions as follows:
- Writes to the buffer the data equivalent to the size set by the SDLN [8:0] bits. (BVAL bit changes to "1").
- Writes "1" to the BVAL bit.

In case of the control write transfer:
CNTMD = "0": Non-continuous receive mode. The receive completes by receiving one packet under the condition as follows:
- Receives the data equivalent to the size set by the DCP_MXPS [6:0] bits of DCP Configuration Register 2.
- Receives the short packet.

CNTMD = "1": Continuous receive mode. The receive completes by receiving several packets under the condition as follows:
- Receives the data equivalent to 256 bytes set by buffer size of DCP.
- Receives the short packet.

2.34 DCP Configuration Register 2

■ DCP Configuration Register 2 (DCPCfg2) <Address: H'84>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
									DCP_MXPS [6:0]						
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: ->

b	Bit name	Function	R	W
15~7	Reserved. Set it to "0".		"0"	"0"
6~0	DCP_MXPS [6:0] DCP Maximum Packet Size	Upper limit of the transmit/receive data for one packet transfer (Settable only 8,16,32 and 64)	○	○

(1) DCP_MXPS [6:0] (DCP Maximum Packet Size) Bits (b6-b0)

These bits set the upper limit (byte count) of the transmit/receive data for one packet transfer in data stage.

For these bits, 8, 16, 32 and 64 are available during operation in the Full-Speed mode, and 64 during operation in the Hi-Speed mode. Other values are not permitted.

At the time of transmitting, the data equivalent to the size set by these bits are read from the buffer for transmission. When the buffer does not have the data equivalent to the size set by these bits, the data are transmitted as the short packet.

At the time of receiving, the data equivalent to the size set by these bits are written to the buffer. If the received packet data are larger than the size set by these bits, the DCP_EMP_OVR bit of the Interrupt Status Register 3 is set to "1".

When initializing DCP, be sure to set these bits before setting the PID bits of DCP Control Register to "01". Also, when changing the value of these bits, be sure to set beforehand the PID bits of DCP Control Register to "00" (NAK).

2.35 DCP Control Register

■ DCP Control Register (DCPCtrl) <Address: H'88>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
BSTS							SQCLR				NYETMD		CCPL	PID [1:0]	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: B'---- ---- ---- -000>

b	Bit name	Function	R	W
15	BSTS Control PIPE Buffer Status	0: Disables to read the data of buffer and to write the data to buffer 1: Enables to read the data of buffer and to write the data to buffer	○	-
14~9	Reserved. Set it to "0".		"0"	"0"
8	SQCLR Sequence Toggle Bit Clear	• Write 0: Invalid (Ignored when written) 1: Sequence bit clear	"0"	○
7~5	Reserved. Set it to "0".		"0"	"0"
4	NYETMD NYET Response Mode	0: Automatic response Mode (ACK/NYET is automatically selected.) 1: ACK response only mode (Always with ACK response. No NYET response.)	○	○
3	Reserved. Set it to "0".		"0"	"0"
2	CCPL Control Transfer Completion Enable	0: NAK response in status stage 1: Normal completion response at status stage (ACK response/zero-length packet transmit)	○	○
1~0	PID [1:0] Response PID	00: NAK response 01: BUF response 1x: STALL response	○	○

(1) BSTS (Control PIPE Buffer Status) Bit (b15)

This bit indicates the buffer status of DCP.

When the ISEL bit of C_FIFO Port Control Register 0 is set to "0", this bit indicates the control write (OUT) buffer status. When the ISEL bit is set to "1", this bit indicates the control read (IN) buffer status.

(2) SQCLR (Sequence Toggle Bit Clear) Bit (b8)

This bit clears the sequence bit of DCP and sets the data PID in the data stage to the "DATA1".

Further, the data PID in the setup stage and status stage are controlled by hardware.

The sequence bit is toggled by hardware control in the transfers after the sequence bit is cleared.

With the USB bus reset, the sequence toggle bit is not cleared. Further, with the setup token having been received, the sequence bit is automatically cleared by hardware and the data PID in the data stage is "DATA1".

Writing of "0" to this bit is invalid. This bit is always read "0". Before setting this bit, be sure to set the PID [1:0] bits to "00" (NAK).

Note: To clear two or more sequence toggle bits of the PIPE continuously, the access cycle time of 200ns or more is required from one SQCLR bit of the PIPE access to the next SQCLR bit of the PIPE access. For example, when the sequence toggle bits of both PIPE1 and PIPE2 are cleared, the access cycle required from when "1" is written to the SQCLR bit of PIPE1 to when "1" is written to the SQCLR bit of PIPE2 is 200ns or more.

(3) NYETMD (NYET Response Mode) Bit (b4)

This bit sets the NYET response mode.
0: Automatic response mode (ACK/NYET is automatically selected.)
1: ACK response only mode (Always with ACK response. No NYET response.)
This bit is valid when the PID [1:0] bits are "01"(BUF) in case the control write transfer operated in the Hi-Speed mode. In any other cases, this bit is invalid.
In the automatic response mode, hardware automatically selects an appropriate response PID (NAK/ACK/NYET) according to the buffer statuses below. However, NAK response is executed instead NYET response when a short packet is received.
(1) When the buffer to receive the data packet is the buffer full, the NAK response is executed.
(2) When an empty space existing in the buffer is equal to or more than twice as large as the max packet size before receiving of the data packet, the ACK response is executed.
(3) When an empty space existing in the buffer is less than twice as large as the max packet size before receiving of the data packet, the NYET response is executed.
In the ACK response only mode, the device does not transmit the NYET packet. The ACK/NAK response is executed.

(4) CCPL (Control Transfer Completion Enable) Bit (b2)

This bit controls the status stage of the control transfer.
When this bit is set to "1", the operations below are executed in status stage of the control transfer and notifies the normal completion of the control transfer:
(1) When set to control write transfer, transmits the zero-length packet after receiving IN token if the PID bits are set to "01".
(2) When set to control read transfer, executes the ACK response to the host after receiving the packet following OUT token if the PID bits are set to "01".
When this bit is set to "0", the NAK response is executed to the host after receiving the IN token/OUT token in status stage of the control transfer.
This bit is automatically cleared to "0" by receiving the setup token.

(5) PID [1:0] (Response PID) Bits (b1-b0)

These bits set the PID for response to the host in data/status stage of the control transfer.
In setup stage, the ACK response is always executed independent of these bits. Further, when receiving the setup token, these bits are automatically set to the NAK response ("00") by hardware.
When the VALID bit is set to"1", writing to these bits are invalid.
00: NAK response
The NAK response is executed independent to buffer status.
01: BUF response
Either one of the ACK response, the NYET response, the NAK response, the DATA0 response, and the DATA1 response is executed according to the value of the NYETMD bit and the sequence toggle bit, and the buffer status.
1x: STALL response
The STALL response is executed independent to buffer status. When data exceeding the max packet size (MXPS) has been received or a sequence error has occurred in the control write transfer, these bits are automatically set to "1x".

2.36 PIPE Configuration Select Register

■ PIPE Configuration Select Register (PipeCfgSel) <Address: H'8C>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
													PIPE_SEL [2:0]		
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: ->

b	Bit name	Function	R	W
15~3	Reserved. Set it to "0".		"0"	"0"
2~0	PIPE_SEL [2:0] PIPE Select PID	Designate the PIPE for access to the configuration register 000: None select 001: Select PIPE1 010: Select PIPE2 011: Select PIPE3 100: Select PIPE4 101: Select PIPE5 110: Select PIPE6 110-111: None select	○	○

(1) PIPE_SEL [2:0] (PIPE Select PID) Bits (b2-b0)

There is a "PIPE Configuration Register" for each PIPE in the internal of M66591. PIPE Configuration Window Register 0 is the window register for these registers.

These bits designate the PIPE for PIPE configuration setting via PIPE Configuration Window Register 0. Refer to Figure 2.4

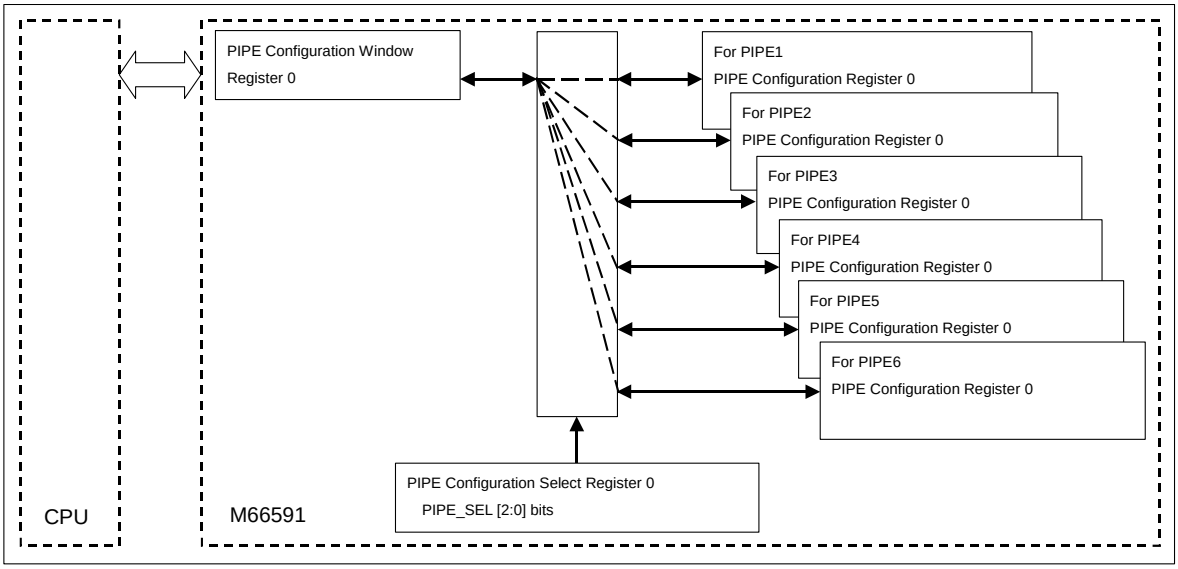


Figure 2.4 The reference of PIPE configuration

2.37 PIPE Configuration Window Register 0

■ PIPE Configuration Window Register 0 (PipeCfgWin0) <Address: H'90>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
PEN		ITMD			BFRE	DBLB	CNTMD				DIR		EP_NUM [2:0]		
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: B'00-- ---- ---- ---->

b	Bit name	Function	R	W
15	PEN PIPE Enable	0: Disable PIPE 1: Enable PIPE	○	○
14	Reserved. Set it to "0".		"0"	"0"
13	ITMD Interrupt Transfer Toggle Mode	0: Enable toggle mode 1: Disable toggle mode This function only can be used for PIPE5 and PIPE6	○	○
12~11	Reserved. Set it to "0".		"0"	"0"
10	BFRE Buffer Ready Interrupt Mode	0: CPU mode 1: DMA mode	○	○
9	DBLB Double Buffer Mode (Bulk Transfer Only)	0: Single buffer mode 1: Double buffer mode	○	○
8	CNTMD Continuous Transmit/Receive Mode	<During operation in Full-Speed mode> 0: Non-continuous transmit/receive mode 1: Continuous transmit/receive mode <During operation in Hi-Speed mode> Set this bit to "1"	○	○
7~5	Reserved. Set it to "0".		"0"	"0"
4	DIR Transfer Direction	0: OUT (Receives data from the host) 1: IN (Transmits data to the host)	○	○
3	Reserved. Set it to "0".		"0"	"0"
2~0	EP_NUM [2:0] Endpoint Number	• Read 000: Not select PIPE 001: EP1 (PIPE1) 010: EP2 (PIPE2) 011: EP3 (PIPE3) 100: EP4 (PIPE4) 101: EP5 (PIPE5) 110: EP6 (PIPE6) Other than those above: Invalid • Write Invalid (Ignored when written)	○	-

(1) PEN (PIPE Enable) Bit (b15)

This bit sets enable/disable for using the PIPE having been selected by the PIPE_SEL [2:0] bits of the PIPE Configuration Select Register.

Before setting this bit, be sure to set the PID [1:0] bits of the PIPE i Control Register (i=1~6) to "00" (NAK).

(2) ITMD (Interrupt Transfer Toggle Mode) Bit (b13)

This bit sets the enable/disable of data resend function at interrupt transfer. This bit is valid only for PIPE5 and PIPE6. The written to this bit is ignored for PIPE1 to PIPE4 which concern the bulk transfer, for which this bit is set to “0”.

When interrupt transfer toggle mode is disabled, the new data is transmitted at the next transmission by toggling the data PID and the buffer, even if the ACK is not received after transmitting the data. In this case, the BVAL bit of C_FIFO Port Control Register 1 is cleared to “0” and the PIPEB _RDY of Interrupt Status Register 1 is set to “1”.

When interrupt transfer toggle mode is enabled, the normal toggle sequence is executed. When the transmission completes normally, the date PID and the buffer get toggled to transmit the next data. In case ACK cannot be received after the data are transmitted, the date PID and the buffer do not get toggled, and the same data in the buffer are resent.

Before setting this bit, be sure to set the PID [1:0] bits of PIPE i Control Register (i=5~6) to “00” (NAK).

(3) BFRE (Buffer Ready Interrupt Mode) Bit (b10)

This bit sets the operation mode for the buffer ready interrupt when the PIPE has been set to OUT.

0:CPU mode

1:DMA mode

For details, refer to “3.3.6 PIPE Buffer Ready Interrupt”.

This bit is valid only for PIPE1 to PIPE4. The written to this bit is ignored for PIPE5 and PIPE6.

Before setting this bit, be sure to set the PID [1:0] bits of the PIPE i Control Register (i=1~4) to “00” (NAK).

(4) DBLB (Double Buffer Mode (Bulk Transfer Only)) Bit (b9)

This bit sets the PIPE to the single buffer mode or double buffer mode.

This bit is valid only for PIPE1 and PIPE2. The written to this bit is ignored for PIPE3 to PIPE6 which concern the single buffer configuration .

Before setting this bit, be sure to set the PID [1:0] bits of the PIPE i Control Register (i=1~2) to “00” (NAK).

(5) CNTMD (Continuous Transmit/Receive Mode) Bit (b8)

This bit sets the transmit/receive mode at the bulk transfer. This bit is valid only for PIPE1 to PIPE4. The written to this bit is ignored for PIPE5 and PIPE6.

During operation in Full-Speed mode

CNTMD = “0”: Non-continuous transmit/receive mode

The transmit completes under any one of the following conditions when setting the PIPE to IN:

- Transmits the data equal to 64 bytes
- Transmits the short packet or transmits the zero-length packet

The writing completes under any one of the following conditions when setting the PIPE to IN:

- Writes to the buffer the data equal to 64 bytes
- Writes “1” to the BVAL bit of the C_FIFO Port Control Register 1.

The receive completes under any one of the following conditions when setting the PIPE to OUT:

- Receives the data equal to 64 bytes
- Receives the short packet or receives the zero-length packet

CNTMD = “1”: Continuous transmit/receive mode

The transmit completes under any one of the following conditions when setting the PIPE to IN:

- The data equal to 64 bytes are automatically transmitted by multiple times and the data equal to 512 bytes are transmitted.
- Transmits the short packet or transmits the zero-length packet

The writing completes under any one of the following conditions when setting the PIPE to IN:

- The numbers of data writing to the buffer is equal to 512 bytes
- Write “1” to the BVAL bit.

The receive completes under any one of the following conditions when setting the PIPE to OUT:

- The data equal to 64 bytes are automatically received by multiple times and the data equal to 512 bytes are received.
- Receives the short packet or receives the zero-length packet
- When the value has been set to the TRCNT [15:0] of the D0_FIFO Port Control Register 3 are correspondent with the number of packet receipts.

Only the non-continuous transmit/receive mode enables to be operated during operation in Hi-Speed mode. In this case, however, this bit needs to be set to “1”.

The transmit completes under any one of the following conditions when setting the PIPE to IN:
- Transmits the data equal to 512 bytes
- Transmits the short packet or transmits the zero-length packet

The writing completes under any one of the following conditions when setting the PIPE to IN:
- Writes to the buffer the data equal to 512 bytes
- Writes “1” to the BVAL bit of the C_FIFO Port Control Register 1.

The receive completes under any one of the following conditions when setting the PIPE to OUT:
- Receives the data equal to 512 bytes
- Receives the short packet or transmits the zero-length packet

Before setting this bit, be sure to set the PID [1:0] bits of the PIPE i Control Register (i=1~4) to “00” (NAK).

(6) DIR (Transfer Direction) Bit (b4)

This bit sets the transfer direction of the PIPE. This bit is valid only for PIPE1 to PIPE4. The written to this bit is ignored for PIPE5 and PIPE6 which concern the IN direction setting.

After switching the transfer direction, clear the buffer by the BCLR bits of the C_FIFO Port Control Register 1 or the D0_FIFO Port Control Register 2.

Before setting this bit, be sure to set the PID [1:0] bits of the PIPE i Control Register (i=1~4) to “00” (NAK).

(7) EP_NUM [2:0] (Endpoint Number) Bits (b2-b0)

These bits read the endpoint number of the PIPE having been set to the PIPE_SEL [2:0] bits of the PIPE Configuration Select Register. The endpoint number is fixed, same as PIPE number.

The endpoint number of PIPE1 is 1 (EP1).
The endpoint number of PIPE2 is 2 (EP2).
The endpoint number of PIPE3 is 3 (EP3).
The endpoint number of PIPE4 is 4 (EP4).
The endpoint number of PIPE5 is 5 (EP5).
The endpoint number of PIPE6 is 6 (EP6).
These bits are read only. Any writing is ignored.

2.38 PIPE i Control Register (i=1~4)

- PIPE 1 Control Register (Pipe1Ctrl) <Address: H'A0>
- PIPE 2 Control Register (Pipe2Ctrl) <Address: H'A2>
- PIPE 3 Control Register (Pipe3Ctrl) <Address: H'A4>
- PIPE 4 Control Register (Pipe4Ctrl) <Address: H'A6>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
BSTS						ACLR	SQCLR				NYETMD			PID [1:0]	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: B'---- ---- ---- --00>

b	Bit name	Function	R	W
15	BSTS Buffer Status	0: Disables to read the data of buffer and to write the data to buffer 1: Enables to read the data of buffer and to write the data to buffer	○	-
14~10	Reserved. Set it to "0".		"0"	"0"
9	ACLR Buffer Automatic Clear Mode	• Write 0: Disable buffer automatic clear 1: Enable buffer automatic clear	○	○
8	SQCLR Sequence Bit Clear	• Write 0: Invalid 1: Sequence bit clear	"0"	○
7~5	Reserved. Set it to "0".		"0"	"0"
4	NYETMD NYET Handshake Mode	0: Automatic response mode (ACK/NYET is automatically selected.) 1: ACK response only mode (Always with ACK response. No NYET response.)	○	○
3~2	Reserved. Set it to "0".		"0"	"0"
1~0	PID [1:0] Response PID	00: NAK response 01: BUF response 1x: STALL response	○	○

(1) BSTS (Buffer Status) Bit (b15)

This bit indicates the buffer status of PIPE1 to PIPE4.

(2) ACLR (Buffer Automatic Clear Mode) Bit (b9)

When this bit is set to "1", all the buffers on the CPU-side/SIE-side are cleared.

This bit is not automatically cleared to "0" on completion of buffer clear, make sure to write "0" after setting "1".

When the PID [1:0] bits are set to "01" (BUF) during setting the OUT buffer and this bit to "1", the NAK response are not executed in the received OUT token. The ACK response is returned to the host after the data being received. At this time, this received data are not written to the buffer. Also, when the PID [1:0] bits have been sets to "00"/"1x" (NAK/STALL), the NAK/STALL response is executed.

Only the SIE-side buffers and the write completion CPU-side buffer are cleared by setting "1" to this bit during setting the IN buffer. To clear the SIE-side buffers, follow the procedure below.

(1) The PID [1:0] bits are set to "00" (NAK)
(2) This bit is set to "1"
(3) This bit is cleared to "0"
(4) The PID [1:0] bits are set to "01" (ACK)

(3) SQCLR (Sequence Bit Clear) Bit (b8)

This bit clears the sequence bit of the PIPE1 to PIPE4 to set the next data PID to the "DATA0".
The sequence bit is toggled through hardware control in the transfers after the sequence bit is cleared.
With the USB bus reset, the sequence toggle bit is not cleared. It is necessary to clear the sequence bit by software.
Writing "0" to this bit is invalid. This bit is always read "0". Before setting this bit, be sure to set the PID [1:0] bits to "00" (NAK).

Note: To clear two or more sequence toggle bits of the PIPE continuously, the access cycle time of 200ns or more is required from one SQCLR bit of the PIPE access to the next SQCLR bit of the PIPE access. For example, when the sequence toggle bits of both PIPE1 and PIPE2 are cleared, the access cycle required from when "1" is written to the SQCLR bit of PIPE1 to when "1" is written to the SQCLR bit of PIPE2 is 200ns or more.

(4) NYETMD (NYET Handshake Mode) Bit (b4)

This bit sets the NYET response mode.
0: Automatic response mode (ACK/NYET is automatically selected.)
1: ACK response only mode (Always with ACK response. No NYET response.)
This bit is valid when the PID [1:0] bits of the OUT transfer are "01"(BUF) in case the bulk transfer operated in the Hi-Speed mode. In any other case, this bit is invalid.
In the automatic response mode, hardware automatically selects an appropriate response PID (NAK/ACK/NYET) according to the buffer status below:
(1) When the buffer to receive the data packet is the buffer full, the NAK response is executed.
(2) When an empty space existing in the buffer is equal to or more than twice as large as the max packet size before receiving of the data packet, the ACK response is executed.
(3) When an empty space existing in the buffer is less than twice as large as the max packet size before receiving of the data packet, the NYET response is executed.

In the ACK response only mode, the device does not transmit the NYET packet. The ACK/NAK response is executed.

(5) PID [1:0] (Response PID) Bits (b1-b0)

These bits set the PID for response of PIPE1 to PIPE4.
00: NAK response
The NAK response is executed irrespective of buffer status.
01: BUF response
The response ID is selected according to the buffer status, the value of the NYETMD bit and the value of the sequence toggle bit.
When the NYETMD bit is "00" and in the bulk OUT transfer, the NYET response is executed in the following conditions:
(1) When the non-continuous transmit/receive mode and the single buffer mode.
(2) When the buffer on the CPU-side is not empty in the non-continuous transmit/receive mode and the double buffer mode before receiving the data packet.
1x: STALL response
The STALL response is executed irrespective of buffer status.
When the data packet exceeding the max packet size (512 bytes when Hi-Speed, 64 bytes when Full-Speed) of PIPE1 to PIPE4 has been received while setting the transfer direction of the PIPE to OUT, these bits are automatically set to "1x".
To set the STALL response, follow the procedure below in accordance with this bit value before setting:
(1) Set to "10" when PID [1:0] are set to "00"
(2) Set to "11" when PID [1:0] are set to "01"

2.39 PIPE i Control Register (i=5~6)

■ PIPE 5 Control Register (Pipe5Ctrl) <Address: H'A8>
■ PIPE 6 Control Register (Pipe6Ctrl) <Address: H'AA>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
BSTS						ACLR	SQCLR							PID [1:0]	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: B'---- ---- ---- --00>

b	Bit name	Function	R	W
15	BSTS Buffer Status	0: Disables to read the data of buffer and to write the data to buffer 1: Enables to read the data of buffer and to write the data to buffer	○	-
14~10	Reserved. Set it to "0".		"0"	"0"
9	ACLR Buffer Automatic Clear Mode	• Write 0: Disable buffer automatic clear 1: Enable buffer automatic clear	○	○
8	SQCLR Sequence Bit Clear	• Write 0: Invalid 1: Sequence bit clear	"0"	○
7~2	Reserved. Set it to "0".		"0"	"0"
1~0	PID [1:0] Response PID	00: NAK response 01: BUF response 1x: STALL response	○	○

(1) BSTS (Buffer Status) Bit (b15)

This bit indicates the buffer status of PIPE5 and PIPE6.

(2) ACLR (Buffer Automatic Clear Mode) Bit (b9)

When this bit is set to "1", all the buffers on the CPU-side/SIE-side are cleared.
This bit is not automatically cleared to "0" on completion of buffer clear, make sure to write "0" after setting "1".
Only the SIE-side buffers and the write completion CPU-side buffer are cleared by setting "1" to this bit. To clear the SIE-side buffers, follow the procedure below.
(1) The PID [1:0] bits are set to "00" (NAK)
(2) This bit is sets to "1"
(3) This bit is cleared to "0"
(4) The PID [1:0] bits are set to "01" (ACK)

(3) SQCLR (Sequence Bit Clear) Bit (b8)

This bit clears the sequence bit of PIPE5 and PIPE6, to set the next data PID to the "DATA0".
The sequence bit is toggled through hardware control in the transfers after the sequence bit is cleared.
With the USB bus reset, the sequence toggle bit is not cleared. It is necessary to clear the sequence bit by software.
Writing "0" to this bit is invalid. This bit is always read "0". Before setting this bit, be sure to set the PID [1:0] bits to "00" (NAK).

Note: To clear two or more sequence toggle bits of the PIPE continuously, the access cycle time of 200ns or more is required from one SQCLR bit of the PIPE access to the next SQCLR bit of the PIPE access. For example, when the sequence toggle bits of both PIPE1 and PIPE2 are cleared, the access cycle required from when "1" is written to the SQCLR bit of PIPE1 to when "1" is written to the SQCLR bit of PIPE2 is 200ns or more.

(4) PID [1:0] (Response PID) Bits (b1-b0)

These bits set the PID for response of PIPE5 and PIPE6.

00: NAK response

The NAK response is executed independent to buffer status.

01: BUF response

The response ID is selected according to the buffer status and the value of the sequence toggle bit.

1x: STALL response

The STALL response is executed independent to buffer status.

To set the STALL response, follow the procedure below in accordance with this bit value before setting.

(1) Set to “10” when PID [1:0] are set to “00”

(2) Set to “11” when PID [1:0] are set to “01”

3 M66591 OPERATIONS

3.1 System Control

3.1.1 Clock

M66591 is able to use the crystal oscillator or the external clock input. Oscillation factor is selected by the XTAL [1:0] bits of USB Transceiver Control Register 0, And internal clock supply disable or enable is controlled by XCKE bit, RCKE bit, PLL bit and SCKE bit of USB Transceiver Control Register 0. The clock control diagram is shown in Figure 3.1.

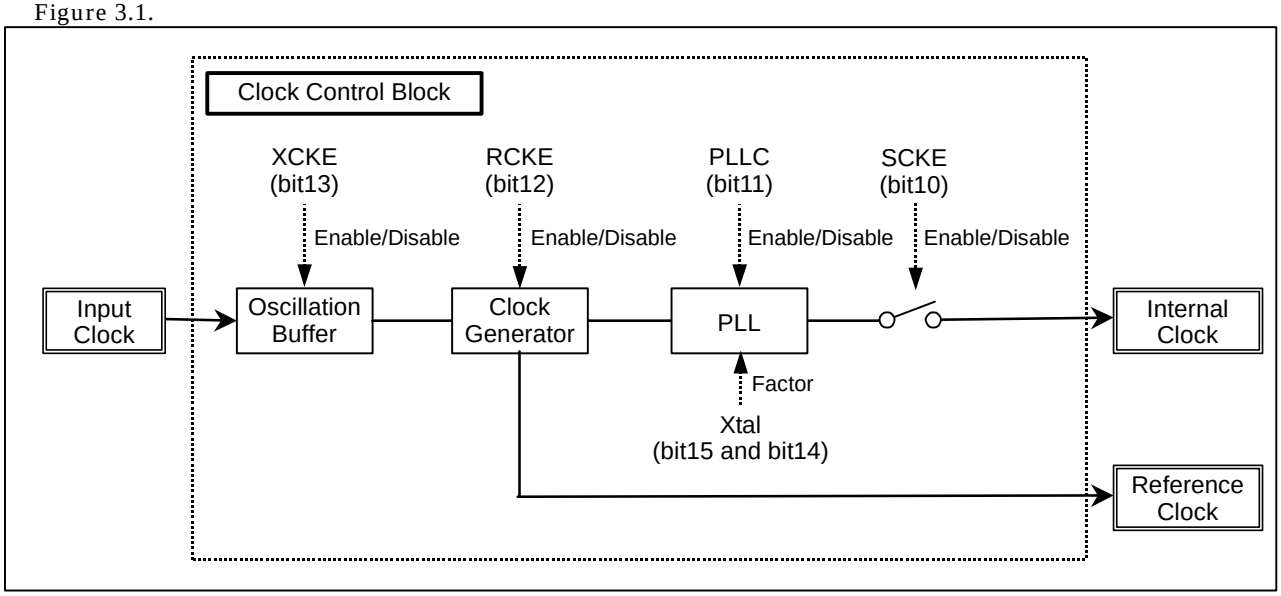


Figure 3.1 M66591 clock control diagram

When enable or disable clock oscillation, the clock stable waiting time is necessary for enabling or disabling these bits mentioned above. The process order and waiting time is shown in

Table 3.1 The process order and waiting time for enabling or disabling clock

Operation	Process Order	Waiting Time After Setting
Enable Clock Oscillation	(1) XCKE = 1	1.5ms (Unnecessary when use external clock input)
	(2) RCKE = 1	--
	(3) PLLC = 1	8.3µs
	(4) SCKE = 1	--
Disable Clock Oscillation	(1) SCKE = 0	3µs
	(2) PLLC = 0	3µs
	(3) RCKE = 0	3µs
	(4) XCKE = 0	--

Note: Because the waiting time is difference according to used crystal oscillator, it necessary to set a appropriate oscillation waiting time and do evaluation.

It is necessary to set the bits which is described below before enabling clock supply.

- Xtal [1:0] bits, USBE bit and HSE bit of USB Transceiver Control Register 0

- LDRV bit of Data Pin & FIFO/DMA Control Pin Configuration Register 1

- DreqA bit of Data Pin & FIFO/DMA Control Pin Configuration Register 2

- INTL bit and INTA bit of INT Pin Configuration Register 1

3.1.2 Reset

M66591 has three types reset, hardware reset, software reset by register setting (USBE bit), and USB reset.

The hardware reset will clear the value of all register.

The software reset retains values of USB Transceiver Control Register0, USB Transceiver Control Register 1, Data Pin & FIFO/DMA Control Pin Configuration Register 0, Data Pin & FIFO/DMA Control Pin Configuration Register 1, Data Pin & FIFO/DMA Control Pin Configuration Register 2, C_FIFO Port Register 0, D0_FIFO Port Register 0 , and Interrupt Pin Configuration Register 1.

In the USB reset, the register values excepting those of HS/FS Mode Register, USB Address Register, USB Request Register 0, USB Request Register 1, USB Request Register 2, USB Request Register 3, PID bits and CCPL bit of DCP Control Register and PID bits of PIPE i Control Register (i = 1-6) are retained.

For details of the reset state, refer to each register.

3.1.3 D+ Pull-up Resistor Control

M66591 includes the TR_ON pin to output the power source (+3.3V) for USB D+ line pull-up and the RPU input pin to control pull-up ON/OFF. The 1.5KΩ resistors to pull up D+ line is connected between the TR_ON pin and the RPU pin, controlling pull-up ON/OFF by the RpuE bit of the USB Transceiver Control Register 0. As for connection of pull-up resistor and peripheral connection of the USB connector, refer to Figure 3.2. (The VBUS pin must be connected to a 1~10µF capacitor conforming to the Universal Serial Bus Specification Revision 2.0.)

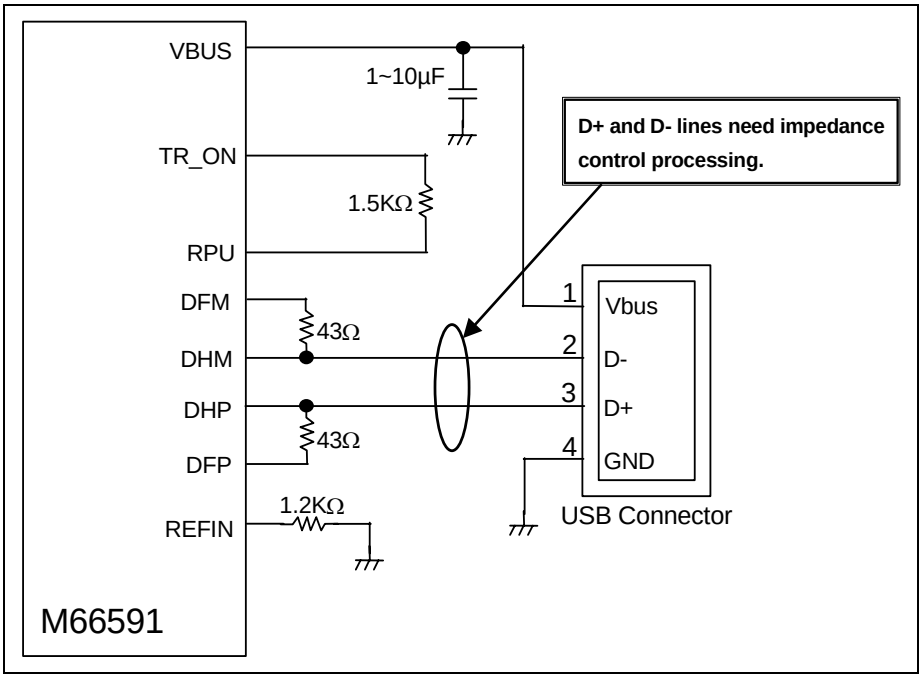


Figure 3.2 Connection of M66591 and USB Connector

3.2 M66591 Initial Setting and Clock Control

This chapter explains the method of initial setting, the detection method of attach/detach to the host, and the execution method of clock control and remote wakeup in suspend/resume concerning M66591.

3.2.1 M66591 Initial Setting

In initial setting process of the M66591, USB operation is enabled and input of the VBUS pin is confirmed by polling the VBUSSTS bit of Interrupt Status Register 0. According to the input status of the VBUS pin, either the VBUS interrupt waiting process or the USB attach processing is executed.

If VBUSSTS bit is “0”, M66591 is not connected to the host, enable the VBUS interrupt and wait for connection to the host.

If VBUSSTS bit is “1”, M66591 is already connected to the host before initial setting, execute attach processing.

The detailed process flowchart is shown in Figure 3.3.

Further, as the VBUS pin is directly input from the VBUS pin of the USB connector, chattering removal process by software is required for confirmation of the input status.

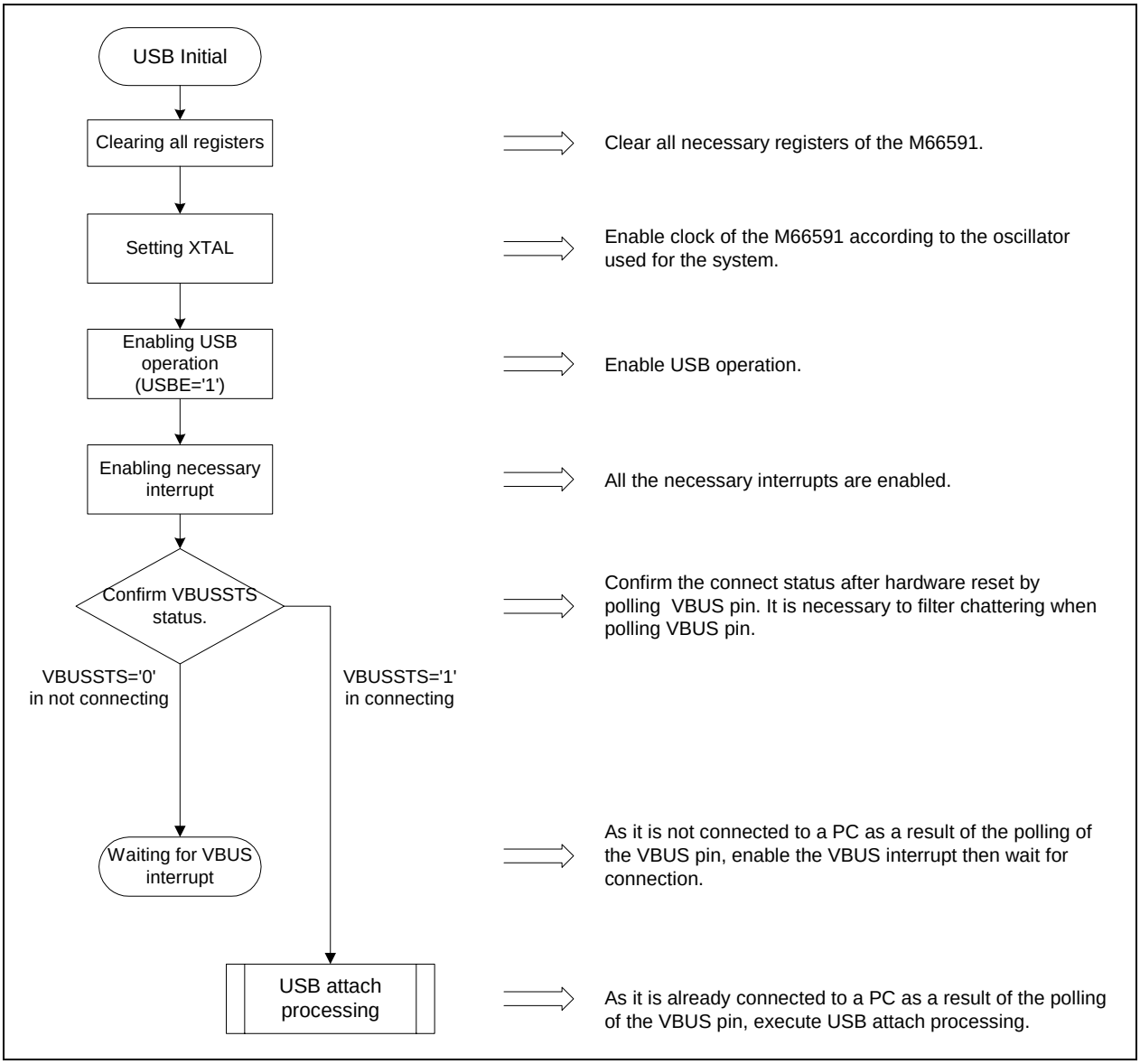


Figure 3.3 M66591 Initial Setting Process Flowchart

3.2.2 Process After Detection of Attach/Detach (VBUS Interrupt)

M66591 uses VBUS interrupt to detect attach to the host to or detach from the host.

The VBUS interrupt occurs when either “Low”->”High” or “High”->“Low” change has occurred in the VBUS pin input. The attach to the host or detach from the host is judged by polling of the VBUSSTS bit of the Interrupt Status Register 0.

When attach to the host has been determined, M66591 execute the USB attach processing.

When detach from the host has been determined, M66591 execute the USB detach processing.

The detailed process flowchart is shown in the following Figure 3.4.

The VBUS interrupt is occurred even while the internal clock (SCKE bit of the USB Transceiver Control Register 0 = “0”) is not supplied. Also, The VBUSSTS bit is capable of reading correct value even if the internal clock is not supplied.

The VBUS interrupt (VBUSINT bit) is cleared by the following two methods according to the internal clock:

(1) State when the internal clock is supplied (SCKE bit of the USB Transceiver Control Register 0 = “1”)
This bit is cleared to “0” by writing “0” to the VBUSINT bit.

(2) State when the internal clock is not supplied (SCKE bit of the USB Transceiver Control Register 0 = “0”)
This bit is cleared to “0” by writing “0” to the VBUSINT bit. Write “1” to this bit once again to enable next VBUS interrupt.

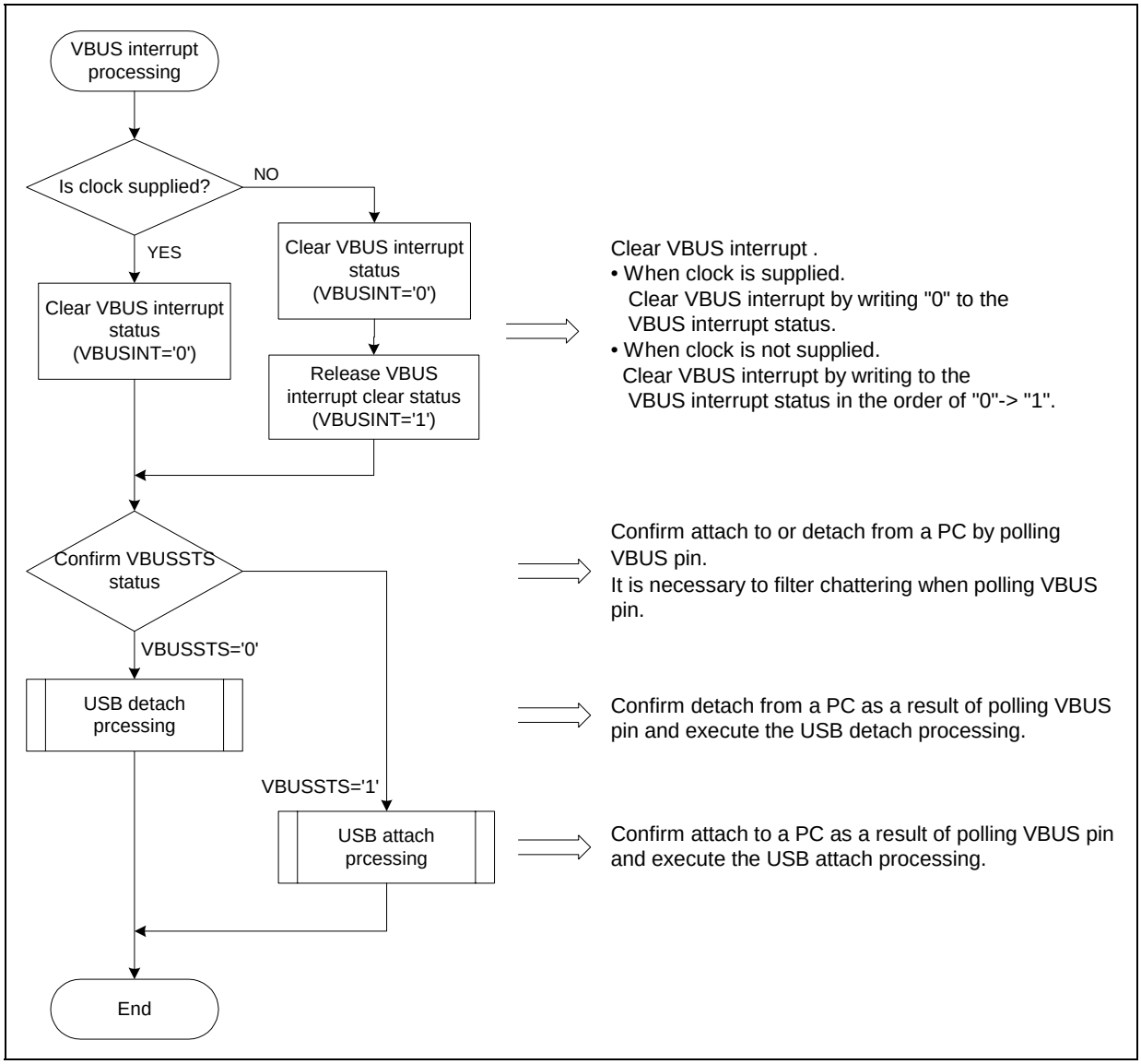


Figure 3.4 M66591 VBUS Interrupt Process Flowchart

3.2.3 USB Attach Process

AfterM66591 detects attach to the host, the USB attach processing is executed.
The basic details of the USB attach processing are as follows:

(1) Select M66591 operation mode:
M66591 can select enable/disable of the Hi-Speed operation mode by the HSE bit of the USB Transceiver Control Register 0.

(2) Enable M66591 clock oscillation:
The sequence consists of enable of the oscillation buffer, enable of the internal reference clock, enable of PLL operation, and enable of the internal clock. In this series of operations, it is necessary to insert wait required for oscillation to be stabilized.

(3) D+ line pull-up:
Connection (Attach) is notified to the host.

The detailed process flowchart is shown in the following Figure 3.5.

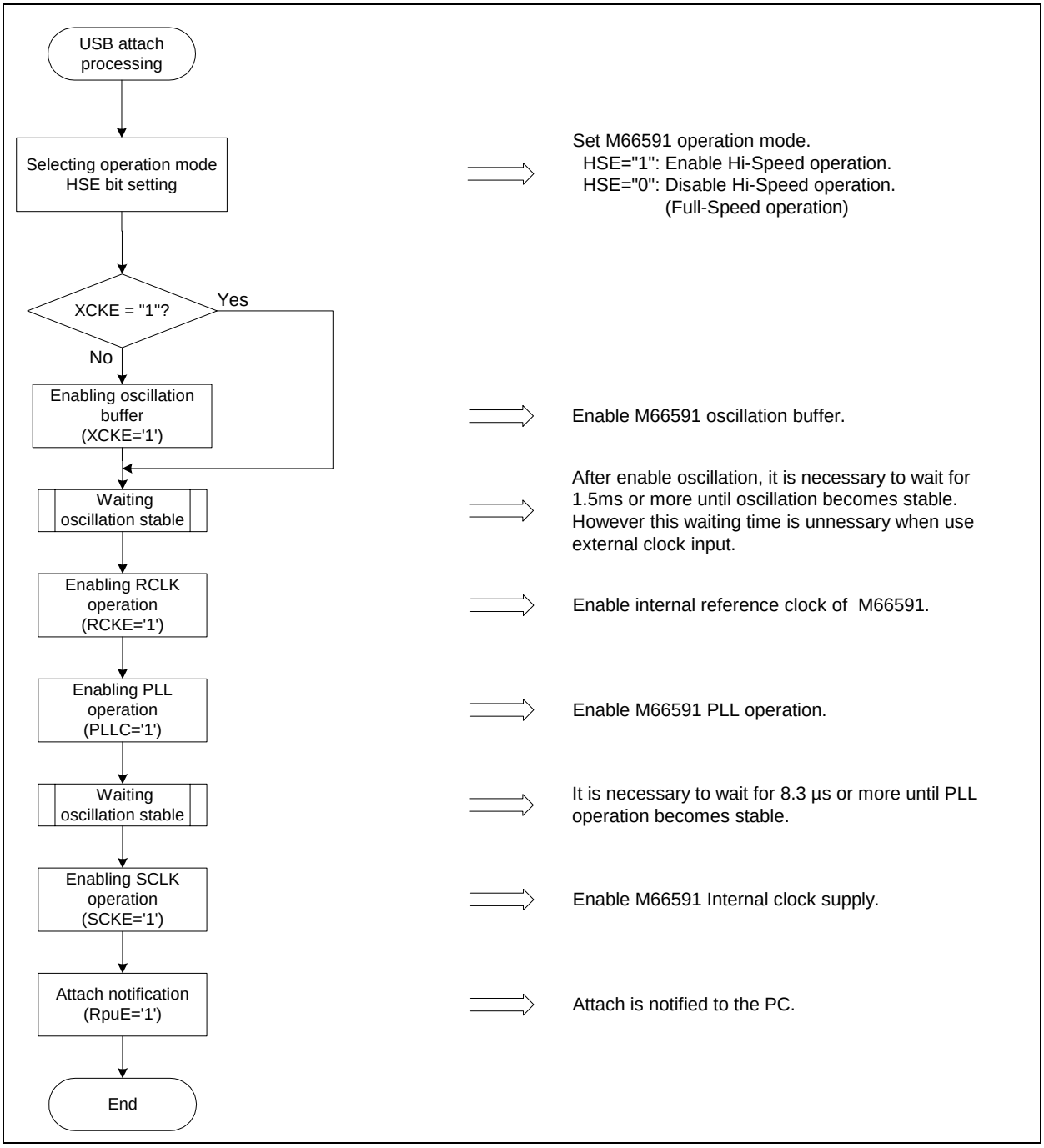


Figure 3.5 M66591 USB Attach Process Flowchart

3.2.4 USB Detach Process

After M66591 detects detach from the host, the USB detach processing is executed.
The basic details of the USB detach processing are as follows:

(1) Suspend of D+ line pull-up:
After M66591 detects detach from the host, pull-up for D+ line is suspended.

(2) Disable M66591 clock oscillation:
M66591 executes disable of the internal clock, disable of the PLL operation, disable of the internal reference clock, and disable of the oscillation buffer. In this series of operations, it is necessary to insert wait required in the same manner as oscillation enable.

The detailed process flowchart is shown in the following Figure 3.6.

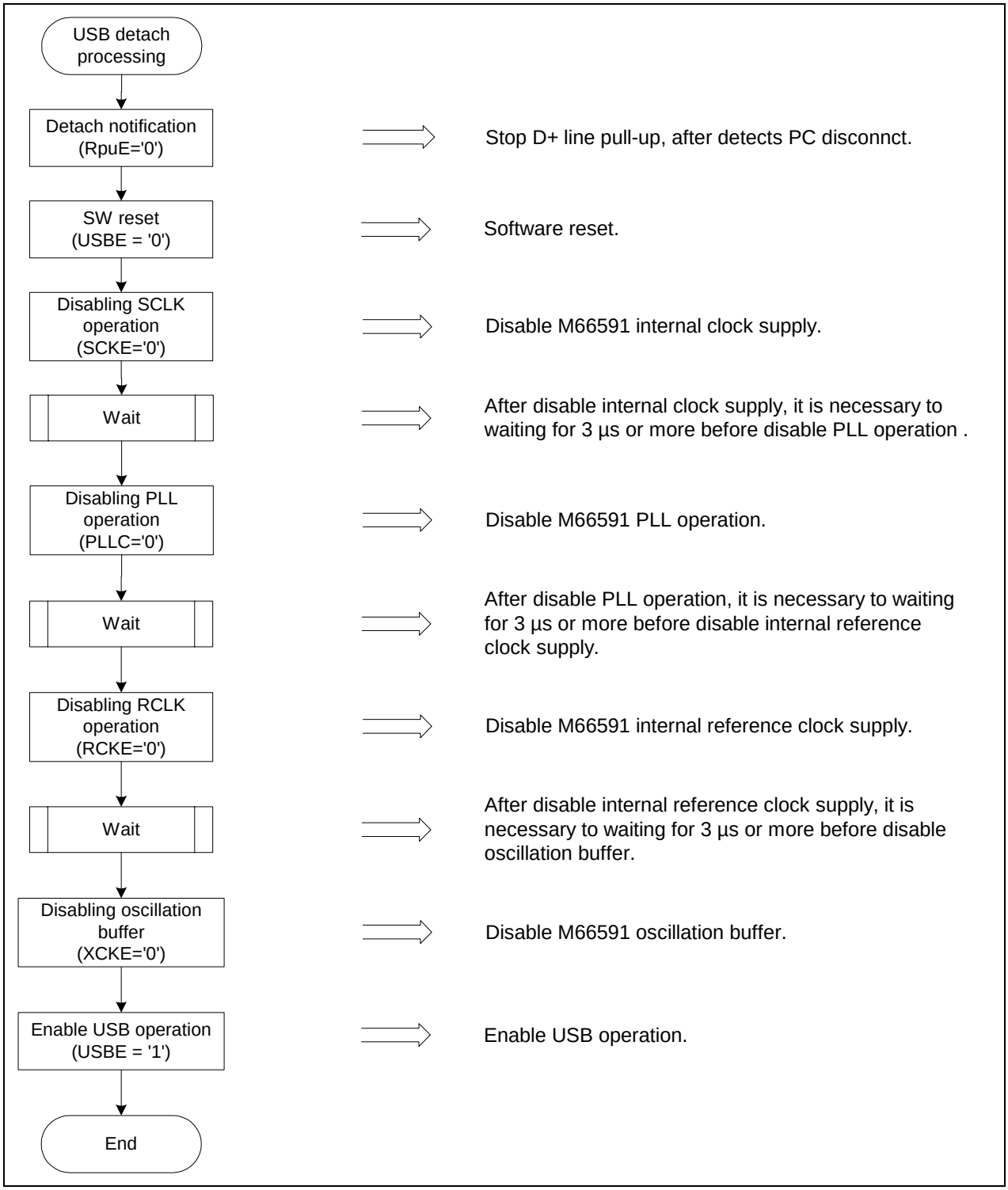


Figure 3.6 M66591 USB Detach Process Flowchart

3.2.5 Clock Control in Suspend/Resume

M66591 clock must be controlled by the USB bus status in a system requiring low power consumption control.

M66591 occurs the device state transition interrupt (DVST) after detecting suspended state of the USB bus. The clock oscillation of M66591 is disabled by suspend interrupt processing.

Further, when the USB bus enters active state from suspended state, M66591 detects it and the resume interrupts occurring. The clock oscillation of M66591 is restarted by resume interrupt processing.

The flowchart of Figure 3.7 below shows the clock control processing in suspend.

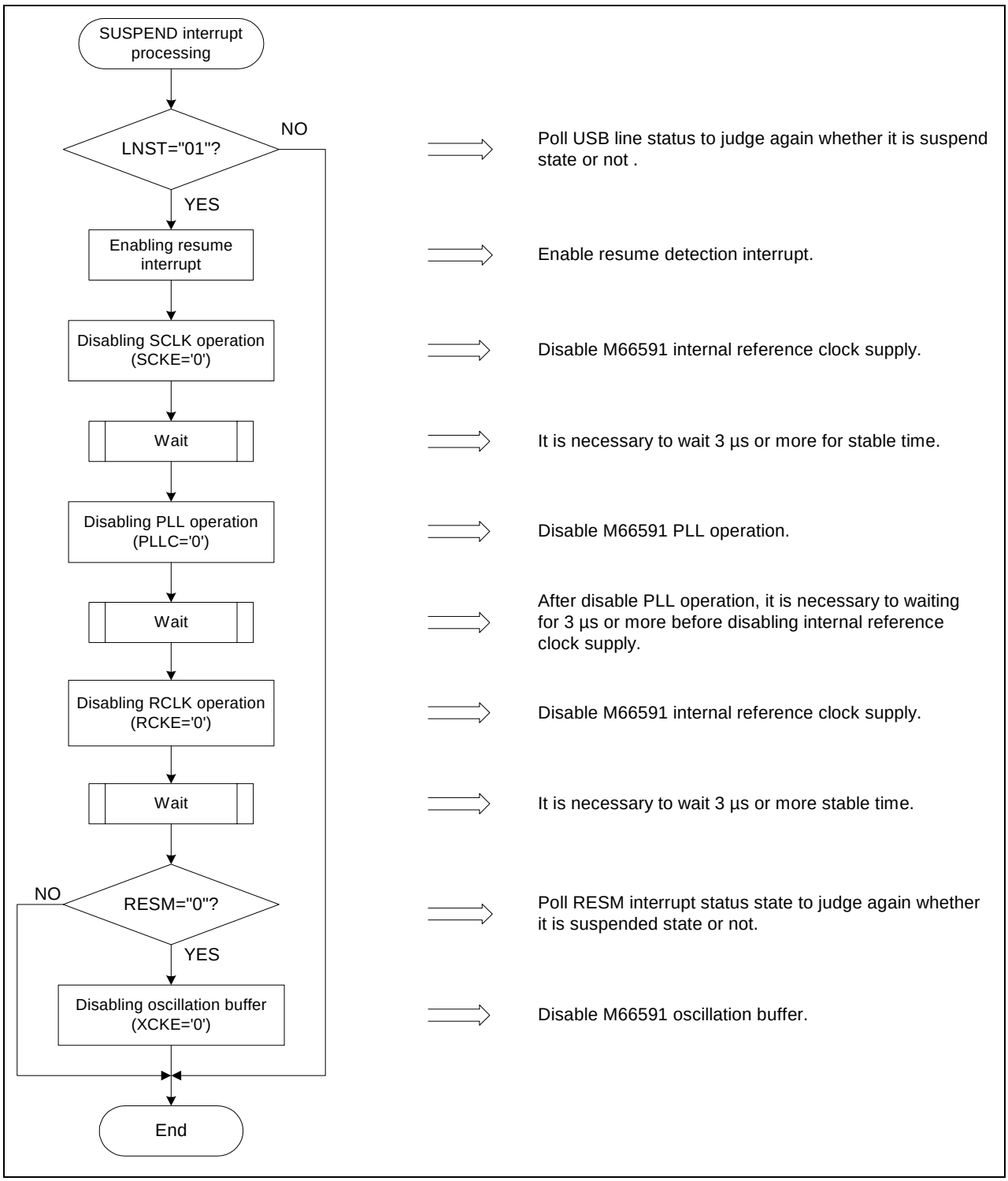


Figure 3.7 M66591 Clock Control Flowchart in Suspend

The flowchart of Figure 3.8 shows the clock control processing in suspend and in resume.

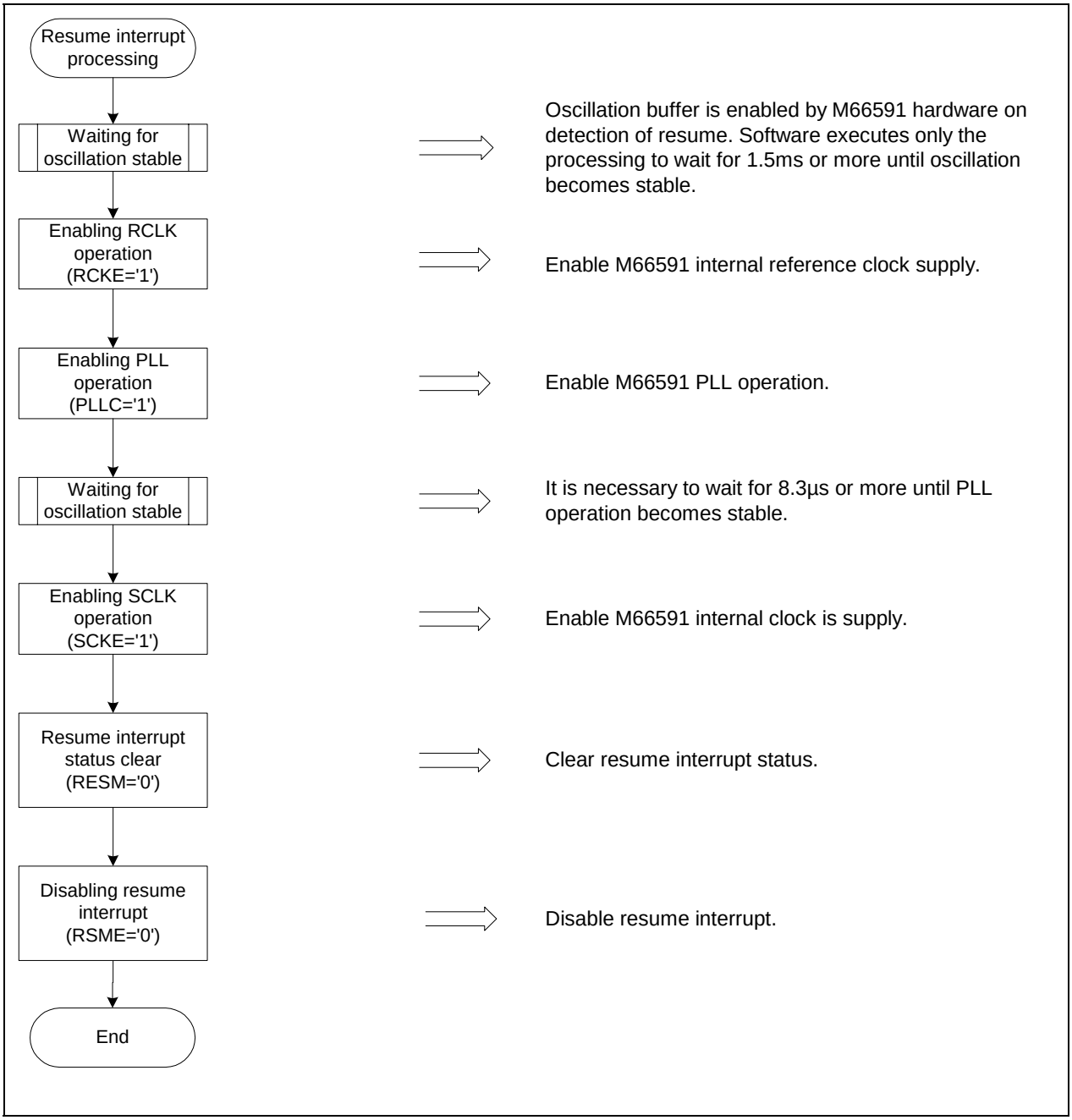


Figure 3.8 M66591 Clock Control Flowchart in Resume

3.2.6 Execution Method of Remote Wakeup Output

The remote wakeup means that the remote wakeup signal is output and the suspended state is canceled when the USB bus is kept in suspended state. M66591 is capable to output remote wakeup signal using registers.

The flowchart of Figure 3.9 below shows the execution method of remote wakeup. Further, concerning this flowchart, it is assumed that the internal clock of M66591 is kept disabled in suspended state.

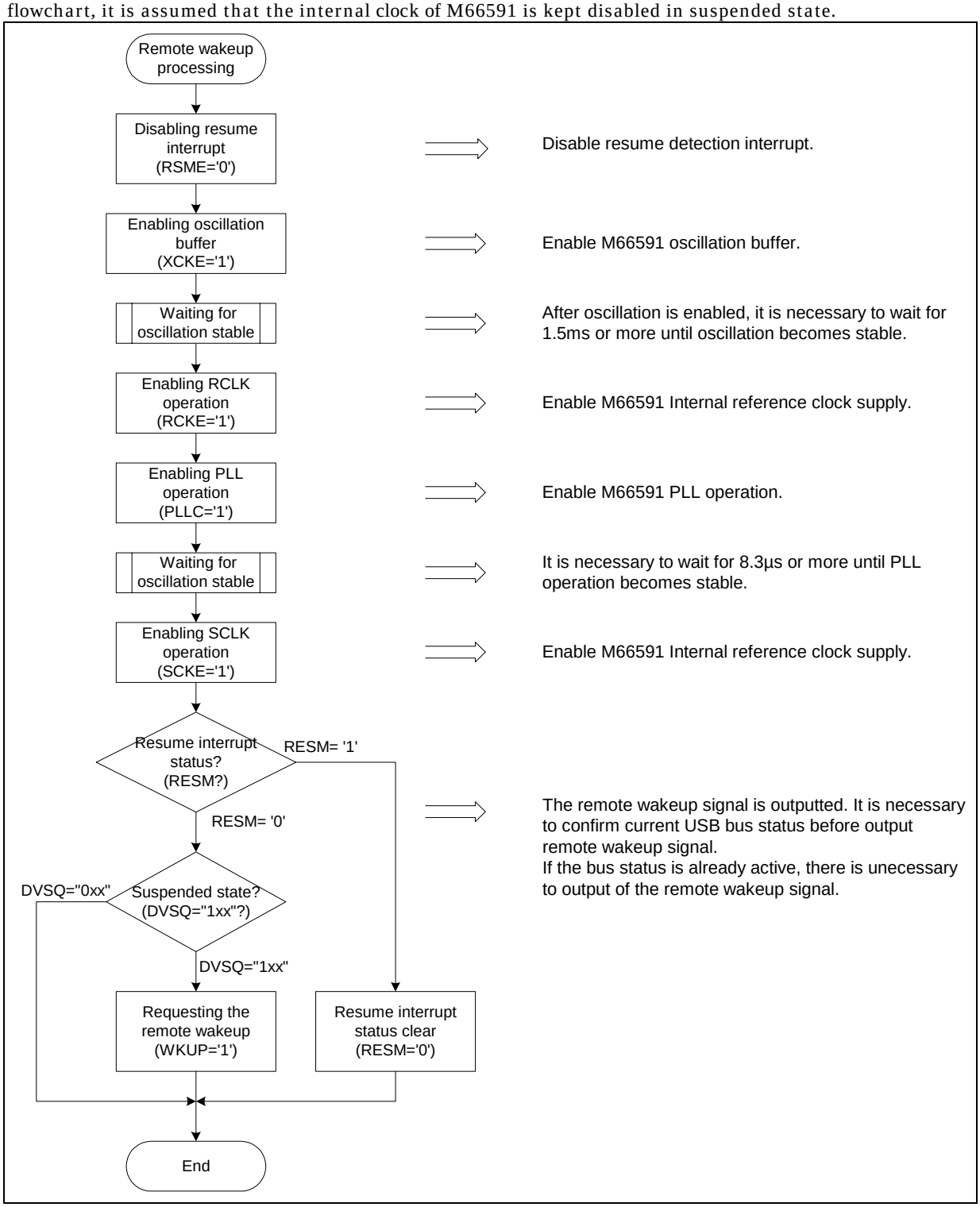


Figure 3.9 M66591 Remote Wakeup Output Flowchart

3.3 Interrupt

3.3.1 Features

There are 7 factors of interrupts in M66591. The 7 factors of interrupts is shown in Table 3.2.

The interrupt factors can set to enable/disable by the INT Pin Configuration Register 0, 2, 3. A diagrams related to the interrupt is shown in Figure 3.10.

The sense mode and polarity of the interrupt output can set to enable by the INT Pin Configuration Register 1. Figure 3.11 shows the interrupt pin output timing.

Table 3.2 List of Interrupts

Status Bit	Interrupt Name	Interrupt Factor	Related Status Bit
VBUSINT	VBUS Interrupt (Detection of attach/detach)	Change of the VBUS input level (change of “Low”->”High”, “High”->”Low”)	VBUSSTS
RESM	Resume Interrupt	Change of the USB bus state in suspended state (J state -> K state, J state -> “SE0”)	-
DVST	Device State Transition Interrupt	Device State Transition • Detection of the USB bus reset • Detection of suspended state • Execution of the SET_ADDRESS • Execution of the SET_CONFIGURATION	DVST [2:0]
CTRT	Control Transfer Stage Transition Interrupt	Control Transfer Stage Transition • Completion of setup stage • Transition of control write transfer status stage • Transition of control read transfer status stage • Completion of control transfer • Occurrence of control transfer sequence error	CTSQ [2:0]
BEMP	PIPE Buffer Empty / Size Error Interrupt	In each PIPE; When all data in the FIFO buffer have been transmitted completely and the buffer has become empty for the IN token. When a packet exceeding the max packet size has been received for the OUT token.	PIPEB_EMP_OVR6, PIPEB_EMP_OVR5, PIPEB_EMP_OVR4, PIPEB_EMP_OVR3, PIPEB_EMP_OVR2, PIPEB_EMP_OVR1, DCP_EMP_OVR
INTN	PIPE Buffer Not Ready Interrupt	In each PIPE; When no transmittable data exist in the FIFO buffer for the IN token. When the FIFO buffer does not have any data storage space and disables receiving for the OUT token.	PIPEB_NRDY6, PIPEB_NRDY5, PIPEB_NRDY4, PIPEB_NRDY3, PIPEB_NRDY2, PIPEB_NRDY1, DCP_NRDY
INTR	PIPE Buffer Ready Interrupt	When each PIPE buffer is ready state (read/write enable state)	PIPEB_RDY6, PIPEB_RDY5, PIPEB_RDY4, PIPEB_RDY3, PIPEB_RDY2, PIPEB_RDY1, DCP_RDY

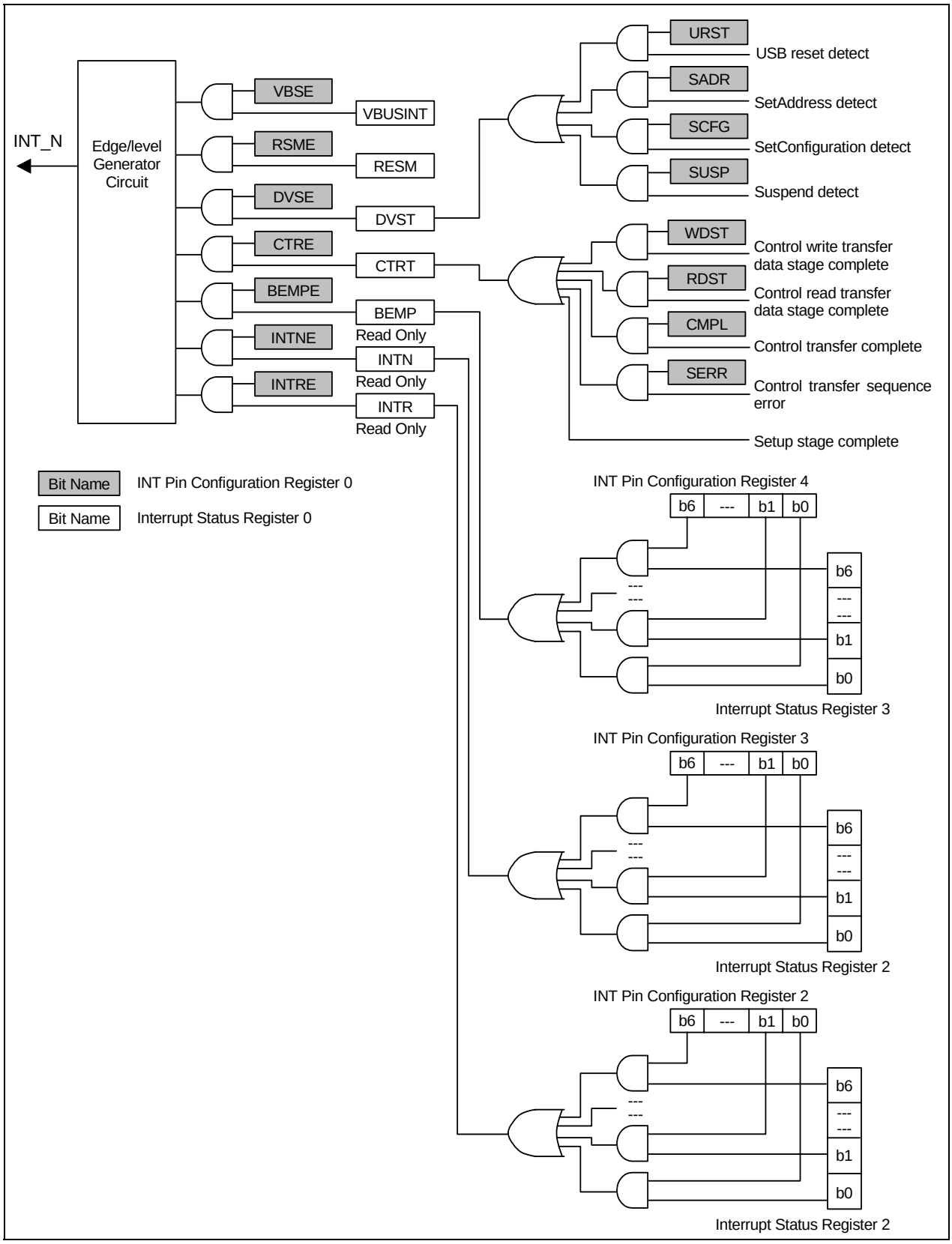


Figure 3.10 Interrupt Related Diagram

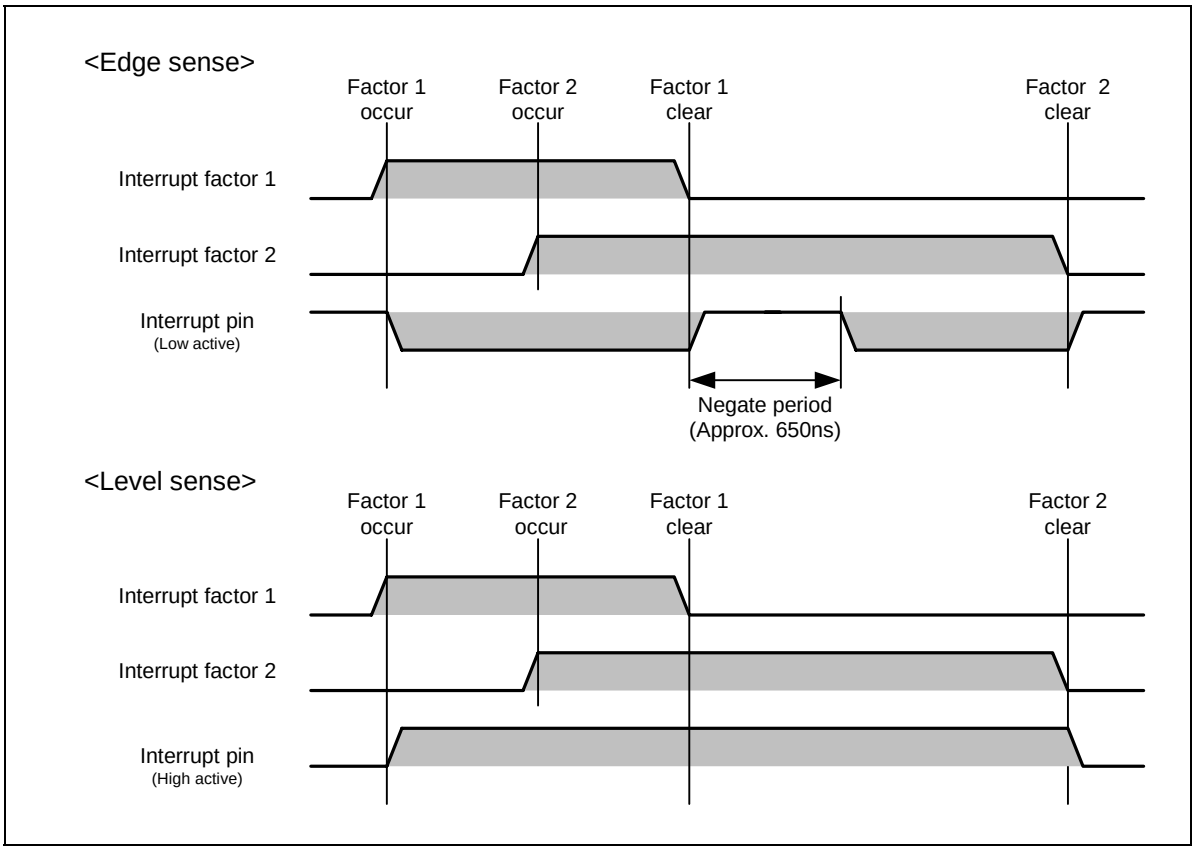


Figure 3.11 Interrupt Pin Output Timing

3.3.2 VBUS (Detection of Attach to Host/Detach from Host) Interrupt

The VBUS interrupt (VBUSINT) occurs when either “Low”->”High” or ”High”->“Low” change has occurred in the VBUS input pin. The connection or disconnection to the host can be detected by confirming VBUS input pin status using VBUSSTS bit of the Interrupt Status Register 0.

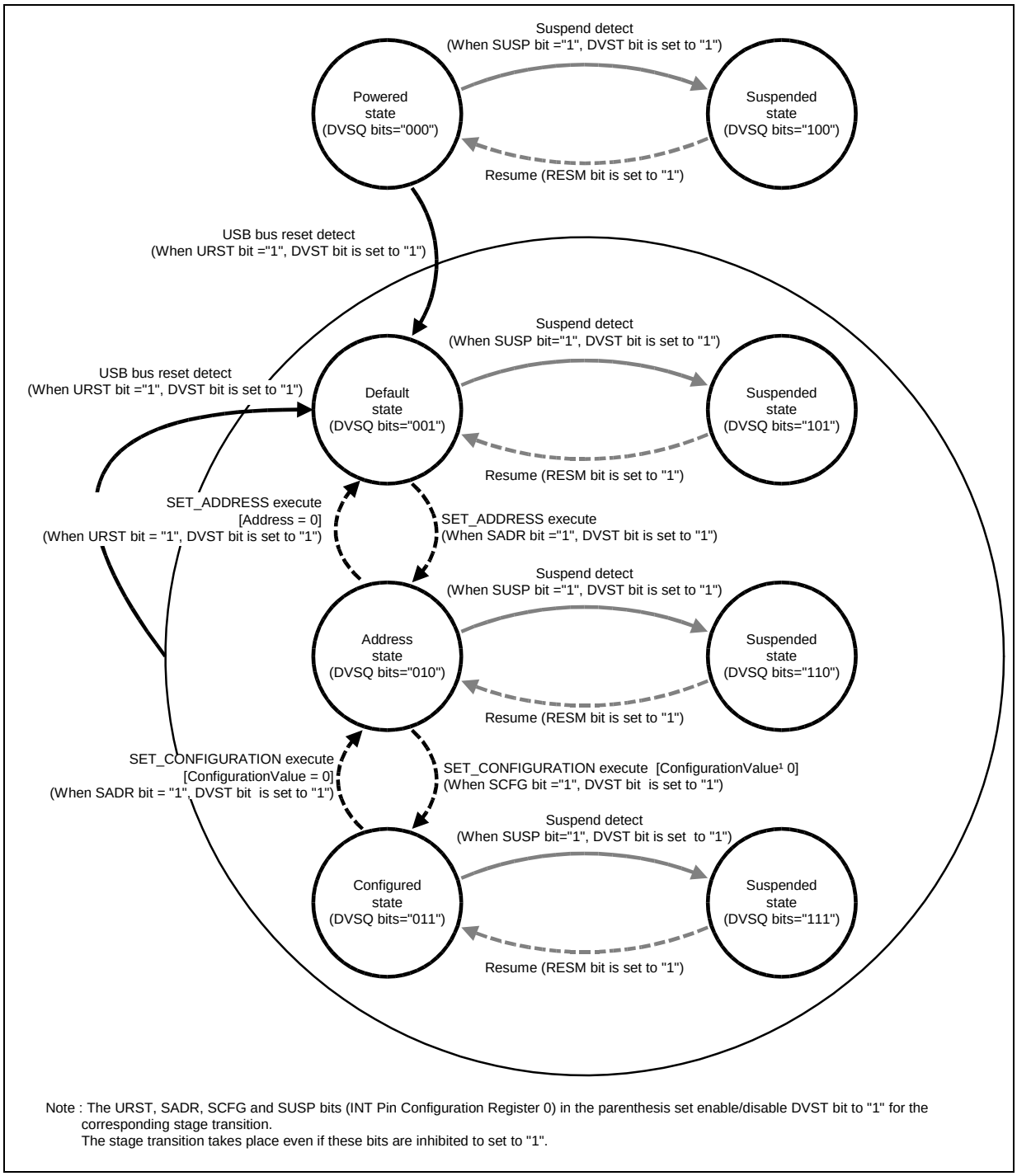
3.3.3 Resume Interrupt

The resume interrupt (RESM) occurs when a change (J state -> K state or J state -> SE0) has occurred in the USB bus status, with the device state kept in suspended. The wakeup from suspend can be detected by resume interrupt.

3.3.4 Device State Transition Interrupt

Device state transition diagram is shown in Figure 3.12. M66591 controls each device state by hardware. Device state transition interrupt occurs when device state is updated. However, device state transition interrupt can not detect resume from suspend. Every state transition can be set to enable /disable by INT Pin Configuration Register 0. Also, The device state can be confirmed by the DVSQ [2:0] bits of the Interrupt Status Register 0.

When the device state transition to default state, device transition interrupt (DVST) occurs on completion of the USB reset handshake process.



Note : The URST, SADR, SCFG and SUSP bits (INT Pin Configuration Register 0) in the parenthesis set enable/disable DVST bit to "1" for the corresponding stage transition.
The stage transition takes place even if these bits are inhibited to set to "1".

Figure 3.12 Device State Transition Diagram

3.3.5 Control Transfer Stage Transition Interrupt

The control transfer stage transition of M66591 is shown in Figure 3.13. Control transfer stage transition interrupt occurs when a stage transition occurs by the control transfer. Interrupt occurs when stage transition is detected except for the SET_ADDRESS request because it is responded automatically. Each stage transition can be individually enabled/disabled by enabling bit of INT Pin Configuration Register 0. However, setup stage completion can not be disabled. The control transfer stage is shown in DVSQ [2:0] bits of Interrupt Status Register 0.

The control transfer sequence errors are shown below. When an error occurs, the PID [1:0] bits of Default Control PIPE Control Register are set to “1X” (STALL).

<In the case of control read transfer>

- Receives the OUT or PING token for the IN token of the data stage when data transfer has not occurred even once.
- Receives the IN token in the status stage
- Receives the DATA packet with PID = DATA0 in the status stage

<In the case of control write transfer>

- Receives the IN token for the OUT token of the data stage when ACK response has not executed even once.
- Receives the first DATA packet with DATA PID = DATA0 in the data stage
- Receives the OUT or PING token in the status stage

<When control write no data transfer>

- Receives the OUT or PING token in the status stage

Further, when the number of the receive data of the data stage in none no data control write transfer has exceeded the wLength value of the request, the control transfer sequence error cannot be detected.

When the CTRT interrupt occurs (“SEER = 1“ setting) by sequence error, the “CTSQ [2:0] = 110” bits is held until “CTRT = 0” is wrote. Therefore, the CTRT interrupt of setup stage completion will not occur even if a new USB request is received in the “CTSQ [2:0] = 110” held state.

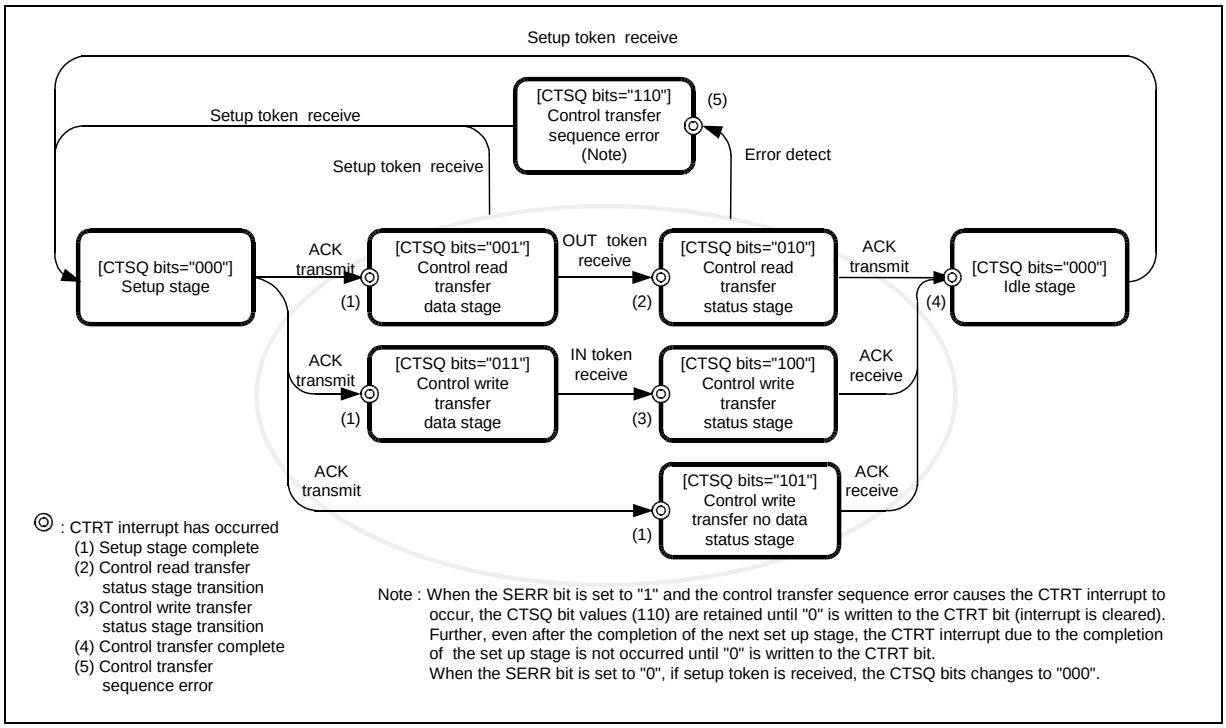


Figure 3.13 Control Transfer Stage Transition Diagram

3.3.6 PIPE Buffer Ready Interrupt

The condition of M66591 INTR interrupt occurring is shown in Table 3.3. The timing of M66591 INTR interrupt occurring is shown in Figure 3.14. The status of each PIPE is confirmed by the appropriate bit of Interrupt Status Register 1. When the DMA transfer is used, an interruption factor sets up by the BFRE bit of PIPE configuration window register 0 and the buffer memory access direction. So that the interrupt may not occur every transaction but every transfer. However, there is no BFRE bit in DCP.

The interrupt request is stored in Interrupt Status Register 1 even if INTRE bit of INT Pin Configuration Register 0 and PIPEB_RE6-1 bits, DCP_RE bit of INT Pin Configuration Register 2 is disabled.

INTR bit of Interrupt Status Register 0 is cleared by clearing all bits of Interrupt Status Register 1.

Table 3.3 INTR interrupt occurring condition

Buffer access	Direction	PIPE	BFRE	Occur condition of INTR interrupt	Remark
Read	OUT	DCP	-	Zero-length packet received	Necessary for buffer clear
				Short packet received, buffer full	
		1-4	0	Zero-length packet received	Necessary for buffer clear
				Short packet received, buffer full or completion of transaction counter	
			1	Zero-length packet received	Necessary for buffer clear
				Read completed after short packet received or completion of transaction counter	Necessary for buffer clear
Write	IN	DCP	-	Not occurred	
		1-4	0	Packet transmit (buffer full)	Writable
			1	Not occurred	
		5-6	-	Packet transmit (buffer full)	Writable

Although INTR bit is set to "1" when a zero-length packet is received, it is necessary to clear buffer even if the zero-length packet cannot be read-out.

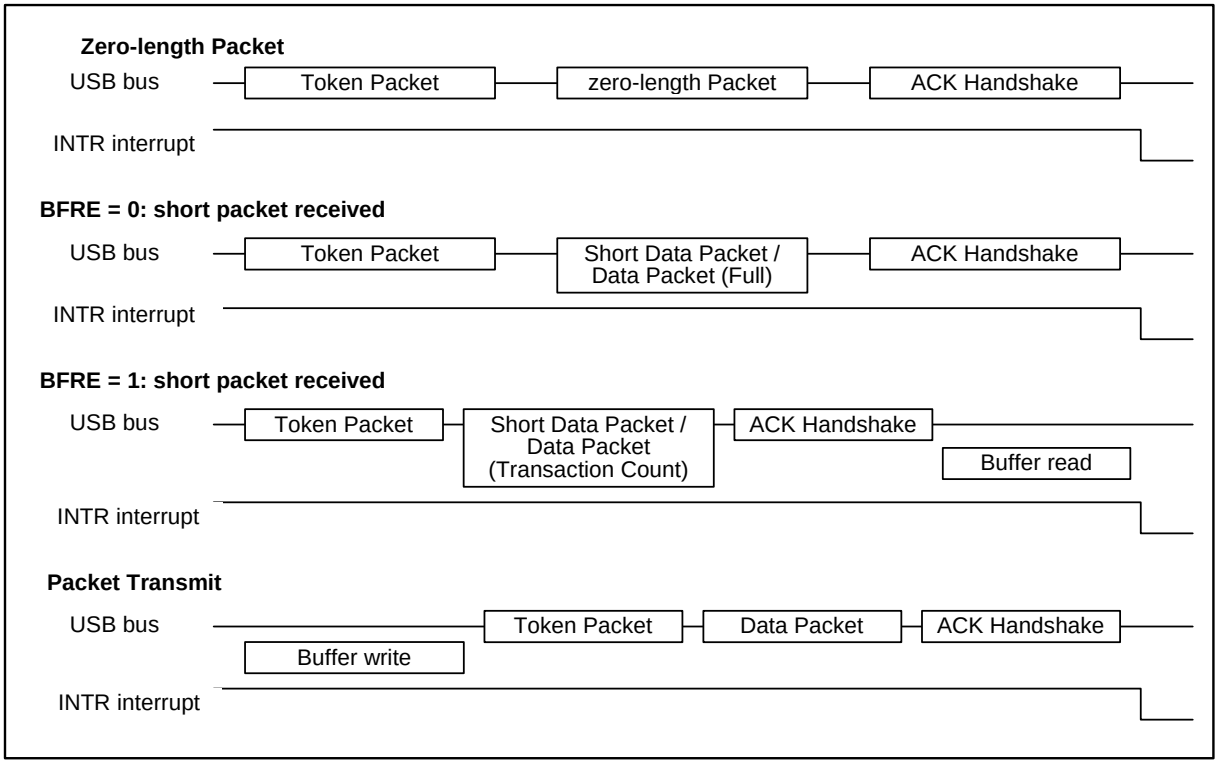


Figure 3.14 INTR interrupt occurring timing

3.3.7 PIPE Buffer Not Ready Interrupt

The timing of M66591INTN interrupt occurring is shown in Figure 3.15. The condition of INTN interrupt occurring is described below. The status of each PIPE is confirmed by the appropriate bit of Interrupt Status Register 1.

1. The case of sending data:
   When an IN token is received (data underrun) under the situation of PID bit of PIPE I Control Register is BUF setting and buffer memory is not ready.
2. The case of receiving data:
   When an OUT token is received (data overrun) under the situation of PID bit of PIPE I Control Register is BUF setting and buffer memory is not ready.

In control transfer status stage, a NAK response is not unready of buffer since respond by CCPL.

The interrupt request is stored in Interrupt Status Register 2 even if INTNE bit of INT Pin Configuration Register 0 and PIPEB_NRE6-1 bits, DCP_NRE bit of INT Pin Configuration Register 3 is disabled.

INTN bit of Interrupt Status Register 0 is cleared by clearing all bits of Interrupt Status Register 2.

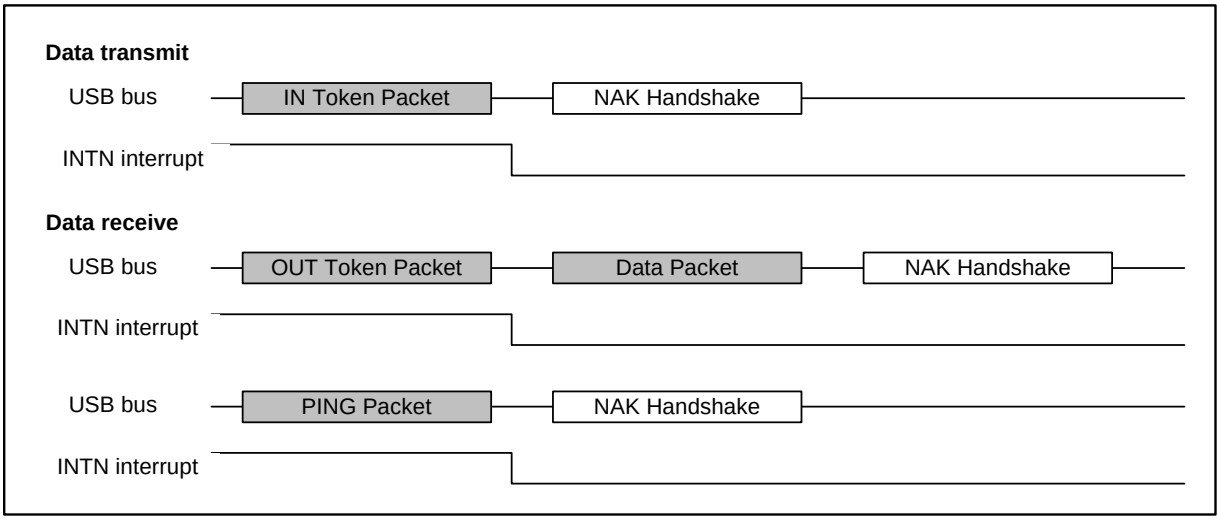


Figure 3.15 INTN interrupt occurring timing

3.3.8 PIPE Buffer Empty/Size Error Interrupt

The timing of M66591 BEMP interrupt occurring is shown in Figure 3.16. The condition of BEMP interrupt occurring is described below.

1. The case of sending data:
   When all of the data in the buffer memory is sent (buffer empty).

In addition, when buffer memory is used as double buffer, BEMP interrupt occurs if SIE side buffer becomes empty by the completion of data transmitting while CPU side buffer is empty. However, BEMP interrupt does not occur if SIE side buffer becomes empty by the completion of data transmitting while CPU side is writing.

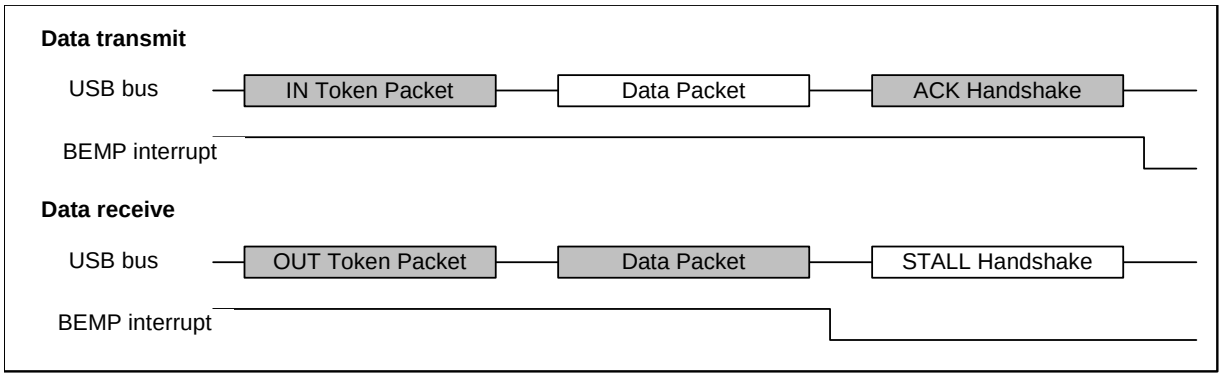


Figure 3.16 BEMP interrupt occurring timing

3.4 Control Transfer and Enumeration

The control transfer consists of the setup stage, data stage, and status stage. M66591 executes the stage control and notifies the CPU of the stage transition by the interrupt.

The control transfer executes the data transfer by using the default control PIPE (EP0).

DCP buffer memory is a fixed 256 bytes single buffer shared with control read and write. The read and write to the DCP buffer is executed via C_FIFO Port Register. C_FIFO Port Register can be accessed only by CPU access.

3.4.1 Setup Stage

According to USB Specification, M66591 respond ACK to setup packet.

USB Request Register 0, USB Request Register 1, USB Request Register 2 and USB Request Register 3 are exclusive registers for storing USB request. The VALID bit of Interrupt Status Register 0 is set to “1”, and PID [1:0] bits of DCP Control Register are set “00 (NAK)” when these request registers are renewed (New USB request is received.).

In order to confirm if new USB request is received, it is necessary to clear VALID bit of Interrupt Status Register 0 to “0” before respond to control transfer. The register bits shown below are protected when VALID = 1. So it is possible to respond to the newest request any time.

1. PID [1:0] bits of DCP Control Register
   These bits can not to be set to “01 (ACK)” to complete data stage when VALID = 1.
2. CCPL bit of DCP Control Register
   This bit can not to be set to “1” to complete status stage correctly (Respond zero-length packet and ACK) when VALID = 1.

M66591 judges if the control transfer is control read transfer or control write transfer or control write no data transfer according to the direction bit (bit 8 of bmRequestType) and request data length (wLength) automatically.

3.4.2 Data Stage

Using DCP buffer memory to send data according to USB request received.

Before access DCP buffer memory, it is necessary to specify the access direction by ISEL bit of C_FIFO Port Control Register 0. It is possible to transfer plural packets using INTR interrupt and BEMP interrupt.

NYET is responded according to the condition of buffer memory in control write transfer. Refer to “3.5.6 PING/NYET Control” about NYET response.

3.4.3 Status Stage

Complete control transfer only by accessing CCPL bit of DCP Control Register not using buffer memory.

M66591 does sending zero-length packet then receiving ACK or receiving zero-length packet then sending ACK.

3.4.4 Automatic Response Control

M66591 respond to correct SET_ADDRESS request automatically. It is necessary to respond to all request except for SET_ADDRESS by software. It is necessary to respond to SET_ADDRESS by software if any error shown below occurs.

1. In the case of control transfer except control read transfer, bmRequestTypq is not equal 0x00.
2. In the case of control transfer with an error, wIndex is not equal 0x00.
3. In the case of control transfer except control write no data transfer, wLength is not 0x00.
4. In the case of control transfer with an request error, wValue is large than 0x7F.
5. In the case of control transfer with an device state error, DVSQ is equal “011 (Configured State)”.

3.4.5 Overview of Control Transfer Operation

The overview of control transfer operation is shown in Figure 3.17 to Figure 3.22

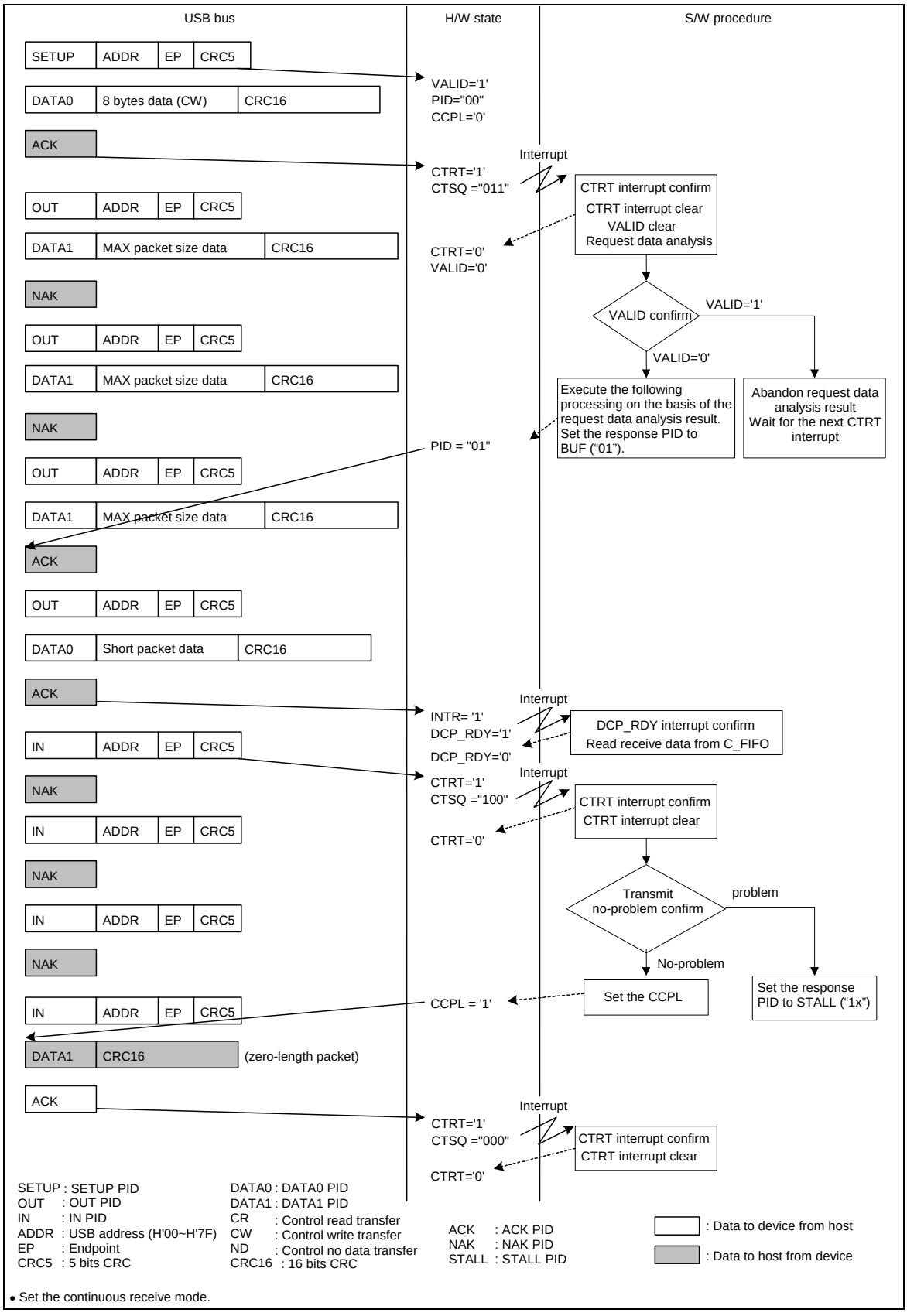


Figure 3.17 Examples of Control Write Transfer Operations

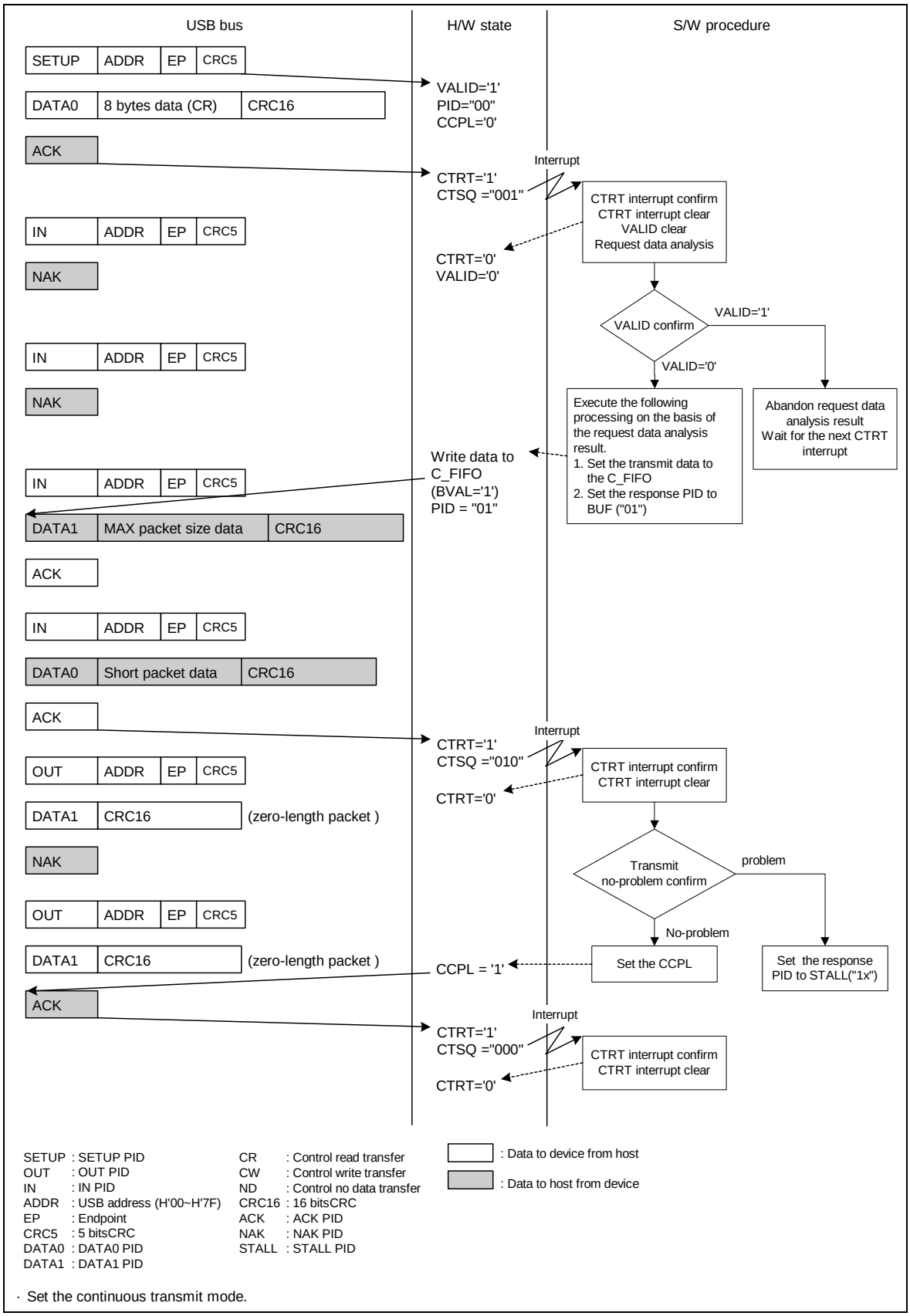


Figure 3.18 Examples of Control Read Transfer Operations

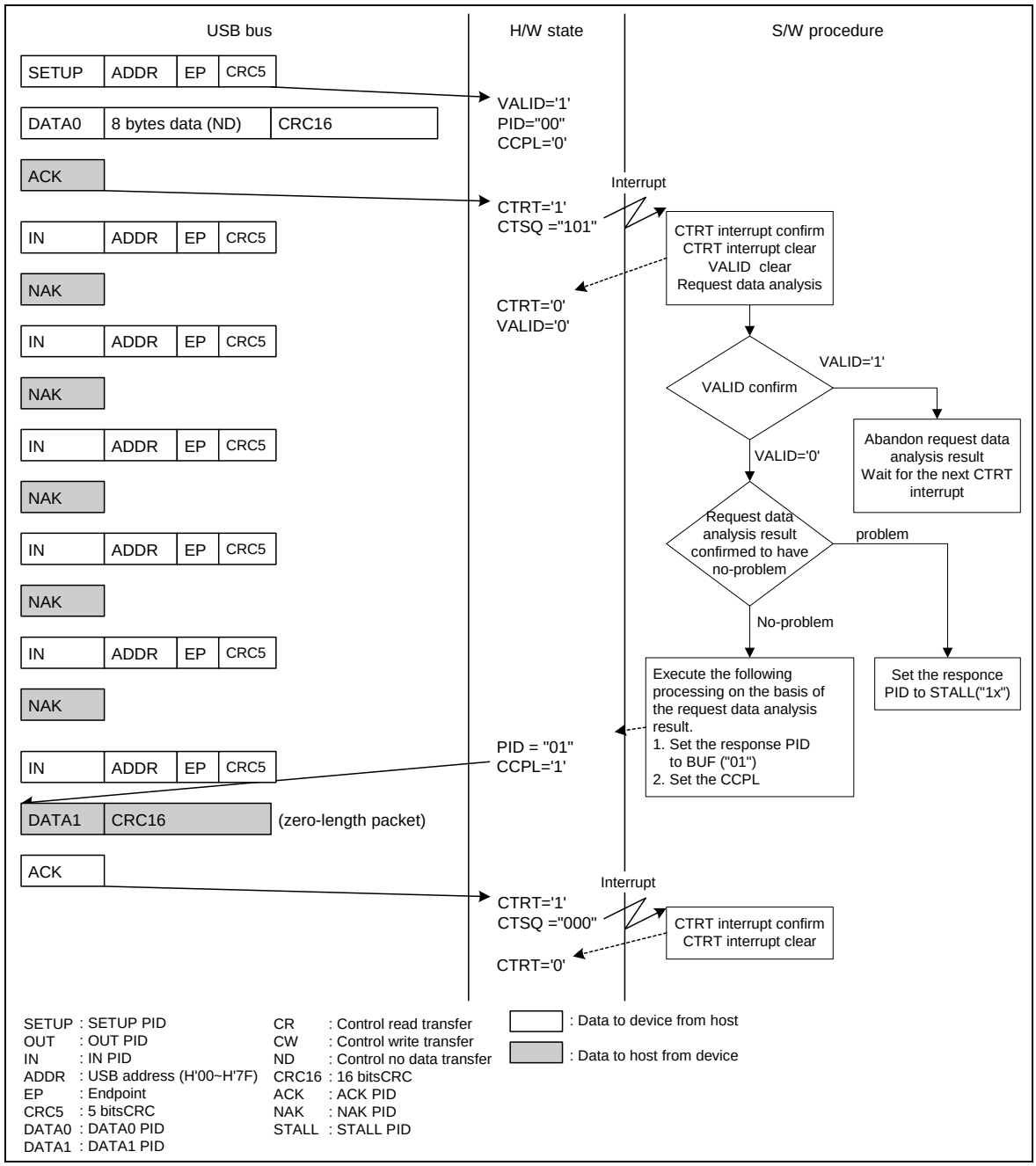


Figure 3.19 Examples of No Data Control Transfer Operations

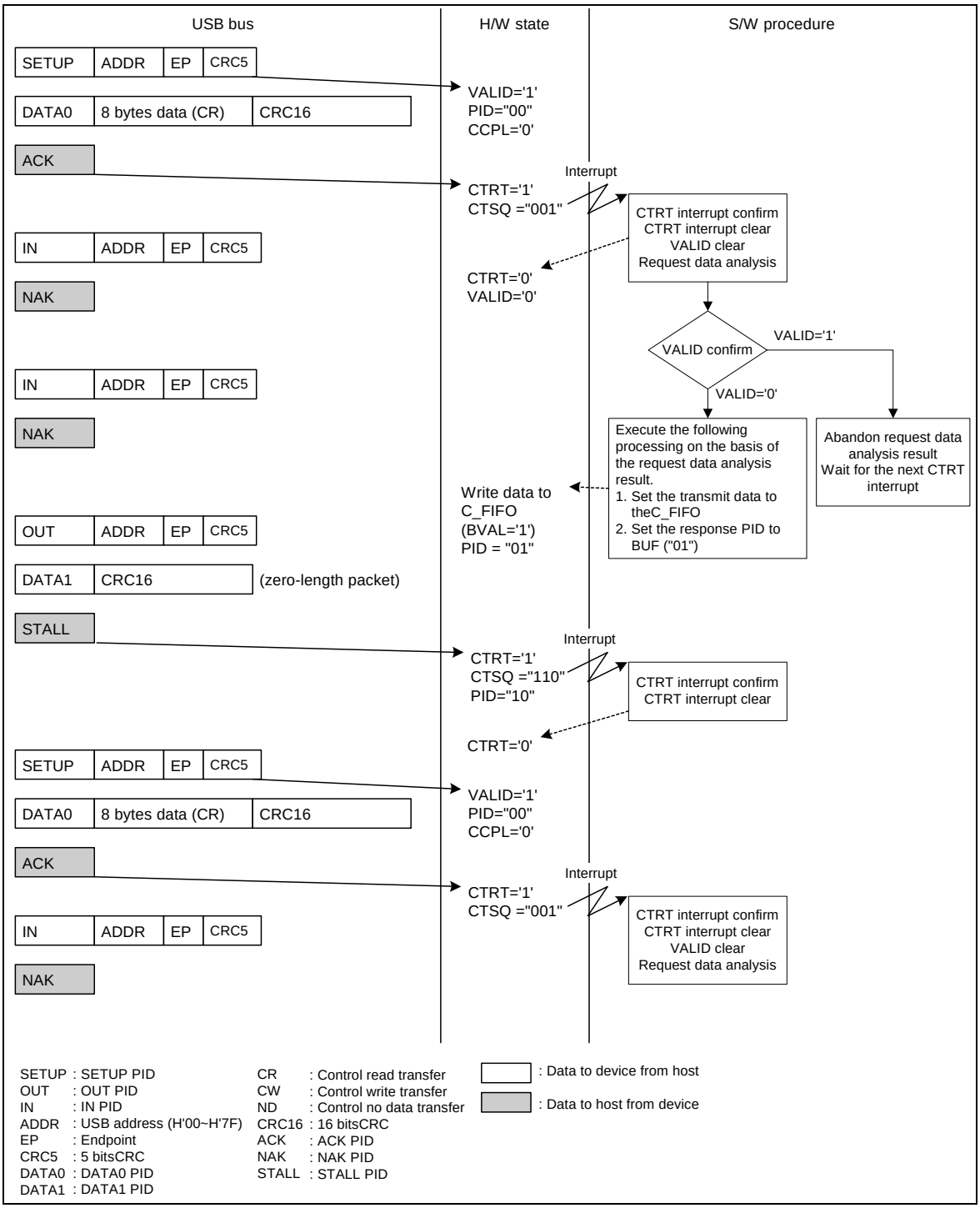


Figure 3.20 Examples of Control Transfer Error Operations

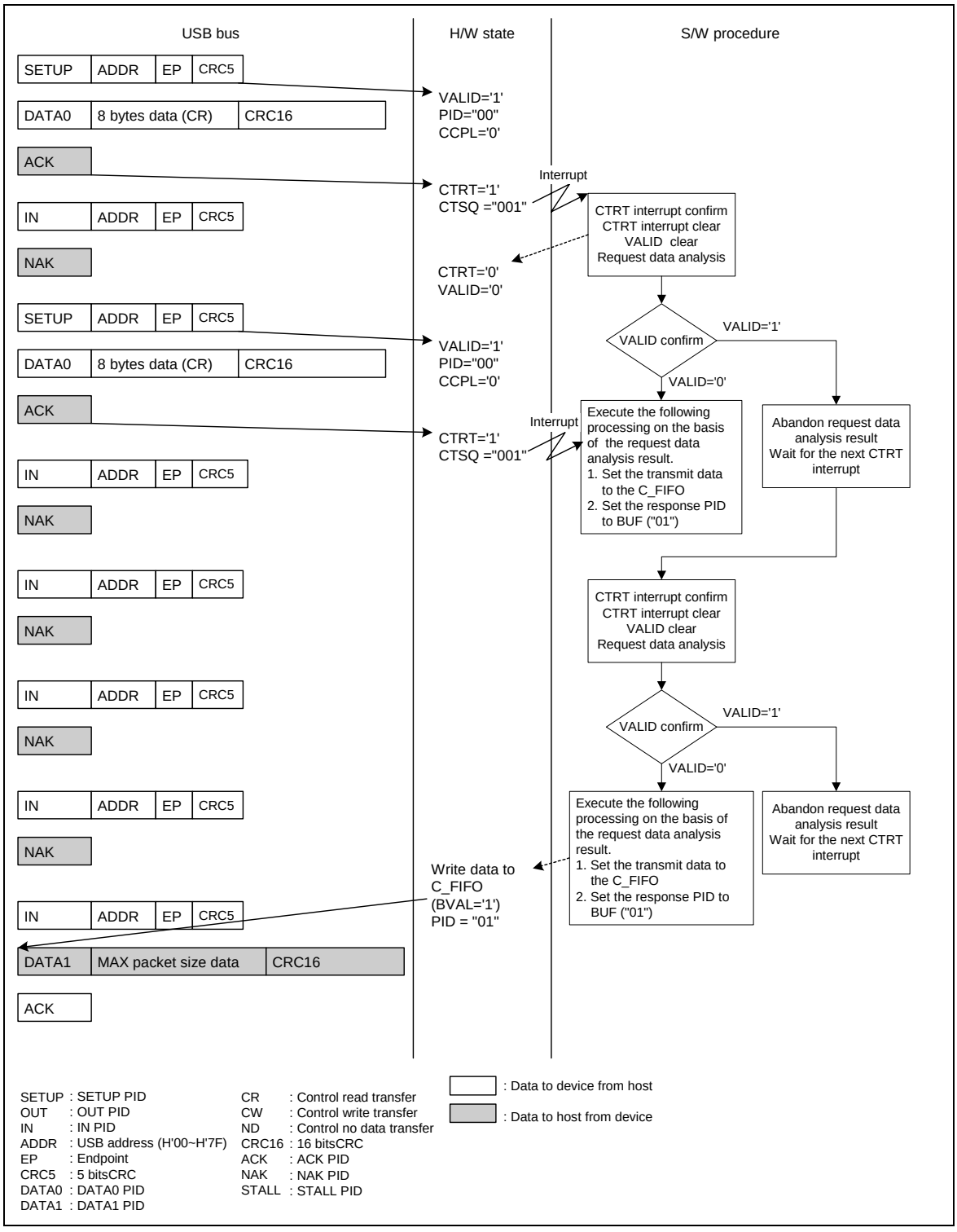


Figure 3.21 Examples of Setup Continuous Operations (1)

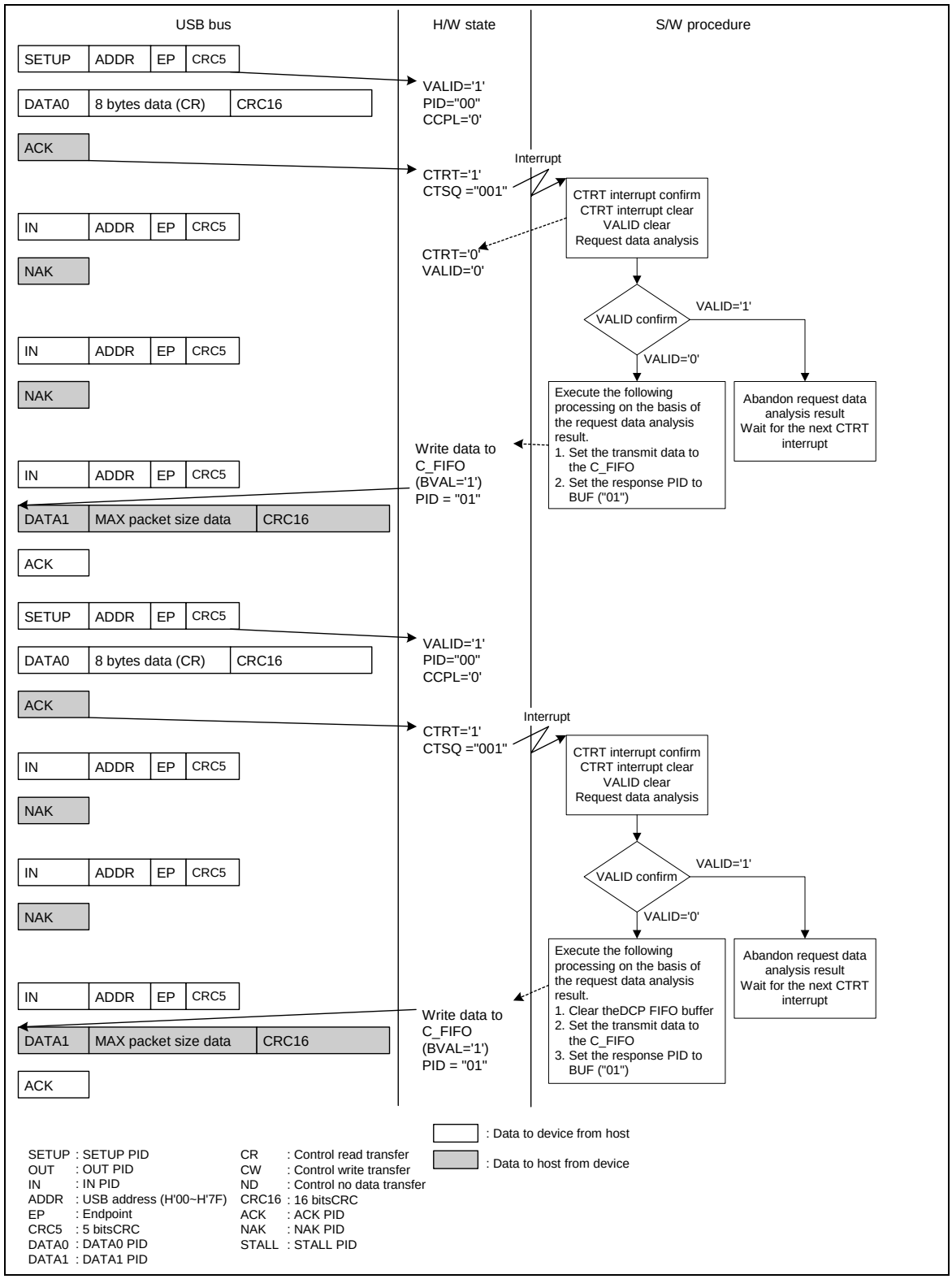


Figure 3.22 Examples of Setup Continuous Operations (2)

3.5 PIPE and PIPE Control

M66591 has 6PIPEs, PIPE1 to PIPE6, except for DCP. Each of these 6PIPEs (PIPE1 to PIPE6) can be set to bulk transfer and interrupt transfer. Table 3.4 shows configurations of PIPE1 to PIPE6.

Table 3.4 List of Setting to PIPEs (PIPE1 to PIPE6)

Register	Bits	Setting
DCP Configuration Register 1	CNTMD	Continuous Transmit/Receive Mode
DCP Configuration Register 2	DCP_MXPS [6:0]	DCP Maximum Packet Size
DCP Control Register	SQCLR	Sequence Toggle Bit Clear for DCP
	NYETMD	NYET Response Mode
	PID [1:0]	Response PID
PIPE Configuration Window Register 0	PEN	PIPE Enable or Disable
	ITMD	Interrupt Transfer Toggle Mode Only capability to PIPE5 and PIPE6.
	BFRE	Buffer Ready Interrupt Mode Only capability to PIPE1 to PIPE4.
	DBLB	Double Buffer Mode (Bulk Transfer Only) Only capability to PIPE1 to PIPE4. PIPE5 and PIPE6 is single buffer fixed.
	CNTMD	Continuous Transmit/Receive Mode Only capability to PIPE1 to PIPE4. PIPE5 and PIPE6 is Non-continuous transmit/received mode fixed.
	DIR	Transfer Direction Only capability to PIPE1 to PIPE4. PIPE5 and PIPE6 is IN direction fixed.
	EP_NUM [2:0]	Endpoint Number Show the selected endpoint number.
PIPEi Control Register (i=1~6)	ACLR	Buffer Automatic Clear Mode
	SQCLR	Sequence Bit Clear for PIPE1 to PIPE6
	NYETMD	NYET Response Mode Only capability to PIPE1 to PIPE4
	PID	Response PID

3.5.1 Transfer Type

The transfer type of each PIPE of M66591 is shown below.

DCP: Control transfer fixed.
PIPE1-4: Bulk transfer fixed.
PIPE5-6 Interrupt IN transfer fixed.

3.5.2 Endpoint Number

The endpoint number of M66591 is fixed. DCP is assigned to EP0, PIPE1 to PIPE6 are assigned to EP1 to EP6. The endpoint number can be read via EP_NUM [2:0] bits of PIPE Configuration Window Register 0.

3.5.3 Max Packet Size

The max packet size of DCP can be set by DCP_MXPS [6:0] bits of DCP Configuration Register 2. The max packet size of PIPE1 to PIPE6 is fixed. Follow is shown the setting of max packet size in the case of Hi-Speed mode and Full-Speed mode.

In the case of Hi-Speed mode,

- DCP is 64 bytes fixed.
- PIPE1 to PIPE4 is 512 bytes fixed.
- PIPE5 and PIPE6 is 64 bytes fixed.

In the case of Full-Speed mode,

- DCP can be selected from 8, 16, 32, 64 bytes.
- PIPE1 to PIPE4 is 64 bytes fixed.
- PIPE5 and PIPE6 is 64 bytes

3.5.4 Response PID

The response PID is set via PID [1:0] bits of DCP Control Register (DCPCtrl) and PIPE i Control Register (i=1~6). In some case, PID [1:0] bits will be set by M66591 H/W according to the results of transaction.

(1) The behavior of M66591 when PID [1:0] bits set by control S/W

NAK (H'00) setting: M66591 responds NAK to occurred transaction regardless of the status of PIPE buffer memory.

BUF (H'01) setting: M66591 responds to occurred transaction regarding to the status of PIPE buffer memory.

STALL (H'1x) setting: M66591 always responds STALL to occurred transaction. M66591 will not respond to isochronous IN when STALL setting.

Also, in the case of DCP, M66591 will always respond ACK to an setup transaction regardless of any PID setting by DCP, then store USB request to exclusive register.

(2) The case of PID [1:0] bits set by M66591 H/W

NAK (00) setting: When USB request is received correctly. (for DCP only)

BUF (01) setting: No this case.

STALL (1x) setting: When a max packet size over error in a received data packet or control transfer stage transition error is detected

It is necessary to set PID [1:0] bits of selected PIPE to NAK before set up the following registers.

(1) The ISEL bit of C_FIFO Port Control Register 0 (C_FIFOPortCtrl0) (only in the case of Current_PIPE [2:0] bits is set to DCP (000))
(2) The BCLR bit of C_FIFO Port Control Register 1 (C_FIFOPortCtrl1) (only in the case of Current_PIPE [2:0] bits is set to DCP (000))
(3) The TGL bit and SCLR bit of C_FIFO Port Control Register 2 (C_FIFOPortCtrl2)
(4) The ABCR bit, TREnb bit and TRclr bit of D0_FIFO Port Control Register 0 (D0_FIFOPortCtrl0)
(5) The TRNCNT [15:0] bits of D0_FIFO Port Control Register 3 (D0_FIFOPortCtrl3)
(6) The CNTMD bit of DCP Configuration Register 1 (DCPCfg1)
(7) The DCP_MXPS [6:0] bits DCP Configuration Register 2 (DCPCfg2)
(8) The SQCLR bit and NYETMD bit of DCP Control Register (DCPCtrl)
(9) The PEN bit, ITMD bit, BFRE bit, DBLB bit, CNTMD bit and DIR bit of PIPE Configuration Window Register 0 (PipeCfgWin0)
(10) The ACLR bit, SQCLR bit and NYETMD bit of PIPE i Control Register (i=1~6) (PipeiCtrl(i=1-6))

3.5.5 Data PID Sequence Bits

Data sequence bit is toggled by M66591 while the data transfer is performed correctly. The sequence bit changes at the timing of receiving ACK response when sending data or sending ACK response when receiving data. The data PID sequence bit can also be changed by setting SQCLR bits of DCP Control Register (DCPCtrl) and PIPE i Control Register (i=1~6) (PipeiCtrl(i=1-6)). The data PID of data stage of control transfer will be set as DATA1 by setting SQCLR bit of DCP to "1". The data PID of each PIPE will be set as DATA0 by setting SQCLR bits of PIPE1-6 to "1".

3.5.6 PING/NYET Control

The PING transfer control is valid only in case of bulk OUT transfer and the data stage OUT transfer of control write at the Hi-Speed mode.

(1) NYET response

The behavior of NYET response of each PIPE is set by the NYETMD bit of the PIPE i Control Register.

NYETMD = "0": A NYET response is automatically executed by M66591 H/W according to buffer status.

In this setting case, A NYET is responded as follows according to buffer mode setting:

- When the PIPE buffer is a single buffer setting, A NYET response is always executed.
- When the PIPE buffer is a double buffer setting, A NYET response is executed according to the FIFO buffer status.

When a short packet is received, A ACK response is executed regardless of the buffer status.

NYETMD = "1": A ACK/NAK response is always executed regardless of the buffer status. A NYET response is not executed.

(2) PING flow control

M66591 responds a ACK to PING packet when the buffer of the corresponding PIPE is ready for receiving data. Otherwise, M66591 responds a NAK and occurs a not ready interrupt when the buffer of the corresponding PIPE is not ready for receiving data.

3.5.7 Continuous Transfer Function

The PIPE buffer can operate either in the continuous mode or the non-continuous mode by setting CNTMD bit of DCP Configuration Register 1 (DCPCfg1) and PIPE Configuration Window Register 0 (PipeCfgWin0). This function is valid only for DCP and PIPE1-PIPE4. A example of the buffer memory operation is shown in Figure 3.23 when either the continuous mode or the non-continuous mode is selected.

The continuous transfer mode function can transmit/receive the multiple transactions data continuously. When the continuous transfer mode is selected, the data can be transferred until reaching the buffer size assigned in each PIPE without occurrence of interrupts to the CPU.

In the case of continuation transmitting mode, the written-in data is divided in the Max packet size, and then transmitted. To transmit smaller than the buffer size data (short packet, or an integral number of max packet size but smaller than the buffer size), it is necessary to set BVAL bit of C_FIFO Port Control Register 1 (C_FIFOPortCtrl1) and D0_FIFO Port Control Register 2 (D0_FIFOPortCtrl2) to “1”.

In the case of continuous receive mode, the data can be received continuously until reaching the buffer size, or completion of transaction counter, or a short packet is received without occurrence of interrupts every packet.

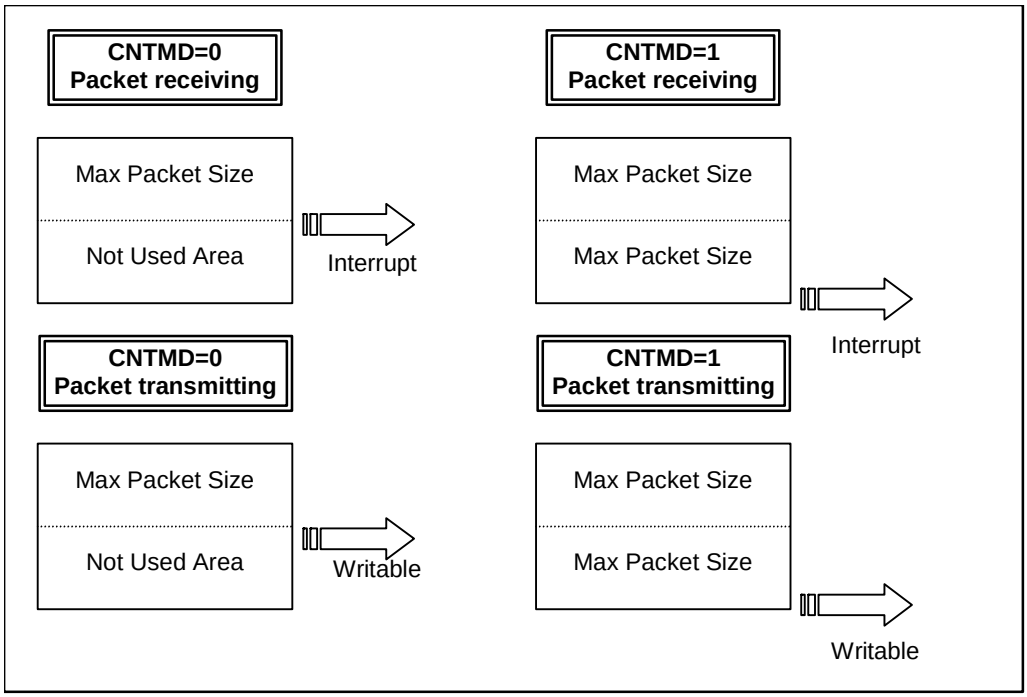


Figure 3.23 The Example of Buffer Memory Operation

3.5.8 Buffer auto clear mode function

All the data packets received are canceled by setting ACLR bit of PIPE i Control Register (i=1~6) (PipeiCtrl(i=1-6)) To “1”. In this mode M66591 receives data packet and respond a ACK. This function is valid only for reading buffer memory direction (the DIR bit of same register is set to “0”).

Also, the buffer memory of the PIPE can be cleared regardless of the access direction by setting ACLR bit to “1” and then setting to "0" continuously.

3.6 Buffer Memory

3.6.1 Buffer Memory Assignment and Buffer Area

The buffer memory of DCP and PIPE1-PIPE6 is assigned to a fixed buffer memory area and size. It is not necessary to assign by S/W.

The FIFO buffer memory area mapping is shown in Table 3.5.

Table 3.5 Buffer Memory Mapping

Buffer memory	Buffer size	Remark
Buffer for DCP	256 bytes	Single buffer, Continuous transfer
Buffer for PIPE1	1K bytes	Double buffer, Continuous transfer for Full-Speed mode
Buffer for PIPE2	1K bytes	Double buffer, Continuous transfer for Full-Speed mode
Buffer for PIPE3	512 bytes	Single buffer, Continuous transfer for Full-Speed mode
Buffer for PIPE4	512 bytes	Single buffer, Continuous transfer for Full-Speed mode
Buffer for PIPE5	64 bytes	Single buffer, Non-continuous transfer only
Buffer for PIPE6	64 bytes	Single buffer, Non-continuous transfer only

3.6.2 FIFO Buffer Access

The FIFO buffer assigned to the DCP and PIPE1 to PIPE6 of M66591 can be accessed via the two FIFO port registers. M66591 contains two FIFO port registers including C_FIFO port (for the CPU access) and D0_FIFO port (for the DMA access).

The FIFO port functional setting of M66591 is shown in Table 3.6.

In the case of access of writing data, the buffer will be ready (VALID state) automatically for transmitting when the data is written till the buffer full (or till the number of max packet size when the PIPE setting is non-continuous transmission). It is necessary to report the end of writing to let buffer be ready for transmitting fraction data by setting BVAL bit of "C_FIFO Port Control Register 1" and "D0_FIFO Port Control Register 2". It is possible to report the end of writing by DEND signal when DMA transfer is used.

In the case of access of reading data, the buffer will be ready (empty state) automatically for receiving new data packets when the all data in the buffer is read out. The received data length can be confirmed by the DTLN [9:0] bits of "C_FIFO Port Control Register 1" and "D0_FIFO Port Control Register 2". Although the buffer will be available to read (ready state) when a zero-length packet is received (DTLN = 0), no data can be read out. At this time, it is necessary to clear the buffer by the BCLR bit of the same register.

Table 3.6 The table of FIFO port functional setting

Register Name	Bit Name	Contents of Setting and Function
C_FIFO Port Control Register 0	RCNT	Read Count Mode
	REW	Buffer Rewind (Re-reading, Re-writing)
	MBW	FIFO Access Maximum Bit Width
	ISEL	DCP Buffer Select
	Current_PIPE [2:0]	C_FIFO Port Access PIPE Designate
C_FIFO Port Control Register 1	BVAL	Buffer Valid Flag
	BCLR	Buffer Clear
	FRDY	C_FIFO Port Ready
	CPU_DTLN	Receive Data Length
C_FIFO Port Control Register 2	TGL	CPU/SIE Buffer Toggle
	SCLR	SIE Buffer Clear
	SBUSY	SIE Buffer Busy
D0_FIFO Port Control Register 0	RCNT	Read Count Mode
	REW	Buffer Rewind (Re-reading, Re-writing)
	ABCR	Automatic Buffer Clear Mode, Only used for D0_FIFO port
	MBW	FIFO Access Maximum Bit Width
	TREnb	Transaction Counter Enable
	TRclr	Transaction Counter Clear
	Current_PIPE [2:0]	D0_FIFO Port Access PIPE Designate
D0_FIFO Port Control Register 2	BVAL	Buffer Valid Flag
	BCLR	Buffer Clear
	FRDY	D0_FIFO Port Ready
	DMA_DTLN	Receive Data Length
D0_FIFO Port Control Register 3	TRNCNT [15:0]	Transaction Counter

3.6.2.1 FIFO Port Select

The FIFO port access of each PIPE of M66591 is shown in Table 3.7. The PIPE accessed by C_FIFO Port Register or D0_FIFO Port Register can be selected by setting the PIPE number to Current_PIPE [2:0] bits of C_FIFO Port Control Register 0 or D0_FIFO Port Control Register 0.

Table 3.7 PIPE Buffer Access

PIPE	Access Method	Register Name
DCP	CPU access	C_FIFO Port Register 0
PIPE1 to PIPE6	CPU access	C_FIFO Port Register 0
	DMA access	D0_FIFO Port Register 0

The function of the PIPE which assigned to FIFO port can be selected by REW bit, MBW bit and Current_PIPE [2:0] bits of C_FIFO Port Control Register and D0_FIFO Port Control Register 0. ISEL bit should be used if the PIPE is DCP.

It is possible to suspend PIPE access under present access, to perform access to another PIPE, and then to perform the present PIPE processing continuously again. The REW bit of C_FIFO Port Control Register 0 and D0_FIFO Port Control Register 0 is used in the case of suspending PIPE access (do another PIPE processing), and then performing the present PIPE processing continuously again.

6 rewinds the access pointer of buffer memory if setting REW = "1" while selecting PIPE. Then it become possible to read or write data from the start pointer of buffer memory again. Moreover, if setting REW = "0" while selecting PIPE, it become possible to read or write data from the continuation pointer of buffer memory without rewinding the pointer of buffer memory.

To access FIFO port, it is necessary to confirm whether FRDY equals "1" after selecting PIPE.

3.6.2.2 The Buffer Status

The buffer status of 6 is shown in Table 3.8. The status of buffer memory can be confirmed BSTS bit of DCP Control Register and PIPEi Control Register (i=1-6).

Table 3.8 The Buffer Status

ISEL or DIR	BSTS	Status of buffer memory
0 (Receiving Direction)	0	No received data or under receiving operation, impossible to read data by CPU
0 (Receiving Direction)	1	Data received or zero-length packet received, possible to read data by CPU However, need to clear buffer when zero-length received
1 (Transmitting Direction)	0	Transmitting not completed, impossible to write data by CPU
1 (Transmitting Direction)	1	Transmitting completed, possible to write data by CPU

3.6.2.3 Buffer Clear

The clear method of each PIPE buffer memory is shown in Table 3.9. Buffer memory can be cleared by the 4 bits described below.

Table 3.9 Table of buffer clear method

Bit name	BCLR	SCLR	ABCR	ACLR
Register	C_FIFO Port Control Register 1 D0_FIFO Port Control Register 2	C_FIFO Port Control Register 2	D0_FIFO Port Control Register 0	PIPEi Control Register (i = 1-6)
Function	Clear CPU side buffer memory.	Clear SIE side buffer memory.	Clear buffer memory by H/W automatically after reading the data of the selected pipe. Refer to 3.7.6	The buffer clear mode to cancel all of received packets by H/W automatically. Refer to 3.5.8.
Clear method	Clear by writing “1” to this bit.	Clear by writing “1” to this bit.	“1”: Buffer clear “0”: Invalid	“1”: Disable automatic buffer clear “0”: Enable automatic buffer clear

3.6.2.4 Reading the buffer memory on the SIE side (CFIFO port reading direction)

Even in the "FRDY=0" state, when data cannot be read from the buffer memory, confirming the SBUSY bit in the CFIFOSIE register and setting "1" for the TGL bit makes it possible for the controller to read and access data on the SIE side.

When using this function, "PID=NAK" should be set and "SBUSY=0" confirmed, and then "TGL=1" written. M66591 is then able to read data from the C_FIFO Port Register.

The INTR interrupt is generated by operation of the TGL bit. "1" should not be written for the TGL bit in the when DCP is selected.

3.6.2.5 Clearing the buffer memory on the SIE side (CFIFO port writing direction)

Even in the "FRDY=0" state, when data cannot written to the buffer memory, M66591 can cancel data that is waiting to be sent, by the SBUSY bit and the SCLR bit of the C_FIFO Port Control Register.

When using this function, "PID=NAK" should be set and "SBUSY=0" confirmed, and then "SCLR=1" written. M66591 is then able to write new data from the C_FIFO Port Register.

The INTR and BEMP interrupt is generated by operation of the SCLR bit. "1" should not be written for the SCLR bit when DCP is selected.

3.6.3 Timing at which the FIFO port can be accessed

3.6.3.1 Timing at which the FIFO port can be accessed when switching pipes

Figure 3.24 shows a diagram of the timing up to the point where the FRDY bit and DTLN [9:0] bit are determined when the pipe specified by the FIFO port has been switched (the Current_PIPE [2:0] bits has been changed).

The same timing applies with respect to the C_FIFO port, when the ISEL bit is changed.

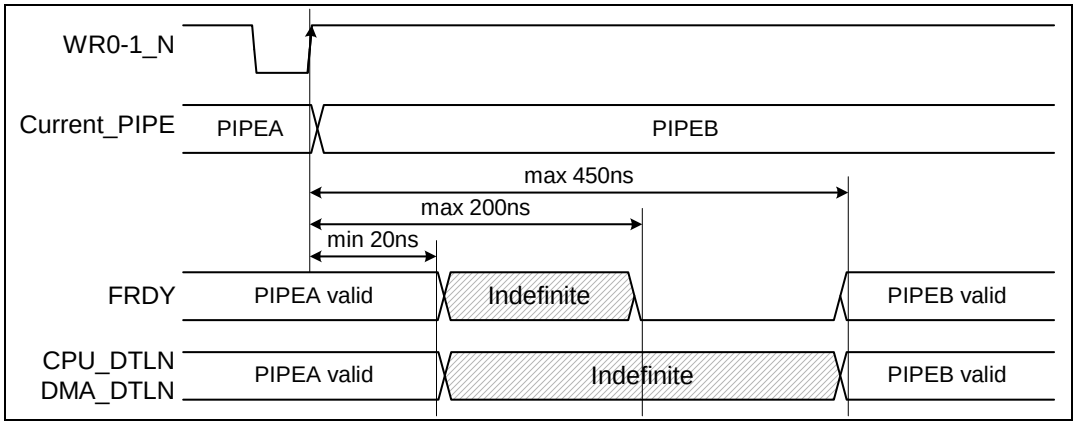


Figure 3.24 Timing at which the FRDY and DTLN bits are determined after changing a pipe

The FRDY and DTLN hold timing after PIPE changed : min 20ns
FRDY = "L" transit timing after PIPE changed : max 200ns
The FRDY and DTLN valid timing after PIPE changed : max 450ns

3.6.3.2 CPU_DTLN [9:0] and DMA_DTLN [9:0] timing when reading

Figure 3.25 shows a diagram of the timing up to the point when CPU_DTLN [9:0] bits and DMA_DTLN [9:0] bits are confirmed at the operation of FIFO access when the RCNT bit of C_FIFO Port Control Register and D0_FIFO Port Control Register is "1".

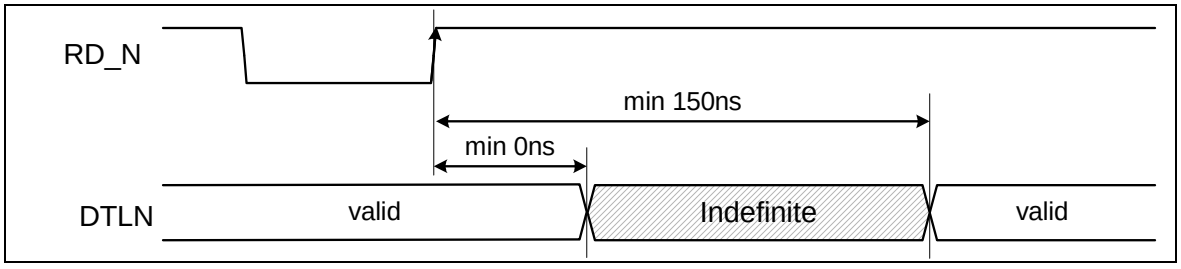


Figure 3.25 CPU_DTLN and DMA_DTLN timing at reading

The DTLN hold timing after FIFO read access : min 0ns
The DTLN valid timing after FIFO read access : max 150ns

Even in the time of FIFO accessing, there no CPU_DTLN [9:0] bits and DMA_DTLN [9:0] bits timing when RCNT="0".

3.6.3.3 Timing at which the FIFO port can be accessed after reading/writing has been completed when using a double buffer

Figure 3.26 shows the timing at which, when using a pipe with a double buffer, the other buffer can be accessed after reading from or writing to one buffer has been completed.

The same timing applies when a short packet is being sent based on the "BVAL=1" setting using the IN direction pipe.

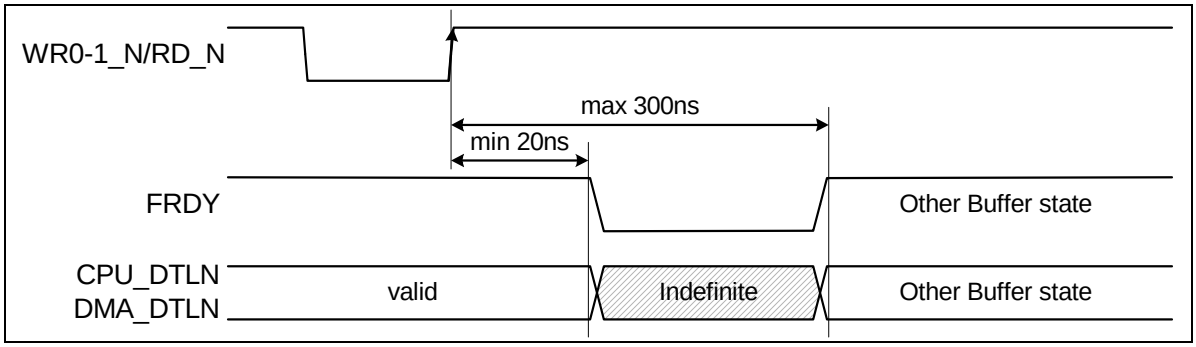


Figure 3.26 Timing at which the FRDY and DTLN bits are determined after reading from or writing to a double buffer has been completed

FRDY = "L" transit timing after FIFO access completed : min 20ns
The another buffer valid timing after double buffer FIFO access completed : max 300ns

3.7 DMA transfers

3.7.1 Overview of DMA transfers

The PIPE1-PIPE6 of M66591 can be accessed by DMA transfer with an external DMA controller in 16-bit/8-bit bus width. The DMA transfer between M66591 and external DMAC is forced by the handshake of DREQ/DACK pins or DREQ/(A7-1+CS_N) pins. For DMA transfers, there are two modes that can be selected. One is the cycle steal transfer mode, in which the DREQ signal is asserted each time a data element (8 or 16 bits) is transferred. The other is the burst transfer mode, in which the DREQ signal continues to be asserted until all of the data in the buffer memory has been transferred. The pipe targeted for the DMA transfer should be selected using the Current_PIPE [2:0] bits of the D0_FIFO Port Control Register 0. The selected pipe should not be changed during the DMA transfer. The DREQ pin is asserted when the PIPE buffer set by the Current_PIPE [2:0] bits of the D0_FIFO Port Control Register 0 is in read/write ready state.

The M66591 setting combination of DMA transfer is shown in Table 3.10. The DMA transfer setting can be set by Data Pin & FIFO/DMA Control Pin Configuration Register 1 and Data Pin & FIFO/DMA Control Pin Configuration Register 2.

Table 3.10 M66591 setting combination of DMA transfer

DMA transfer setting	Data Pin & FIFO/DMA Control Pin Configuration Register				The pin used by DMA transfer						
	1	2									
	DB_Cfg	DreqE	RWstb	DackE	D15-0	SD7-0	DREQ	DACK	AD7-1+CS	RD/WR	DSTB
DMA transfer by CPU bus (Using DACK)	0	1	0	1	√	------	√	√	------	√	------
DMA transfer by CPU bus (Using AD7-1 and CS)	0	1	0	0	√	------	√	------	√	√	------
DMA transfer split bus (Using SD7-1)	1	1	1	1	------	√	√	√	------	------	√

3.7.2 DMA transfer method

The DMA transfer can be selected as the cycle steal mode or the burst transfer mode. It can be selected by the Burst bit of Data Pin & FIFO/DMA Control Pin Configuration Register 2.

(1) Cycle steal mode (Burst = “0”)

At cycle steal mode, the DREQ pin is asserted at every one data (8-bit/16-bit) completion.

(A-1) DMA transfer control by the DACK pin and RD_N/WR0-1_N pins (DackE = “1”, RWstb = “0”):
At this mode, the DACK pin and RD_N/WR0-1_N pins are used to access the D0_FIFO Port Register 0. It is necessary to fix CS_N pin to “H” level at the access (DACK pin and RD_N/WR0-1_N pins are active at same time.).
Please refer to the (A-1) of the Figure 3.27

(A-2) DMA transfer control by the DACK pin and DSTB_N pin (DackE = “1”, RWstb = “1”):
At this mode, the DACK pin and DSTB_N pin are used to access the D0_FIFO Port Register 0. The RD_N/WR0-1_N pins are not used in this mode.
Please refer to the (A-2) of the Figure 3.27.

(A-3) DMA transfer control by the CS_N pin and the address pins (DackE = “0”, RWstb = “0”):
At this mode, the address pins, RD_N/WR0-1_N pins, and CS_N pin are used to access the D0_FIFO Port Register 0. The DACK pin is not used in this mode.
Please refer to the (A-3) of the Figure 3.27.

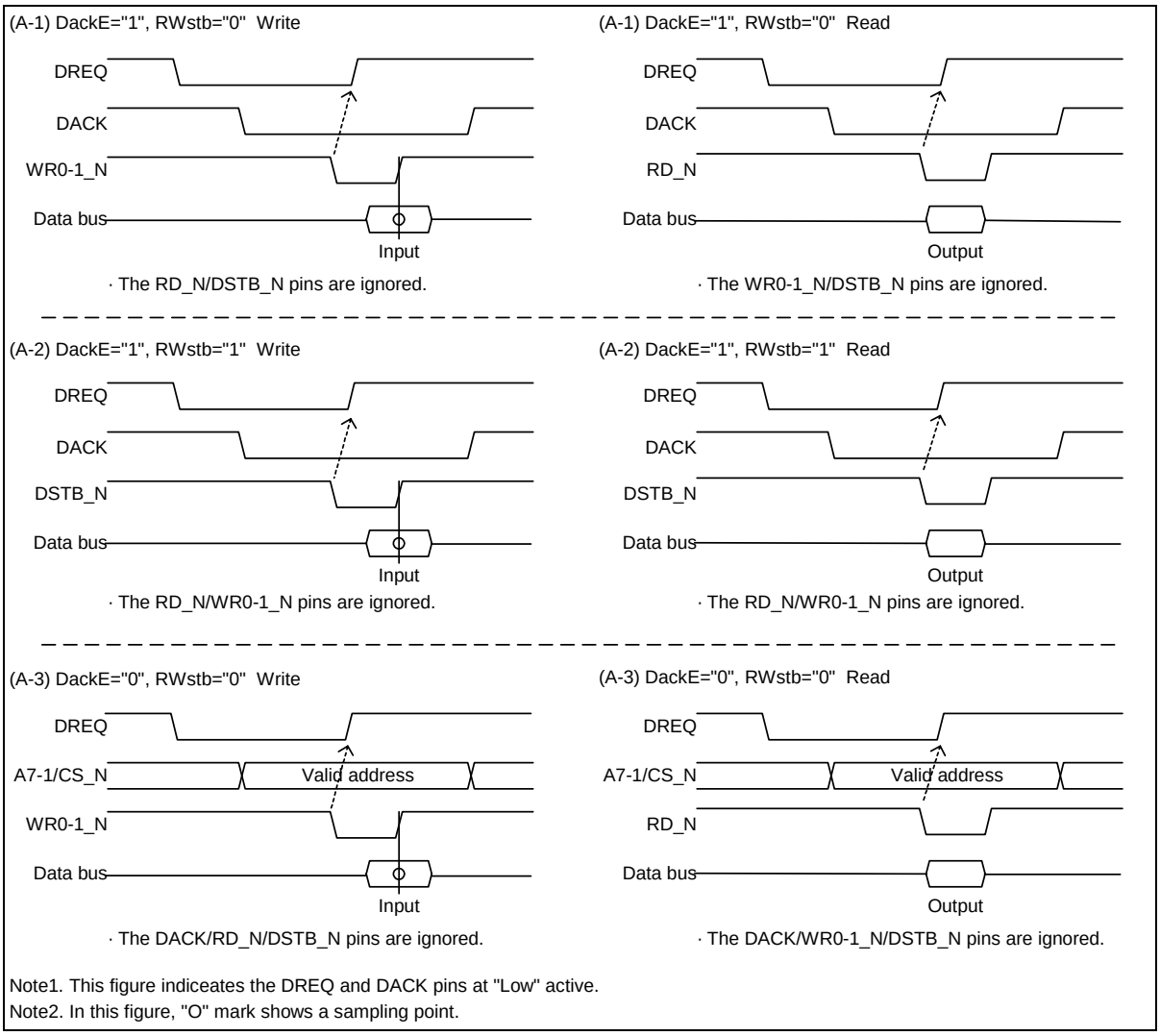


Figure 3.27 The access timing at DMA cycle steal transfer

(2) Burst mode (Burst = “1”)

At burst mode, the DREQ pin is asserted until all data transfers in the buffer are completed, and is negated when the transfer completes.

(B-1) DMA transfer control by the DACK pin and RD_N/WR0-1_N pins (DackE = “1”, RWstb = “0”):

At this mode, the DACK pin and RD_N/WR01_N pins are used to access the D0_FIFO Port Register 0. It is necessary to fix CS_N pin to “H” level at the access (DACK pin and RD_N/WR0-1_N pins are active at same time.).

Please refer to the (B-1) of the Figure 3.28.

(B-2) DMA transfer control by the DACK pin and DSTB_N pin (DackE = “1”, RWstb = “1”):

At this mode, the DACK pin and DSTB_N pin are used to access the D0_FIFO Port Register 0. The RD_N/WR0-1_N pins are not used in this mode.

Please refer to the (B-2) of the Figure 3.28.

(B-3) DMA transfer control by the CS_N pin and the address pins (DackE = “0”, RWstb = “0”):

At this mode, the address pins, RD_N/WR0-1_N pins, and CS_N pin are used to access the D0_FIFO Port Register 0. The DACK pin is not used in this mode.

Please refer to the (B-3) of the Figure 3.28

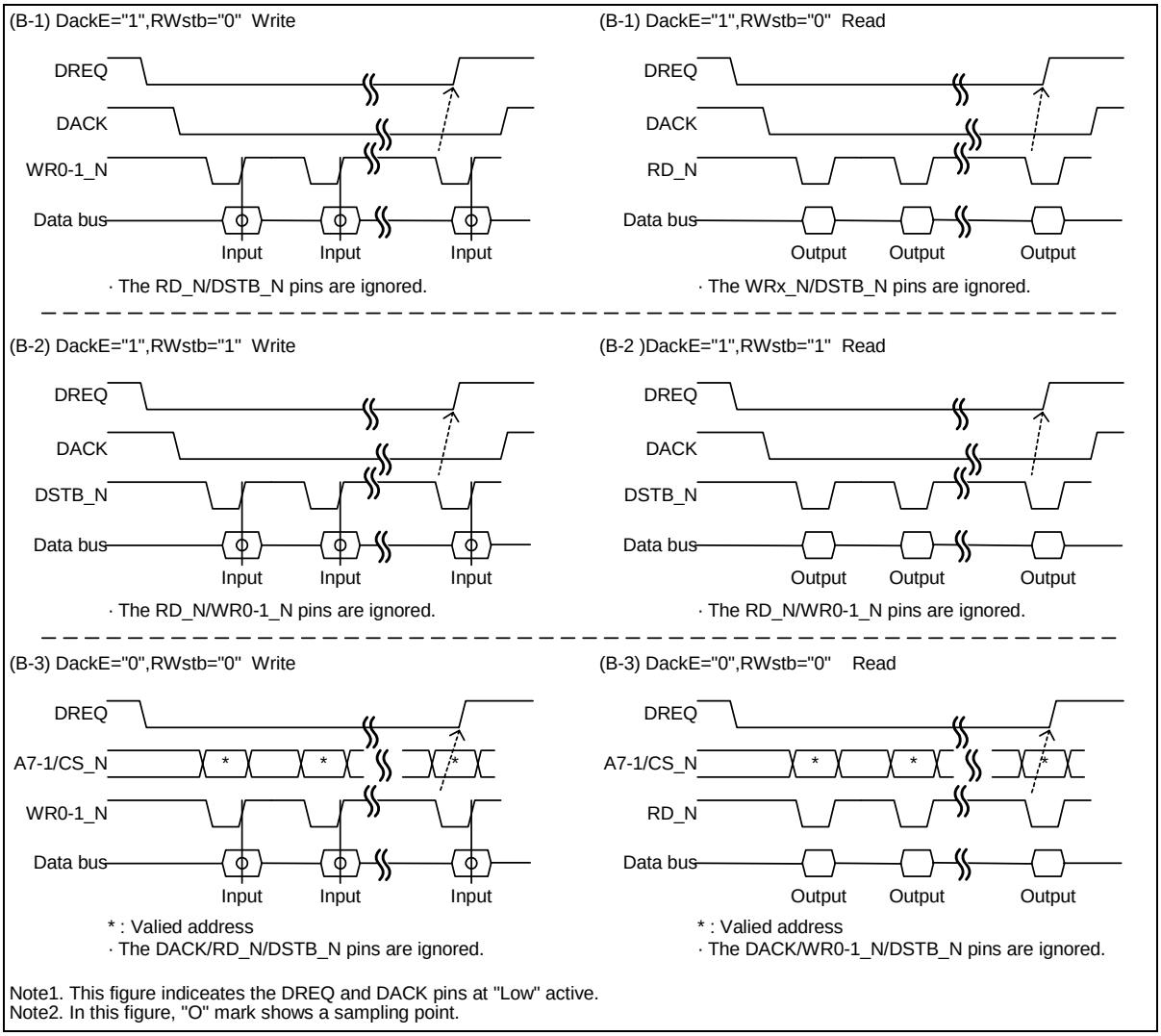


Figure 3.28 The access timing at DMA burst transfer

3.7.3 DEND Pin

M66591 is able to terminate DMA transfers that used the DEND pin. The DEND pin has separate input and output functions, depending on the USB data transfer direction.

(1) Buffer memory reading direction

The DEND pin becomes an output pin, making it possible to notify the external DMA controller of the final data transfer. The conditions under which the DEND signal is asserted can be set using the PKTM bit of Data Pin & FIFO/DMA Control Pin Configuration Register 2.

Table 3.11 shows the DEND pin assertion conditions for M66591.

Table 3.11 DEND pin assertions

Event / PKTM	Transaction count ended	INTR generated upon reception of packet	Reception of short packet other than zero-length packet	Reception of zero-length packet when buffer is not empty	Reception of zero-length packet when buffer is empty *1)
0	Asserted	Not asserted	Asserted	Asserted	Asserted
1	Asserted	Asserted	Asserted	Asserted	Not asserted

***1)** With reception of a zero-length packet when the buffer is empty, the DREQ signal is not asserted.

(2) Buffer memory writing direction

The DEND pin becomes the input pin, and data can be sent from the buffer memory (the same situation as when "BVAL=1" is set).

3.7.4 Obus bit

With this controller, the timing of the SD0-7 and DEND pin can be changed as shown in Table 3.12, using the Obus bit of Data Pin & FIFO/DMA Control Pin Configuration Register 2. The Obus bit is a function that is valid only for DMA transfers using a split bus. When using the CPU bus for DMA transfers, the setting of the Obus bit is ignored.

Table 3.12 Differences in operation based on the value set for the Obus bit

Direction	Obus bit setting	Operation
Reading	0	The SD0-7 and DEND signals are output on an ongoing basis, regardless of the control signal. The next data is output when the control signal is negated. This assures data setup time for the DMAC and enables high-performance DMA transfers.
	1	The SD0-7 and DEND signals are output after DACK and DSTB_N has been asserted. The SD0-7 and DEND signals go to the Hi-z state when DACK and DSTB_N are negated.
Writing	0	The SD0-7 and DEND signals can be input on an ongoing basis, regardless of the DACK_N signal. The DMAC can output the next data before the DACK_N signal is asserted. This assures data setup time for the controller and enables high-performance DMA transfers.
	1	The SD0-7 and DEND signals can be input only if the DACK_N signal is asserted. The SD0-7 and DEND signals are ignored if the DACK_N signal is negated.

If "Obus=0" is set in the reading direction, the SD0-7 and DEND signals are output on an ongoing basis, so please be aware that sharing the bus with another device can cause the signals to collide.

If "Obus=0" is set in the writing direction, the SD0-7 and DEND signals can be input on an ongoing basis, so the user should make sure that the signals are not set to an intermediate potential.

Figure 3.29 shows a schematic diagram of the data setup timing based on the Obus bit.

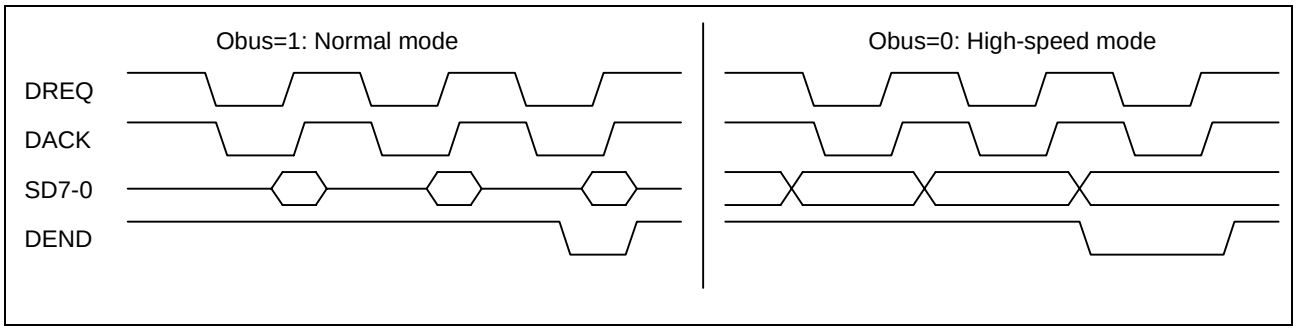


Figure 3.29 Schematic diagram of data setup timing

3.7.5 Transaction counter (D0_FIFO port reading direction)

The transaction counter is a function that operates when the pipe selected for the D0_FIFO port has been set in the direction of reading data from the buffer memory.

The transaction counter has a D0_FIFO Port Control Register 3 that specifies the number of transactions and a current counter that counts the transactions internally. When the current counter matches the number of transactions specified in the D0_FIFO Port Control Register 3, reading is enabled for the buffer memory. The current counter of the transaction counter function is initialized by the TRclr bit of D0_FIFO Port Control Register 0, so that the transactions can be counted again starting from the beginning.

The information read by the TRNCNT [15:0] bits of D0_FIFO Port Control Register 3 differs depending on the setting of the TREnb bit of D0_FIFO Port Control Register 0.

TREnb = 0: The set transaction counter value can be read.

TREnb = 1: The value of the current counter that counts the transactions internally can be read.

The conditions for changing the Current_PIPE [2:0] bits are as noted below.

1. The Current_PIPE [2:0] bits should not be changed until the transaction for the specified pipe has ended.
2. The Current_PIPE [2:0] bits cannot be changed if the current counter has not been cleared.

The operation conditions for the TRclr bit are as noted below.

1. If the transactions are being counted and “PID = BUF”, the current counter cannot be cleared.
2. If there is any data left in the buffer, the current counter cannot be cleared.

3.7.6 Automatic buffer clear mode (D0_FIFO port reading direction)

M66591 clears the pipe's buffer memory automatically at the timing of the completion of reading data from the buffer memory when ABCR bit of D0_FIFO Port Control Register 0 is set to “1”.

If using this function, it is unnecessary to clear buffer memory by control software evenif the buffer clear state is needed. So it is able to do DMA transfer without using control software. This function can be only used for buffer memory reading direction.

Table 3.13 shows the processing of receiving packet and clearing buffer memory.

Table 3.13 Packet receiving and buffer clear processing

Register setting / Buffer state when receiving	ABCR = “0”		ABCR = “1”	
	BFRE = “0”	BFRE = “1”	BFRE = “0”	BFRE = “1”
Buffer full	Unnecessary to clear	Unnecessary to clear	Unnecessary to clear	Unnecessary to clear
Receiving zero-length packet	**Necessary to clear**	**Necessary to clear**	**Unnecessary to clear**	**Unnecessary to clear**
Receiving normal short packet	Unnecessary to clear	**Necessary to clear**	Unnecessary to clear	**Unnecessary to clear**
Completion of trransaction counter	Unnecessary to clear	**Necessary to clear**	Unnecessary to clear	**Unnecessary to clear**

4 Electrical characteristics

4.1 Absolute maximum ratings

Symbol	Parameter	Ratings	Unit
VDD	Core supply voltage	-0.3 ~ +4.2	V
VIF	IO supply voltage	-0.3 ~ +4.2	V
AFEAVDD	USB transceiver block analog supply voltage	-0.3 ~ +4.2	V
AFEDVDD	USB transceiver block digital supply voltage	-0.3 ~ +4.2	V
BIASVDD	BIAS supply voltage	-0.3 ~ +4.2	V
PLLVDD	PLL supply voltage	-0.3 ~ +4.2	V
Vbus	Vbus input voltage	-0.3 ~ +5.5	V
V_I (IO)	System interface input voltage	-0.3 ~ VIF+0.3	V
V_O (IO)	System interface output voltage	-0.3 ~ VIF+0.3	V
Pd	Power dissipation	1250	mW
Tstg	Storage temperature	-55 ~ +150	°C

4.2 Recommended operating conditions

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
VDD	Core supply voltage		3.0	3.3	3.6	V
VIF	IO supply voltage	1.8V	1.7	1.8	2.0	V
		3.3V	2.7	3.3	3.6	V
AFEAVDD	USB transceiver block analog supply voltage		3.0	3.3	3.6	V
AFEDVDD	USB transceiver block digital supply voltage		3.0	3.3	3.6	V
BIASVDD	BIAS supply voltage		3.0	3.3	3.6	V
PLLVDD	PLL supply voltage		3.0	3.3	3.6	V
AFEAGND	USB transceiver block analog supply ground			0		V
AFEDGND	USB transceiver block digital supply ground			0		V
BIASGND	BIAS supply ground			0		V
PLLGND	PLL supply ground			0		V
DGND	Supply ground			0		V
V_I (IO)	System interface input voltage		0		VIF	V
V_I (Vbus)	Input voltage (only Vbus input)		0		5.25	V
V_O (IO)	System interface output voltage		0		VIF	V
Topr	Operating temperature		-20	+25	+85	°C
tr, tf	Input rise, fall time	Normal input			500	ns
		Schmidt trigger input			5	ms

4.3 Electrical Characteristics (VIF = 2.7~3.6V, VDD = 3.0~3.6V)

Symbol	Parameter		Conditions		Limits			Unit
					Min.	Typ.	Max.	
V_{IH}	High input voltage	Xin	VDD = 3.6V		2.52		3.6	V
V_{IL}	Low input voltage		VDD = 3.0V		0		0.9	V
V_{IH}	High input voltage	Note 1	VIF = 3.6V		0.7VIF		3.6	V
V_{IL}	Low input voltage		VIF = 2.7V		0		0.3VIF	V
VT+	Threshold voltage in positive direction	Note 2	VIF = 3.3V		1.4		2.4	V
VT-	Threshold voltage in negative direction				0.5		1.65	V
VTH	Hysteresis voltage					0.8		V
V_{OH}	High output voltage	Xout	VDD = 3.0V	I_{OH} = -50µA	2.6			V
V_{OL}	Low output voltage			I_{OL} = 50µA			0.4	V
V_{OH}	High output voltage	Note 3	VIF = 2.7V	I_{OH} = -2mA	VIF-0.4			V
V_{OL}	Low output voltage			I_{OL} = 2mA			0.4	V
V_{OL}	Low output voltage	Note 4	VIF = 2.7V	I_{OL} = 2mA			0.4	V
V_{OH}	High output voltage	Note 5	VIF = 2.7V	I_{OH} = -4mA	VIF-0.4			V
V_{OL}	Low output voltage			I_{OL} = 4mA			0.4	V
VT+	Threshold voltage in positive direction	Note 6	VDD = 3.3V		1.4		2.4	V
VT-	Threshold voltage in negative direction				0.5		1.65	V
I_{IH}	High input current		VIF = 3.6V	V_I = VIF			10	µA
I_{IL}	Low input current			V_I = GND			-10	µA
I_{OZH}	High output current in off status	Note 4	VIF = 3.6V	V_O = VIF			10	µA
I_{OZH}	High output current in off status	Note 5	VIF = 3.6V	V_O = VIF			10	µA
I_{OZL}	Low output current in off status			V_O = GND			-10	µA
Rdv	Pull-down resistance	Note 6				500		kΩ
Rdt	Pull-down resistance	Note 7				50		kΩ
Icc(A)	Average supply current at Full-Speed operation	Note 8	VDD = VIF = 3.3V, AFEAVDD = AFEDVDD = 3.3V, BIASVDD = PLLVDD = 3.3V Ta = 25°C PIPE1-4 Bulk transfer, PIPE5-6 Interrupt transfer			15		mA
			f(Xin) = 48MHz VDD = 3.6V, VIF = 3.6V, AFEAVDD = AFEDVDD = 3.6V, BIASVDD = PLLVDD = 3.6V PIPE1-4 Bulk transfer, PIPE5-6 Interrupt transfer			18		mA

Symbol	Parameter		Conditions	Limits			Unit
				Min.	Typ.	Max.	
Icc(A)	Average supply current at Hi-Speed operation	Note 8	VDD = VIF = 3.3V, AFEAVDD = AFEDVDD = 3.3V, BIASVDD = PLLVDD = 3.3V Ta = 25°C PIPE1-4 Bulk transfer, PIPE5-6 Interrupt transfer		180		mA
			f(Xin) = 48MHz VDD = 3.6V, VIF = 3.6V, AFEAVDD = AFEDVDD = 3.6V, BIASVDD = PLLVDD = 3.6V PIPE1-4 Bulk transfer, PIPE5-6 Interrupt transfer			280	mA
Icc(S)	Supply current in static mode	Note 8	USB suspend state f(Xin) clock stop state Ta = 25°C		30		uA
			USB suspend state f(Xin) clock stop state VDD = 3.6V, VIF = 3.6V, AFEAVDD = AFEDVDD = 3.6V, BIASVDD = PLLVDD = 3.6V			300	uA
C_{IN}	Pin density (Input)			4	7	15	pF
C_{OUT}	Pin density (Output, Input/Output)			4	7	15	pF

Note 1: A7-1, TEST0, TEST1, MPBUS input pins and D15-0, SD7-0 input/output pins
Note 2: CS_N, RD_N, WR0_N, WR1_N, DACK, DSTB_N, RST_N input pins and DEND input/output pin
Note 3: INT, DREQ output pins and DEND input/output pin
Note 4: CONF_ON, SUSP_ON output pins
Note 5: D15-0, SD7-0 input/output pins
Note 6: VBUS input pin (supply AFEDVDD)
Note 7: TEST0, TEST1 input pins
Note 8: The supply current is the total of VDD, VIF, AFEAVDD, AFEDVDD, BIASVDD and PLLVDD.

4.4 Electrical Characteristics (VIF = 1.7~2.0V, VDD = 3.0~3.6V)

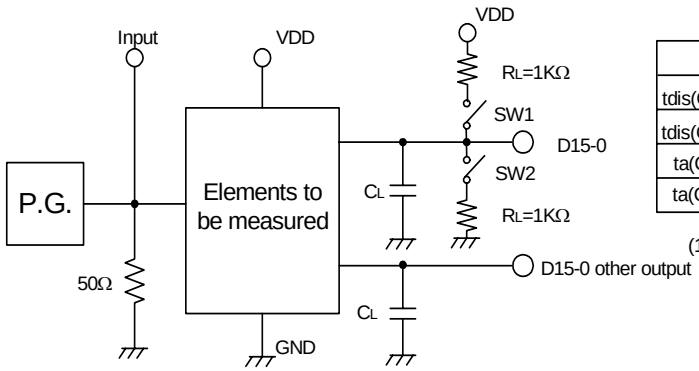
Symbol	Parameter		Conditions		Limits			Unit
					Min.	Typ.	Max.	
V_{IH}	High input voltage	Xin	VDD = 3.6V		2.52		3.6	V
V_{IL}	Low input voltage		VDD = 3.0V		0		0.9	V
V_{IH}	High input voltage	Note 1	VIF = 2.0V		0.7VIF		2.0	V
V_{IL}	Low input voltage		VIF = 1.7V		0		0.3VIF	V
VT+	Threshold voltage in positive direction	Note 2	VIF = 1.8V		0.7		1.4	V
VT-	Threshold voltage in negative direction				0.2		0.8	V
VTH	Hysteresis voltage					0.5		V
V_{OH}	High output voltage	Xout	VDD = 3.0V	I_{OH} = -50µA	2.6			V
V_{OL}	Low output voltage			I_{OL} = 50µA			0.4	V
V_{OH}	High output voltage	Note 3	VIF = 1.7V	I_{OH} = -2mA	VIF-0.4			V
V_{OL}	Low output voltage			I_{OL} = 2mA			0.4	V
V_{OL}	Low output voltage	Note 4	VIF = 1.7V	I_{OL} = 2mA			0.4	V
V_{OH}	High output voltage	Note 5	VIF = 1.7V	I_{OH} = -4mA	VIF-0.4			V
V_{OL}	Low output voltage			I_{OL} = 4mA			0.4	V
VT+	Threshold voltage in positive direction	Note 6	VDD = 3.3V		1.4		2.4	V
VT-	Threshold voltage in negative direction				0.5		1.65	V
I_{IH}	High input current		VIF = 2.0V	V_I= VIF			10	µA
I_{IL}	Low input current			V_I = GND			-10	µA
I_{OZH}	High output current in off status	Note 4	VIF = 2.0V	Vo = VIF			10	µA
I_{OZH}	High output current in off status	Note 5	VIF = 2.0V	Vo = VIF			10	µA
I_{OZL}	Low output current in off status			Vo = GND			-10	µA
Rdv	Pull-down resistance	Note 6				500		kΩ
Rdt	Pull-down resistance	Note 7				50		kΩ
Icc(A)	Average supply current in operation mode (in Full-Speed)	Note 8	VDD = 3.3V, VIF = 1.8V, AFEAVDD = AFEDVDD = 3.3V, BIASVDD = PLLVDD = 3.3V Ta = 25°C PIPE1-4 Bulk transfer, PIPE5-6 Interrupt transfer			15		mA
			f(Xin) = 48MHz VDD = 3.3V, VIF = 2.0V, AFEAVDD = AFEDVDD = 3.6V, BIASVDD = PLLVDD = 3.6V PIPE1-4 Bulk transfer, PIPE5-6 Interrupt transfer				18	mA

Symbol	Parameter		Conditions	Limits			Unit
				Min.	Typ.	Max.	
Icc(A)	Average supply current in operation mode (in Hi-Speed)	Note 8	VDD = 3.3V, VIF = 1.8V, AFEAVDD = AFEDVDD = 3.3V, BIASVDD = PLLVDD = 3.3V Ta = 25°C PIPE1-4 Bulk transfer, PIPE5-6 Interrupt transfer		180		mA
			f(Xin) = 48MHz VDD = 3.6V, VIF = 2.0V, AFEAVDD = AFEDVDD = 3.6V, BIASVDD = PLLVDD = 3.6V PIPE1-4 Bulk transfer, PIPE5-6 Interrupt transfer			280	mA
Icc(S)	Supply current in static mode	Note 8	USB suspend state f(Xin) clock stop state Ta = 25°C		30		uA
			USB suspend state f(Xin) clock stop state VDD = 3.6V, VIF = 2.0V, AFEAVDD = AFEDVDD = 3.6V, BIASVDD = PLLVDD = 3.6V PIPE1-4 Bulk transfer, PIPE5-6 Interrupt transfer			300	uA
C_{IN}	Pin density (Input)			4	7	15	pF
C_{OUT}	Pin density (Output, Input/Output)			4	7	15	pF

Note 1: A7-1, TEST0, TEST1, MPBUS input pins and D15-0, SD7-0 input/output pins
Note 2: CS_N, RD_N, WR0_N, WR1_N, DACK, DSTB_N, RST_N input pins and DEND input/output pin
Note 3: INT, DREQ output pins and DEND input/output pin
Note 4: CONF_ON, SUSP_ON output pins
Note 5: D15-0, SD7-0 input/output pins
Note 6: VBUS input pin (supply AFEDVDD)
Note 7: TEST0, TEST1 input pins
Note 8: The supply current is the total of VDD, VIF, AFEAVDD, AFEDVDD, BIASVDD and PLLVDD.

4.5 Measurement circuit

4.5.1 Pins except for USB buffer block

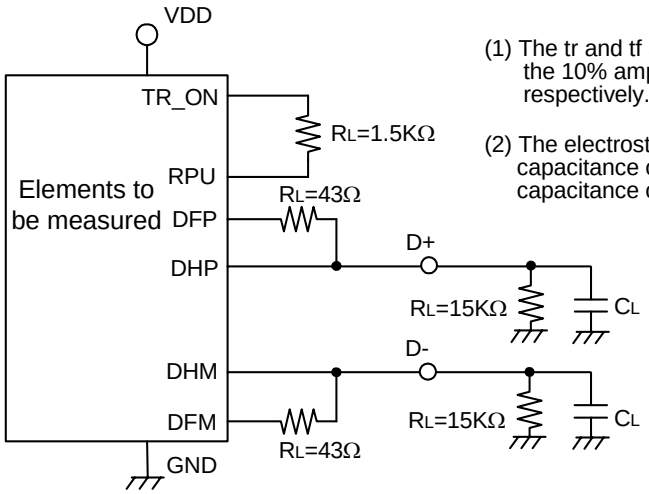


Item	SW1	SW2
tdis(CTRL(LZ))	close	open
tdis(CTRL(HZ))	open	close
ta(CTRL(ZL))	close	open
ta(CTRL(ZH))	open	close

(1) Input pulse level : 0 ~ 3.3V, 0 ~ 1.8V
Input pulse rise/fall time : tr,tf=3ns
Input timing standard voltage : VIF/2
Output timing judge voltage : VIF/2
(The tdis (LZ) is judged by 10% of the output amplitude and the tdis (HZ) by 90% of the output amplitude.)

(2) The electrostatic capacity CL includes the stray capacitance of the wire connection and the input capacitance of the probe.

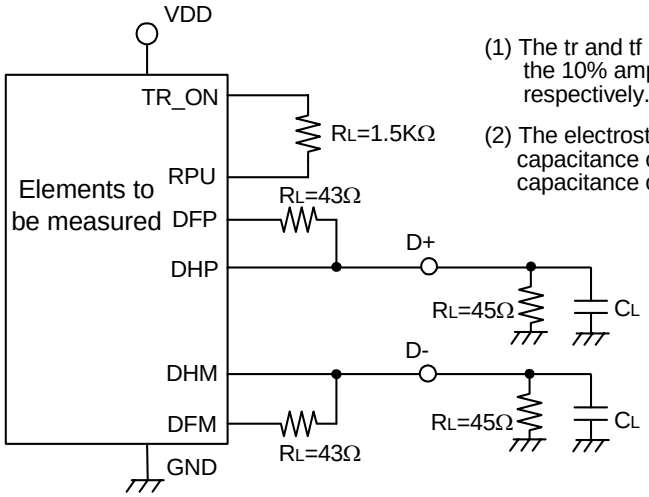
4.5.2 USB buffer block (Full-Speed)



(1) The tr and tf are judged by the transition time of the 10% amplitude point and 90% amplitude point respectively.

(2) The electrostatic capacity CL includes the stray capacitance of the wire connection and the input capacitance of the probe.

4.5.3 USB buffer block (Hi-Speed)



(1) The tr and tf are judged by the transition time of the 10% amplitude point and 90% amplitude point respectively.

(2) The electrostatic capacity CL includes the stray capacitance of the wire connection and the input capacitance of the probe.

4.6 Electrical characteristics (D+/D-)

4.6.1 DC characteristics

Symbol	Parameter	Conditions		Limits			Unit
				Min.	Typ.	Max.	
R_s	Serial resistance between DFP (DFM) and DHP (DHF)			42.57	43	43.43	Ω
R_o	Output impedance	Include serial resistance Rs		40.5	45	49.5	Ω
R_{pu}	D+ pull-up resistance			1.425	1.5	1.575	KΩ
Input characteristics when set to Full-Speed							
V_{IH}	High input voltage			2.0			V
V_{IL}	Low input voltage					0.8	V
V_{DI}	Differential input sensitivity	| (D+) - (D-) |		0.2			V
V_{CM}	Differential common mode range			0.8		2.5	V
Output characteristics when set to Full-Speed							
V_{OL}	Low output voltage	AFEAVDD = 3.0V	RL of 1.5KΩ to 3.6V			0.3	V
V_{OH}	High output voltage		RL of 15KΩ to GND	2.8		3.6	V
V_{OSE1}	SE1 output voltage			0.8			V
V_{ORS}	Output signal crossover voltage	CL = 50pF		1.3		2.0	V
Input characteristics when set to Hi-Speed							
V_{HSSQ}	Squelch detection threshold voltage (Differential voltage)			100		150	mV
V_{HSCM}	Common mode voltage range			-50		500	mV
Output characteristics when set to Hi-Speed							
V_{HSOI}	Idle state			-10.0		10	mV
V_{HSOH}	High output voltage			360		440	mV
V_{HSOL}	Low output voltage			-10.0		10	mV
V_{CHIRPJ}	Chirp J output voltage (Differential)			700		1100	mV
V_{CHIRPK}	Chirp K output voltage (Differential)			-900		-500	mV

4.6.2 AC characteristics (Full-Speed)

Symbol	Parameter	Conditions		Limits			Unit
				Min.	Typ.	Max.	
tr	Rise transition time	10% to 90% of the data signal: amplitude	CL = 50pF	4		20	ns
tf	Fall transition time	90% to 10% of the data signal: amplitude	CL = 50pF	4		20	ns
TRFM	Rise/fall time matching	tr/tf		90		111.11	%

4.7 Switching Characteristics (VIF = 3.0~3.6V or 1.7~2.0V)

Symbol	Parameter	Conditions, others	Limits			Unit	Refer No.
			Min.	Typ.	Max.		
ta (A)	Address access time	CL=50pF			40	ns	1
tv (A)	Data valid time after address	CL=10pF	2			ns	2
ta (CTRL - D)	Data access time after control	CL=50pF			30	ns	3
tv (CTRL - D)	Data valid time after control	CL=10pF	2			ns	4
ten (CTRL - D)	Data output enable time after control		2			ns	5
tdis (CTRL - D)	Data output disable time after control	CL=50pF			30	ns	6
ta (CTRL - DV)	Data access time after control when set to split bus (DMA Interface) Obus=0	CL=30pF			30	ns	9
tv (CTRL – DV)	Data valid time after control when set to split bus (DMA Interface) Obus=0	CL=10pF	2			ns	10
ta (CTRL - DendV)	DEND output access time after control	CL=30pF			30	ns	11
tv (CTRL - DendV)	DEND output valid time after control	CL=10pF	2			ns	12
ta (CTRL - Dend)	DEND output access time after control when set to split bus (DMA Interface) Obus=1	CL=30pF			30	ns	13
tv (CTRL - DendV)	DEND output valid time after control when set to split bus (DMA Interface) Obus=1	CL=10pF	2			ns	14
ten (CTRL - DendV)	DEND output enable time after control when set to split bus (DMA Interface) Obus=1		2			ns	15
tdis (CTRL-DendV)	DEND output disable time after control when set to split bus (DMA Interface) Obus=1	CL=30pF			30	ns	16
tdis (CTRL – Dreq)	DREQ output disable time after control				70	ns	17
tdis (CTRLH –Dreq)	DREQ output disable time after control when completed transfer End signal by the DEND signal				70	ns	18
ten (CTRL – Dreq)	DREQ output enable time after control		30			ns	19
twh (Dreq)	DREQ output high pulse width		20		50	ns	20
td (CTRL - INT)	INT output negate delay time				250	ns	21
twh (INT)	INT output high pulse width		650			ns	22
td (DREQ - DV)	Data access time after starting assert the DREQ signal when set to split bus Obus=0				0	ns	23
td (DREQ - DendV)	DEND output access time after starting assert the DREQ signal when set to split bus Obus=0				0	ns	24

4.8 Required Timing Conditions (VIF = 3.0~3.6V or 1.7~2.0V)

Symbol	Parameter		Conditions, others	Limits			Unit	Refer No.
				Min.	Typ.	Max.		
tsuw (A)	Address write setup time		CL=50pF	30			ns	30
tsur (A)	Address read setup time			0			ns	31
tsu (A - ALE)	Address write setup time when multiplex bus			10			ns	32
thw (A)	Address write hold time			0			ns	33
thr (A)	Address read hold time			30			ns	34
th (A - ALE)	Address hold time when multiplex bus			0			ns	35
tw (ALE)	ALE pulse width when multiplex bus			10			ns	36
tdwr (ALE - CTRL)	Write/read delay time when multiplex bus			7			ns	37
trec (ALE)	ALE recovery time when multiplex bus			0			ns	38
tw (CTRL)	Control pulse width (Write)			30			ns	39
trec (CTRL)	Control recovery time (FIFO)			30			ns	40
trecr (CTRL)	Control recovery time (REG)			12			ns	41
twr (CTRL)	Control pulse width (Read)			30			ns	42
tsu (D)	Data setup time			20			ns	43
th (D)	Data hold time			0			ns	44
tsu (Dend)	DEND input setup time			30			ns	45
th (Dend)	DEND input hold time			0			ns	46
tw (cycle)	FIFO access cycle time	8-bit FIFO access		30			ns	47
		16-bit FIFO access		50			ns	
		8/16-bit FIFO access when multiplex bus		84			ns	
tw (CTRL_B)	Control pulse width when set to burst transfer	when set to split bus Obus=0		12			ns	48
		when set to split bus Obus=1 (*1)		30			ns	
		When using DMA transfers with CPU bus		30			ns	
trec (CTRL_B)	Control recovery time when set to burst transfer			12			ns	49
tsud (A)	DMA address write setup time			15			ns	50
thd (A)	DMA address write hold time			0			ns	51
tw (RST)	Reset pulse width time			100			ns	52
tst (RST)	Control start time after reset			500			ns	53

*1) Only for data writing, when the DACK0_N signal is assuring an active period of at least 30 ns, the DSTB0_N signal can be accessed at a minimum of 12 ns.

4.9 Timing diagrams

Table 4.1 and Table 4.2 shows index for register access and FIFO of M66591.

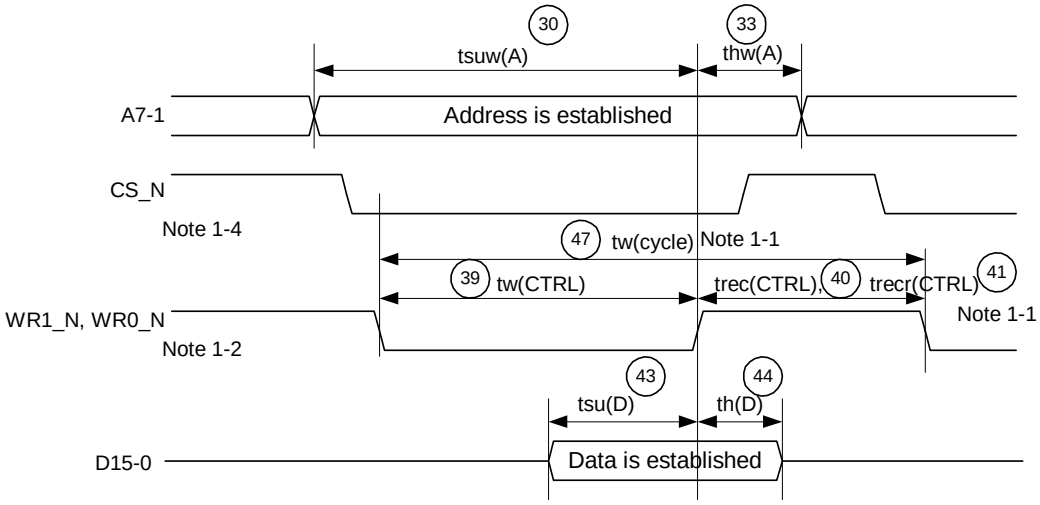
Table 4.1 Index for register access timing diagram

Bus specification	Access	R/W	INDEX	Note
Separate bus	CPU	WRITE	4.9.1	
Separate bus	CPU	READ	4.9.2	
Multiplex bus	CPU	WRITE	4.9.3	
Multiplex bus	CPU	READ	4.9.4	

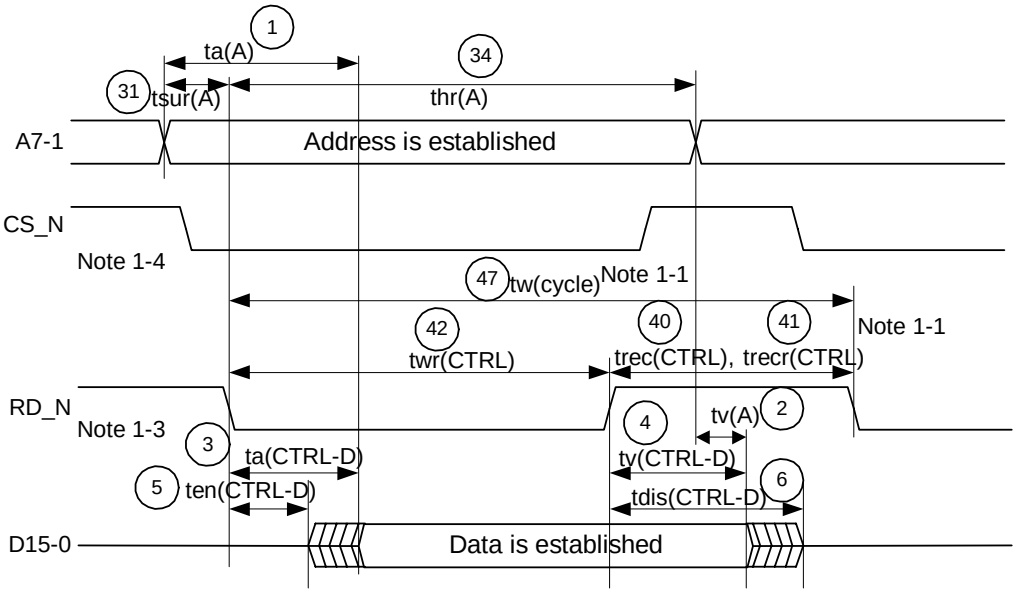
Table 4.2 Index for FIFO port access

Bus specification	Access	R/W	DackE	RWstb	Obus	INDEX	Note
Separate bus	CPU	WRITE	-	-	-	4.9.1	
Separate bus	CPU	READ	-	-	-	4.9.2	
Multiplex bus	CPU	WRITE	-	-	-	4.9.3	
Multiplex bus	CPU	READ	-	-	-	4.9.4	
Separate bus with CPU bus	DMA	WRITE	1	0	-	4.9.5	Cycle steal transfer
Separate bus with CPU bus	DMA	READ	1	0	-	4.9.6	Cycle steal transfer
With Split bus	DMA	WRITE	1	1	1	4.9.7	Cycle steal transfer
With Split bus	DMA	READ	1	1	1	4.9.8	Cycle steal transfer
With Split bus	DMA	WRITE	1	1	0	4.9.7	Cycle steal transfer
With Split bus	DMA	READ	1	1	0	4.9.9	Cycle steal transfer
Separate bus with CPU bus	DMA	WRITE	0	0	-	4.9.10	Cycle steal transfer
Separate bus with CPU bus	DMA	READ	0	0	-	4.9.11	Cycle steal transfer
Multiplex bus with CPU bus	DMA	WRITE	0	0	-	4.9.12	Cycle steal transfer
Multiplex bus with CPU bus	DMA	READ	0	0	-	4.9.13	Cycle steal transfer
Separate bus with CPU bus	DMA	WRITE	1	0	-	4.9.14	Burst transfer
Separate bus with CPU bus	DMA	READ	1	0	-	4.9.15	Burst transfer
With Split bus	DMA	WRITE	1	1	1	4.9.16	Burst transfer
With Split bus	DMA	READ	1	1	1	4.9.17	Burst transfer
With Split bus	DMA	WRITE	1	1	0	4.9.16	Burst transfer
With Split bus	DMA	READ	1	1	0	4.9.18	Burst transfer
Separate bus with CPU bus	DMA	WRITE	0	0	-	4.9.19	Burst transfer
Separate bus with CPU bus	DMA	READ	0	0	-	4.9.20	Burst transfer
Multiplex bus with CPU bus	DMA	WRITE	0	0	-	4.9.21	Burst transfer
Multiplex bus with CPU bus	DMA	READ	0	0	-	4.9.22	Burst transfer

4.9.1 CPU write timing (when set to separate bus)

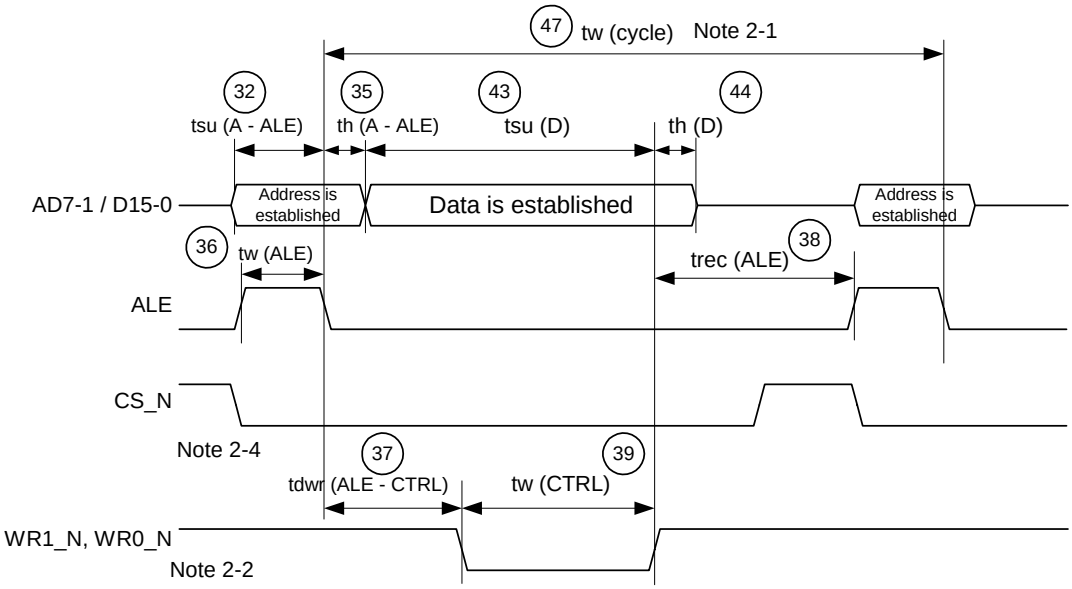


4.9.2 CPU read timing (when set to separate bus)

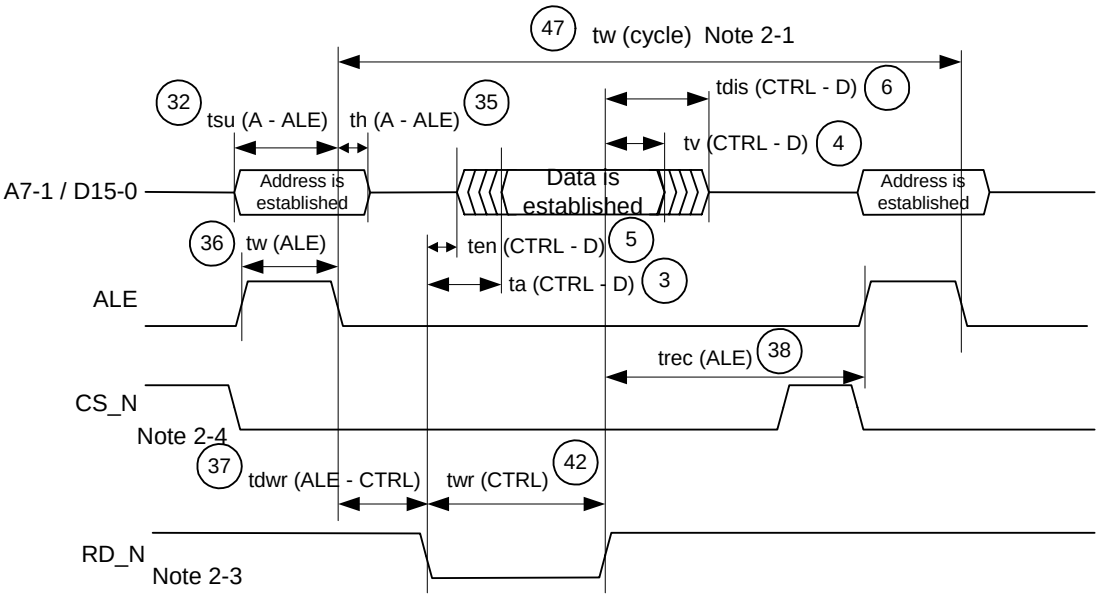


Note 1-1: tw (cycle) is necessary for making access to FIFO.
Note 1-2: Writing through the combination of CS_N, WR1_N and WR0_N is carried out during the overlap of active (Low).
The specification from the rising edge is valid from the earliest inactive signal.
The specification of pulse width becomes valid during the overlap of active (Low).
Note 1-3: Reading through the combination of CS_N and RD_N is carried out during the overlap of active (Low).
The specification from the falling edge is valid from the latest active signal.
The specification from the rising edge is valid from the earliest inactive signal.
The specification of pulse width becomes valid during the overlap of active (Low).
Note 1-4: Do not change RD_N, WR0_N and WR1_N to low concurrently with rising of CS_N.
Do not change CS_N to low concurrently with rising of the RD_N, WR0_N or WR1_N.
In the case above, it is necessary to make an interval of 10ns or more.

4.9.3 CPU write timing (when set to multiplex bus)

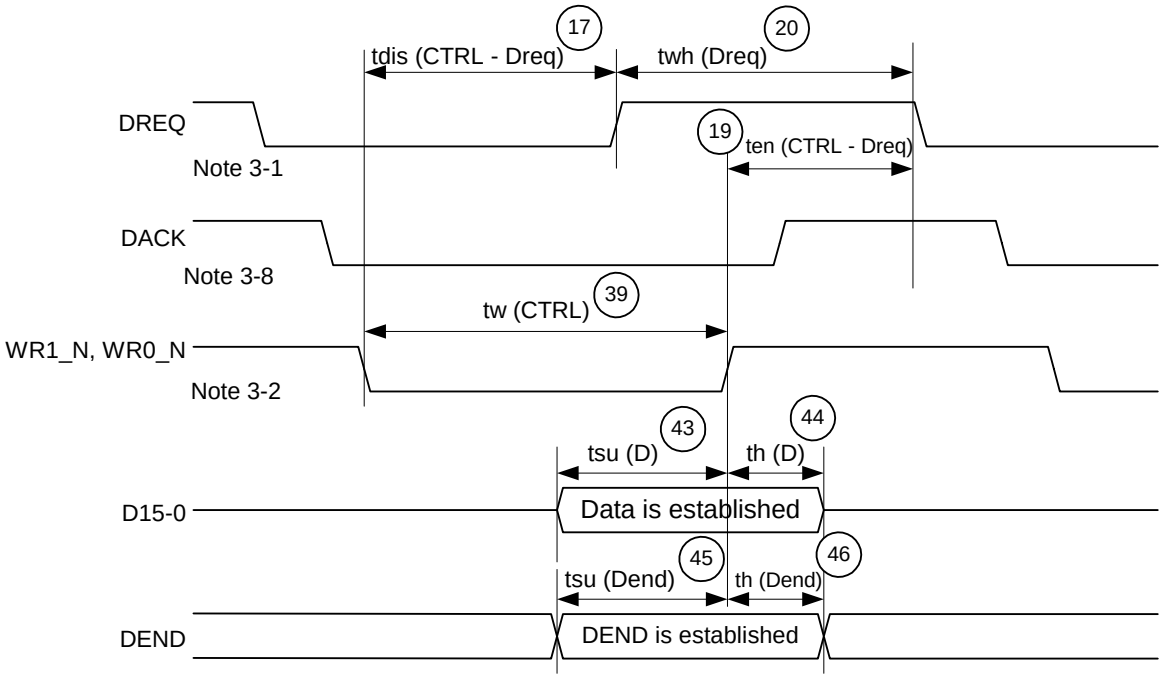


4.9.4 CPU read timing (when set to multiplex bus)

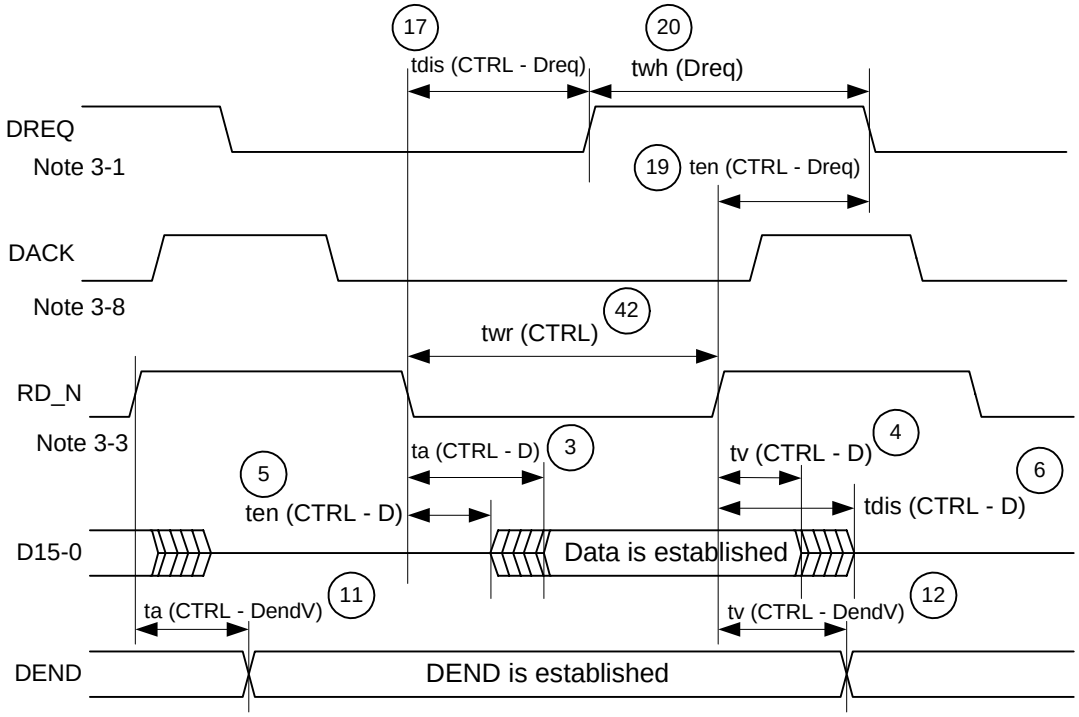


Note 2-1: tw (cycle) is necessary for making access to FIFO.
Note 2-2: Writing through the combination of CS_N, WR1_N and WR0_N is carried out during the overlap of active (Low).
The specification from the rising edge is valid from the earliest inactive signal.
The specification of pulse width becomes valid during the overlap of active (Low).
Note 2-3: Reading through the combination of CS_N and RD_N is carried out during the overlap of active (Low).
The specification from the falling edge is valid from the latest active signal.
The specification from the rising edge is valid from the earliest inactive signal.
The specification of pulse width becomes valid during the overlap of active (Low).
Note 2-4: Do not change RD_N, WR0_N and WR1_N to Low concurrently with rising of CS_N.
Do not change CS_N to Low concurrently with rising of the RD_N, WR0_N or WR1_N.
In the case above, it is necessary to make an interval of 10ns or more.

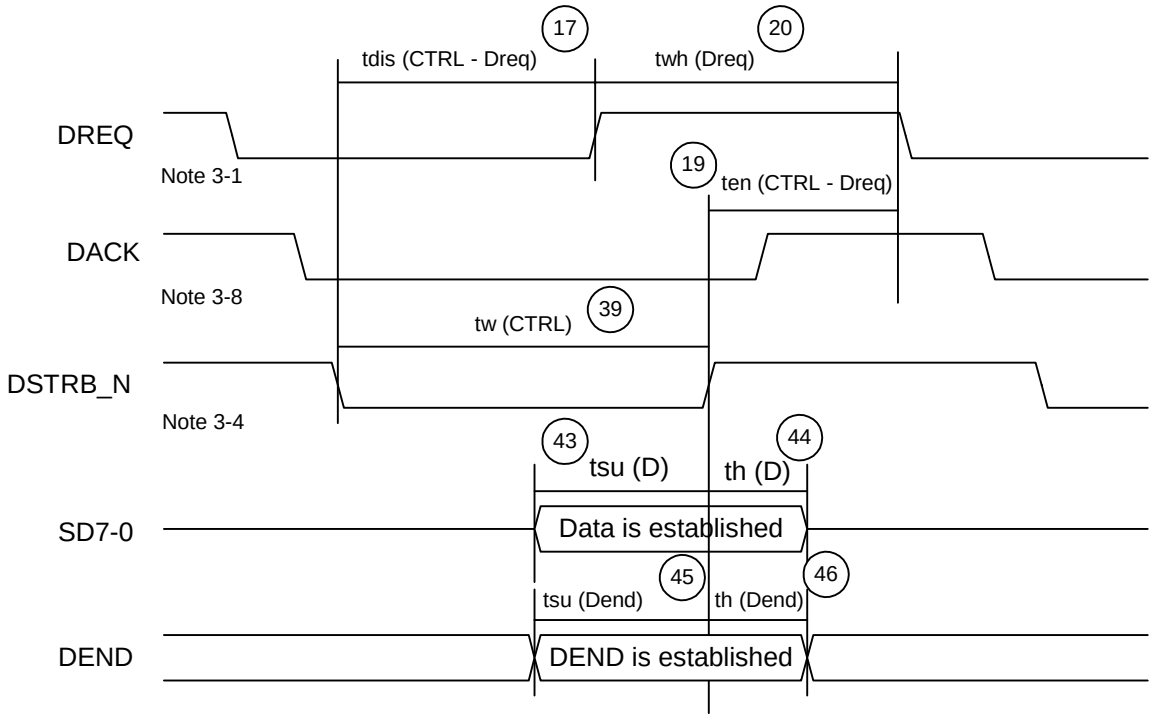
4.9.5 DMA transfer write timing (when set to separate bus and cycle steal transfer)



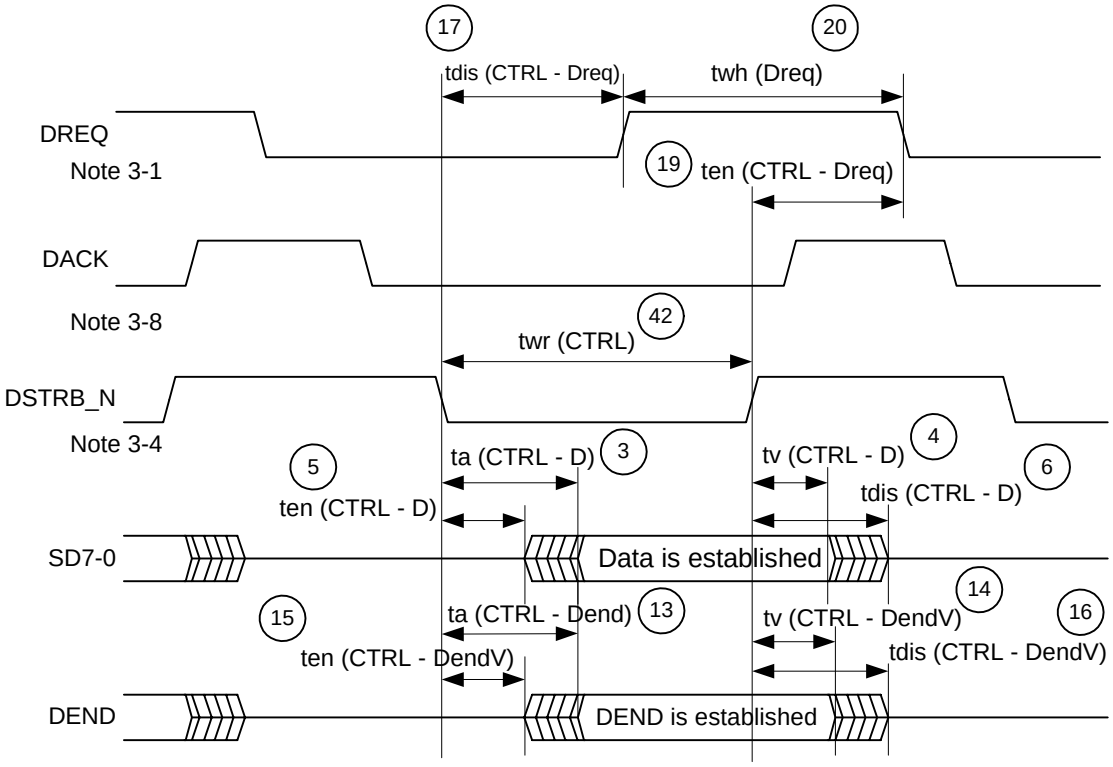
4.9.6 DMA transfer read timing (when set to separate bus and cycle steal transfer)



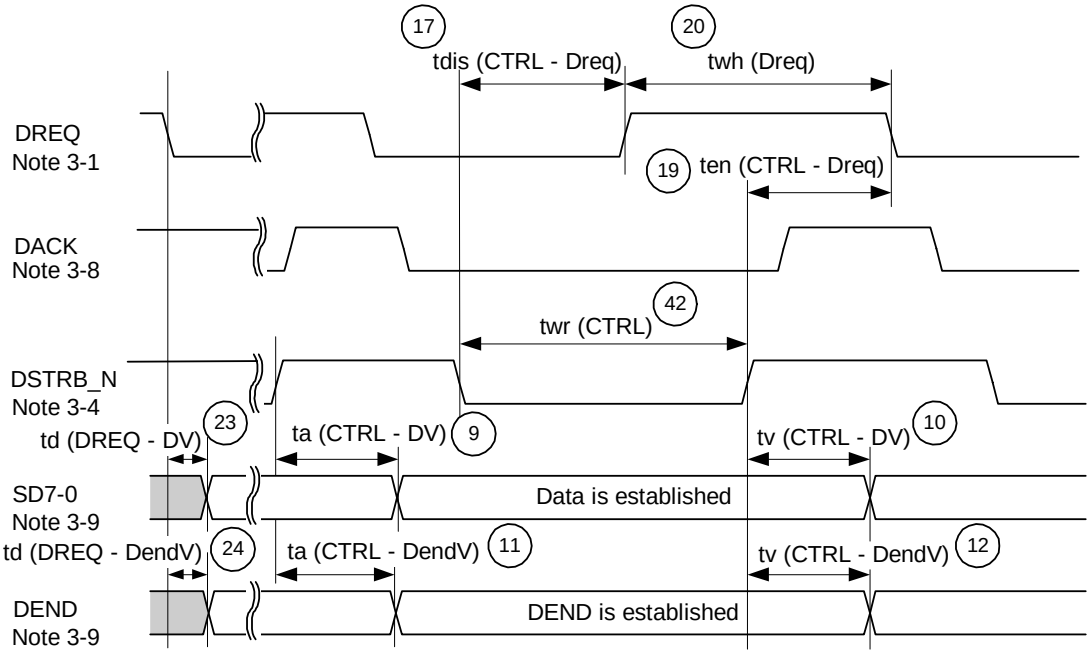
4.9.7 DMA transfer write timing (when set to split bus and cycle steal transfer)



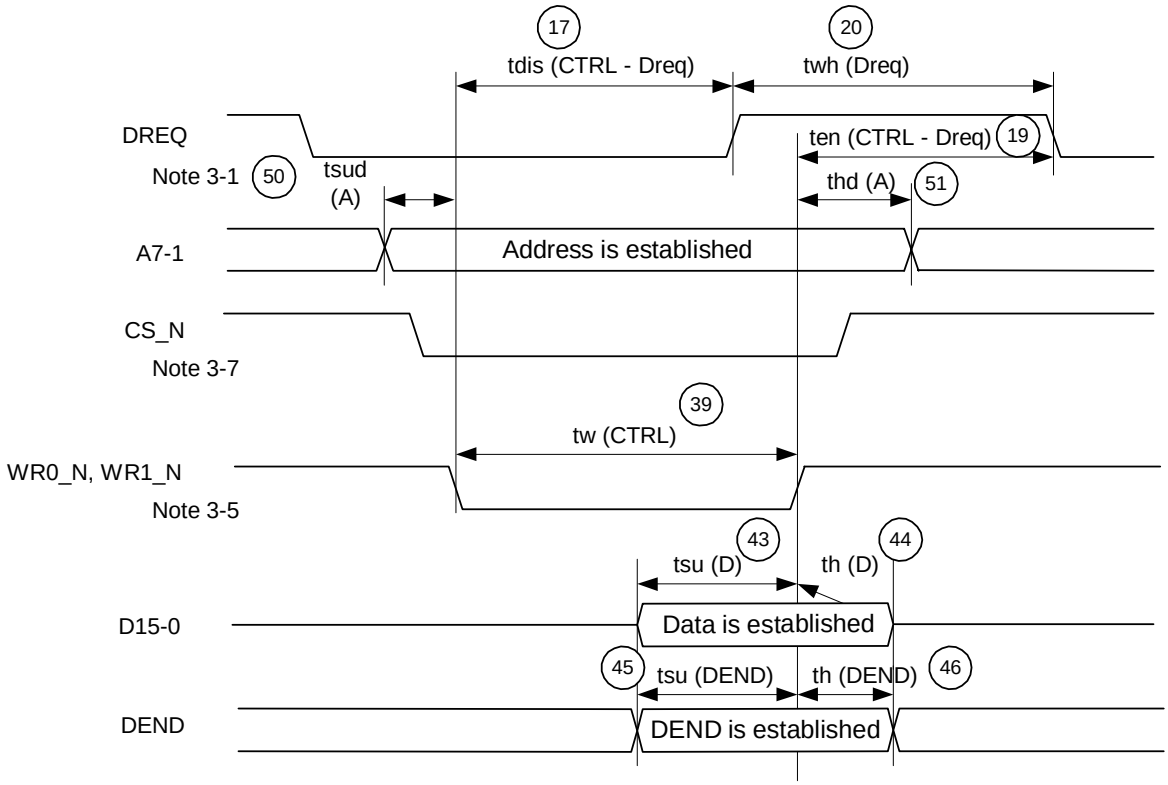
4.9.8 DMA transfer read timing (when set to split bus and cycle steal transfer: Obus = 1)



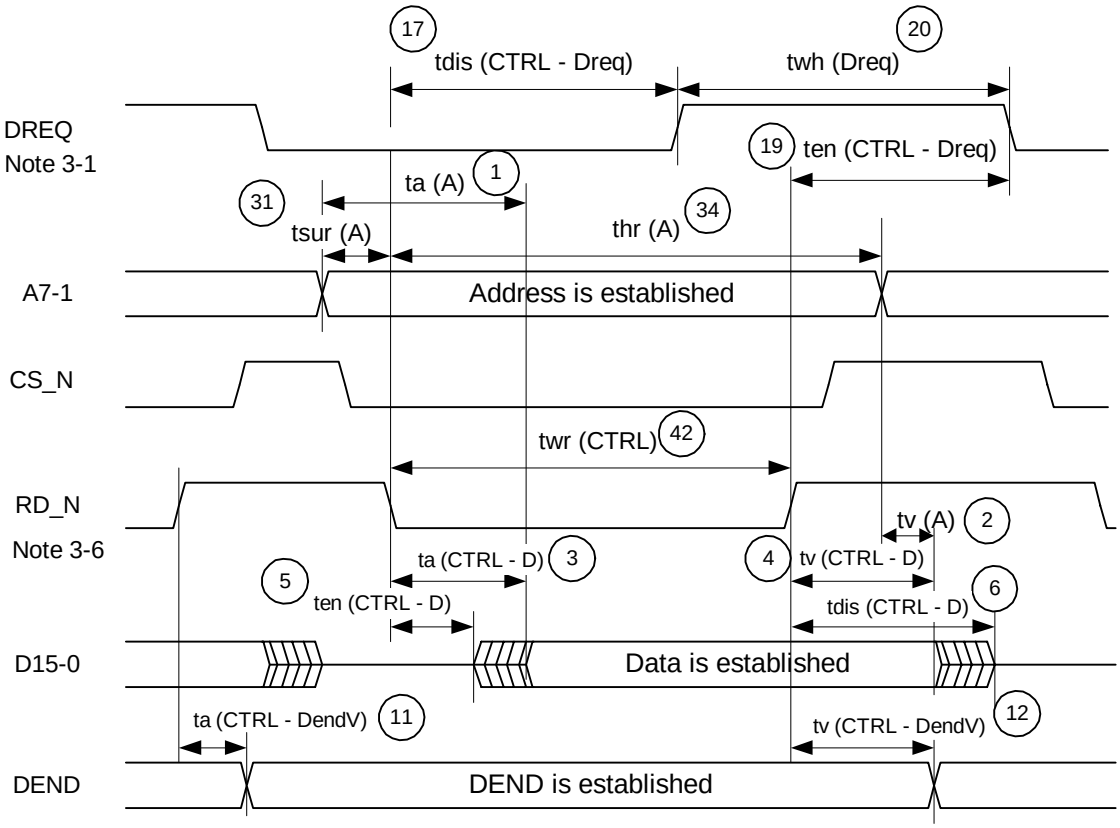
4.9.9 DMA transfer read timing (when set to split bus and cycle steal transfer: Obus = 0)



4.9.10 DMA transfer write timing (when set to separate bus and cycle steal transfer)

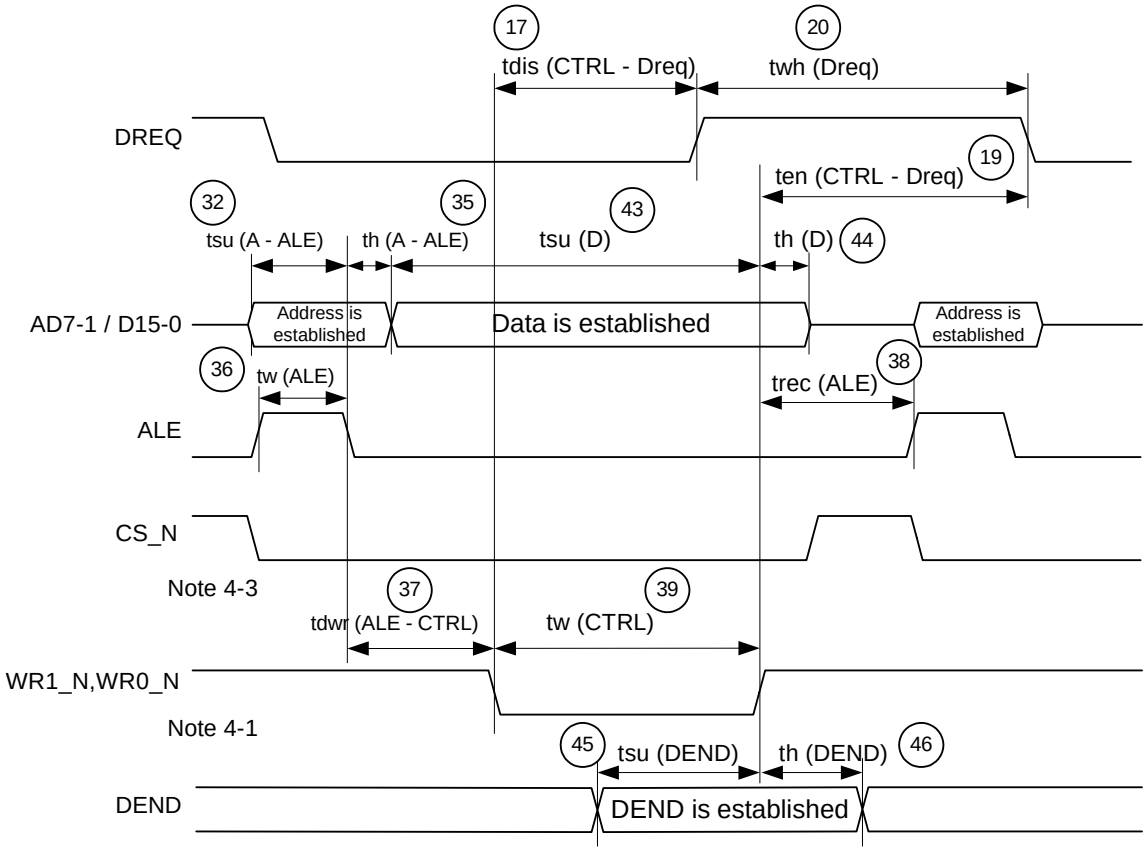


4.9.11 DMA transfer read timing (when set to separate bus and cycle steal transfer)

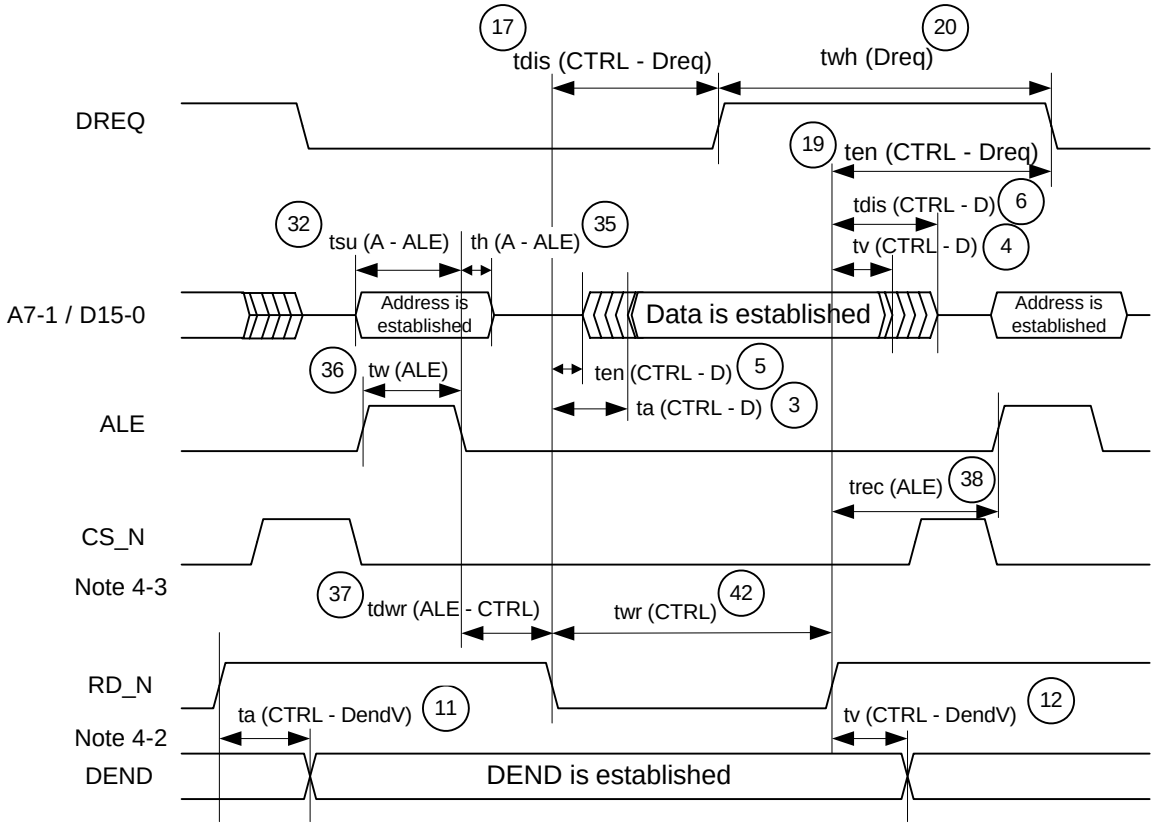


Note 3-1: DACK=Low level is the condition for inactive DREQ, and the latter signal of twh (Dreq) or ten (CTRL-Dreq) becomes valid as the specification of active DREQ at the time of next DMA transfer.
Note 3-2: Writing through the combination of DACK, WR1_N and WR0_N is carried out during the overlap of active (Low).
The specification from the rising edge is valid from the earliest inactive signal.
The specification of pulse width becomes valid during the overlap of active (Low).
Note 3-3: Reading through the combination of DACK and RD_N is carried out during the overlap of active (Low).
The specification from the falling edge is valid from the latest active signal.
The specification from the rising edge is valid from the earliest inactive signal.
The specification of pulse width becomes valid during the overlap of active (Low).
Note 3-4: Writing/Reading through the combination of DACK and DSTRB_N is carried out during the overlap of active (Low).
The specification from the falling edge is valid from the latest active signal.
The specification from the rising edge is valid from the earliest inactive signal.
The specification of pulse width becomes valid during the overlap of active (Low).
Note 3-5: Writing through the combination of CS_N, WR0_N and WR1_N is carried out during the overlap of active (Low).
The specification from the rising edge is valid from the earliest inactive signal.
The specification of pulse width becomes valid during the overlap of active (Low).
Note 3-6: Reading through the combination of CS_N and RD_N is carried out during the overlap of active (Low).
The specification from the falling edge is valid from the latest active signal.
The specification from the rising edge is valid from the earliest inactive signal.
The specification of pulse width becomes valid during the overlap of active (Low).
Note 3-7: Do not change RD_N, WR0_N and WR1_N to low concurrently with rising of CS_N.
Do not change CS_N to Low concurrently with rising of the RD_N, WR0_N or WR1_N.
In the case above, it is necessary to make an interval of 10ns or more.
Note 3-8: Do not change RD_N, WR0_N and WR1_N to low concurrently with rising (or falling) of DACK.
Do not change DACK to Low (High) concurrently with rising of the RD_N, WR0_N or WR1_N.
In the case above, it is necessary to make an interval of 10ns or more.
Note 3-9: When the receipt data is one byte, the data determined time is "(23)td(DREQ-DV)" and the DEND determined time is "(24)td(DREQ-DendV)".

4.9.12 DMA transfer write timing (when set to multiplex bus and cycle steal transfer)

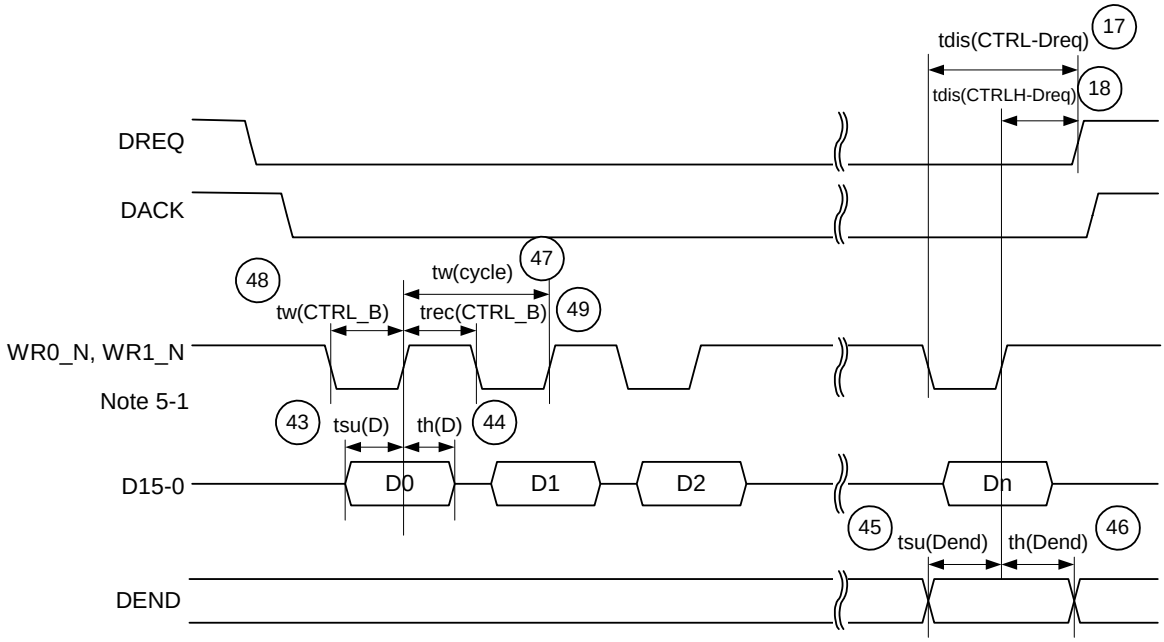


4.9.13 DMA transfer read timing (when set to multiplex bus and cycle steal transfer)

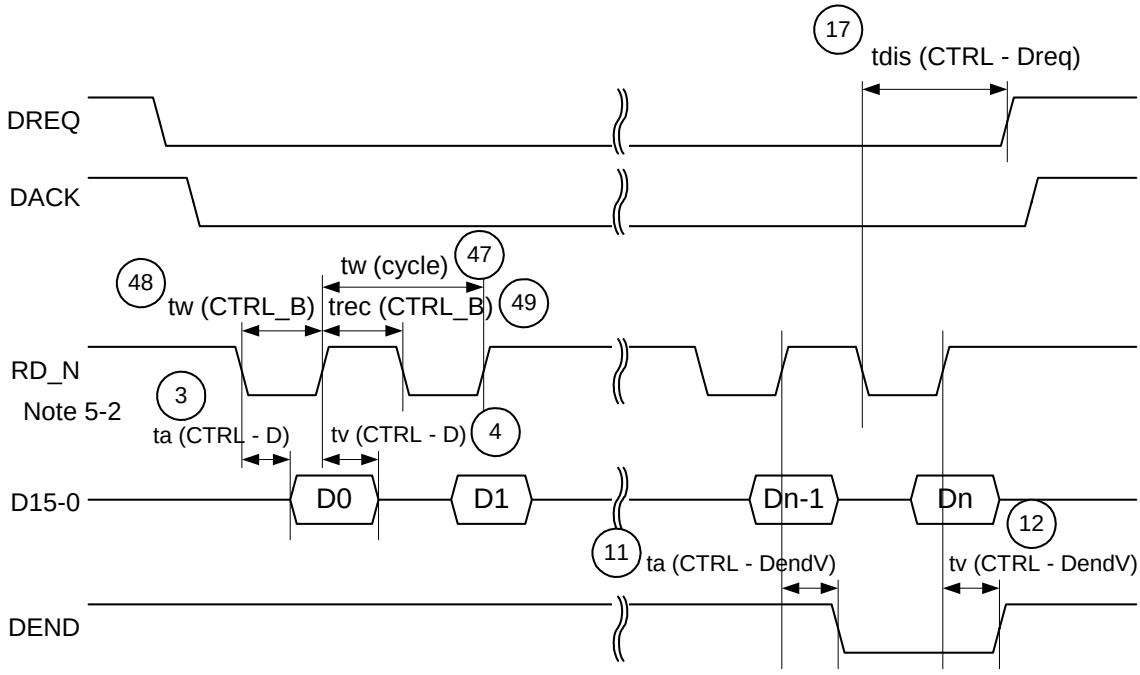


Note 4-1: Writing through the combination of CS_N, WR0_N and WR1_N is carried out during the overlap of active (Low).
The specification from the rising edge is valid from the earliest inactive signal.
The specification of pulse width becomes valid during the overlap of active (Low).
Note 4-2: Reading through the combination of CS_N and RD_N is carried out during the overlap of active (Low).
The specification from the falling edge is valid from the latest active signal.
The specification from the rising edge is valid from the earliest inactive signal.
The specification of pulse width becomes valid during the overlap of active (Low).
Note 4-3: Do not change RD_N, WR0_N and WR1_N to Low concurrently with rising of CS_N.
Do not change CS_N to Low concurrently with rising of the RD_N, WR0_N or WR1_N.
In the case above, it is necessary to make an interval of 10ns or more.

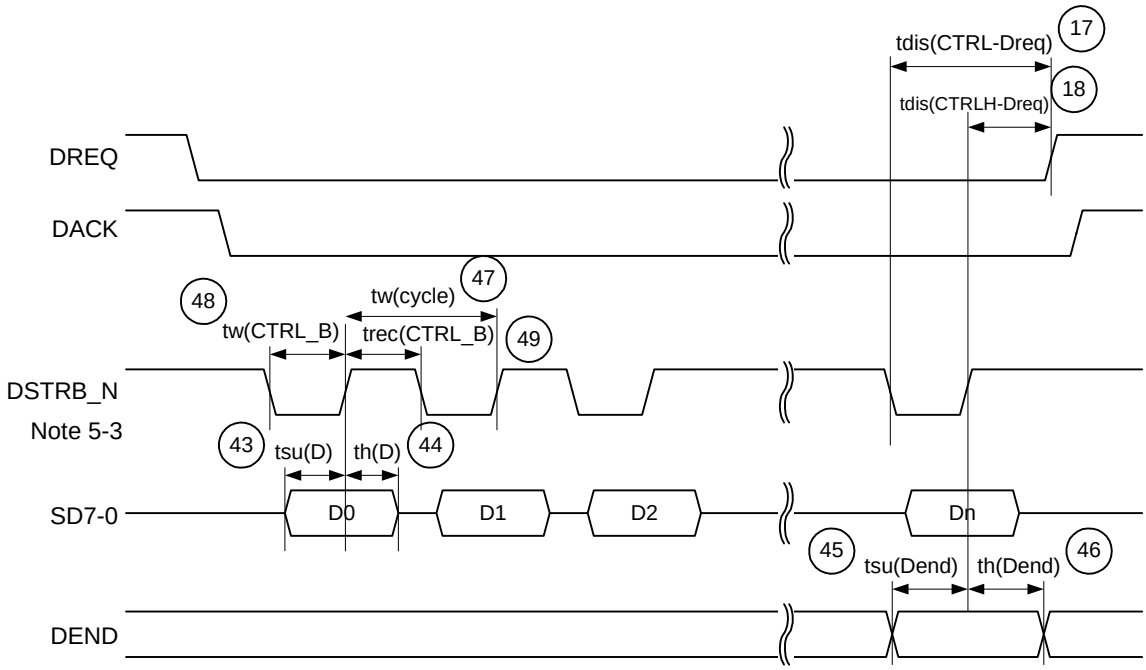
4.9.14 DMA transfer write timing (when set to separate bus and burst transfer)



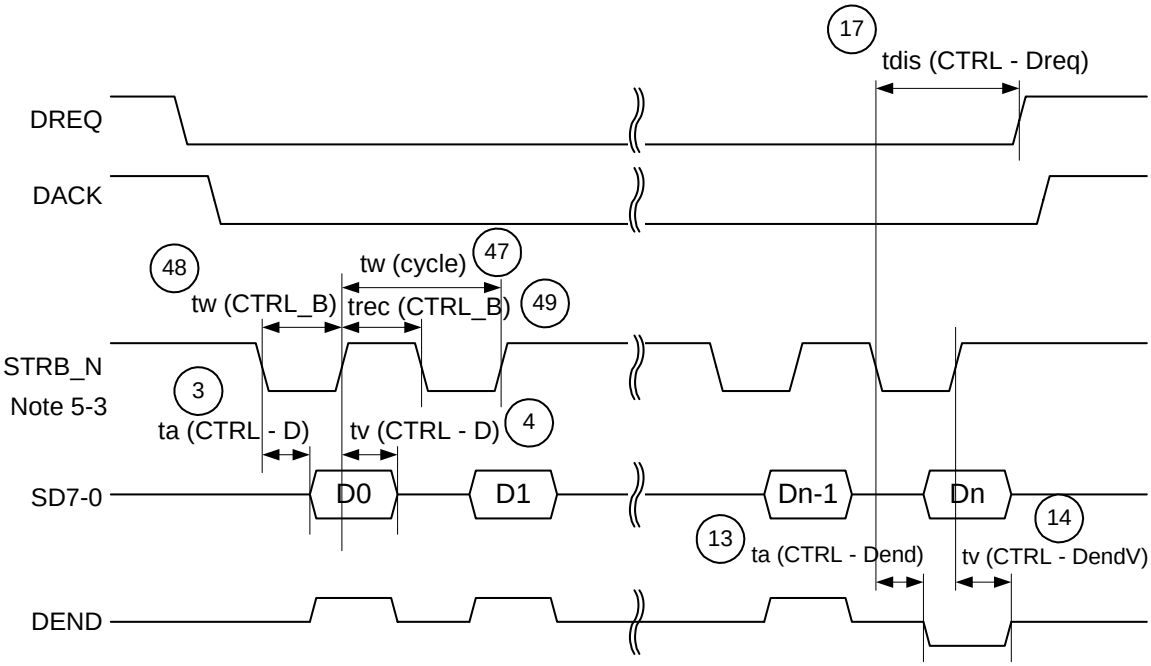
4.9.15 DMA transfer read timing (when set to separate bus and burst transfer)



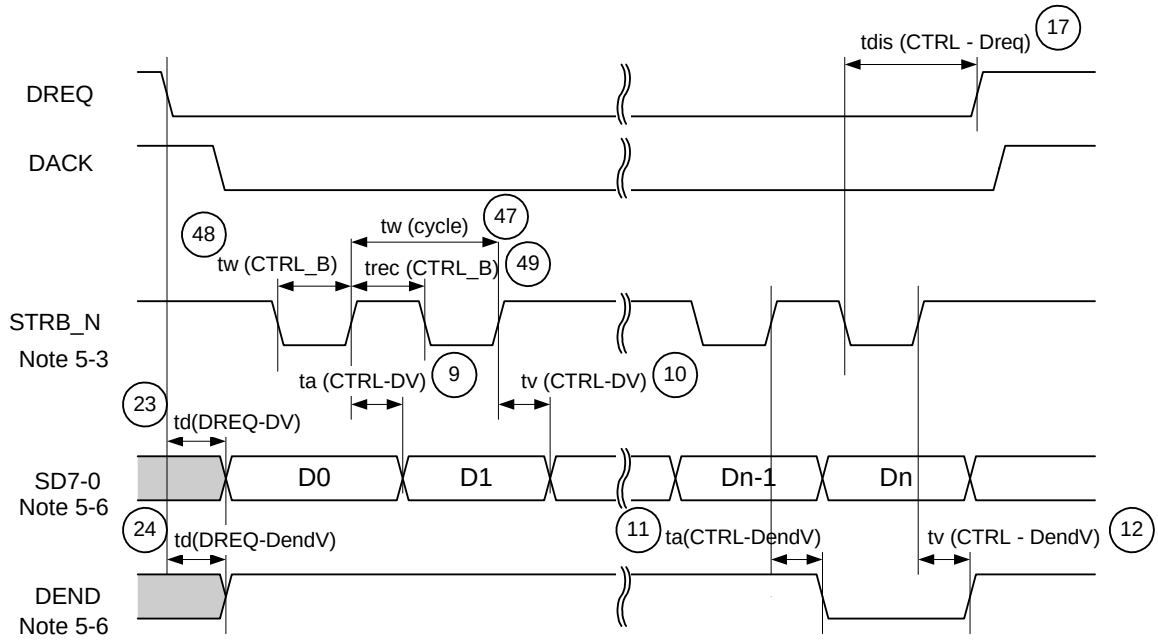
4.9.16 DMA transfer write timing (when set to split bus and burst transfer)



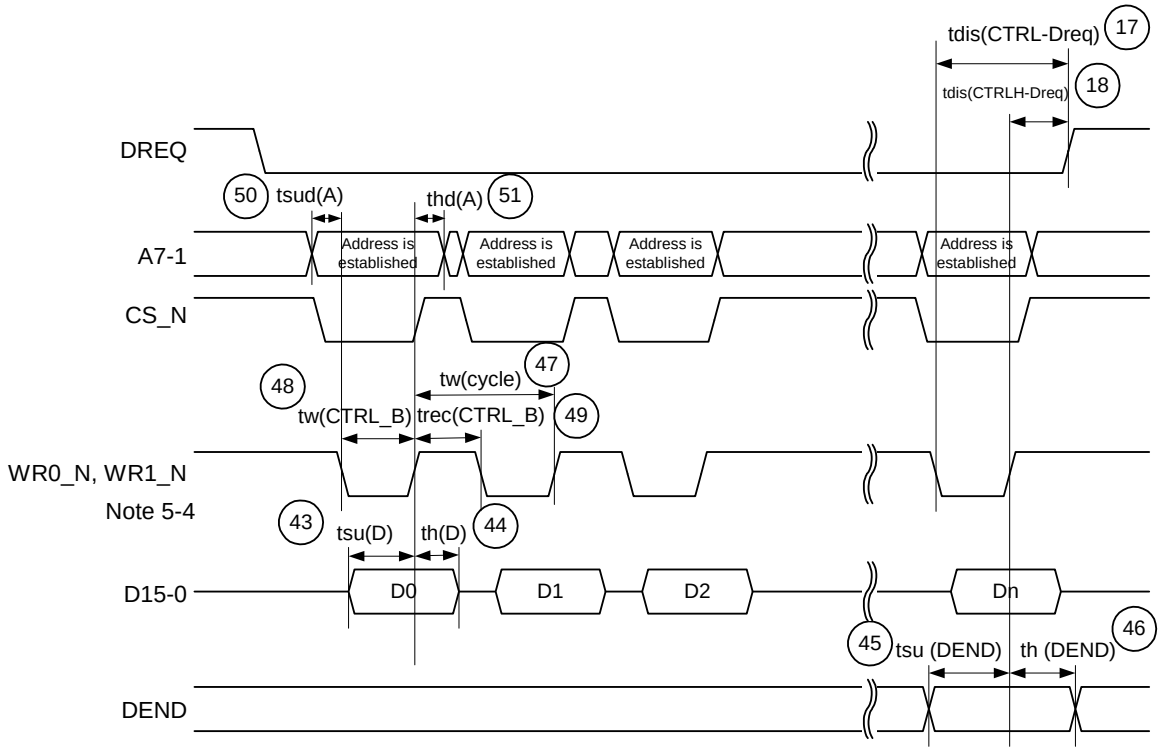
4.9.17 DMA transfer read timing (when set to split bus and burst transfer: Obus = 1)



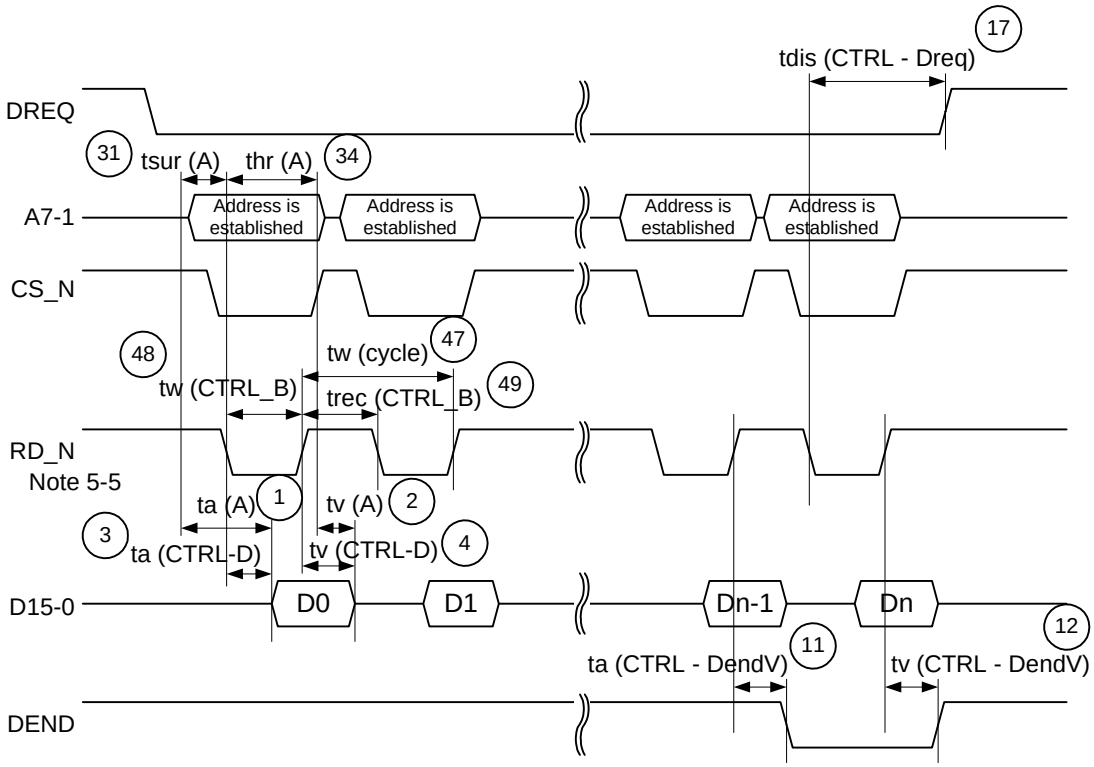
4.9.18 DMA transfer read timing (when set to split bus and burst transfer: Obus = 0)



4.9.19 DMA transfer write timing (when set to separate bus and burst transfer)



4.9.20 DMA transfer read timing (when set to separate bus and burst transfer)



Note 5-1: Writing through the combination of DACK, WR0_N and WR1_N is carried out during the overlap of active (Low).
The specification from the rising edge is valid from the earliest inactive signal.
The specification of pulse width becomes valid during the overlap of active (Low).

Note 5-2: Reading through the combination of DACK and RD_N is carried out during the overlap of active (Low).
The specification from the falling edge is valid from the latest active signal.
The specification from the rising edge is valid from the earliest inactive signal.
The specification of pulse width becomes valid during the overlap of active (Low).

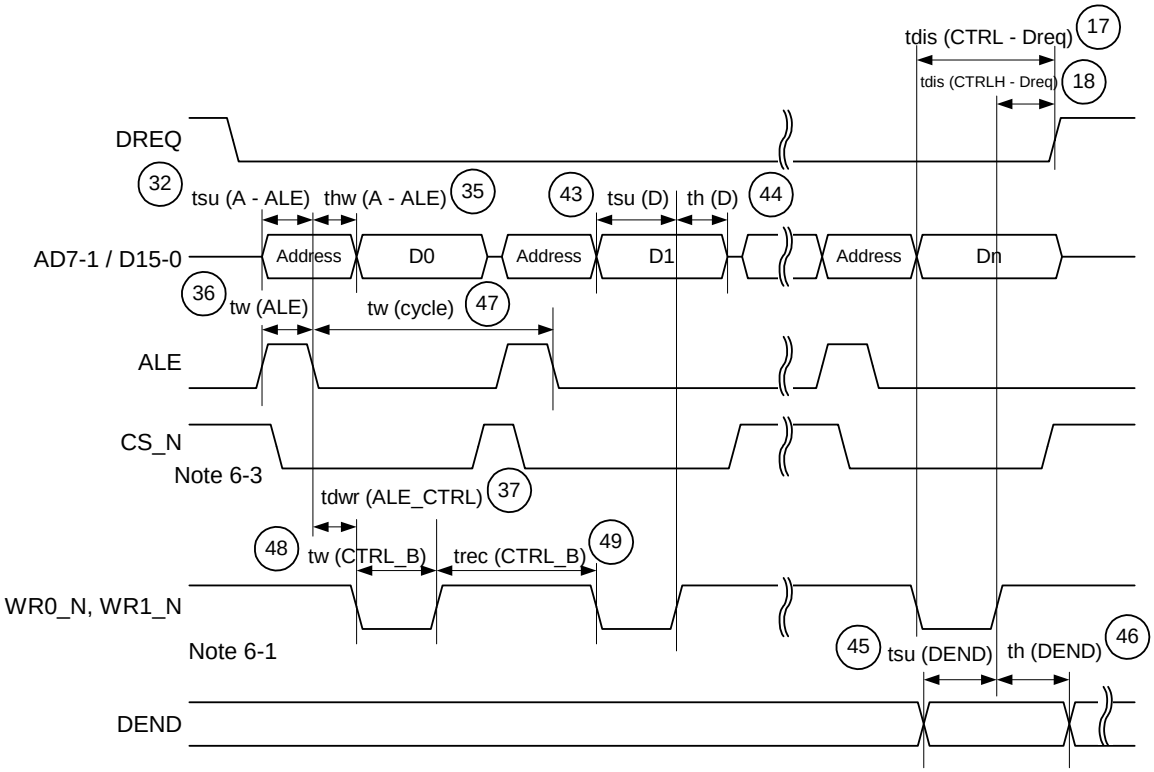
Note 5-3: Writing/reading through the combination of DACK and DSTRB_N is carried out during the overlap of active (Low).
The specification from the falling edge is valid from the latest active signal.
The specification from the rising edge is valid from the earliest inactive signal.
The specification of pulse width becomes valid during the overlap of active (Low).

Note 5-4: Writing through the combination of CS_N, WR0_N and WR1_N is carried out during the overlap of active (Low).
The specification from the rising edge is valid from the earliest inactive signal.
The specification of pulse width becomes valid during the overlap of active (Low).

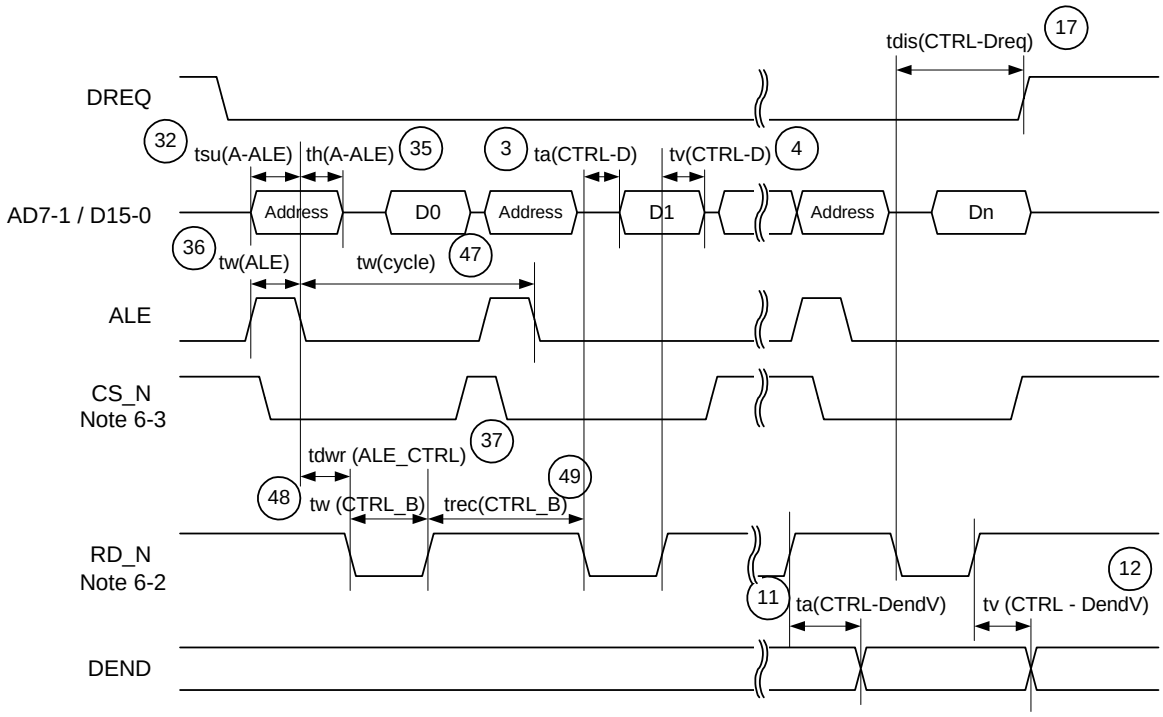
Note 5-5: Reading through the combination of CS_N and RD_N is carried out during the overlap of active (Low).
The specification from the falling edge is valid from the latest active signal.
The specification from the rising edge is valid from the earliest inactive signal.
The specification of pulse width becomes valid during the overlap of active (Low).

Note 5-6: When the receipt data is one byte, the data determined time is "(23) td (DREQ-DV)" and the DEND determined time is "(24)td(DREQ-DendV)".

4.9.21 DMA transfer write timing (when set to multiplex bus and burst transfer)

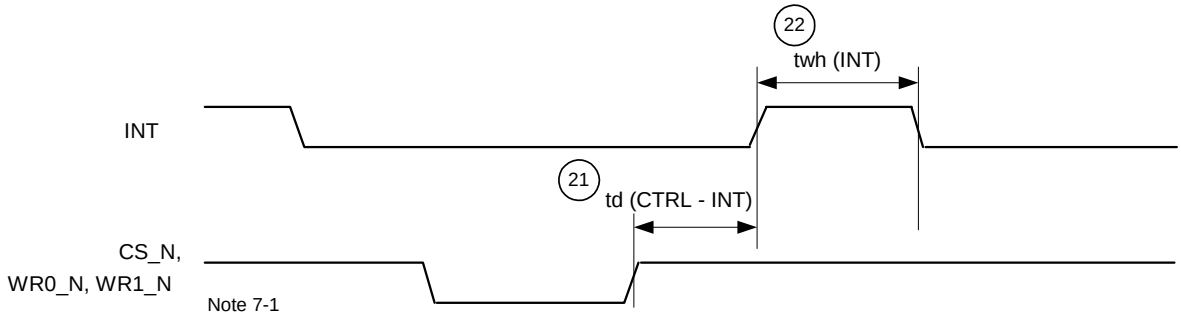


4.9.22 DMA transfer read timing (when set to multiplex bus and burst transfer)



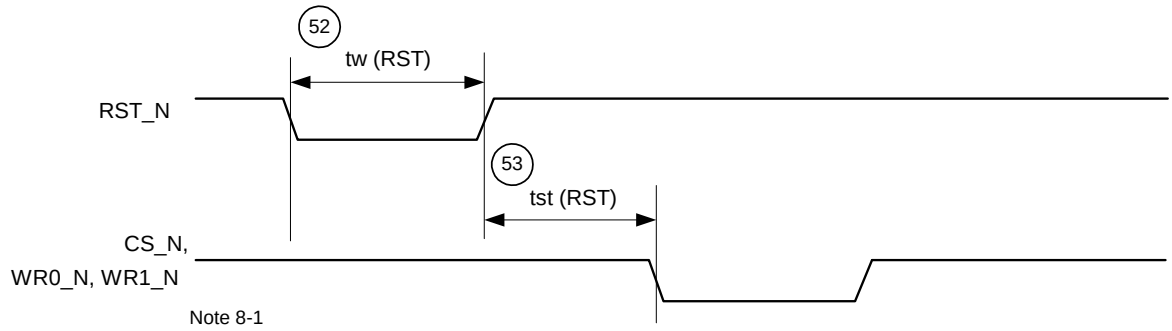
Note 6-1: Writing through the combination of CS_N, WR0_N and WR1_N is carried out during the overlap of active (Low).
The specification from the rising edge is valid from the earliest inactive signal.
The specification of pulse width becomes valid during the overlap of active (Low).
Note 6-2: Reading through the combination of CS_N and RD_N is carried out during the overlap of active (Low).
The specification from the falling edge is valid from the latest active signal.
The specification from the rising edge is valid from the earliest inactive signal.
The specification of pulse width becomes valid during the overlap of active (Low).
Note 6-3: Do not change RD_N, WR0_N and WR1_N to Low concurrently with rising of CS_N.
Do not change CS_N to Low concurrently with rising of the RD_N, WR0_N or WR1_N.
In the case above, it is necessary to make an interval of 10ns or more.

4.10 Interrupt Timing



Note 7-1: Writing through the combination of CS_N, WR0_N and WR1_N is carried out during the overlap of active (Low). The specification from the rising edge is valid from the earliest inactive signal.

4.11 Reset Timing



Note 8-1: Writing through the combination of CS_N, WR0_N and WR1_N is carried out during the overlap of active (Low). The specification from the rising edge is valid from the earliest inactive signal.

REVISION HISTORY	M66591 Data Sheet

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