

FDW2601NZ

Dual N-Channel 2.5V Specified PowerTrench® MOSFET

Features

- 8.2A, 30V $r_{DS(ON)} = 0.015\Omega$, $V_{GS} = 4.5V$
 $r_{DS(ON)} = 0.020\Omega$, $V_{GS} = 2.5V$
- Extended V_{GS} range ($\pm 12V$) for battery applications
- HBM ESD Protection Level of 3.5kV Typical (note 3)
- High performance trench technology for extremely low $r_{DS(ON)}$
- Low profile TSSOP-8 package

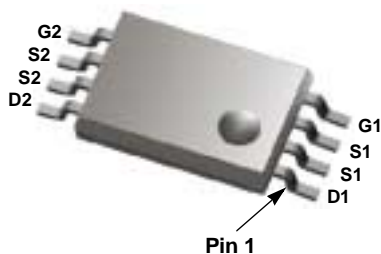
Applications

- Load switch
- Battery charge
- Battery disconnect circuits

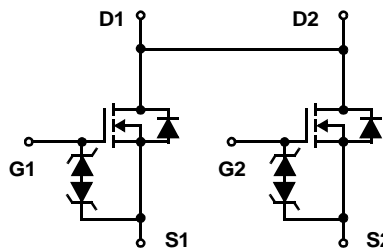


General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance. These devices are well suited for portable electronics applications.



TSSOP-8



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	± 12	V
I_D	Drain Current		
	Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 4.5\text{V}$, $R_{\theta JA} = 77^\circ\text{C/W}$)	8.2	A
	Continuous ($T_C = 100^\circ\text{C}$, $V_{GS} = 2.5\text{V}$, $R_{\theta JA} = 77^\circ\text{C/W}$)	4.5	A
	Pulsed	Figure 4	A
P_D	Power dissipation	1.6	W
	Derate above 25°C	13	mW/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 1)	77	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 2)	114	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
2601NZ	FDW2601NZ	TSSOP-8	13"	12 mm	2500 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

B_{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}$ $V_{GS} = 0\text{V}$	-	-	1	μA
		$T_A = 100^\circ\text{C}$	-	-	5	
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 12\text{V}$	-	-	± 10	μA
		$V_{GS} = \pm 4.5\text{V}$			± 250	nA

On Characteristics

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	0.6	0.8	1.5	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 8.2\text{A}$, $V_{GS} = 4.5\text{V}$	-	0.011	0.015	Ω
		$I_D = 7.9\text{A}$, $V_{GS} = 4.0\text{V}$	-	0.011	0.016	
		$I_D = 7.3\text{A}$, $V_{GS} = 3.1\text{V}$	-	0.012	0.019	
		$I_D = 7.1\text{A}$, $V_{GS} = 2.5\text{V}$	-	0.012	0.020	

Dynamic Characteristics

C_{ISS}	Input Capacitance	$V_{DS} = 15\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$	-	1840	-	pF	
C_{OSS}	Output Capacitance		-	250	-	pF	
C_{RSS}	Reverse Transfer Capacitance		-	160	-	pF	
R_G	Gate Resistance	$V_{GS} = 0.5\text{V}$, $f = 1\text{MHz}$	-	2.6	-	Ω	
$Q_{g(TOT)}$	Total Gate Charge at 4.5V	$V_{GS} = 0\text{V}$ to 4.5V	$V_{DD} = 15\text{V}$ $I_D = 8.2\text{A}$ $I_g = 1.0\text{mA}$	-	20	30	nC
$Q_{g(2.5)}$	Total Gate Charge at 2.5V	$V_{GS} = 0\text{V}$ to 2.5V		-	12	18	nC
Q_{gs}	Gate to Source Gate Charge			-	2.7	-	nC
Q_{gd}	Gate to Drain "Miller" Charge			-	5.1	-	nC

Switching Characteristics ($V_{GS} = 4.5V$)

t_{ON}	Turn-On Time	$V_{DD} = 15V, I_D = 8.2A$ $V_{GS} = 4.5V, R_{GS} = 6.8\Omega$	-	-	113	ns
$t_{d(ON)}$	Turn-On Delay Time		-	18	-	ns
t_r	Rise Time		-	57	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	69	-	ns
t_f	Fall Time		-	71	-	ns
t_{OFF}	Turn-Off Time		-	-	210	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 1.3A$	-	0.7	1.2	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 8.2A, dI_{SD}/dt = 100A/\mu s$	-	-	28	ns
Q_{RR}	Reverse Recovered Charge	$I_{SD} = 8.2A, dI_{SD}/dt = 100A/\mu s$	-	-	17	nC

Notes:

- $R_{\theta JA}$ is 77 °C/W (steady state) when mounted on a 1 inch² copper pad on FR-4.
- $R_{\theta JA}$ is 114 °C/W (steady state) when mounted on a minimum copper pad on FR-4.
- The diode connected to the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristic $T_A = 25^\circ\text{C}$ unless otherwise noted

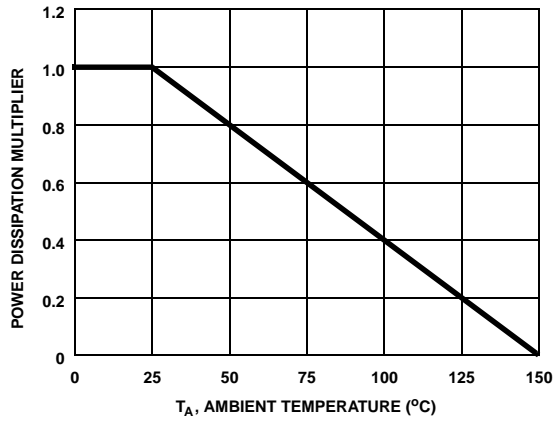


Figure 1. Normalized Power Dissipation vs Ambient Temperature

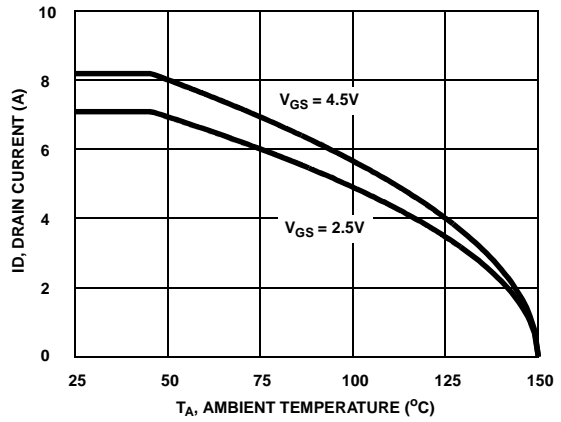


Figure 2. Maximum Continuous Drain Current vs Ambient Temperature

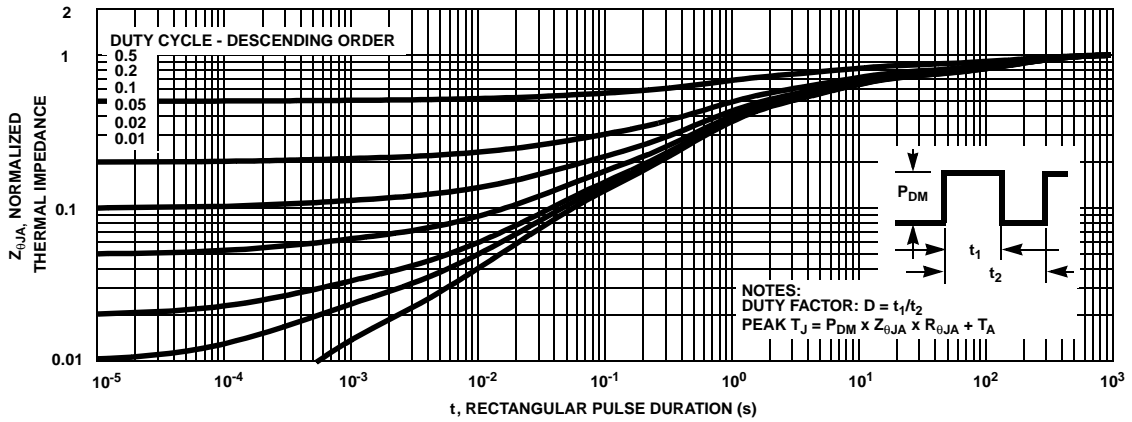


Figure 3. Normalized Maximum Transient Thermal Impedance

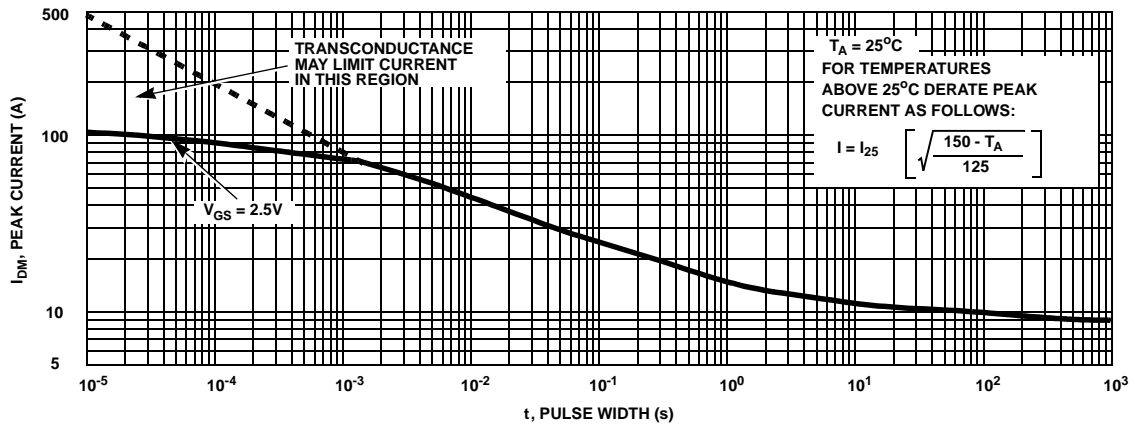


Figure 4. Peak Current Capability

Typical Characteristic (Continued) $T_A = 25^\circ\text{C}$ unless otherwise noted

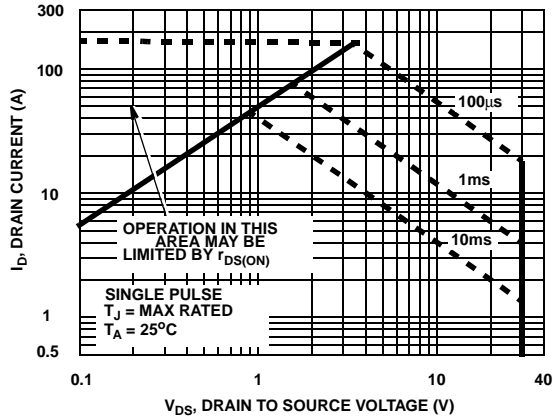


Figure 5. Forward Bias Safe Operating Area

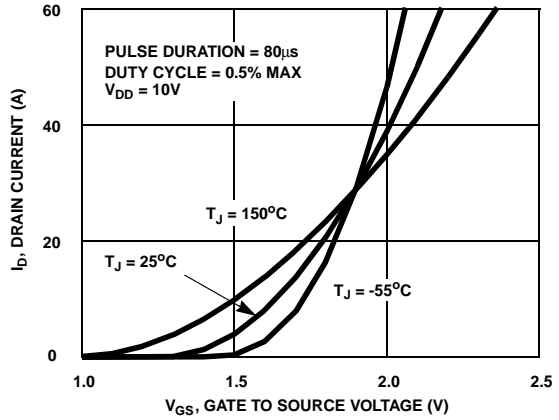


Figure 6. Transfer Characteristics

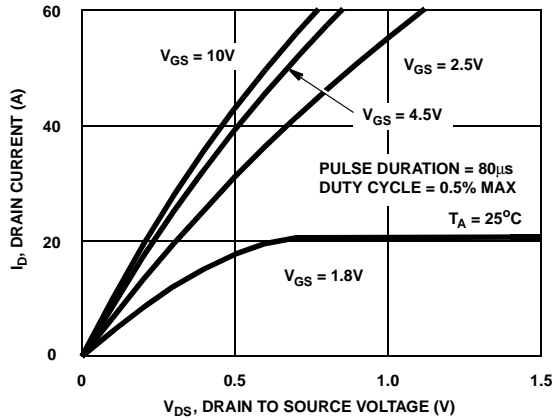


Figure 7. Saturation Characteristics

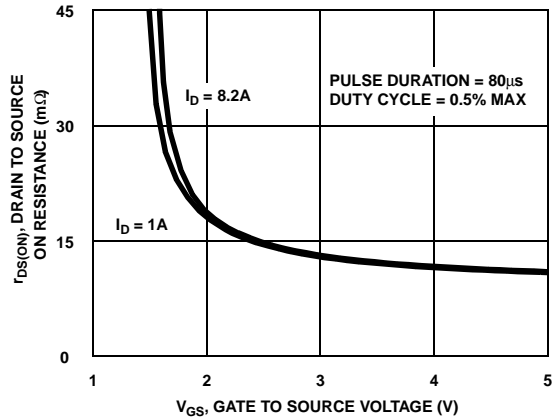


Figure 8. Drain to Source On Resistance vs Gate Voltage and Drain Current

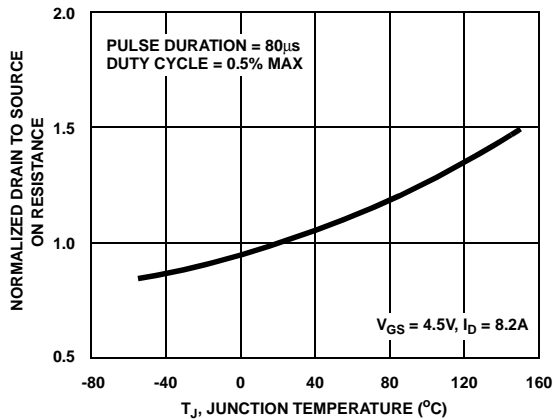


Figure 9. Normalized Drain to Source On Resistance vs Junction Temperature

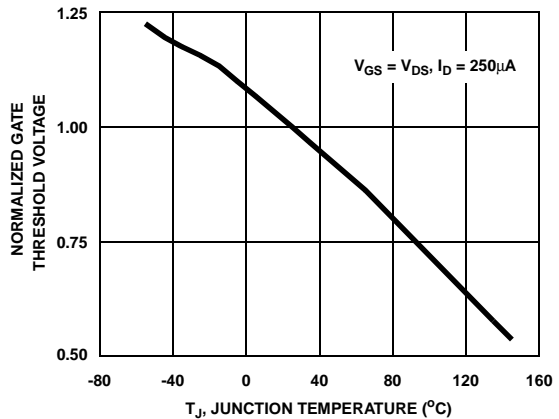


Figure 10. Normalized Gate Threshold Voltage vs Junction Temperature

Typical Characteristic (Continued) $T_A = 25^\circ\text{C}$ unless otherwise noted

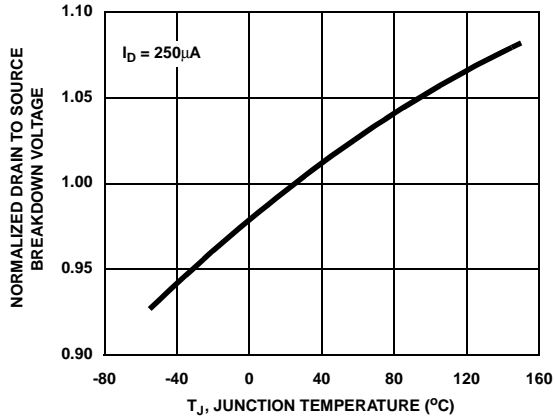


Figure 11. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

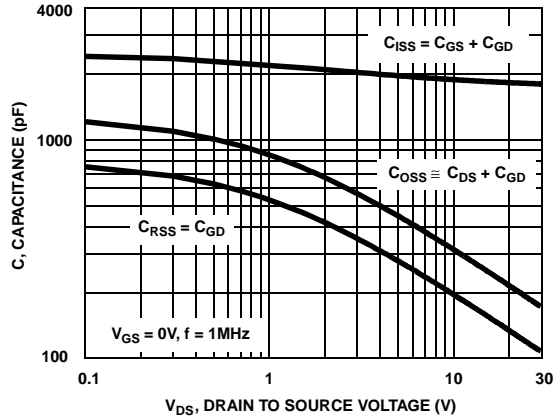


Figure 12. Capacitance vs Drain to Source Voltage

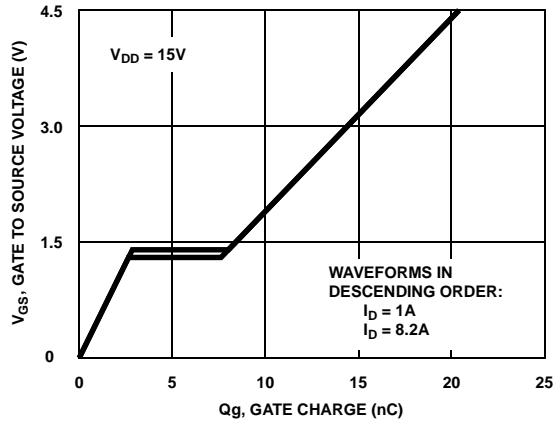


Figure 13. Gate Charge Waveforms for Constant Gate Currents

Test Circuits and Waveforms

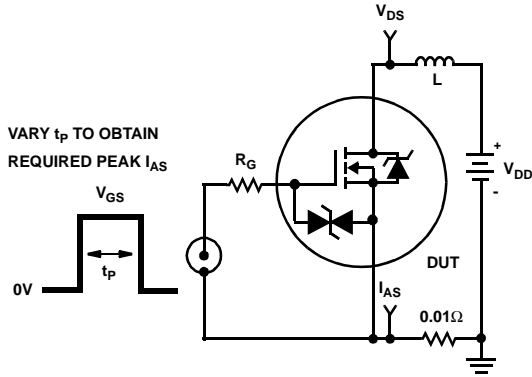


Figure 14. Unclamped Energy Test Circuit

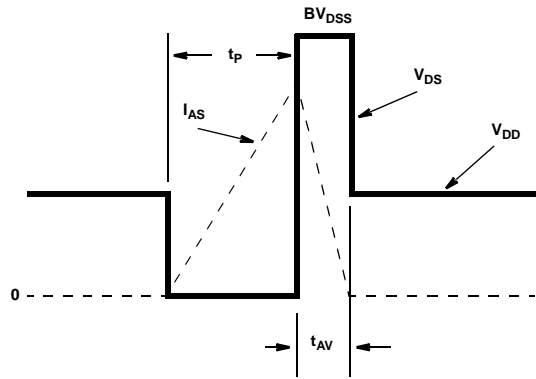


Figure 15. Unclamped Energy Waveforms

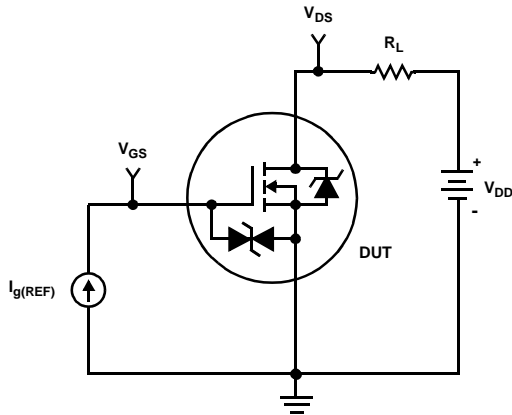


Figure 16. Gate Charge Test Circuit

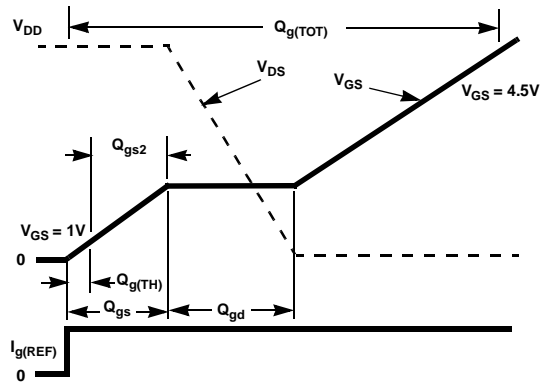


Figure 17. Gate Charge Waveforms

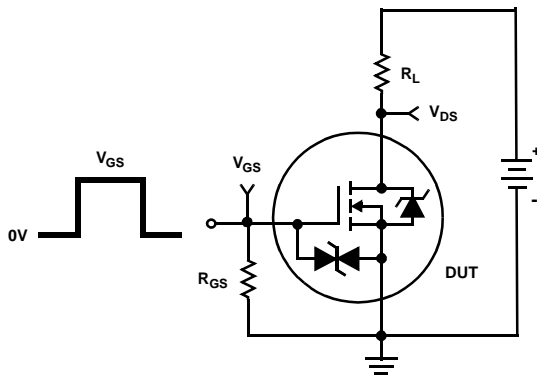


Figure 18. Switching Time Test Circuit

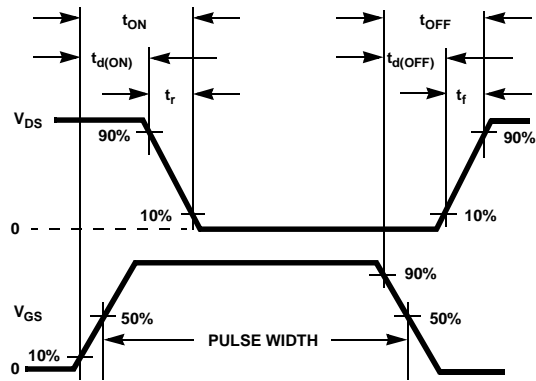


Figure 19. Switching Time Waveforms

SABER Electrical Model

REV June 2004
 template fdw2601nz n2,n1,n3
 electrical n2,n1,n3

```
{
var i iscl
dp..model dbodymod = (isl = 18.6e-12, nl=0.93, rs = 6.6e-3, trs1 = 1.7e-3, trs2 = 2e-6, xti=0.1, cjo = 5.2e-10, ikf=0.2, tt = 8.7e-9,
m = 0.58, tikf=0.001)
dp..model dbreakmod = (rs = 1e-1, trs1 = 9e-3, trs2 = -2.0e-5)
dp..model dplcapmod = (cjo = 0.76e-9, isl=10e-30, nl=10, m=0.58)
dp..model desd1mod = (bv=10.5, tbv1=-0.0018, nl=9.4, rs=5)
dp..model desd2mod = (bv=10.5, tbv1=-0.0018, nl=9.4, rs=5)
m..model mmedmod = (type=_n, vto = 1.0, kp=1.7, is=1e-30, tox=1)
m..model mstrongmod = (type=_n, vto = 1.27, kp = 147, is = 1e-30, tox = 1)
m..model mweakmod = (type=_n, vto = 0.83, kp = 0.05, is = 1e-30, tox = 1, rs=0.1)
sw_vcsp..model s1amod = (ron = 1e-5, roff = 0.1, von = -6, voff = -1.5)
sw_vcsp..model s1bmod = (ron = 1e-5, roff = 0.1, von = -1.5, voff = -6)
sw_vcsp..model s2amod = (ron = 1e-5, roff = 0.1, von = -0.5, voff = 0.3)
sw_vcsp..model s2bmod = (ron = 1e-5, roff = 0.1, von = 0.3, voff = -0.5)
```

```
c.ca n12 n8 = 19.3e-10
c.cb n15 n14 = 19.3e-10
c.cin n6 n8 = 1.7e-9
```

```
dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod
dp.desd1 n91 n9 = model=desd1mod
dp.desd2 n91 n7 = model=desd2mod
```

```
spe.ebreak n11 n7 n17 n18 = 33.3
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1
```

```
i.it n8 n17 = 1
```

```
l.l drain n2 n5 = 1e-9
l.l gate n1 n9 = 0.96e-9
l.l source n3 n7 = 0.19e-9
```

```
res.r drain n2 n5 = 10
res.r gate n1 n9 = 9.6
res.r source n3 n7 = 1.9
```

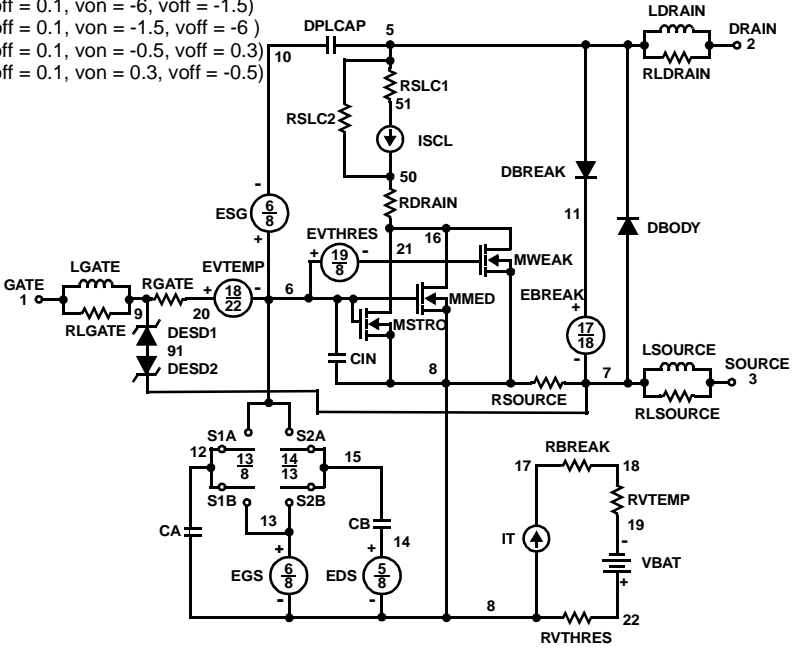
```
m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u
```

```
res.r break n17 n18 = 1, tc1 = 8.8e-4, tc2 = -13e-7
res.r drain n50 n16 = 8.8e-3, tc1 = 1e-9, tc2 = 1e-5
res.r gate n9 n20 = 2.75
res.r slc1 n5 n51 = 1e-6, tc1 = 2e-9, tc2 = 5e-8
res.r slc2 n5 n50 = 1e3
res.r source n8 n7 = 3e-4, tc1 = 8.2e-2, tc2 = 1e-6
res.r vtemp n18 n19 = 1, tc1 = -1.3e-3, tc2 = 1e-6
res.r vthres n22 n8 = 1, tc1 = -13e-4, tc2 = -2.8e-6
```

```
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod
```

```
v.vbat n22 n19 = dc=1
```

```
equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51))*1e6/120)** 2.5))
}
}
```



SPICE Thermal Model

REV June 2004
 FDW2601NZ_JA Junction Ambient
 Minimum copper pad area

CTHERM1 Junction c2 5.7e-4
 CHERM2 c2 c3 5.72e-4
 CHERM3 c3 c4 5.8e-4
 CHERM4 c4 c5 4.7e-3
 CHERM5 c5 c6 5.1e-3
 CHERM6 c6 c7 0.02
 CHERM7 c7 c8 0.2
 CHERM8 c8 Ambient 6

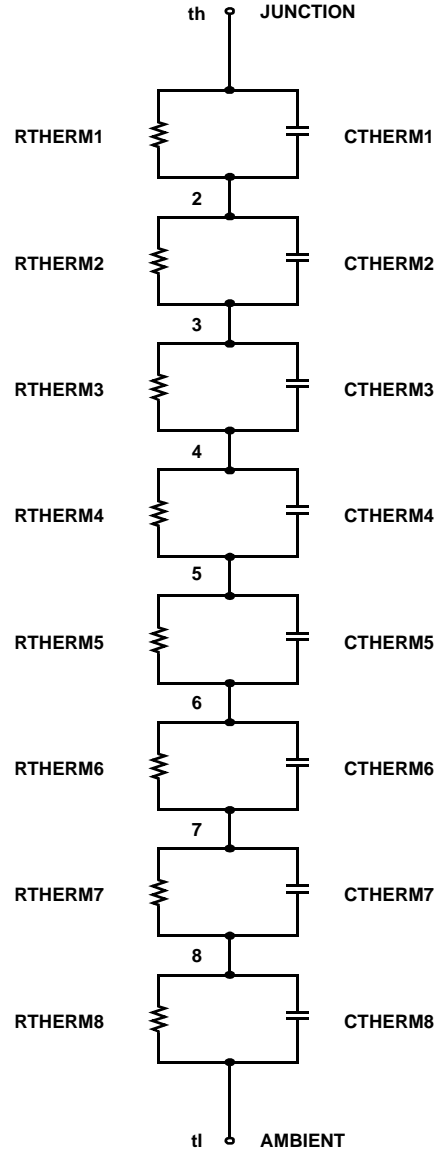
R THERM1 Junction c2 0.003
 R THERM2 c2 c3 0.25
 R THERM3 c3 c4 1.0
 R THERM4 c4 c5 1.1
 R THERM5 c5 c6 7.5
 R THERM6 c6 c7 33.6
 R THERM7 c7 c8 33.7
 R THERM8 c8 Ambient 33.8

SABER Thermal Model

SABER thermal model FDW2601NZ
 Minimum copper pad area
 template thermal_model th tl
 thermal_c th, tl

```
{
    ctherm.ctherm1 th c2 = 5.7e-4
    ctherm.ctherm2 c2 c3 = 5.72e-4
    ctherm.ctherm3 c3 c4 = 5.8e-4
    ctherm.ctherm4 c4 c5 = 4.7e-3
    ctherm.ctherm5 c5 c6 = 5.1e-3
    ctherm.ctherm6 c6 c7 = 0.02
    ctherm.ctherm7 c7 c8 = 0.2
    ctherm.ctherm8 c8 tl = 6
}
```




```
rtherm.rtherm1 th c2 = 0.003
rtherm.rtherm2 c2 c3 = 0.25
rtherm.rtherm3 c3 c4 = 1.0
rtherm.rtherm4 c4 c5 = 1.1
rtherm.rtherm5 c5 c6 = 7.5
rtherm.rtherm6 c6 c7 = 33.6
rtherm.rtherm7 c7 c8 = 33.7
rtherm.rtherm8 c8 tl = 33.8
}
```





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