



1:4 Differential Clock/Data Fanout Buffer

Features

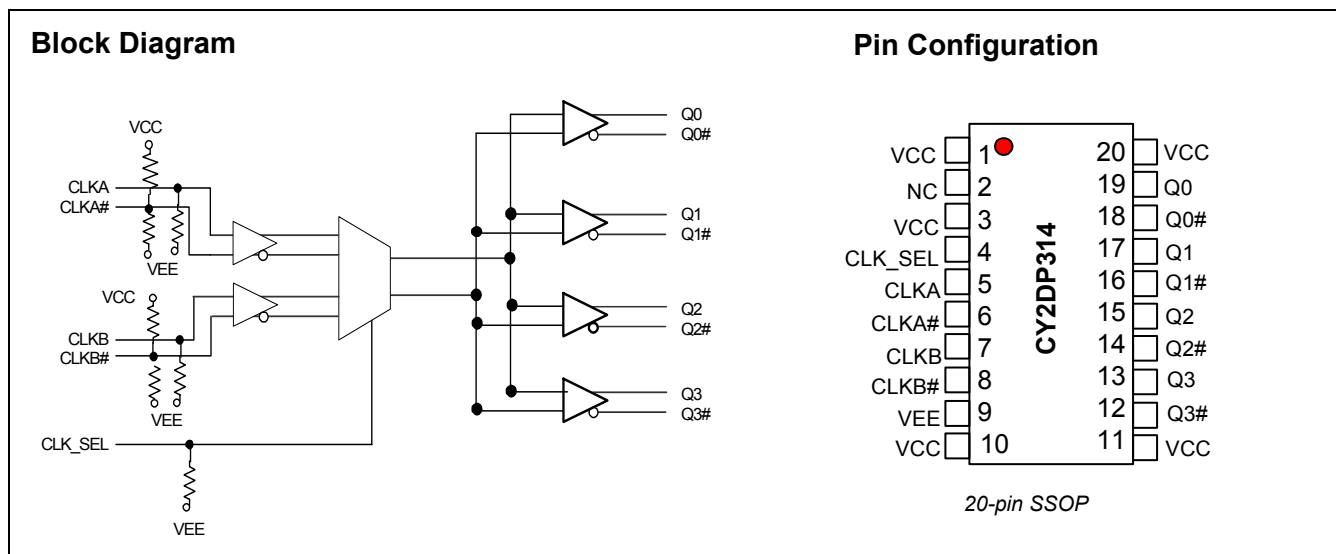
- Four ECL/PECL differential outputs
- One ECL/PECL differential or single-ended inputs (CLKA)
- One HSTL differential or single-ended inputs (CLKB)
- Hot-swappable/-insertable
- 29 ps typical output-to-output skew
- 95 ps typical part-to-part skew
- 400 ps typical propagation delay
- 0.16 ps typical RMS phase jitter
- 7 ps typical peak period jitter
- 1.5-GHz operation (2.7-GHz maximum toggle frequency)
- PECL and HSTL mode supply range: $V_{CC} = 2.5V \pm 5\%$ to $3.3V \pm 5\%$ with $V_{EE} = 0V$
- ECL mode supply range: $V_{EE} = -2.5V \pm 5\%$ to $-3.3V \pm 5\%$ with $V_{CC} = 0V$
- Industrial temperature range: $-40^{\circ}C$ to $85^{\circ}C$
- 20-pin SSOP package
- Temperature compensation like 100K ECL

Functional Description

The CY2DP314 is a low-skew, low propagation delay 2-to-4 differential fanout buffer targeted to meet the requirements of high-performance clock and data distribution applications. The device is implemented on SiGe technology and has a fully differential internal architecture that is optimized to achieve low signal skews at operating frequencies of up to 1.5 GHz (full swing).

The device features two differential input paths that are multiplexed internally. This mux is controlled by the CLK_SEL pin. The CY2DP314 may function not only as a differential clock buffer but also as a signal-level translator and fanout on HSTL or LVCMOS /LVTTTL single-ended signal to four ECL/PECL differential loads.

Since the CY2DP314 introduces negligible jitter to the timing budget, it is the ideal choice for distributing high frequency, high precision clocks across back-planes and boards in communication systems. Furthermore, advanced circuit design schemes, such as internal temperature compensation, ensure that the CY2DP314 delivers consistent performance over various platforms.



Pin Definitions

Pin	Name	I/O	Type	Description
1,10,11,20,3	VCC	+PWR	Power	Power supply, positive connection
2	NC			No connect
4	CLK_SEL	I,PD	ECL/PECL	Input Clock Select
5	CLKA	I,PD ^[1]	ECL/PECL	Default differential clock input
6	CLKA#	I, PD/PU	ECL/PECL	Default differential clock input
7	CLKB	I,PD	HSTL	Alternate differential clock input
8	CLKB#	I, PD/PU	HSTL	Alternate differential clock input
9	VEE ^[2]	-PWR	Power	Power supply, negative connection
18,16,14,12	Q[0:3]#	O	ECL/PECL	Complement output
19,17,15,13	Q[0:3]	O	ECL/PECL	True output

Table 1.

Control	Operation
CLK_SEL	
0	CLKA, CLKA# input pair is active (Default condition with no connection to pin) CLKA can be driven with ECL- or PECL-compatible signals with respective power configurations
1	CLKB, CLKB# input pair is active. CLKB can be driven with HSTL-compatible signals with respective power configurations

Governing Agencies

The following agencies provide specifications that apply to the CY2DP314. The agency name and relevant specification is listed below in *Table 2*.

Table 2.

Agency Name	Specification
JEDEC	JESD 020B (MSL) JESD 8-6 (HSTL) JESD 51 (Theta JA) JESD 8-2 (ECL) JESD 65-B (skew,jitter)
Mil-Spec	883E Method 1012.1 (Thermal Theta JC)

Notes:

- In the I/O column, the following notation is used: I for Input, O for Output, PD for Pull-Down, PU for Pull-Up, and PWR for Power.
- In ECL mode (negative power supply mode), V_{EE} is either $-3.3V$ or $-2.5V$ and V_{CC} is connected to GND (0V). In PECL mode (positive power supply mode), V_{EE} is connected to GND (0V) and V_{CC} is either $+3.3V$ or $+2.5V$. In both modes, the input and output levels are referenced to the most positive supply (V_{CC}) and are between V_{CC} and V_{EE} .

Absolute Maximum Ratings

Parameter	Description	Condition	Min.	Max.	Unit
V _{CC}	Positive Supply Voltage	Non-Functional	-0.3	4.6	V
V _{EE}	Negative Supply Voltage	Non-Functional	-4.6	0.3	V
T _S	Temperature, Storage	Non-Functional	-65	+150	°C
T _J	Temperature, Junction	Non-Functional		150	°C
ESD _h	ESD Protection	Human Body Model	2000		V
M _{SL}	Moisture Sensitivity Level		3		N.A.
Gate Count	Total Number of Used Gates	Assembled Die	50		gates

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

Operating Conditions

Parameter	Description	Condition	Min.	Max.	Unit
LU _I	Latch Up Immunity	Functional, typical	100		mA
T _A	Temperature, Operating Ambient	Functional	-40	+85	°C
∅ _{Jc}	Dissipation, Junction to Case	Functional	37 ^[3]		°C/W
∅ _{Ja}	Dissipation, Junction to Ambient	Functional	132 ^[3]		°C/W
I _{EE}	Maximum Quiescent Supply Current	V _{EE} pin		130 ^[4]	mA
C _{IN}	Input pin capacitance			3	pF
L _{IN}	Pin Inductance			1	nH
V _{IN}	Input Voltage	Relative to V _{CC} ^[5]	-0.3	V _{CC} + 0.3	V
V _{TT}	Output Termination Voltage	Relative to V _{CC} ^[5]	V _{CC} - 2		V
V _{OUT}	Output Voltage	Relative to V _{CC} ^[5]	-0.3	V _{CC} + 0.3	V
I _{IN}	Input Current ^[6]	V _{IN} = V _{IL} , or V _{IN} = V _{IH}		±150I	µA

PECL/HSTL DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
V _{CC}	Operating Voltage	2.5V ± 5%, V _{EE} = 0.0V 3.3V ± 5%, V _{EE} = 0.0V	2.375 3.135	2.625 3.465	V V
V _{CMR}	PECL Input Differential Crosspoint Voltage ^[7]	Differential operation	1.2	V _{CC}	V
V _X	HSTL Input Differential Crosspoint Voltage ^[8]	Standard Load Differential Operation	0.68	0.9	V
V _{OH}	Output High Voltage	I _{OH} = -30 mA ^[9]	V _{CC} - 1.25	V _{CC} - 0.7	V
V _{OL}	Output Low Voltage V _{CC} = 3.3V ± 5% V _{CC} = 2.5V ± 5%	I _{OL} = -5 mA ^[9]	V _{CC} - 1.995 V _{CC} - 1.995	V _{CC} - 1.5 V _{CC} - 1.3	V V
V _{IH}	Input Voltage, High	Single-ended operation	V _{CC} - 1.165	V _{CC} - 0.880 ^[10]	V
V _{IL}	Input Voltage, Low	Single-ended operation	V _{CC} - 1.945 ^[10]	V _{CC} - 1.625	V

Notes:

- Theta JA EIA JEDEC 51 test board conditions (typical value); Theta JC 883E Method 1012.1.
- Power Calculation: V_{CC} * I_{EE} + 0.5 (I_{OH} + I_{OL}) (V_{OH} - V_{OL}) (number of differential outputs used); I_{EE} does not include current going off chip.
- where V_{CC} is 3.3V±5% or 2.5V±5%.
- Inputs have internal pull-up/pull-down or biasing resistors which affect the input current.
- Refer to Figure 1.
- V_X(AC) is the crosspoint of the differential HSTL input signal. Normal AC operation is obtained when the crosspoint is within the V_X(AC) range and the input swing lies within the V_{DIF}(AC) specification. Violation of V_X(AC) or V_{DIF}(AC) impacts the device propagation delay, device and part-to-part skew. Refer to Figure 2.
- Equivalent to a termination of 50Ω to V_{TT}. I_{OHMIN} = (V_{OHMIN}-V_{TT})/50; I_{OHMAX}=(V_{OHMAX}-V_{TT})/50; I_{OLMIN}=(V_{OLMIN}-V_{TT})/50; I_{OLMAX}=(V_{OLMAX}-V_{TT})/50.
- V_{IL} will operate down to V_{EE}; V_{IH} will operate up to V_{CC}.

ECL DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
V _{EE}	Negative Power Supply	-2.5V ± 5%, V _{CC} = 0.0V -3.3V ± 5%, V _{CC} = 0.0V	-2.625 -3.465	-2.375 -3.135	V
V _{CMR}	ECL Input Differential cross point voltage ^[7]	Differential operation	V _{EE} + 1.2	0V	V
V _{OH}	Output High Voltage	I _{OH} = -30 mA ^[9]	-1.25	-0.7	V
V _{OL}	Output Low Voltage V _{EE} = -3.3V ± 5% V _{EE} = -2.5V ± 5%	I _{OL} = -5 mA ^[9]	-1.995 -1.995	-1.5 -1.3	V
V _{IH}	Input Voltage, High	Single-ended operation	-1.165	-0.880 ^[10]	V
V _{IL}	Input Voltage, Low	Single-ended operation	-1.945 ^[10]	-1.625	V

AC Electrical Specifications

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
V _{PP}	ECL/PECL Input Differential Input Voltage ^[7]	Differential operation	0.1		1.3	V
V _{CMRO}	Output Common Voltage Range			V _{CC} - 1.425		V
F _{CLK}	Input Frequency	50% duty cycle Standard load	-		1.5	GHz
T _{PD}	Propagation Delay CLKA or CLKB to Output pair ^[12]	PECL, ECL < 660 MHz HSTL < 1 GHz	280 280	400 400	650 750	ps ps
V _{DIF}	HSTL Differential Input Voltage ^[11]	Duty Cycle Standard Load Differential Operation	0.4		1.9	V
V _X	HSTL Input Differential Crosspoint Voltage ^[8]	Standard Load Differential Operation	0.68		0.9	V
V _o	Output Voltage (peak-to-peak; see Figure 2)	< 1 GHz	0.375		-	V
tsk ₍₀₎	Output-to-output Skew	<660 MHz ^[12] , See Figure 3	-	29	50	ps
tsk _(PP)	Part-to-Part Output Skew ^[12]		-	95	150	ps
t _{jit(per)}	Output Period Jitter (peak) ^[13]	156.25 MHz ^[12]	-	7	15	ps
t _{jit(pn)}	Output RMS Phase Jitter ^[12, 13] (see Figure 6)	156.25 MHz, broadband, 3.3V	-	0.175	-	ps
		156.25 MHz, Filtered, 3.3V	-	0.159	-	ps
		312.5 MHz, broadband, 3.3V	-	0.266	-	ps
		312.5 MHz, Filtered, 3.3V	-	0.260	-	ps
tsk _(P)	Output Pulse Skew ^[14]	660 MHz ^[12] , See Figure 3	-		50	ps
T _R , T _F	Output Rise/Fall Time (see Figure 2)	50% duty cycle Differential 20% to 80%	0.08		0.3	ns

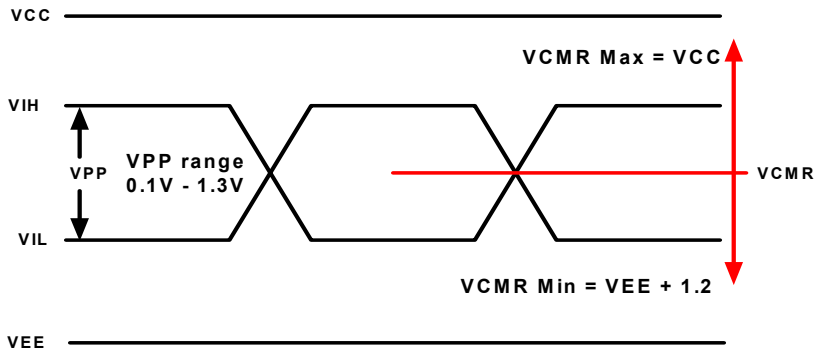
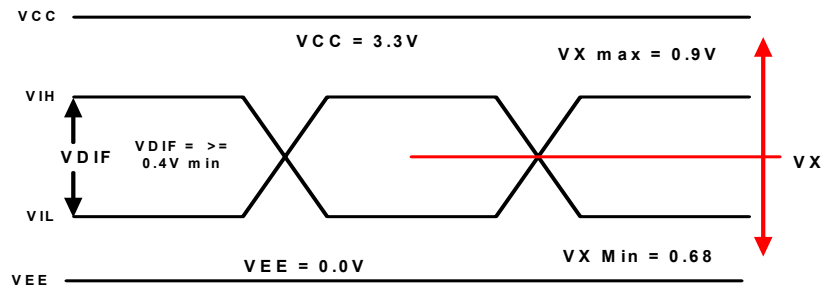
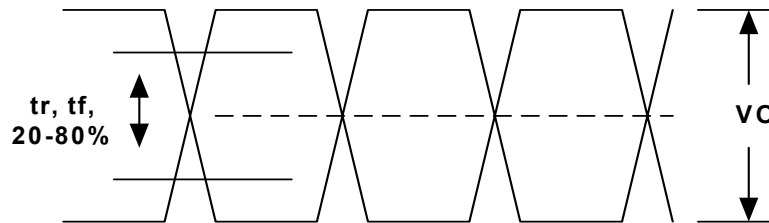
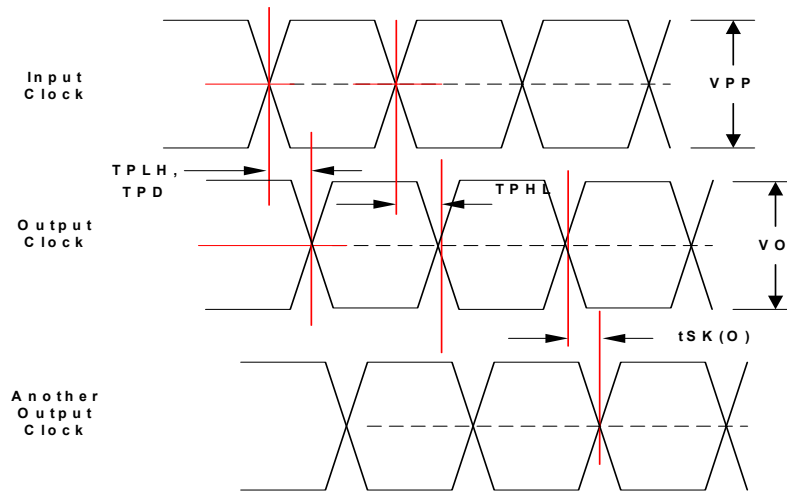
Notes:

11. V_{DIF} (AC) is the minimum differential HSTL input voltage swing required to maintain AC characteristics including tkpd and device-to-device skew.

12. 50% duty cycle; standard load; differential operation.

13. For further information regarding jitter, please refer to the application note "Understanding data sheet jitter specifications for Cypress timing products".

14. Output pulse skew is the absolute difference of the propagation delay times: | t_{PLH} - t_{PHL} |.

Timing Definitions

Figure 1. PECL/ECL Input Waveform Definitions

Figure 2. HSTL Differential Input Waveform Definitions

Figure 3. ECL/LVPECL Output

Figure 4. Propagation Delay (T_{PD}), output pulse skew ($|t_{PLH} - t_{PHL}|$), and output-to-output skew ($t_{SK(O)}$) for both CLKA or CLKB to Output Pair, PECL/ECL to PECL/ECL

Test Configuration

Standard test load using a differential pulse generator and differential measurement instrument.

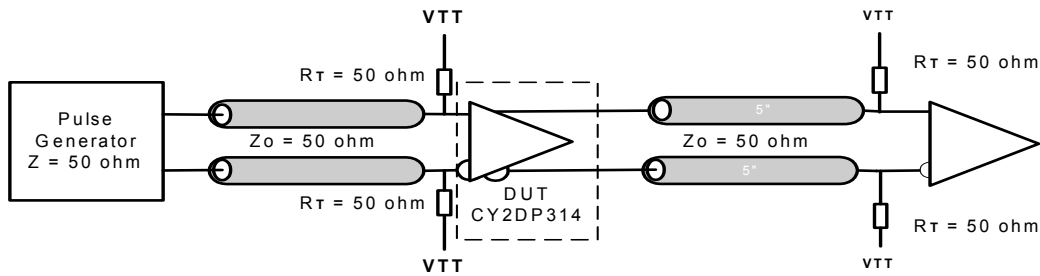


Figure 5. CY2DP314 AC Test Reference

Supplemental Parametric Information

RMS Phase Jitter: 0.159 ps typical @ 156.25 MHz, 10 GbE Filter (1.875 MHz – 20 MHz)
 0.175 ps typical @ 156.25 MHz, Broadband (Raw Data from 10 Hz – 20 MHz)

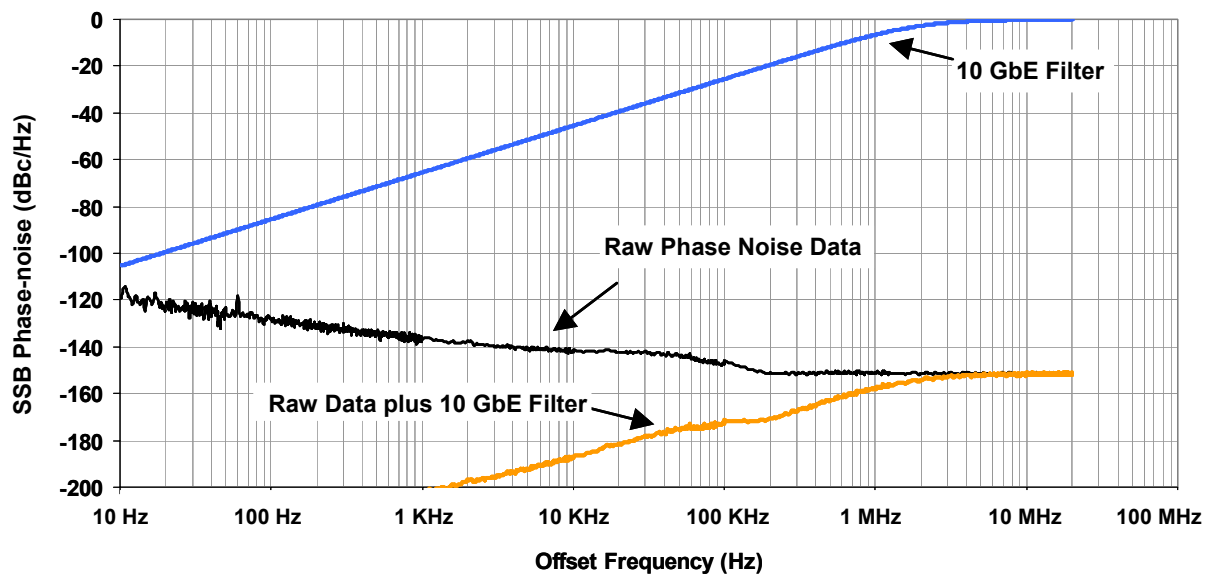
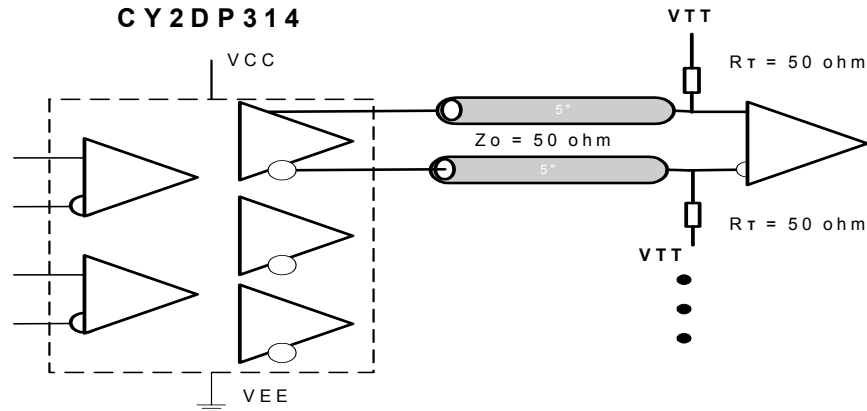
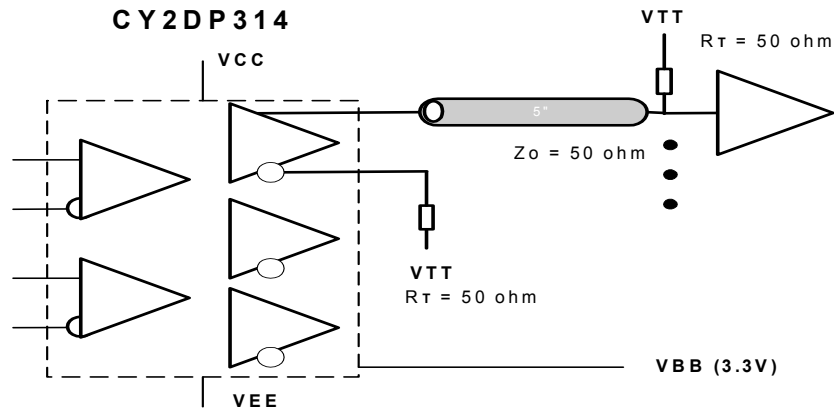
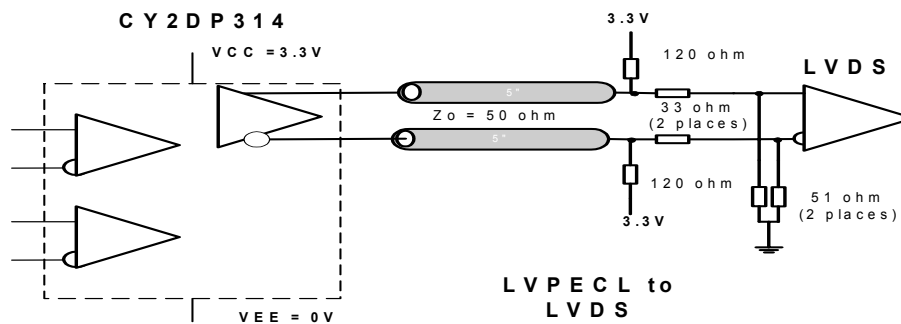
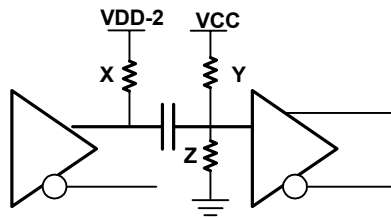


Figure 6. Typical Phase-noise Characteristics at 156.25 MHz, 3.3V, Room Temperature

Applications Information
Termination Examples

Figure 7. Standard LVPECL – PECL Output Termination

Figure 8. Driving a PECL/ECL Single-ended Input

Figure 9. Low-voltage Positive Emitter-coupled Logic (LVPECL) to a Low-voltage Differential Signaling (LVDS) Interface



One output is shown for clarity

Figure 10. Termination for LVPECL to H I S L interface for VCC = 2.5V would use X = 50 Ohms, Y = 2300 Ohms, and Z = 1000 Ohms. See application note titled *PECL Translation, SAW Oscillators, and Specs for Other Signalling Standards and Supplies*

Ordering Information

Part Number	Package Type	Product Flow
CY2DP314OI	20-pin SSOP	Industrial, -40° to 85°C
CY2DP314OIT	20-pin SSOP – Tape and Reel	Industrial, -40° to 85°C
Lead-free		
CY2DP314OXI	20-pin SSOP	Industrial, -40° to 85°C
CY2DP314OXIT	20-pin SSOP – Tape and Reel	Industrial, -40° to 85°C

Document History Page

Document Title: CY2DP314 FastEdge™ SERIES 1:4 Differential Clock/Data Fanout Buffer				
Document Number: 38-07550				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	126779	06/13/03	RGL	New data sheet
*A	128940	08/19/03	RGL	Changed the operation value from 1.5 GHz, reduced swing to 3 GHz to from DC to above 1.5 GHz Changed V_{CC} value in the I_{IN} parameter from 3.6V to 3.645V. Changed the V_{OL} min value from $V_{CC}-1.9$ to $V_{CC}-1.945$ Changed the I_{EE} max value from 48 mA to 130 mA Specified the max input frequency (F_{CLK}) to 2200 MHz Specified the TTB max value to 250 ps
*B	207710	See ECN	RGL	Added Junction Temperature (T_J) parameter in the Absolute Max. Conditions table Replaced I_{CC} calculation with power calculation in the footnote
*C	237748	See ECN	RGL	Provided data for TBDs to match the device
*D	247603	See ECN	RGL/GGK	Changed V_{OH} and V_{OL} to match the Char Data
*E	270151	See ECN	RGL	Removed all V_{BB} references Added Lead-free devices
*F	346157	See ECN	RGL	Minor Change: corrected the CLK_SEL input type to ECL/PECL
*G	393406	See ECN	RGL	Updated Jitter values, Added typical values