Peregrine Semiconductor

Preliminary Specification

PE95420

RF SPDT Switch
Hermetically sealed ceramic package
DC – 8500 MHz

Product Description

The PE95420 is an RF SPDT (single pole double throw) switch and is available in a hermetically sealed ceramic package. The PE95420 is designed to cover a broad range of applications from near DC to 8500 MHz for use in various Hi-Rel industries and applications requiring broadband performance. It uses Peregrine's UltraCMOS™ process and features HaRP™ technology enhancements to deliver high linearity and exceptional harmonics performance. HaRP technology is an innovative feature of the UltraCMOS™ process providing upgraded linearity performance.

The PE95420 is an absorptive/non-reflective switch design which is an ideal termination method for RF elements in a system design. A single-pin 2.2V CMOS logic control in a single chip solution reduces the number of control lines.

Features

- HaRP™-Technology-Enhanced
  - Eliminates Gate and Phase Lag
  - No insertion loss or phase drift
- High linearity 60 dBm IIP3
- Low insertion loss:
  - 0.8 dB at 100 MHz
  - 1.4 dB at 3000 MHz
  - 1.5 dB at 6000 MHz
- High isolation
  - 65 dB at 100 MHz
  - 42 dB at 3000 MHz
  - 40 dB at 6000 MHz
- 1 dB compression point of +30 dBm
- Single-pin 3.3 V CMOS logic control
- ESD tolerant to 2000 V HBM
- Absorptive/Non-Reflective
- Offered in a 7-lead Hermetic CSOIC Surface-Mount Package and in DIE form

Typical Industries

- Medical
- Automotive
- Telecom Infrastructure
- Test Instrumentation
- Down-hole oil/gas
- Military
- Screening available for commercial space applications

Figure 1. Functional Diagram

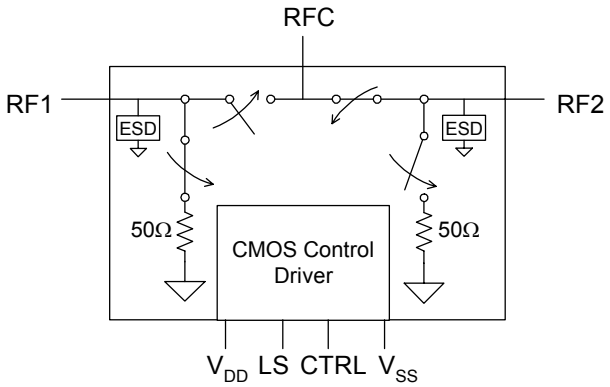


Figure 2. Package Type

7-lead CSOIC

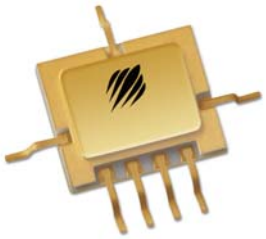
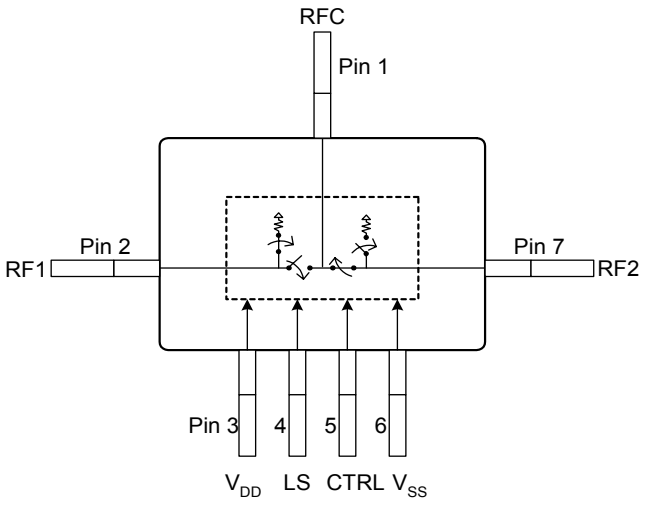


Table 1. Electrical Specifications @ +25°C, V_{DD} = 3.3 V

Parameter	Conditions	Min	Typical	Max	Units
Operation Frequency		DC		8500	MHz
Insertion Loss	100 MHz, 0 dBm 3000 MHz, 0 dBm 6000 MHz, 0 dBm 8500 MHz, 0 dBm		0.8 1.2 1.5 1.7		dB dB dB dB
Isolation – RF1 to RF2	100 MHz 3000 MHz 6000 MHz 8500 MHz		82 48 35 30		dB dB dB dB
Isolation - RFC to RF1/RF2	100 MHz 3000 MHz 6000 MHz 8500 MHz		74 46 42 33		dB dB dB dB
Return Loss ON State	100 MHz 3000 MHz 6000 MHz 8500 MHz		20 21 16 9		dB dB dB dB
Return Loss OFF State	100 MHz 3000 MHz 6000 MHz 8500 MHz		19 18 15 10		dB dB dB dB
Switching Time	50% CTRL to 0.1 dB final value		2		µs
Input 1 dB Compression	6000 MHz		33		dBm
Input IP3	6000 MHz		60		dBm

Figure 3. Pin Layout (Top View)



Note 1: No DC voltage should be applied at RF ports.

Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	RFC[1]	RF Common
2	RF1[1]	RF Port 1
3	V_{DD}	Nominal 3.3 V supply connection
4	LS	Selects the RF1 to RFC path (See Table 5)
5	CTRL	Selects the RF2 to RFC path (See Table 5)
6	V_{SS}	Negative power supply. Apply nominal – 3.3 V supply
7	RF2[1]	RF Port 2

Table 3. Operating Ranges

Parameter	Min	Typ	Max	Units
V_{DD} Positive Power Supply Voltage	3.0	3.3	3.6	V
V_{DD} Negative Power Supply Voltage	-3.6	-3.3	-3.0	V
I_{DD} Power Supply Current (V_{DD} = 3.3V, LS or CTRL = 3.3V)		100		µA
Control Voltage High	0.7xV_{DD}			V
Control Voltage Low			0.3xV_{DD}	V
Operating temperature range	-40		85	°C
RF Power In: 20 MHz ≤ 8.5 GHz			24	dBm

Table 4. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_{C1}	Voltage on LS input	-0.3	V_{DD}+ 0.3	V
V_{C2}	Voltage on CTRL input	-0.3	V_{DD}+ 0.3	V
T_{ST}	Storage temperature range	-65	150	°C
V_{ESD}	ESD voltage (Human Body Model)		2000	V

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Table 5. Truth Table

LS	CTRL	RFC-RF1	RFC-RF2
0	0	off	off
0	1	off	on
1	0	on	off
1	1	on	on

Exposed Solder Pad Connection

The exposed solder pad on the bottom of the package must be grounded for proper device operation.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rate specified.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Switching Frequency

The PE95420 has a maximum 25 kHz switching rate.

Performance Plots

Figure 4. Isolation, RFC-RF1, V_{DD}=3.3V across Temperature

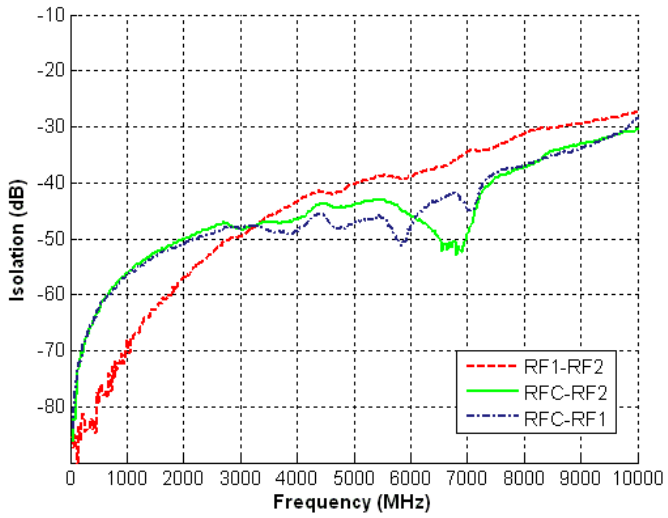


Figure 5. Isolation, OFF-State

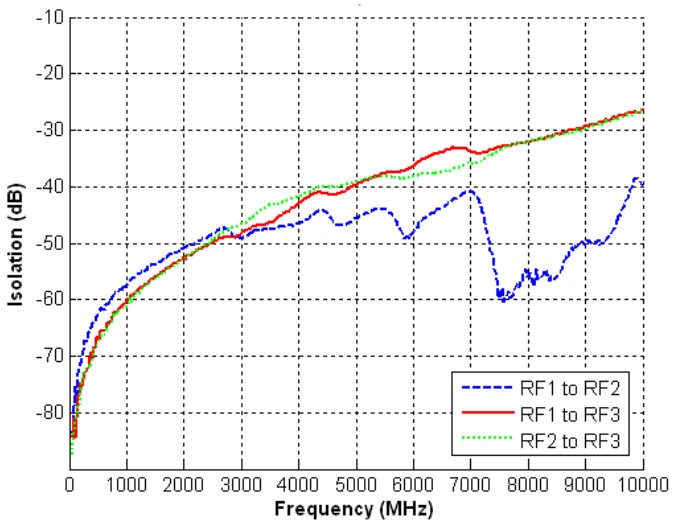


Figure 6. Insertion Loss

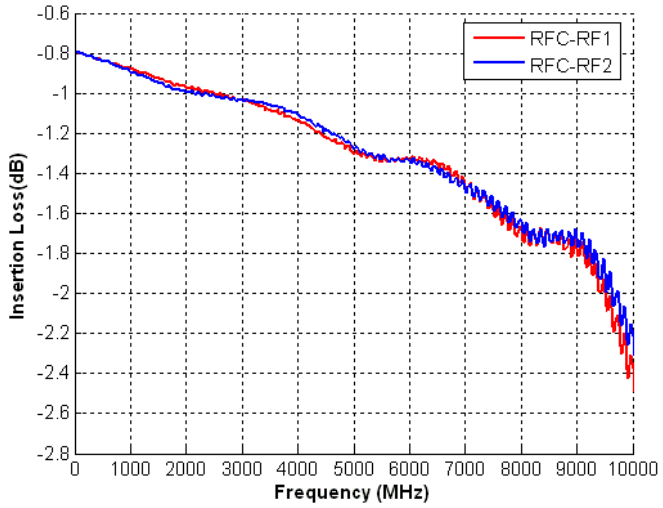


Figure 7. Return Loss, RFC ON

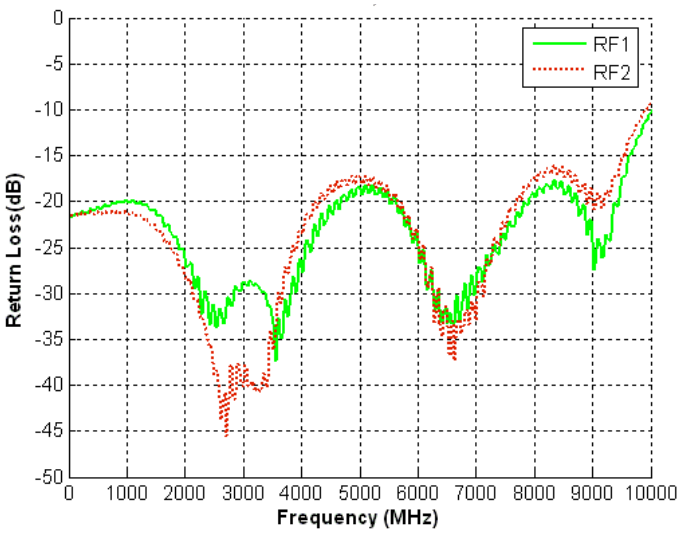
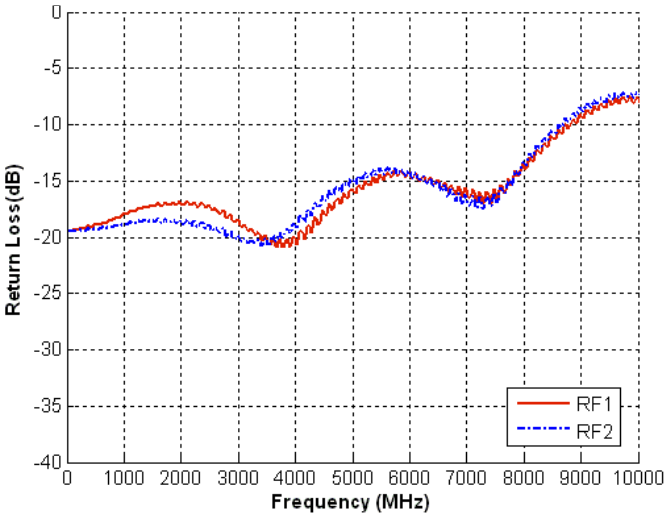


Figure 8. Return Loss, RFC OFF



Evaluation Boards

The SPDT switch EK Board was designed to ease customer evaluation of Peregrine's PE95420. The RF common port is connected through a 50 Ω transmission line via the top SMA connector, J1. RF1 and RF2 are connected through 50 Ω transmission lines via SMA connectors J2 and J3, respectively. A through 50 Ω transmission is available via SMA connectors J5 and J6. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The evaluation kit board is constructed of four metal layers. The dual clad top RF layer is Rogers RO4003 material with an 8 mil RF core and er = 3.55. The other two dielectric layers are FR4 for DC control and overall board strength with an cumulative board thickness of 62 mils. The RF transmission lines were designed using a Grounded co-planar waveguide with a linewidth of 15 mils and gap of 7 mils.

Figure 9. Evaluation Board Layouts

Peregrine Specification 101-0345

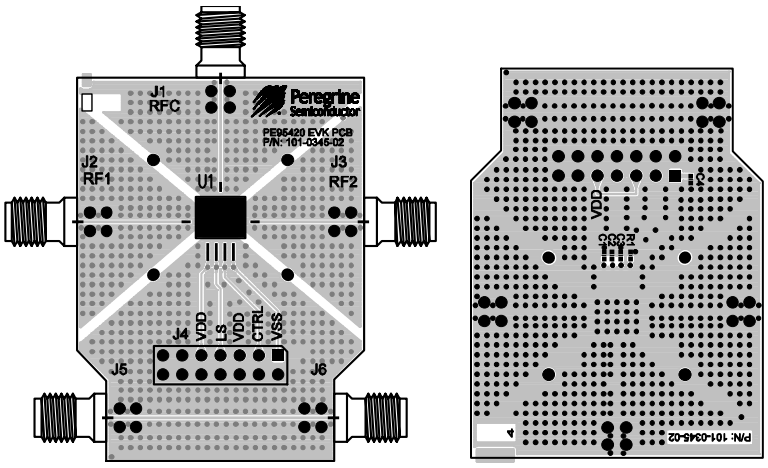


Figure 10. Evaluation Kit Schematic

Peregrine Specification 102-0417

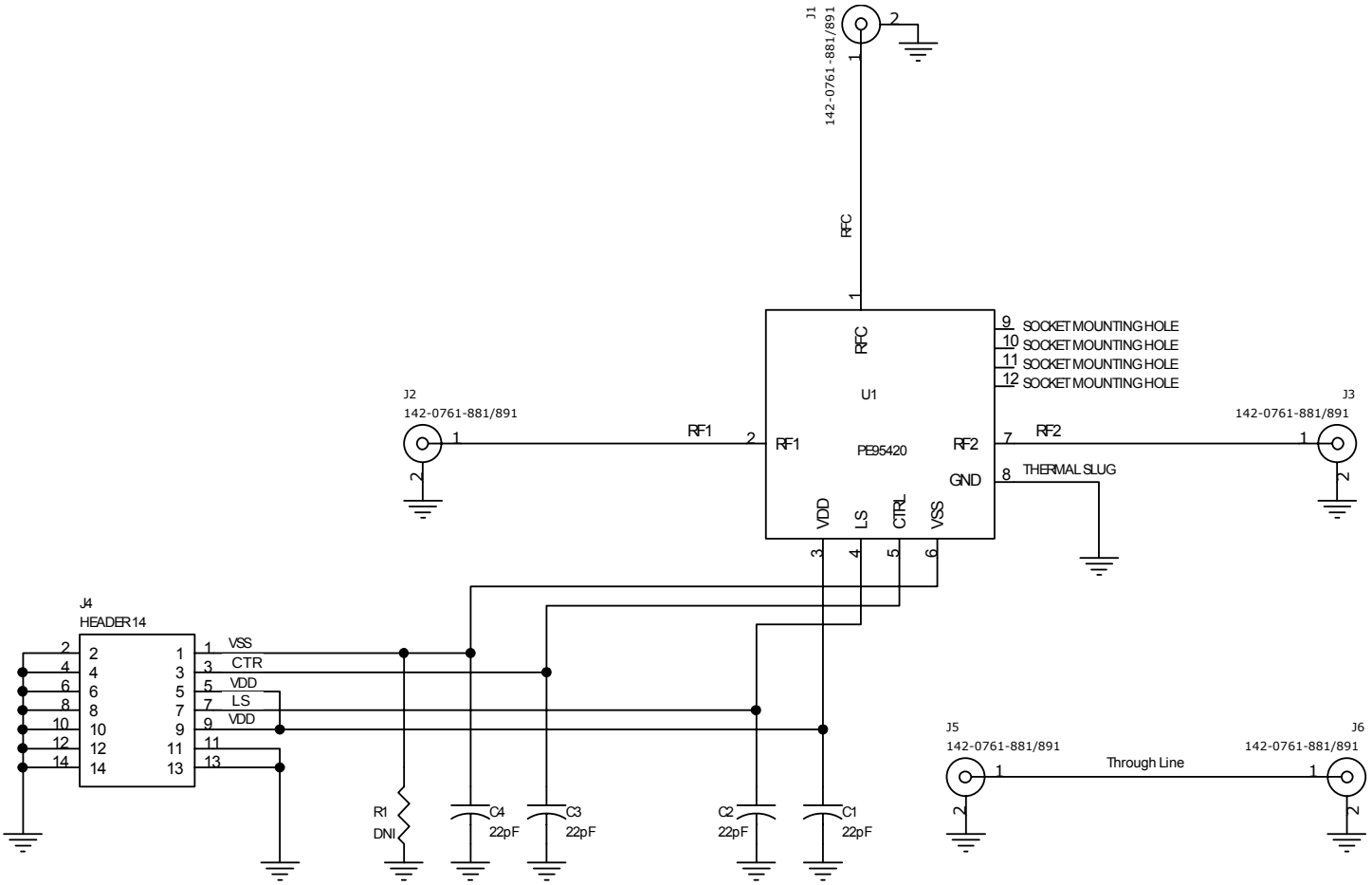
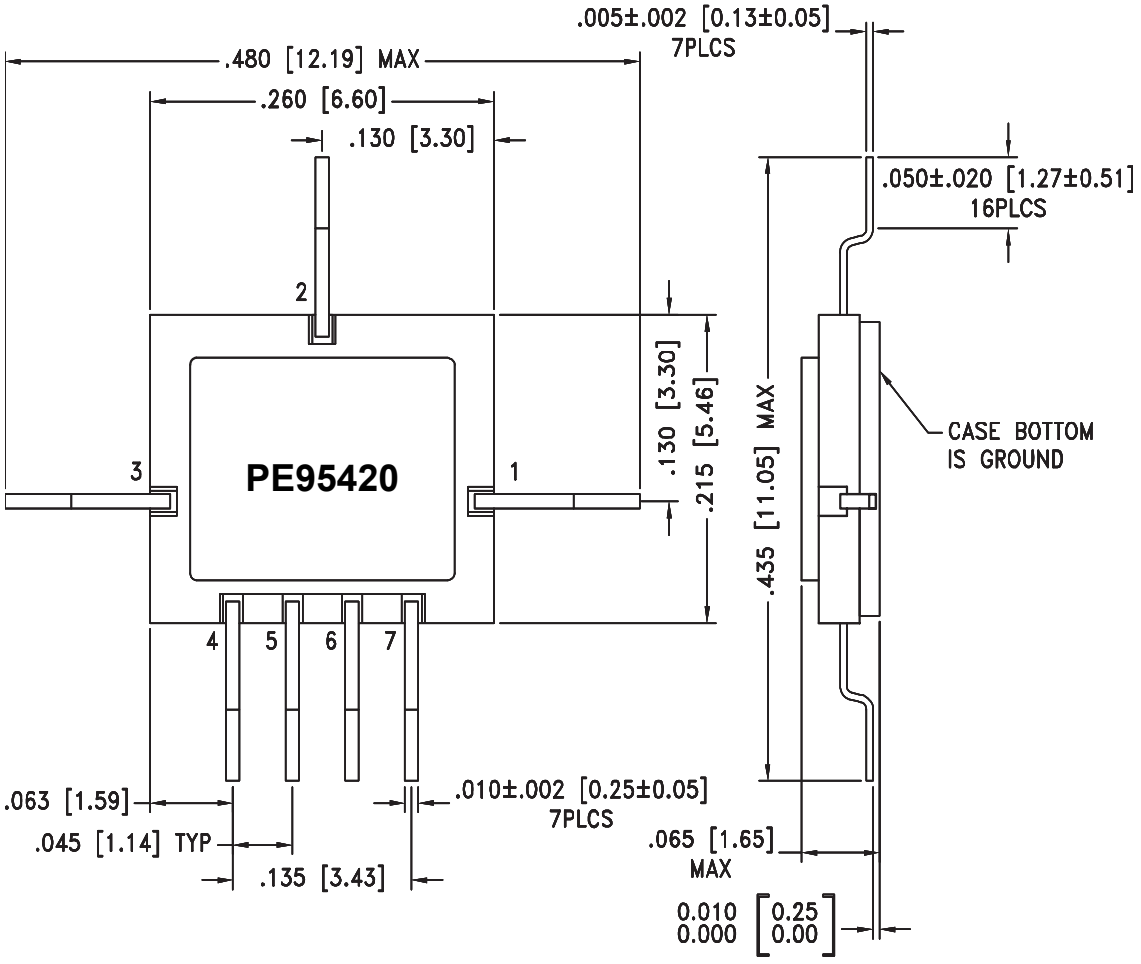


Figure 11. Package Drawing

7-lead CSOIC



NOTES:
1. PACKAGE BODY MATERIAL: WHITE ALUMINA 92%
2. CONDUCTOR TRACES MATERIAL: THICK FILM TUNGSTEN
3. LEAD IS Fe-Ni-Co ALLOY
4. BASE IS Cu-W
5. PLATING: ELECTROLYTIC GOLD 50 MICRO-INCHES MIN, OVER ELECTROLYTIC NICKEL 75 MICRO-INCHES MIN.
6. ALL DIMENSIONS ARE IN INCHES [MILLIMETERS]
7. TOLERANCES: ±.005 [0.13] UNLESS OTHERWISE SPECIFIED.
8. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

Table 6. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
95420-01	9542001	PE95420-7CSOIC-50B Engineering Samples	7-lead CSOIC	50 Count Trays
95420-11	9542011	PE95420-7CSOIC-50B Production Units	7-lead CSOIC	50 Count Trays
95420-99		Production Die	Die	400 Units/Waffle Pack
95420-00	PE95420-EK	PE95420 Evaluation Kit	Evaluation Board	1 / Box

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Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

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