Features

- 80C51 Core
  - 12 or 6 Clocks per Instruction (X1 and X2 Modes)
  - 256 Bytes Scratchpad RAM
  - Dual Data Pointer
  - Two 16-bit Timer/Counters: T0 and T1
- T83C5121 with 16 Kbytes Mask ROM
- T85C5121 with 16 Kbytes Code RAM
- T89C5121 with 16 Kbytes Code RAM and 16 Kbytes EEPROM
- On-chip Expanded RAM (XRAM): 256 Bytes
- Versatile Host Serial Interface
  - Full-duplex Enhanced UART (EUART) with Dedicated Baud Rate Generator (BRG): Most Standard Speeds up to 230K bits/s at 7.36 MHz
  - Output Enable Input
  - Multiple Logic Level Shifters Options (1.8V to V_{CC})
  - Automatic Level Shifter Option
- Multi-protocol Smart Card Interface
  - Certified with Dedicated Firmware According to ISO 7816, EMV96, GIE-CB, GSM 11.12V and WHQL Standards
  - Asynchronous Protocols T = 0 and T = 1 with Direct and Inverse Modes
  - Baud Rate Generator Supporting All ISO7816 Speeds up to D = 32/F = 372
  - Parity Error Detection and Indication
  - Automatic Character Repetition on Parity Errors
  - Programmable Timeout Detection
  - Card Clock Stop High or Low for Card Power-down Mode
  - Support Synchronous Card with C4 and C8 Programmable Outputs
  - Card Detection and Automatic De-activation Sequence
  - Step-up/down Converter with Programmable Voltage Output: 5V, 3V (± 8% at 60 mA) and 1.8V (±8% at 20 mA)
  - Direct Connection to Smart Card Terminals:
    Short Circuit Current Limitation
    Logic Level Shifters
    4 kV ESD Protection (MIL/STD 833 Class 3)
- Alternate Card Support with CLK, I/O and RST According to GSM 11.12V Standard
- 2x I/O Ports: 6 I/O Port1 and 8 I/O Port3
- 2x LED Outputs with Programmable Current Sources: 2, 4, or 10 mA
- Hardware Watchdog
- Reset Output Includes
  - Hardware Watchdog Reset
  - Power-on Reset (POR)
  - Power-fail Detector (PFD)
- 4-level Priority Interrupt System with 7 Sources
- 7.36 to 16 MHz On-chip Oscillator with Clock Prescaler
- Absolute CPU Maximal Frequency: 16 MHz in X1 mode, 8MHz in X2 mode
- Idle and Power-down Modes
- Voltage Operation: 2.85V to 5.4V
- Low Power Consumption
  - 8 mA Operating Current (at 5.4V and 3.68 MHz)
  - 150 mA Maximum Current with Smart Card Power-on (at 16 MHz X1 Mode)
  - 20 µA Maximum Power-down Current at 3.0V (without Smart Card)
  - 30 µA Maximum Power-down Current at 3.6V (without Smart Card)
  - 100 µA Maximum Power-down Current at 5.4V (without Smart Card)
- Temperature Range
  - Commercial: 0 to +70°C Operating Temperature
  - Industrial: -40 to +85°C Operating Temperature
- Packages
  - SSOP24
  - PLCC52

8-bit Microcontroller with Multi-protocol Smart Card Interface

T83C5121
T85C5121
T89C5121

Rev. 4164C–SCR–07/03

Description

T8xC5121 is a high performance CMOS ROM/CRAM derivative of the 80C51 CMOS single chip 8-bit microcontrollers.

T8xC5121 retains the features of the Atmel 80C51 with extended ROM capacity (16 Kbytes), 512 bytes of internal RAM, a 4-level interrupt system, two 16-bit timer/counters (T0/T1), a full duplex enhanced UART (EUART) with baud rate generator (BRG) and an on-chip oscillator.

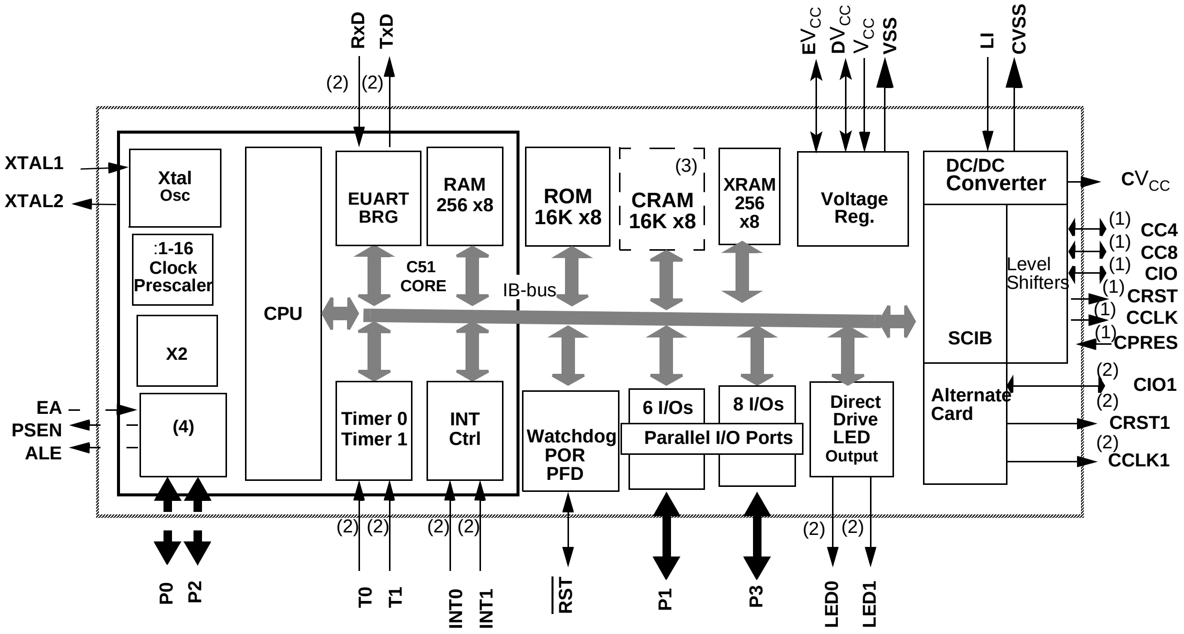
In addition, the T8xC5121 have, a Multi protocol Smart Card Interface, a dual data pointer, 2 programmable LED current sources (2-4-10 mA) and a hardware Watchdog.

T89C5121 Flash RAM version and T85C5121 Code RAM version can be loaded by In-System Programming (ISP) software residing in the on-chip ROM from a low-cost external serial EEPROM or from R232 interface.

T8xC5121 have 2 software-selectable modes of reduced activity for further reduction in power consumption.

Block Diagram

Figure 1. Block Diagram



Notes:
1. Alternate function of Port 1
2. Alternate function of Port 3
3. Only for the Code RAM version
4. Only for PLCC52

Pin Description

Figure 2. T8xC5121 24-pin SSOP Pinout

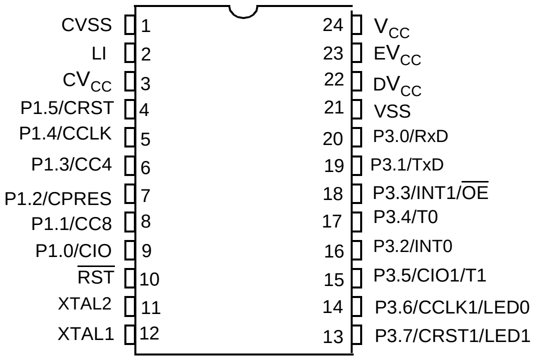
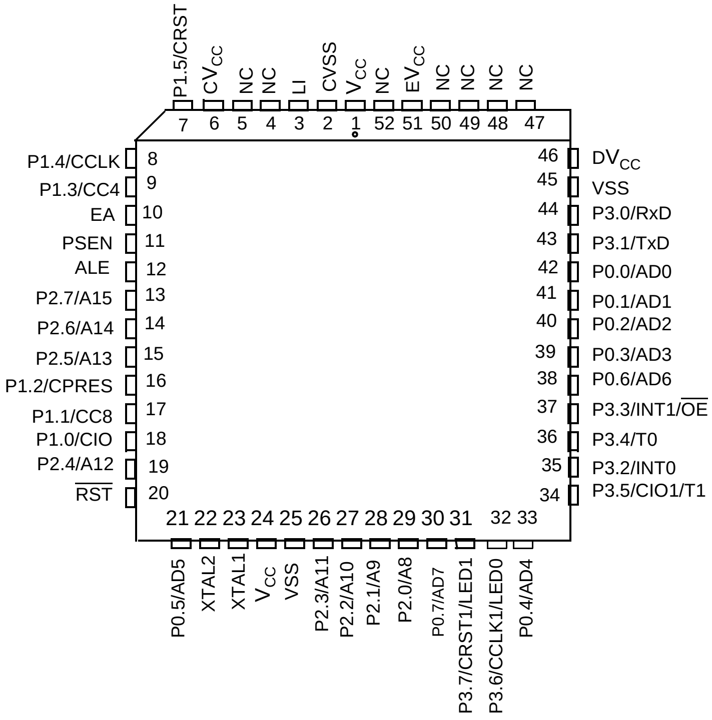


Figure 3. T8xC5121 PLCC52 Pinout



Signals

All the T8xC5121 signals are detailed in Table 1.

The port structure is described in Section “Port Structure Description”.

Table 1. Ports Description

Port	Signal Name	Alternate	Internal Power Supply	ESD	Type	Description
P1.0	CIO		CV_{CC}	4 kV	I/O	**Smart card interface function** Card I/O.
					I/O	**Input/Output function** P1.0 is a bi-directional I/O port .
					I	**Reset configuration** Input .
P1.1	CC8		CV_{CC}	4 kV	O	**Smart card interface function** Card contact 8
					O	**Output function** P1.1 is a Push-pull port.
					I	**Reset configuration** Input
P1.2	CPRES		V_{CC}	4 kV	I	**Smart card interface function** Card presence
					I/O	**Input/Output function** P1.2 is a bi-directional I/O port with internal pull-ups- (External Pull-up configuration can be selected).
					I	**Reset configuration** Input (high level due to internal pull-up)
P1.3	CC4		CV_{CC}	4 kV	O	**Smart card interface function** Card contact 4
					O	**Output function** P1.3 is a Push-pull port.
					I	**Reset configuration** Input (high level due to internal pull-up)
P1.4	CCLK		CV_{CC}	4 kV	O	**Smart card interface function** Card clock
					I/O	**Input/Output function** P1.4 is a a Push-pull port.
					O	**Reset configuration** Output at low level
P1.5	CRST		CV_{CC}	4 kV	O	**Smart card interface function** Card reset
					I/O	**Input/Output function** P1.5 is a a Push-pull port.
					O	**Reset configuration** Output at low level

Table 1. Ports Description (Continued)

Port	Signal Name	Alternate	Internal Power Supply	ESD	Type	Description
P3.0	RxD		EV_{CC}		I	**UART function** Receive data input
					I/O	**Input/Output function** P3.0 is a bi-directional I/O port with internal pull-ups.
					I	**Reset configuration** Input (high level)
P3.1	TxD		EV_{CC}		O	**UART function** Transmit data output OE active at low or high level depending of PMSOEN bits in SIOCON Reg.
					I/O	**Input/Output function** P3.1 is a bi-directional I/O port with internal pull-ups.
					Z	**Reset configuration** High impedance due to PMOS switched OFF
P3.2	INT0		DV_{CC}		I	**External interrupt 0** $\overline{\text{INT0}}$ input set IE0 in the TCON register. If bit IT0 in this register is set, bits IE0 are set by a falling edge on $\overline{\text{INT0}}$. If bit IT0 is cleared, bits IE0 is set by a low level on $\overline{\text{INT0}}$.
					I/O	**Input/Output function** P3.2 is a bi-directional I/O port with internal pull-ups.
					I	**Timer 0: Gate input** INT0 serves as external run control for Timer 0 when selected in TCON register.
					I	**Reset configuration** Input (high level)
P3.3	INT1	OE	EV_{CC}		I	**External Interrupt 1** $\overline{\text{INT1}}$ input set OEIT in ISEL Register, IE1 in the TCON register. If bit IT1 in this register is set, bits OEIT and IE1 are set by a falling edge on $\overline{\text{INT1}}$. If bit IT1 is cleared, bits OEIT and IE1 is set by a low level on $\overline{\text{INT1}}$
					I	**UART function** Output enable. A low or high level (depending OELEV bit in ISEL Register) on this pin disables the PMOS transistors of TxD (P3.1) and T0 (P3.4). This function can be disabled by software
					I/O	**Input/Output function** P3.3 is a bi-directional I/O port with internal pull-ups.
					I	**Timer 1 function: Gate input** INT1 serves as external run control for Timer 1 when selected in TCON register.
					I	**Reset configuration** Input (high level)
P3.4		T0	EV_{CC}		O	**UART function** OE active at low or high level depending of PMSOEN bits in SIOCON Reg.

Table 1. Ports Description (Continued)

Port	Signal Name	Alternate	Internal Power Supply	ESD	Type	Description
					I/O	**Input/Output function** P3.4 is a bi-directional I/O port with internal pull-ups.
					I	**Timer 0 function: External clock input** When Timer 0 operates as a counter, a falling edge on the T0 pin increments the count.
					Z	**Reset configuration** High impedance due to PMOS switched OFF
P3.5	CIO1		DV_{CC}		I/O	**Alternate card function** Card I/O
					I/O	**Input/Output function** P3.5 is a bi-directional I/O port with internal pull-ups.
					I	**Timer 1 function: External clock input** When Timer 1 operates as a counter, a falling edge on the T1 pin increments the count.
					I	**Reset configuration** Input (high level due to internal pull-up)
P3.6	CCLK1	LED1	DV_{CC}		O	**Alternate card function** Card clock
					O	**LED function** These pins can be directly connected to the cathode of standard LED without external current limiting resistors. The typical current of each output can be programmed by software to 2, 4 or 10 mA (LEDCON register).
					I/O	**Input/Output function** P3.6 is a LED port.
					I	**Reset configuration** Input at high level
P3.7	CRST1		DV_{CC}		O	**Alternate card function** Card reset
P3.7	CRST1	LED0	DV_{CC}		O	**LED function** These pins can be directly connected to the cathode of standard LED without external current limiting resistors. The typical current of each output can be programmed by software to 2, 4 or 10 mA (LEDCON register).
					I/O	**Input/Output function** P3.7 is a a LED port.
					I	**Reset configuration** Input at high level

Table 1. Ports Description (Continued)

Port	Signal Name	Alternate	Internal Power Supply	ESD	Type	Description
RST			V_{CC}		I/O	**Reset input** Holding this pin low for 64 oscillator periods while the oscillator is running resets the device. The Port pins are driven to their reset conditions when a voltage lower than V_{IL} is applied, whether or not the oscillator is running. This pin has an internal pull-up resistor which allows the device to be reset by connecting a capacitor between this pin and VSS. Asserting $\overline{\text{RST}}$ when the chip is in Idle mode or Power-down mode returns the chip to normal operation. The output is active for at least 12 oscillator periods when an internal reset occurs.
XTAL1			V_{CC}		I	**Input to the on-chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin.
XTAL2			V_{CC}		O	**Output of the on-chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, XTAL2 may be left unconnected.
V_{CC}					PWR	**Supply voltage** V_{CC} is used to power the internal voltage regulators and internal I/O's.
LI					PWR	**DC/DC input** LI must be tied to V_{CC} through an external coil (typically 4, 7 µH) and provide the current for the pump charge of the DC/DC converter.
CV_{CC}					PWR	**Card Supply voltage** CV_{CC} is the programmable voltage output for the Card interface. It must be connected to an external decoupling capacitor.
DV_{CC}					PWR	**Digital Supply voltage** DV_{CC} is used to supply the digital core and internal I/Os. It is internally connected to the output of a 3V regulator and must be connected to an external decoupling capacitor.
EV_{CC}			V_{CC}		PWR	**Extra supply voltage** EV_{CC} is used to supply the level shifters of UART interface I/O pins. It must be connected to an external decoupling capacitor. This reference voltage is generated internally (automatically or not), or it can be connected to an external voltage reference.
CVSS					GND	**DC/DC ground** CVSS is used to sink high shunt currents from the external coil.
VSS					GND	**Ground**

ONLY FOR PLCC52 version

Table 1. Ports Description (Continued)

Port	Signal Name	Alternate	Internal Power Supply	ESD	Type	Description
P0[7:0]	AD[7:0]		V_{CC}		I/O	**Input/Output function Port 0** P0 is an 8-bit open-drain bi-directional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. To avoid any parasitic current consumption, Floating P0 inputs must be pulled to V_{CC} or V_{SS}.
					I/O	**Address/Data low** Mutiplexed Address/Data LSB for external access
P2[7:0]	A[15:8]		V_{CC}		I/O	**Input/Output function Port 2** P2 is an 8-bit open-drain bi-directional I/O port with internal pull-ups
					O	**Address high** Address Bus MSB for external access
P3.6	WR		DV_{CC}		O	**Write signal** Write signal asserted during external data memory write operation
P3.7	RD		DV_{CC}		I	**Read signal** Read signal asserted during external data memory read operation
ALE			V_{CC}		O	**Address latch enable output** The falling edge of ALE strobes the address into external latch
PSEN	PSEN		V_{CC}		O	**Program strobe enable**
EA	EA		V_{CC}		I	**External access enable** This pin must be held low to force the device to fetch code from external program memory starting at address 0000h. It is latched during reset and cannot be dynamically changed during operation.

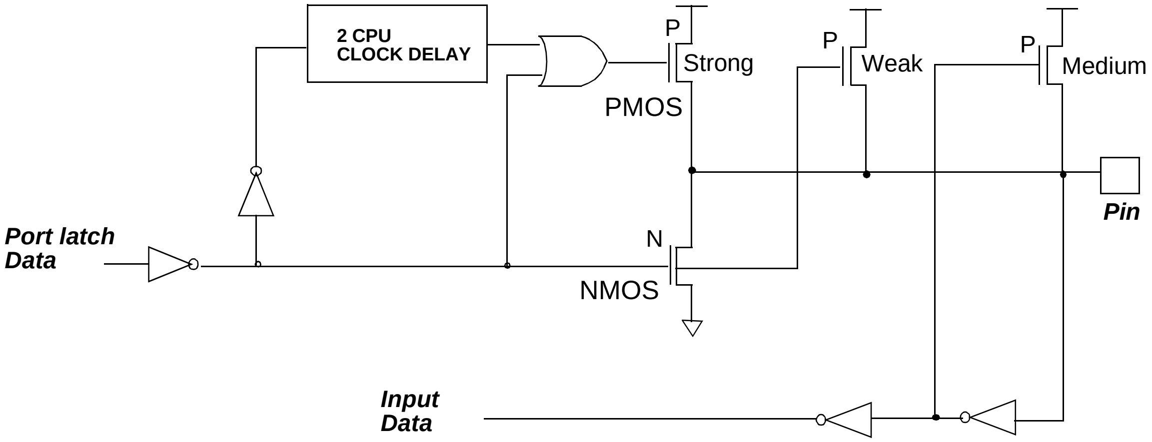
Port Structure Description

The different ports structures are described as follows.

Quasi Bi-directional Output Configuration

The default port output configuration for standard I/O ports is the quasi bi-directional output that is common on the 80C51 and most of its derivatives. This output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic high, it is weakly driven, allowing an external device to pull the pin low. When the port outputs a logic low state, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open drain output except that there are three pull-up transistors in the quasi bi-directional output that serve different purposes. One of these pull-ups, called the weak pull-up, is turned on whenever the port latch for the pin contains a logic 1. The weak pull-up sources a very small current that will pull the pin high if it is left floating. A second pull-up, called the medium pull-up, is turned on when the port latch for the pin contains a logic 1 and the pin itself is also at a logic 1 level. This pull-up provides the primary source current for a quasi bi-directional pin that is outputting a 1. If a pin that has a logic 1 on it is pulled low by an external device, the medium pull-up turns off, and only the weak pull-up remains on. In order to pull the pin low under these conditions, the external device has to sink enough current to overpower the medium pull-up and take the voltage on the port pin below its input threshold.

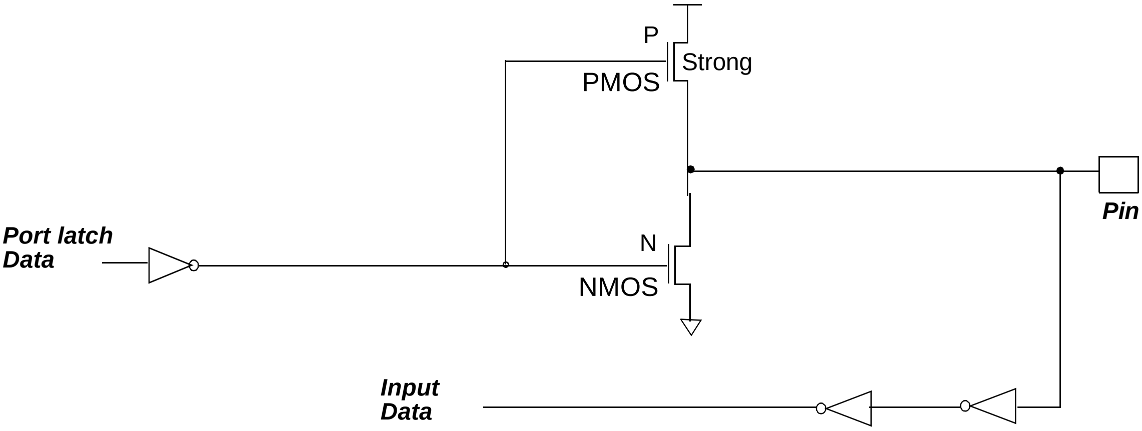
Figure 4. Quasi Bi-directional Output Configuration



Push-pull Output Configuration

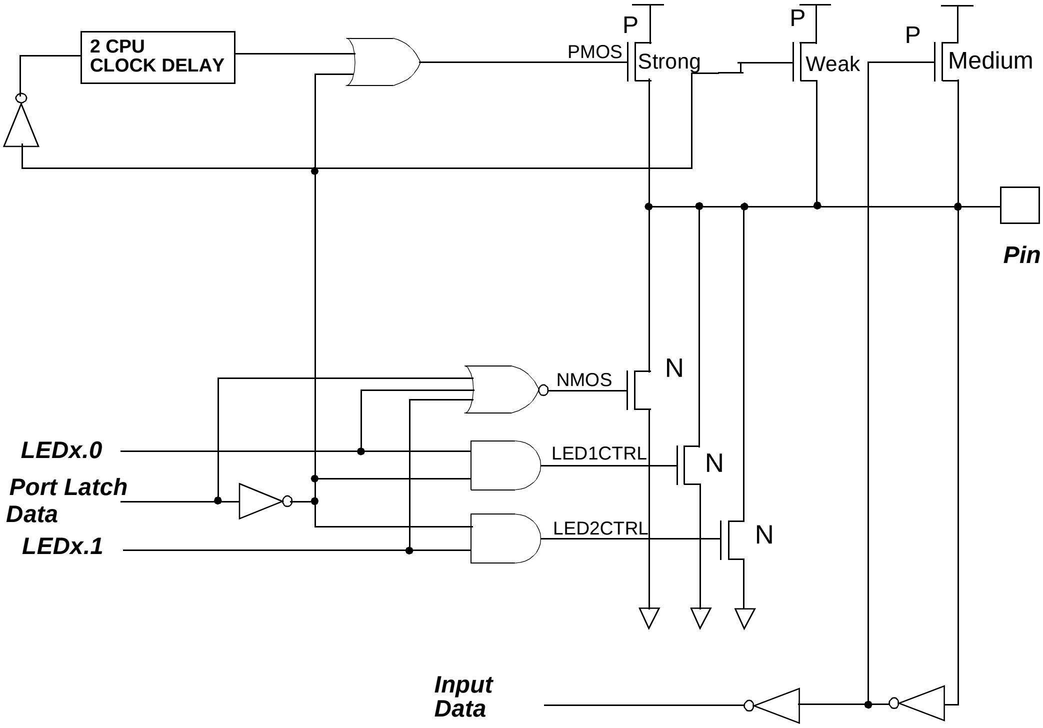
The Push-pull output configuration has the same pull-down structure as the quasi bi-directional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The Push-pull mode may be used when more source current is needed from a port output. The Push-pull port configuration is shown in Figure 5.

Figure 5. Push-pull Output Configuration



LED Output Configuration The input only configuration is shown in Figure 6.

Figure 6. LED Source Current Configuration



Note: The port can be configured in quasi bi-directional mode and the level of current can be programmed by means of LEDCON0 and LEDCON1 registers before switching the led on by writing a logical 0 in Port latch.

SFR Mapping

The Special Function Registers (SFR) of the T8xC5121 belongs to the following categories:

- C51 core registers: ACC, B, DPH, DPL, PSW, SP
- I/O port registers: P0, P1, P2, P3
- Timer 0 registers: TCON, TH0, TH1, TMOD, TL0, TL1
- Serial I/O port registers: SADDR, SADEN, SBUF, SCON, BRL, BDRCON
- Power and clock control registers: PCON, CKRL, CKCON0, CKCON1, DCCKPS
- Interrupt system registers: IE0, IPL0, IPH0, IE1,IPL1, IPH1, ISEL
- Watchdog Timer 0: WDTRST, WDTPRG
- Others: AUXR, AUXR1, RCON
- Smart Card Interface: SCSR, SCCON/SCETU0, SCISR/SCETU1, SCIER/SCIIR, SCTBUF/SCRBUF, SCGT0/SCWT0, SCGT1/SCWT1, SCICR/SCWT2
- Port configuration: SIOCON, LEDCON

Table 2. SFR Addresses and Reset Values

	0/8	1/9		2/A	3/B		4/C		5/D		6/E	7/F	
F8h	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	FFh
F0h	B 0000 0000	LEDCON XXXX 0000	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	F7h
E8h	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	EFh
E0h	ACC 0000 0000	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	E7h
D8h	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	DFh
D0h	PSW 0000 0000	RCON XXXX OXXX	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	D7h
C8h	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	CFh
C0h	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	C7h
B8h	IPL0 XXX0 0000	SADEN 0000 0000		ISEL 0000 0100	▨	▨	▨	▨	▨	▨	▨	DCCKPS XXXX XX11	BFh
B0h	P3 1111 1111	IE1 XXXX 0XXX		IPL1 XXXX 0XXX	IPH1 XXXX 0XXX	0	SCWT0 * 1000 0000	0	SCWT1 * 0010 0101	0	SCWT2 * 0000 0000	IPH0 XXX0 0000	B7h
						1	SCGT0 * 0000 1100	1	SCGT1* 0000 0000	1	SCICR * 0000 0000		
A8h	IE0 0XX0 0000	SADDR 0000 0000	0	SCTBUF* 0000 0000	SCSR XXX0 1000	0	SCCON * 0X000	0	SCISR* 10X0 0000	0	SCIIR* 0X00 0000	CKCON1 XXXX 0XXX	AFh
			1	SCRBUF 0000 000		1	SCETU0 0111 0100	1	SCETU1 0XXX	1	SCIER * 0X00 0000		
A0h	P2 1111 1111	▨		AUXR1 XXX XXX0	▨	▨	▨	▨	▨	▨	WDTRST XXXX XXXX	WDTPRG XXXX X0000	A7h
98h	SCON XXX0 0000	SBUF XXXX XXXX		BRL 0000 0000	BDRCON XXX0 0000	▨	▨	▨	▨	▨	▨	▨	9Fh
90h	P1 XX11 1111	SIOCON 00XX 0000	▨	▨	▨	▨	▨	▨	▨	▨	▨	CKRL XXXX 111X	97h
88h	TCON 0000 0000	TMOD 0000 0000		TL0 0000 0000	TL1 0000 0000		TH0 0000 0000		TH1 0000 0000		AUXR 00XX XX00	CKCON0 X0X0 X000	8Fh
80h	P0 1111 1111	SP 0000 0111		DPL 0000 0000	DPH 0000 0000	▨	20	▨	▨	▨	▨	PCON 00XX XX00	87h
	0/8	1/9		2/A	3/B		4/C		5/D		6/E	7/F	

Reserved ▨

SCRS Bit (SCSR.0)	(*)
0	SFR value
1	SFR value

PowerMonitor

The PowerMonitor function supervises the evolution of the voltages feeding the microcontroller, and if needed, suspends its activity when the detected value is out of specification.

It is guaranteed to start up properly when T8xC5121 is powered up and prevents code execution errors when the power supply becomes lower than the functional threshold.

This section describes the functions of the PowerMonitor.

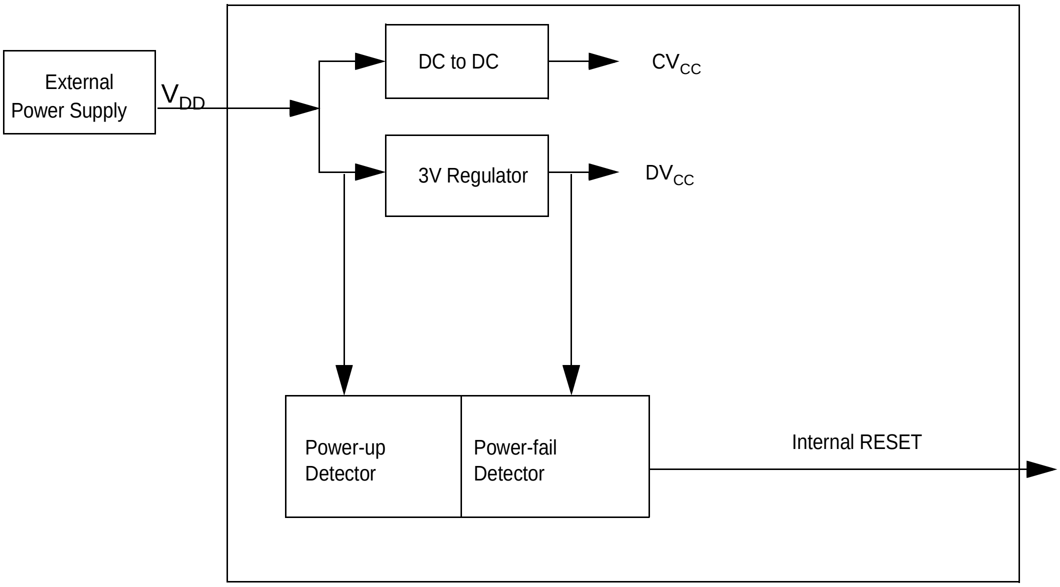
Description

In order to start up and to properly maintain the microcontroller operation, V_{DD} has to be stabilized in the V_{DD} operating range and the oscillator has to be stabilised with a nominal amplitude compatible with logic threshold.

This control is carried out during three phases which are the power-up, normal operation and stop. It complies with the following requirements:

- It guarantees an operational Reset when the microcontroller is powered
- and a protection if the power supply goes out from the functional range of the microcontroller.

Figure 7. PowerMonitor Block Diagram



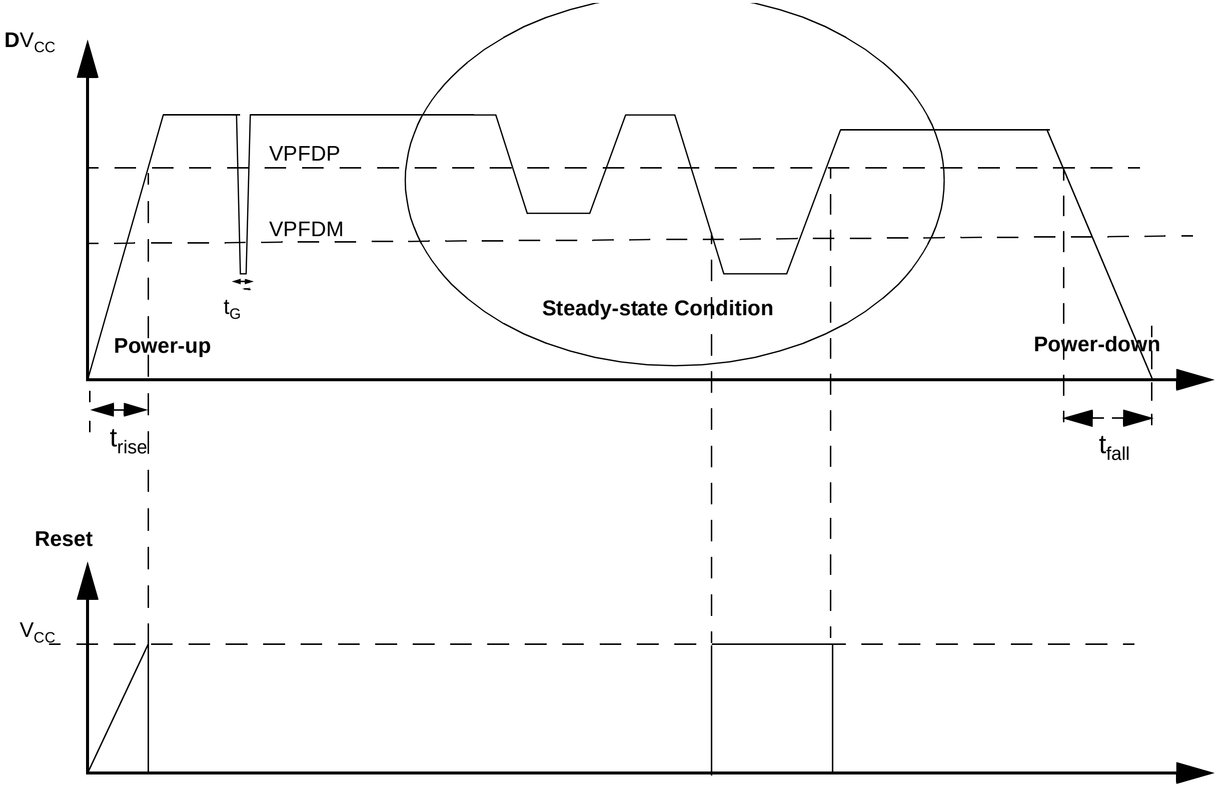
PowerMonitor Diagram

The target of the PowerMonitor is to survey the power supply in order to detect any voltage drops which are not in the target specification. This PowerMonitor block checks two kind of situations that occur:

- During the power-up condition, when V_{DD} is reaching the product specification
- During a steady-state condition, when V_{DD} is stable but disturbed by any undesirable voltage drops.

Figure 8 shows some configurations that can be met by the PowerMonitor.

Figure 8. Power-Up and Steady-state Conditions Monitored



Such device when it is integrated in a microcontroller, forces the CPU in reset mode when V_{DD} reaches a voltage condition which is out of the specification.

The thresholds and their functions are:

- V_{PFDP}: the output voltage of the regulator has reached a minimum functional value at the power-up. The circuit leaves the RESET mode.
- V_{PFDM}: the output voltage of the regulator has reached a low threshold functional value for the microcontroller. An internal RESET is set.

Glitch filtering prevents the system from RESET when short duration glitches are carried on V_{DD} power supply.

The electrical parameters V_{PFDP}, V_{PFDM}, t_{rise}, t_{fall}, t_G are specified in the DCparameters section.

Power Monitoring and Clock Management

Introduction

For applications where power consumption is a critical factor, three power modes are provided:

- Idle mode
- Power-down mode
- Clock Management (X2 feature and Clock Prescaler)
- 3V Regulator Modes (pulsed or not pulsed)

Idle Mode

An instruction that sets PCON.0 causes the last instruction to be executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer 0, and Serial Port functions. The CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels.

There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bit GF0 can be used to give an indication if an interrupt occurred during normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

Power-down Mode

Entering Power-down Mode

To save maximum power, a Power-down mode can be invoked by software (refer to Table 3, PCON register).

In Power-down mode, the oscillator is stopped and the instruction that invoked Power-down mode is the last instruction executed. The internal RAM and SFRs retain their value until the Power-down mode is terminated. V_{CC} can be lowered to save further power. Either a hardware reset or an external interrupt can cause an exit from Power-down. To properly terminate Power-down, the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.

Only external interrupts $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ are useful to exit from Power-down. For that, interrupt must be enabled and configured as level or edge sensitive interrupt input.

Holding the pin low restarts the oscillator but bringing the pin high completes the exit as detailed in Figure 9. When both interrupts are enabled, the oscillator restarts as soon as one of the two inputs is held low and Power-Down exit will be completed when the first input will be released. In this case the higher priority interrupt service routine is executed.

Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put it into Power-down mode.

Exit from Power-down Mode

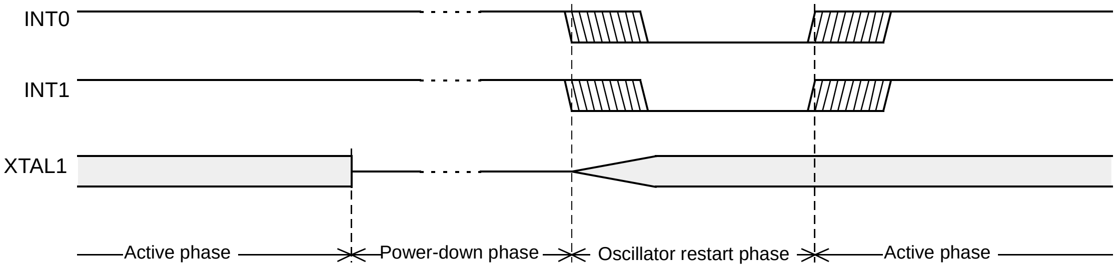
Exiting from Power-down by external interrupt does not affect the SFRs and the internal RAM content.

The ports status under Power-down is the status which was valid before entering this mode.

The INT1 interrupt is a multiplexed input (see Interrupt paragraph) with CPRES (Card detection) and Rxd (UART Rx). So these three inputs can be used to exit from Power-down mode. The configurations which must be set are detailed below:

- Rxd input:
  - RXEN (ISEL.0) must be set
  - EX1 (IE0.2) must be set
  - A low level detected during more than 100 microseconds exit from Power-down
- CPRES input:
  - PRSEN (ISEL.1) must be set
  - EX1 (IEO.2) must be set
  - EA (IE0.7) must be set
  - In the INT1 interrupt vector, the CPLEV Bit (ISEL.7) must be inverted and PRESIT Bit (ISEL.5) must be reset.

Figure 9. Power-down Exit Waveform



Exiting from Power-down by reset redefines all the SFRs, exiting from Power-down by external interrupt does no affect the SFRs.

Exiting from Power-down by either reset or external interrupt does not affect the internal RAM content.

Note: If idle mode is activated with Power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.

SCI Control

Prior to entering Power-down mode, a de-activation of the Smart Card system must be performed.

LED Control

Prior to entering Power-down mode, if the LED mode output is used, the medium pull-up must be disconnected by setting the LEDPD bit in the PCON Register (PCON 3).

Low Power Mode

Only in Power-down mode, in order to reduce the power consumption, the user can choose to select this low-power mode.

The activation reference is the following.

- First select the Low-power mode by setting the LP bit in the AUXR Register (AUXR. 6)
- The activation of Power-down can then be done.

Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated.

Only in case of PLCC52 version, in order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0 (See Table 4). As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

Power Modes Control Registers

Table 3. PCON Register

PCON (S:87h)
Power Configuration Register

7	6	5	4	3	2	1	0
SMOD1	**SMOD0**	**-**	**-**	**LEDPD**	**GF0**	**PD**	**IDL**

Bit Number	Bit Mnemonic	Description
7	SMOD1	**Double Baud Rate bit** Set to double the Baud Rate when Timer 1 is used and mode 1, 2 or 3 is selected in SCON register.
6	SMOD0	**SCON Select bit** When cleared, read/write accesses to SCON.7 are to SM0 bit and read/write accesses to SCON.6 are to SM1 bit. When set, read/write accesses to SCON.7 are to FE bit and read/write accesses to SCON.6 are to OVR bit. SCON is Serial Port Control register.
5		**Reserved**
4		**Reserved**
3	LEDPD	**LED Control Power-Down Mode bits** When cleaned the I/O pull-up is the standard C51 pull-up control. When set the medium pull-up is disconnected.
2	GF0	**General-purpose flag 0** One use is to indicate wether an interrupt occurred during normal operation or during Idle mode.
1	PD	**Power-down Mode bit** Cleared by hardware when an interrupt or reset occurs. Set to activate the Power-down mode. If IDL and PD are both set, PD takes precedence.
0	IDL	**Idle Mode bit** Cleared by hardware when an interrupt or reset occurs. Set to activate the Idle mode. If IDL and PD are both set, PD takes precedence.

Reset Value = X0XX XX00b

Table 4. AUXR Register

AUXR (S:8Eh)
Auxiliary Register

7	6	5	4	3	2	1	0
-	LP	-	-	-	-	EXTRAM	AO

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	LP	**Low Power mode selection** Clear to select standard mode Set to select low consumption mode
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	EXTRAM	**EXTRAM select** **(ONLY for PLCC52 version)** Clear to map XRAM datas in internal XRAM memory. Set to map XRAM datas in external XRAM memory.
0	AO	**ALE Output bit** **(ONLY for PLCC52 version)** Clear to restore ALE operation during internal fetches. Set to disable ALE operation during internal fetches.

Reset Value = 00XX XX00b

Table 5. IE0 Register

IE0
Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	-	-	ES	ET1	EX1	ET0	EX0

Bit Number	Bit Mnemonic	Description
7	EA	**Enable All interrupt bit** Clear to disable all interrupts. Set to enable all interrupts. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its interrupt enable bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	ES	**Serial port Enable bit** Clear to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	**Timer 1 overflow interrupt Enable bit** Clear to disable Timer 1 overflow interrupt. Set to enable Timer 1 overflow interrupt.
2	EX1	**External interrupt 1 Enable bit** Clear to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	**Timer 0 overflow interrupt Enable bit** Clear to disable Timer 0 overflow interrupt. Set to enable Timer 0 overflow interrupt.
0	EX0	**External interrupt 0 Enable bit** Clear to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0XX0 0000b

Table 6. ISEL Register

ISEL (S:BAh)
Interrupt Enable Register

7	6	5	4	3	2	1	0
CPLEV	-	RXIT	PRESIT	OELEV	OEEN	RXEN	PRESEN

Bit Number	Bit Mnemonic	Description
7	CPLEV	**Card presence detection level** This bit indicates which CPRES level will bring about an interrupt Set this bit to indicate that Card Presence IT will appear if CPRES is at high level. Clear this bit to indicate that Card Presence IT will appear if CPRES is at low level.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	PRESIT	**Card presence detection interrupt flag** Set by hardware Must be cleared by software
4	RXIT	**Received data interrupt flag** Set by hardware Must be cleared by software
3	OELEV	**OE/INT1 signal active level** Set this bit to indicate that high level is active. Clear this bit to indicate that low level is active.
2	OEEN	**OE/INT1 interrupt disable bit** Clear to disable INT1 interrupt Set to enable INT1 interrupt
1	PRESEN	**Card presence detection interrupt enable bit** Clear to disable the card presence detection interrupt coming from SCIB. Set to enable the card presence detection interrupt coming from SCIB.
0	RXEN	**Received data Interrupt enable bit** Clear to disable the RxD interrupt. Set to enable the RxD interrupt

Reset Value = 0X00 0000b

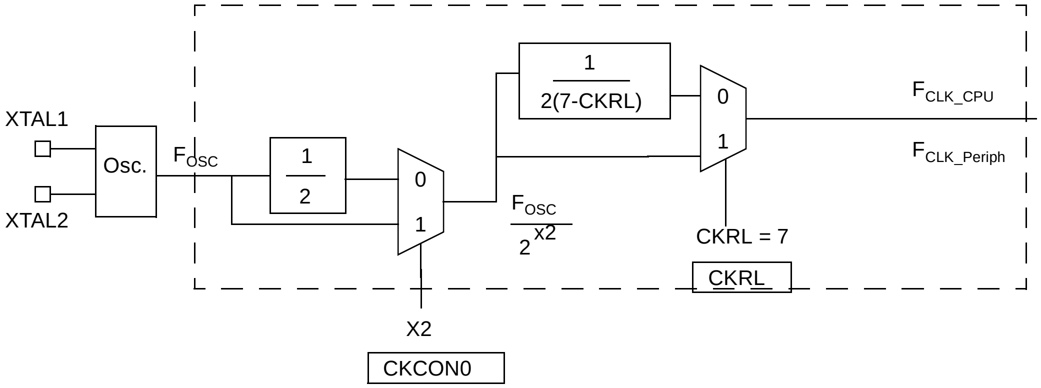
Clock Management

Overview

In order to optimize the power consumption and the execution time needed for a specific task, an internal prescaler feature and a X2 feature have been implemented between the oscillator and the CPU.

Functional Block Diagram

Figure 10. Clock Generation Diagram



If CKRL<>7 then:

$$F_{CLK-CPU} = \frac{F_{OSC}}{2^{(x2)}} x \frac{1}{2(7-CKRL)}$$

If CKRL = 7 then:

$$F_{CLK-CPU} = \frac{F_{osc}}{2^{x2}}$$

CKRL	Prescalor Factor
7	1
6	2
5	4
4	6
3	8
2	10
1	12
0	14

X2 Feature

The T8xC5121 core needs only 6 clock periods per machine cycle. This feature called ”X2” provides the following advantages:

- Divides frequency crystals by 2 (cheaper crystals) while keeping same CPU power.
- Saves power consumption while keeping same CPU power (oscillator power saving).
- Saves power consumption by dynamically dividing the operating frequency by 2 in operating and idle modes.
- Increases CPU power by 2 while keeping same crystal frequency.

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

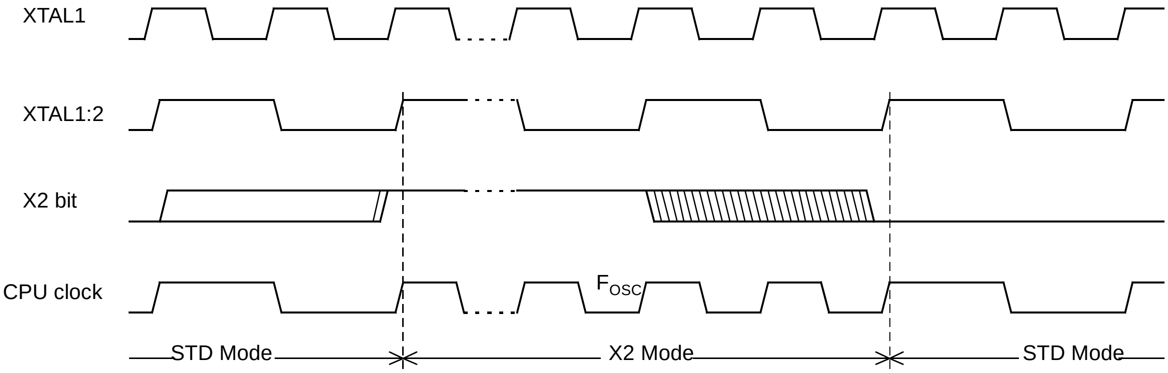
Description

The clock for the whole circuit and peripherals is first divided by two before being used by the CPU core and the peripherals.

This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio from 40 to 60%.

As shown in Figure 10, X2 bit is validated on the rising edge of the XTAL1÷2 to avoid glitches when switching from X2 to standard mode. Figure 11 shows the switching mode waveforms.

Figure 11. Mode Switching Waveforms



The X2 bit in the CKCON0 register (see Table 9) allows to switch from 12 clock periods per instruction to 6 clock periods and vice versa.

The T0X2, T1X2, UartX2, and WdX2 bits in the CKCON0 register (see Table 9) and SCX2 bit in the CKCON1 register (see Table 10) allow to switch from standard peripheral speed (12 clock periods per peripheral clock cycle) to fast peripheral speed (6 clock periods per peripheral clock cycle). These bits are active only in X2 mode.

More information about the X2 mode can be found in the application note "How to Take Advantage of the X2 Features in TS80C51 Microcontroller?".

Clock Prescaler

Before supplying the CPU and the peripherals, the main clock is divided by a factor 2 to 30 to reduce the CPU power consumption. This factor is controlled with the CKRL register.

Table 7. Examples of Factors

XTAL (MHz)	X2 CPU CKCON0	CKRL Value	Prescaler Factor	F_{CLK_CPU}, F_{CLK_Periph} (MHz)
16	0 (reset mode)	07h	1	8
16	1 (X2 mode)	07h	1	16
16	1	07h	1	16
16	0	07h	1	8
16	0	06h	2	4
16	1	06h	2	8

Clock Control Registers

Clock Prescaler Register

This register is used to reload the clock prescaler of the CPU and peripheral clock.

Table 8. CKRL Register

CKRL - Clock Reload Register (97h)

7	6	5	4	3	2	1	0
-	-	-	-	CKRL	CKRL	CKRL	-

Bit Number	Bit Mnemonic	Description
7 - 4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3 - 1	CKRL	**Clock Reload Register** Prescaler value XXXX 000Xb: Division factor equals 14 XXXX 110Xb: division factor equals 2 XXXX 111Xb: division factor equals 1
0	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.

Reset Value = XXXX 111Xb

Table 9. CKCON0 Register

CKCON0 - Clock Control Register (8Fh)

7	6	5	4	3	2	1	0
-	WDX2	-	SIX2	-	T1X2	T0X2	X2

Bit Number	Bit Mnemonic	Description
7	-	**Reserved**
6	WDX2	**Watchdog clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect) Cleared to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
5	-	**Reserved**
4	SIX2	**Enhanced UART clock (Mode 0 and 2)** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect) Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
3	-	**Reserved**
2	T1X2	**Timer 1 clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect) Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle
1	T0X2	**Timer 0 clock** (This control bit is validated when the CPU clock X2 is set; when X2 is low, this bit has no effect) Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle
0	X2	**CPU clock** Clear to select 12 clock periods per machine cycle (Standard mode) for CPU and all the peripherals. Set to select 6 clock periods per machine cycle (X2 mode) and to enable the individual peripherals "X2" bits.

Reset Value = X0X0 X000b

Table 10. CKCON1 Register

CKCON1 - Clock Control Register (AFh)

7	6	5	4	3	2	1	0
-	-	-	-	SCX2	-	-	-

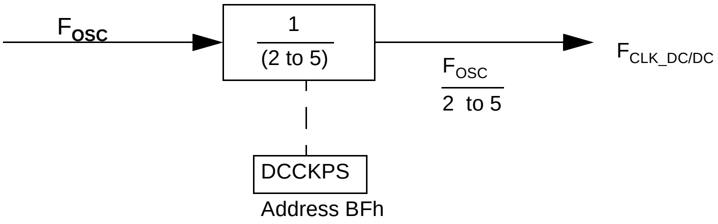
Bit Number	Bit Mnemonic	Description
7	-	**Reserved**
6	-	**Reserved**
5	-	**Reserved**
4	-	**Reserved**
3	SCX2	**SCIB clock** Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
2	-	**Reserved**
1	-	**Reserved**
0	-	**Reserved**

Reset Value = XXXX 0XXXb

DC/DC Clock

The DC/DC block needs a clock with a 50% duty cycle. The frequency must also respect a value between 3.68 MHz and 4 MHz. The first requirement imposes a divider in the clock path and the second constraint is solved with the use of a prescaler.

Figure 12. Functional Block Diagram



Clock Control Register

This register is used to reload the clock prescaler of the DC/DC converter clock.

Table 11. DCCKPS Register

DCCKPS - DC/DC converter Reload Register (BFh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	DCCKPS	DCCKPS

Bit Number	Bit Mnemonic	Description
7:2	-	**Reserved** Do not use write those bits
1:0	DCCKPS	**Clock Reload Register** Prescaler value 00b: Division factor equals 2 01b: division factor equals 3 10b: division factor equals 4 11b: division factor equals 5 (reset value which minimize the consumption)

Reset Value = XXXX XX11b

Clock Prescaler

Before supplying the DC/DC block, the oscillator clock is divided by a factor 2 to 5 to adapt the clock needed by the DC/DC converter. This factor is controlled with the DCCKPS register.

The prescaler factor must be chosen to match the requirement range which is 4MHz.

Table 12. Examples of Factors

XTAL (MHz)	DCCKPS Value	Prescaler Factor	DC/DC Converter CLK (MHz)
8	00h	2	4
12	01h	3	4
14.756	02h	4	3.689
16	02h	4	4
20	03h	5	4

Smart Card Interface Block (SCIB)

Introduction

The SCIB provides all signals to directly interface a smart card. Compliance with the ISO7816, EMV'2000, GSM and WHQL standards has been certified.

Both synchronous (e.g. memory card) and asynchronous smart cards (e.g. microprocessor card) are supported. The component supplies the different voltages requested by the smart card. The power-off sequence is directly managed by the SCIB.

The card presence switch of the smart card connector is used to detect card insertion or card removal. In case of card removal, the SCIB de-activates the smart card using the de-activation sequence. An interrupt can be generated when a card is inserted or removed.

Any malfunction is reported to the microcontroller (interrupt + control register).

The different operating modes are configured by internal registers.

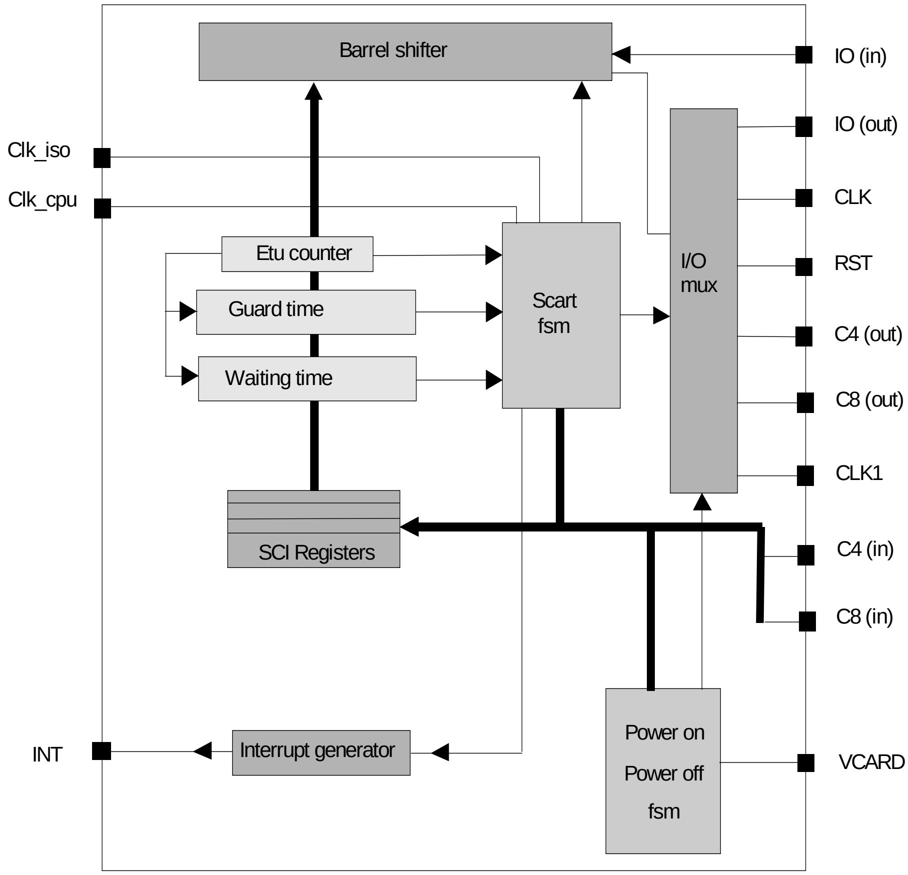
Main Features

- Support of ISO/IEC7816
- Character mode
- 1 transmit buffer + 1 receive buffer
- 11 bits ETU counter
- 9 bits guard time counter
- 24 bits waiting time counter
- Auto-character repetition on error signal detection in transmit mode
- Auto-error signal generation on parity error detection in receive mode
- Power-on and power-off sequence generation
- Manual mode to directly drive the card I/O

Block Diagram

The Smart Card Interface Block diagram is shown in Figure 13.

Figure 13. SCIB Block Diagram



Functional Description

The architecture of the Smart Card Interface Block is detailed below.

Barrel Shifter

It allows the translation between 1 bit serial data and 8 bits parallel data.

The barrel function is useful for character repetition since the character is still present in the shifter at the end of the character transmission.

This shifter is able to shift the data in both directions and to invert the input or output value in order to manage both direct and inverse ISO7816-3 convention.

Coupled with the barrel shifter there is a parity checker and generator.

There are 2 registers connected to this barrel shifter, one for the transmission and one for the reception.

They act as buffers to relieve the CPU of timing constraints.

SCART FSM

(Smart Card Asynchronous Receiver Transmitter Finite State Machine)

This is the core of the design. Its purpose is to control the barrel shifter. To sequence correctly the barrel shifter for a reception or a transmission, it uses the signals issued by the different counters. One of the most important counters is the guard time counter that gives time slots corresponding to the character frame.

It is enabled only in UART mode.

The transition from the receipt mode to the transmit mode is done automatically. Priority is given to the transmission.

ETU Counter

The ETU (Elementary Timing Unit) counter controls the working frequency of the barrel shifter, in fact, it generates the enable signal of the barrel shifter.

It is 11 bits wide and there is a special compensation mode activated with the most significant bit that allows non integer ETU value with a working clock equal to the card clock .

But the decimal value is limited to a half clock cycle. In fact the bit duration is not fixed. It takes turns in n clock cycles and n-1 clock cycles. The character duration (10 bits) is also equal to 10*(n+1/2) clock cycles.

This allows to reach the required precision of the character duration specified by the ISO7816 standard.

example: F = 372 D = 32 = > ETU = 11.625 clock cycles.

ETU = (ETU[10-0] -0.5 * COMP)*f with ETU[10-0] = 12, COMP = 1 (bit 7 of SCETU1)

To achieve this clock rate we activated the compensation mode and we programmed the ETU duration to 12 clock cycles.

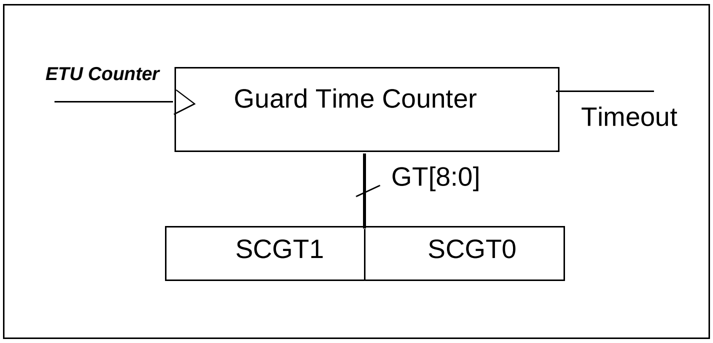
The result will be a full character duration (10 bits) equal to 11.5 clock cycles.

Guard Time Counter

The minimum time between the leading edge of the start bit of a character and the leading edge of the start bit of the following character transmitted (Guard time) is controlled by one counter.

It is 9 bits wide and is incremented at the ETU rate.

Figure 14. Guard Time Counter

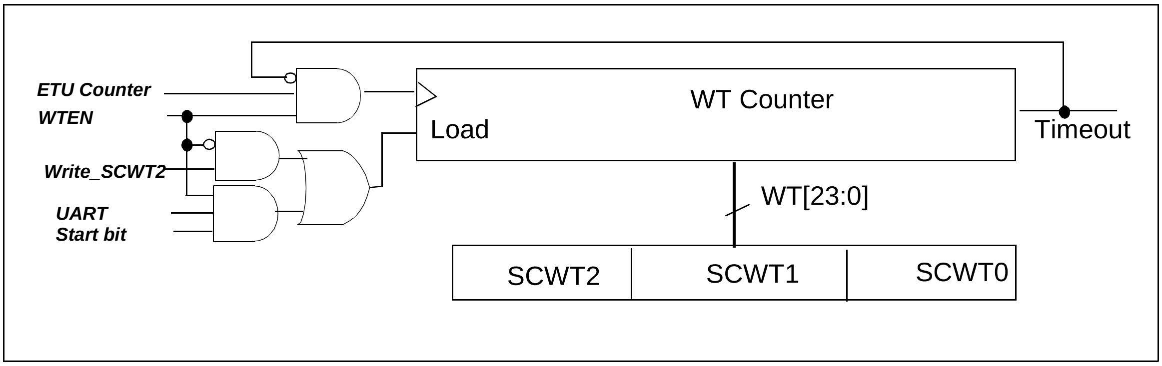


Waiting Time Counter (WT)

The WT counter is a 24 bits down counter which can be loaded with the value contained in the SCWT2, SCWT1, SCWT0 registers. Its main purpose is time out signal generation. It is 24 bits wide and is decremented at the ETU rate. The ETU counter acts as a prescaler (See Figure 15).

When the WT counter timeout, an interrupt is generated and the SCIB function is locked: reception and emission are disabled. It can be enabled by resetting the macro or reloading the counter.

Figure 15. Waiting Time Counter



The counter is loaded, if WTEN = 0, during the write of SCWT2 register.

This counter is available in both UART and manual modes. But the behaviour depends on the selected mode.

In manual mode, the WTEN signal controls the start of the counter (rising edge) and the stop of the counter (falling edge). After a time out of the counter, a falling edge on WTEN, a reload of SCWT2 and a rising edge of WTEN are necessary to start again the counter and to release the SCIB macro. The reload of SCWT2 transfers all SCWT0, SCWT1 and SCWT2 registers to the WT counter.

In UART mode there is an automatic load on the start bit detection. This automatic load is very useful for changing on-the-fly the Timeout value since there is a register to hold the load value. This is the case, for example, when in T = 1 a launch is performed on the BWT Timeout on the start bit of the last transmitted character. But on the receipt of the first character an other time out value (CWT) must be used . For this, the new load value of the waiting time counter must be loaded with CWT before the transmission of the last character. The reload of SCWT[2-0] with the new value occurs with WTEN = 1.

After a time out of the counter in UART mode, the restart is done as in manual mode.

The maximum interval between the start leading edge of a character and the start leading edge of the next character is loaded in the SCWT2, SCWT1, SCWT0 registers.

In T = 1 mode, the CWT (character waiting time) or the BWT (block waiting time) are loaded in the same registers.

The maximum time between two consecutive start bit is WT[23:0] * ETU.

When used to check BWT according to ISO 7816, WT can be set between 971 and 15728651.

Figure 16. T = 0 Mode

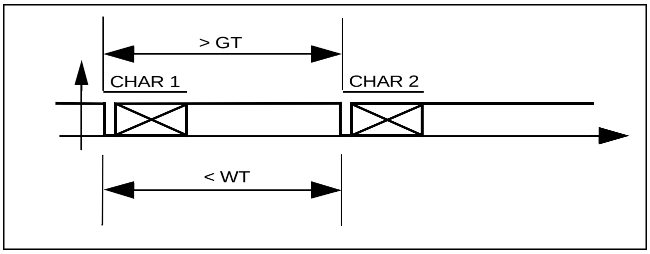
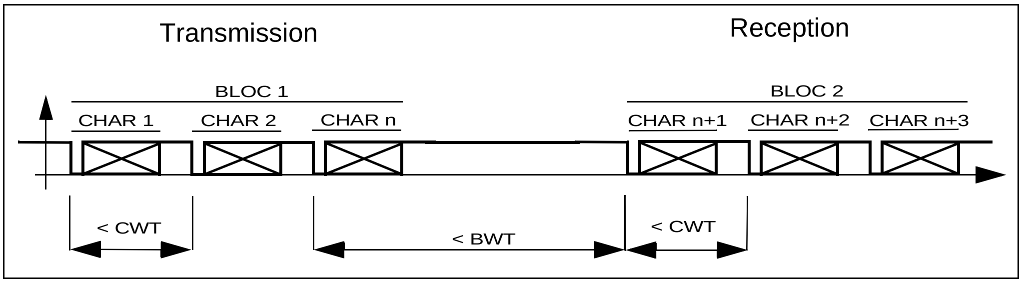


Figure 17. T = 1 Mode



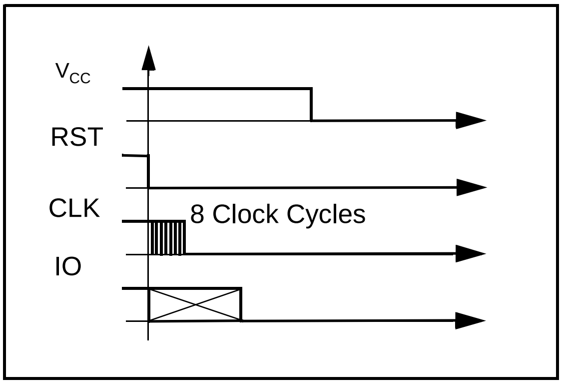
Power-on and Power-off FSM

In this state, the machine applies the signals on the smart card in accordance with ISO7816 standard.

To be able to power-on the SCIB, the card presence is mandatory.

Removal of the smart card will automatically start the power-off sequence as described in Figure 18.

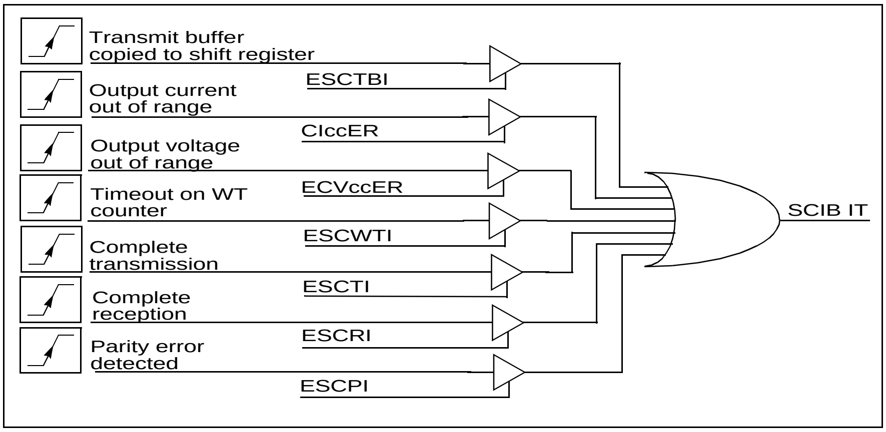
Figure 18. SCI Deactivation Sequence after a Card Extraction



Interrupt Generator

There are several sources of interruption but the SCIB macro-cell issues only one interrupt signal: SCIB IT.

Figure 19. SCIB Interrupt Sources



This signal is high level active. One of the sources is able to set up the interrupt signal and this is the read of the Smart Card Interrupt register by the CPU that clears this signal.

If during the read of the Smart Card Interrupt register an interrupt occurs, the set of the corresponding bit into the Smart Card Interrupt register and the set of the interrupt signal will be delayed after the read access.

Registers

There are fourteen registers to control the SCIB macro-cell. They will be described in the Section “DC/DC Converter”.

Some of the register widths are greater than a byte. Despite the 8 bits access provided by the BIU, the address mapping of this kind of register respects the following rule:

- The Lowest significant byte register is implemented at the higher address.

This implementation makes access to these registers easier when using high level programming language (C,C++).

Other Features

Clock

The Ck-ISO input must be in the range 1 - 5 MHz according to ISO7816.

The ISO Clock diagram and the configuration examples are shown in Figure 20.

Figure 20. Clock Diagram of the SCIB Block

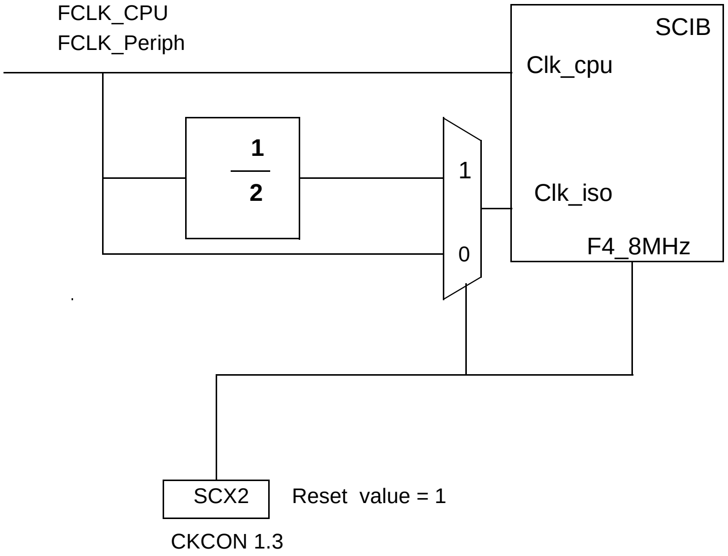


Table 13. Examples of Settings for Clocks

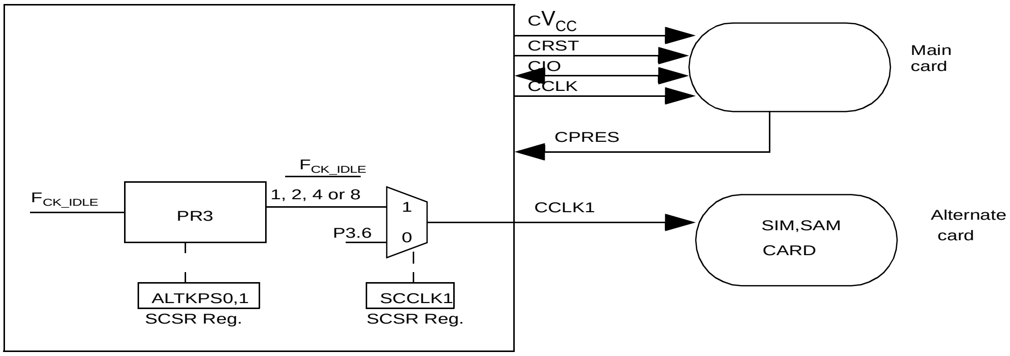
Xtal (MHz)	X2 CKCON0	FCLK Cpu + FCLK Periph (MHz)	SCX2	Clk_ iso (1 to 5 MHz)
4	0	2	0	2
4	1 (mode X2)	4	0	4
8	1	8	1	4
11.059	0	5.5295	1	2.7648
14.7456	0	7.3728	1	3.6864
16	0	8	1	4
20	0	10	1	5

Alternate Card

A second card named "Alternate card" can be controlled.

The Clock signal CCLK1 can be adapted to the XTAL frequency. Thanks to the clock prescaler which can divide the frequency by 1, 2, 4 or 8. The bits ALTKPS0 and ALTKPS1 in SCSR Register are used to set this factor.

Figure 21. Alternate Card



Card Presence Input

The internal pull-up on Card Presence input can be disconnected in order to reduce the consumption (CPRESRES, bit 3 in PMOD0).

In this case, an external resistor (typically 1 MΩ) must be externally tied to V_{CC}.

CPRES input can generate an interrupt (see Interrupt system section).

The detection level can be selected.

SCIB Reset

The SCICR register contains a reset bit. If set, this bit generates a reset of the SCI and its registers. Table 15 shows the SCIB registers that are reseted and their reset values.

Table 14. Reset Values for SCI Registers

Register Name	**SCIB Reset Value (Binary)**
SCICR	0000 0000b
SCCON	0X00 0000b
SCISR	1000 0000b
SCIIR	0X00 0000b
SCIER	0X00 0000b
SCSR	XXX0 1000b
SCTBUF	0000 0000b
SCRBUF	0000 0000b
SCETU1, SCETU0	XXX X001b, 0111 0100b (372)
SCGT1, SCGT0	XXXX XXX0b, 0000 1100b (12)
SCWT2, SCWT1, SCWT0	0000 0000b, 0010 0101b, 1000 0000b (9600)

DC/DC Converter

The Smart Card supply voltage (Cv_{CC}) is generated by the integrated DC/DC converter. It is controlled by several registers:

- The register described in Section “SCICR Register” controls the CVCC voltage with bits CVcc0, CVcc1
- The register described in Section “SCCON Register”, switches ON/OFF the DC/DC converter with bit $CARDV_{CC}$
- After the selection of the card voltage (CVcc[1:0]), the $CARV_{CC}$ bit is used to switch on the DC\DC converter. The CVccOK bit indicates that the card voltage is within the voltage range.
- It is mandatory to switch off the CV_{CC} before entering in power-down mode.

Registers Description

Table 15. SCICR Register

SCICR (S:B6h, SCRS = 1)

Smart Card Interface Control Register

7	6	5	4	3	2	1	0
RESET	**CARDDET**	**CVcc1**	**CVcc0**	**UART**	**WTEN**	**CREP**	**CONV**

Bit Number	Bit Mnemonic	Description
7	RESET	**Reset** Set this bit to reset the SCIB and its configuration
6	CARDDET	**Card presence detector sense** Clear this bit to indicate the card presence detector is opened when no card is inserted (CPRES is high). Set this bit to indicate the card presence detector is closed when no card is inserted (CPRES is low).
5 - 4	CVcc[1:0]	**Card Voltage Selection:** CVcc[1] CVcc[0] CVcc 0 0 0V 0 1 1.8V 1 0 3V 1 1 5V
3	UART	**Card UART selection** Clear this bit to use the Card I/O bit to drive the Card I/O pin. Set this bit to use the Smart Card UART to drive the Card I/O pin. Also controls the Wait Time Counter as described in Section “Waiting Time Counter (WT)”
2	WTEN	**Wait time counter enable** Clear this bit to stop the counter and enable the load of the Wait Time counter hold registers. The hold registers are loaded with SCWT0, SCWT1 and SCWT2 values when SCWT2 is written. Set this bit to start the Wait Time counter. The counters stop when it reaches the timeout value. If the UART bit is set, the Wait Time counter automatically reloads with the hold registers whenever a start bit is sent or received.
1	CREP	**Character repetition** Clear this bit to disable parity error detection and indication on the Card I/O pin in receive mode and to disable character repetition in transmit mode. Set this bit to enable parity error indication on the Card I/O pin in receive mode and to set automatic character repetition when a parity error is indicated in transmit mode. In receive mode, three times error indication is performed and the parity error flag is set after four times parity error detection. In transmit mode, up to three times character repetition is allowed and the parity error flag is set after five times (reset configuration, can be set at 4 using CREPSET bit in SCSR Register) consecutive parity error indication.
0	CONV	**ISO convention** Clear this bit to use the direct convention: b0 bit (LSB) is sent first, the parity bit is added after b7 bit and a low level on the Card I/O pin represents a “0”. Set this bit to use the inverse convention: b7 bit (LSB) is sent first, the parity bit is added after b0 bit and a low level on the Card I/O pin represents a “1”.

Reset Value = 0000 0000b

Table 16. SCCON Register

SCCON (S:ACh, SCRS = 0)
Smart Card Contacts Register

7	6	5	4	3	2	1	0
CLK	-	CARDC8	CARDC4	CARDIO	CARDCLK	CARDRST	CARDVCC

Bit Number	Bit Mnemonic	Description
7	CLK	**Card Clock Selection** Clear this bit to use the CardClk bit (CARDCLK) to drive Card CLK pin. Set this bit to use XTAL signal to drive the Card CLK pin. **Note:** internal synchronization avoids any glitch on the CLK pin when switching this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not change this bit or write 0.
5	CARDC8	**Card C8** Clear this bit to drive a low level on the Card C8 pin. Set this bit to set a high level on the Card C8 pin.
4	CARDC4	**Card C4** Clear this bit to drive a low level on the Card C4 pin. Set this bit to set a high level on the Card C4 pin.
3	CARDIO	**Card I/O** When the UART bit is cleared in SCICR Register, the value of this bit is driven to the Card I/O pin. Then this pin can be used as a pseudo bi-directional I/O when this bit is set. To be used as an input, this bit must contain a 1.
2	CARDCLK	**Card CLK** When the CLK bit is cleared in SCCON Register, the value of this bit is driven to the Card CLK pin.
1	CARDRST	**Card RST** Clear this bit to drive a low level on the Card RST pin. Set this bit to set a high level on the Card RST pin.
0	CARDV$_{CC}$	**Card VCC Control** Clear this bit to desactivate the Card interface and set its power-off. The other bits of SCC register have no effect while this bit is cleared. Set this bit to power-on the Card interface. The activation sequence shall be handled by software.

Reset Value = 0X00 0000b

Table 17. SCISR Register

SCISR (S:ADh, SCRS = 0)
Smart Card UART Interface Status Register

7	6	5	4	3	2	1	0
SCTBE	**CARDIN**	**CIccOVF**	**CVccOK**	**SCWTO**	**SCTC**	**SCRC**	**SCPE**

Bit Number	Bit Mnemonic	Description
7	SCTBE	**SCIB transmit buffer empty** This bit is set by hardware when the Transmit Buffer is copied to the transmit shift register of the Smart Card UART. It is cleared by hardware when SCTBUF is written to.
6	CARDIN	**Card presence status** This bit is set when a card is detected (debouncing filter has to be done in software). It is cleared otherwise.
5	CIccOVF	**ICC overflow on card** This bit is set when the current on card is above the limit It shall be cleared by the hardware .
4	CVccOK	**Card voltage status** This bit is set when the output voltage is within the voltage range specified by CVcc field. It is cleared otherwise.
3	SCWTO	**Smart card wait Timeout** This bit is set by hardware when the Smart card wait time counter times out. It shall be cleared by the reload of the counter or by the reset of the SCIB.
2	SCTC	**Smart card transmitted character** This bit is set by hardware when the Smart Card UART has transmitted a character. It shall be cleared by software after this register has been read.
1	SCRC	**Smart card received character** This bit is set by hardware when the Smart Card UART has received a character It is cleared by hardware when SCBUF is read.
0	SCPE	**Smart card parity error** This bit is set at the same time as SCTI or SCRI if a parity error is detected. It shall be cleared by software after this register has been read.

Reset Value = 1000 0000b

Table 18. SCIIR Register

SCIIR (S:AEh, SCRS = 0)
Smart Card UART Interrupt
Identification Register (read only)

7	6	5	4	3	2	1	0
SCTBI	**-**	**CIccERR**	**CVccERR**	**SCWTI**	**SCTI**	**SCRI**	**SCPI**

Bit Number	Bit Mnemonic	Description
7	SCTBI	**SCIB transmit buffer interrupt** This bit is set by hardware when the Transmit Buffer is copied to the transmit shift register of the Smart Card UART. It is cleared by hardware when this register is read.
6	-	**Reserved** The value read from this bit is indeterminate. Do not change this bit or write 0.
5	CIccERR	**Card current status** This bit is set when the output current goes out of the current range. It is cleared by hardware when this register is read.
4	CVccERR	**Card voltage status** This bit is set when the output voltage goes out of the voltage range specified by CVcc field. It is cleared by hardware when this register is read.
3	SCWTI	**Smart card wait Timeout interrupt** This bit is set by hardware when the Smart Card Timer 0 times out. It is cleared by hardware when this register is read.
2	SCTI	**Smart card transmit interrupt** This bit is set by hardware when the Smart Card UART completes a character transmission. It is cleared by hardware when this register is read.
1	SCRI	**Smart card receive interrupt** This bit is set by hardware when the Smart Card UART completes a character reception. It is cleared by hardware when this register is read.
0	SCPI	**Smart card parity error interrupt** This bit is set at the same time as SCTI or SCRI if a parity error is detected. It is cleared by hardware when this register is read.

Reset Value = 0X00 0000b

Table 19. SCIER Register

SCIER (S:AEh, SCRS = 1)
Smart Card UART Interrupt Enable Register

7	6	5	4	3	2	1	0
ESCTBI	-	CIccER	ECVccER	ESCWTI	ESCTI	ESCRI	ESCPI

Bit Number	Bit Mnemonic	Description
7	ESCTBI	**Smart Card UART Transmit Buffer Empty Interrupt Enable** Clear this bit to disable the Smart Card UART Transmit Buffer Empty interrupt. Set this bit to enable the Smart Card UART Transmit Buffer Empty interrupt.
6	-	**Reserved** The value read from this bit is indeterminate. Do not change this bit .
5	CIccER	**Card Current Error Interrupt Enable** Clear this bit to disable the Card Current Error interrupt. Set this bit to enable the Card Current Error interrupt.
4	ECVccER	**Card Voltage Error Interrupt Enable** Clear this bit to disable the Card Voltage Error interrupt. Set this bit to enable the Card Voltage Error interrupt.
3	ESCWTI	**Smart Card Wait Timeout Interrupt Enable** Clear this bit to disable the Smart Card Wait timeout interrupt. Set this bit to enable the Smart Card Wait timeout interrupt.
2	ESCTI	**Smart Card Transmit Interrupt Enable** Clear this bit to disable the Smart Card UART Transmit interrupt. Set this bit to enable the Smart Card UART Transmit interrupt.
1	ESCRI	**Smart Card Receive Interrupt Enable** Clear this bit to disable the Smart Card UART Receive interrupt. Set this bit to enable the Smart Card UART Receive interrupt.
0	ESCPI	**Smart Card Parity Error Interrupt Enable** Clear this bit to disable the Smart Card UART Parity Error interrupt. Set this bit to enable the Smart Card UART Parity Error interrupt.

Reset Value = 0X00 0000b

Table 20. SCSR Register

SCSR (S:ABh) Smart Card Selection Register

7	6	5	4	3	2	1	0
-	-	-	CREPSEL	ALTKPS1	ALTKPS0	SCCLK1	SCRS

Bit Number	Bit Mnemonic	Description
7	-	**Reserved**
6	-	**Reserved**
5	-	**Reserved**
4	CREPSEL	**Character repetition selection** Clear this bit to select 5 times repetition before parity error indication Set this bit to select 4 times repetition before parity error indication
3-2	ALTKPS1 ALTKPS0	**Alternate Card Clock prescaler factor** 00ALTKPS = 0: prescaler factor equals 1 01 ALTKPS = 1: prescaler factor equals 2 10ALTKPS = 2: prescaler factor equals 4 (reset value) 11ALTKPS = 3: prescaler factor equals 8
1	SCCLK1	**Alternate card clock selection** Set to select the prescaled clock (CCLK1) Clear to select the standard port configuration (P3.6)
0	SCRS	**Smart card register selection** The SCRS bit selects which set of the SCIB registers is accessed.

Reset Value = XXX0 1000b

Table 21. SCTBUF Register

SCTBUF (S:AA, write-only, SCRS = 0) Smart Card Transmit Buffer Register

7	6	5	4	3	2	1	0

Bit Number	Bit Mnemonic	Description
–	–	Can store a new byte to be transmitted on the I/O pin when SCTBE is set. Bit ordering on the I/O pin depends on the Convention (see SCICR Register).

Reset Value = 0000 0000b

Table 22. SCRBUF Register

SCRBUF (S:AA read-only, SCRS = 1)
Smart Card Receive Buffer Register

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	–

Bit Number	Bit Mnemonic	Description
–	–	**Provides the byte received from the I/O pin when SCRI is set.** Bit ordering on the I/O pin depends on the Convention (see SCICR Register).

Reset Value = 0000 0000b

Table 23. SCETU1 Register

SCETU1 (S:ADh, SCRS = 1)
Smart Card ETU Register 1

7	6	5	4	3	2	1	0
COMP	–	–	–	–	**ETU10**	**ETU9**	**ETU8**

Bit Number	Bit Mnemonic	Description
7	COMP	**Compensation** Clear this bit when no time compensation is needed (i.e. when the ETU to Card CLK period ratio is close to an integer with an error less than 1/4 of Card CLK period). Set this bit otherwise and reduce the ETU period by 1 Card CLK cycle for even bits.
6-3	–	**Reserved** The value read from these bits is indeterminate. Do not change these bits .
2-0	ETU[10:8]	**ETU MSB** Used together with the ETU LSB (see SCETU0 Register).

Reset Value = 0XXX X001b

Table 24. SCETU0 Register

SCETU0 (S:ACh, SCRS = 1)
Smart Card ETU Register 0

7	6	5	4	3	2	1	0
ETU7	**ETU6**	**ETU5**	**ETU4**	**ETU3**	**ETU2**	**ETU1**	**ETU0**

Bit Number	Bit Mnemonic	Description
7-0	ETU[7:0]	**ETU LSB** The Elementary Time Unit is (ETU[10:0] - 0.5*COMP)/f, where f is the Card CLK frequency. According to ISO7816, ETU[10:0] can be set between 11 and 2047. The default reset value of ETU[10:0] is 372 (F = 372, D = 1).

Reset Value = 0111 0100b

Table 25. SCGT1 Register

SCGT1 (S:B5h, SCRS = 1)
Smart Card Transmit Guard Time Register 1

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	**GT8**

Bit Number	Bit Mnemonic	Description
7-1	–	**Reserved** The value read from these bits is indeterminate. Do not change these bits .
0	GT8	**Transmit Guard Time MSB** Used together with the Transmit Guard Time LSB (see SCGT0 Register).

Reset Value = XXXX XXX0b

Table 26. SCGT0 Register

SCGT0 (S:B4h, SCRS = 1)
Smart Card Transmit Guard Time Register 0

7	6	5	4	3	2	1	0
GT7	**GT6**	**GT5**	**GT4**	**GT3**	**GT2**	**GT1**	**GT0**

Bit Number	Bit Mnemonic	Description
7-0	GT[7:0]	**Transmit Guard Time LSB** The minimum time between two consecutive start bits in transmit mode is GT[8:0] * ETU. According to ISO 7816, GT can be set between 11 and 266 (11 to 254+12 ETU).

Reset Value = 0000 1100b

Table 27. SCWT2 Register

SCWT2 (S:B6h, SCRS = 0)
Smart Card Character/Block Wait Time Register 2

7	6	5	4	3	2	1	0
WT23	WT22	WT21	WT20	WT19	WT18	WT17	WT16

Bit Number	Bit Mnemonic	Description
7-0	WT[23:16]	**Wait Time Byte 2** Used together with WT[15:0] (see SCWT0 Register).

Reset Value = 0000 0000b

Table 28. SCWT1 Register

SCWT1 (S:B5h, SCRS = 0) Smart Card Character/Block Wait Time Register 1

7	6	5	4	3	2	1	0
WT15	WT14	WT13	WT12	WT11	WT10	WT9	WT8

Bit Number	Bit Mnemonic	Description
7-0	WT[15:8]	**Wait Time Byte 1** Used together with WT[23:16] and WT[7:0] (see SCWT0 Register).

Reset Value = 0010 0101b

Table 29. SCWT0 Register

SCWT0 (S:B4h, SCRS = 0)
Smart Card Character/Block Wait Time Register 0

7	6	5	4	3	2	1	0
WT7	WT6	WT5	WT4	WT3	WT2	WT1	WT0

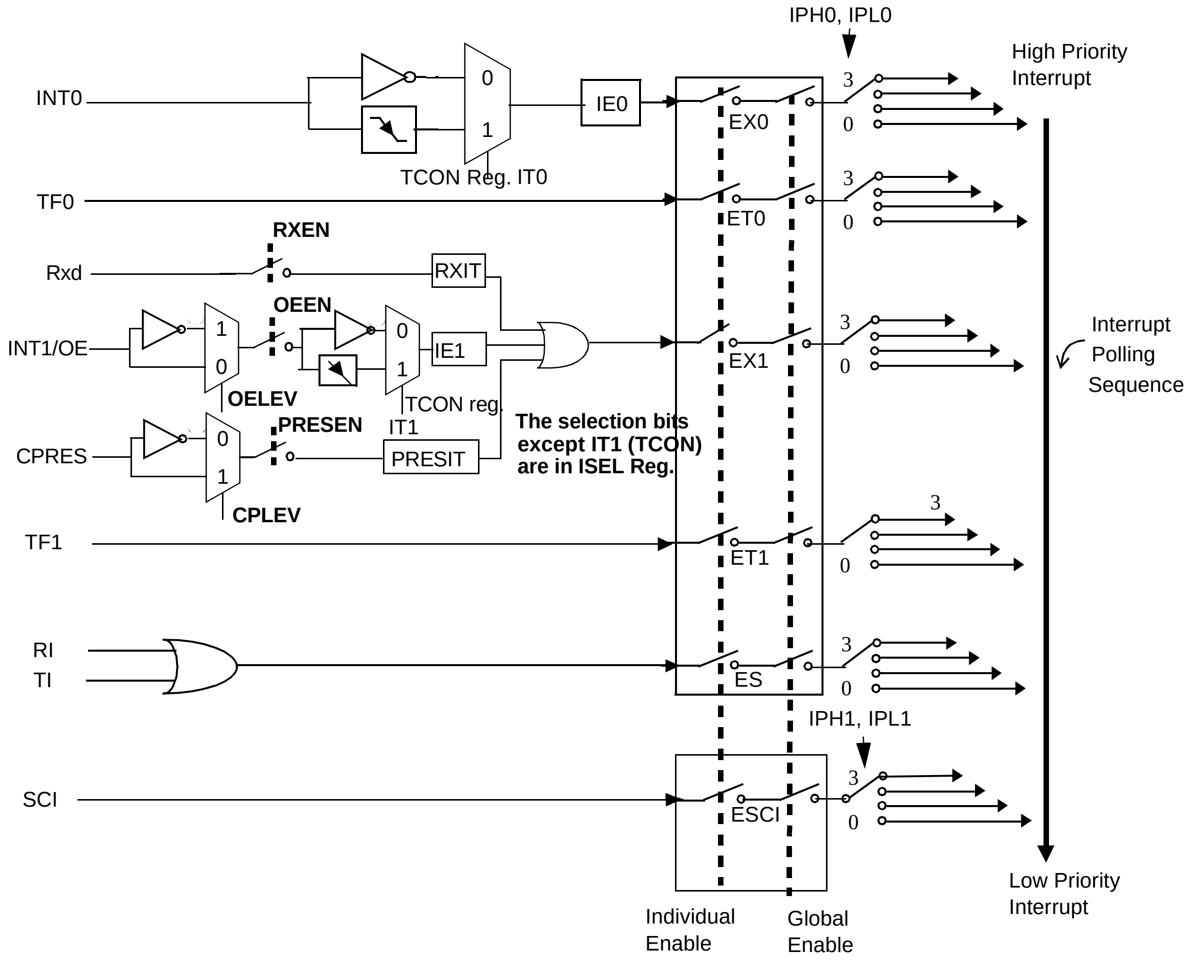
Bit Number	Bit Mnemonic	Description
7-0	WT[7:0]	**Wait Time Byte 0** WT[23:0] is the reload value of the Wait Time counter WTC. The WTC is a general-purpose Timer 0. It is using the ETU clock and is controlled by the WTEN bit (see Section “Waiting Time Counter (WT)”). When UART bit of SCICR Register is set, the WTC is automatically reloaded at each start bit of the UART. It is used to check the maximum time between to consecutive start bits.

Reset Value = 1000 0000b

Interrupt System

The T8xC5121 has a total of 6 interrupt vectors: four external interrupts ($\overline{\text{INT0}}$, $\overline{\text{INT1}}$/OE, CPRES, RxD), two Timer 0 interrupts (Timer 0s 0 and 1), serial port interrupt and Smart Card Interface interrupt. These interrupts are shown in Figure 22.

Figure 22. Interrupt Control System



Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (see Figure 32). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one of four priority levels by setting or clearing a bit in the Interrupt Priority register (see Figure 36) and in the Interrupt Priority High register (see Figure 38). Table 30 shows the bit values and priority levels associated with each combination.

Table 30. Priority Level Bit Values

IPH.x	IP.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

Table 31. Interrupt Vector Addresses

Interrupt Source	Vector Address
IE0	0003h
TF0	000Bh
IE1 & RxIt & PrIt	0013h
TF1	001Bh
RI & TI	0023h
SCI	0053h

INT1 Interrupt Vector

The INT1 interrupt is multiplexed with the three following inputs:

- INT1/$\overline{\text{OE}}$: Standard 8051 interrupt input
- Rxd: Received data on UART
- CPRES: Insertion or removall of the main card

The setting configurations for each input is detailed below:

INT1/$\overline{\text{OE}}$ Input

This interrupt input is active under the following conditions:

- It must be enabled thanks to OEEN Bit (ISEL Register)
- It can be active on a level or falling edge: thanks to IT1 Bit (TCON Register)
- If level triggering selection is set, the active level 0 or 1 can be selected with OELEV Bit (ISEL Register)

The Bit IE1 (TCON Register) is set by hardware when external interrupt detected. It is cleared when interrupt is processed.

Rxd Input

A second vector interrupt input is the reception of a character. UART Rx input can generate an interrupt if enabled with Bit RXEN (ISEL.0). The global enable bits EX1 and EA must also be set.

Then, the Bit RXIT (ISEL Register) is set by hardware when a low level is detected on P3.0/RXD input.

CPRES Input

The third input is the detection of a level change on CPRES input (P1.2). This input can generate an interrupt if enabled with PRESEN (ISEL.1), EX1 (IE0.2) and EA (IE0.7) Bits.

This detection is done according to the level selected with Bit CPLEV (ISEL.7).

Then the Bit PRESIT (ISEL.5) is set by hardware when the triggering conditions are met. This Bit must be cleared by software.

Table 32. IE0 Register

7	6	5	4	3	2	1	0
EA	-	-	ES	ET1	EX1	ET0	EX0

Bit Number	Bit Mnemonic	Description
7	EA	**Enable All interrupt bit** Clear to disable all interrupts. Set to enable all interrupts. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its interrupt enable bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	ES	**Serial port Enable bit** Clear to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	**Timer 1 overflow interrupt Enable bit** Clear to disable Timer 1 overflow interrupt. Set to enable Timer 1 overflow interrupt.
2	EX1	**External interrupt 1 Enable bit** Clear to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	**Timer 0 overflow interrupt Enable bit** Clear to disable Timer 0 overflow interrupt. Set to enable Timer 0 overflow interrupt.
0	EX0	**External interrupt 0 Enable bit** Clear to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0XX0 0000b
Bit addressable

Table 33. IE1 Register

7	6	5	4	3	2	1	0
-	-	-	-	ESCI	-	-	-

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	ESCI	**SCI Interrupt Enable** Clear to disable the SCI interrupt. Set to enable the SCI interrupt.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.

Reset Value = XXXX 0XXXb

Table 34. TCON Register
TCON (S:88h)
Timer 0/Counter Control Register

7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Bit Number	Bit Mnemonic	Description
7	TF1	**Timer 1 Overflow flag** Cleared by the hardware when processor vectors to interrupt routine. Set by the hardware on Timer 0/Counter overflow when Timer 1 register overflows.
6	TR1	**Timer 1 Run Control bit** Clear to turn off Timer 0/Counter 1. Set to turn on Timer 0/Counter 1.
5	TF0	**Timer 0 Overflow flag** Cleared by the hardware when processor vectors to interrupt routine. Set by the hardware on Timer 0/Counter overflow when Timer 0 register overflows.
4	TR0	**Timer 0 Run Control bit** Clear to turn off Timer 0/Counter 0. Set to turn on Timer 0/Counter 0.
3	IE1	**Interrupt 1 Edge flag** Cleared by the hardware when interrupt is processed if edge-triggered (see IT1). Set by the hardware when external interrupt is detected on the $\overline{\text{INT}}$1 pin.
2	IT1	**Interrupt 1 Type Control bit** Clear to select low level active (level triggered) for external interrupt 1 ($\overline{\text{INT}}$1). Set to select falling edge active (edge triggered) for external interrupt 1.
1	IE0	**Interrupt 0 Edge flag** Cleared by the hardware when interrupt is processed if edge-triggered (see IT0). Set by the hardware when external interrupt is detected on $\overline{\text{INT}}$0 pin.
0	IT0	**Interrupt 0 Type Control bit** Clear to select low level active (level triggered) for external interrupt 0 ($\overline{\text{INT}}$0). Set to select falling edge active (edge triggered) for external interrupt 0.

Reset Value = 0000 0000b

Table 35. ISEL Register

7	6	5	4	3	2	1	0
CPLEV	OEIT	PRESIT	RXIT	OELEV	OEEN	PRESEN	RXEN

Bit Number	Bit Mnemonic	Description
7	CPLEV	**Card presence detection level** This bit indicates which CPRES level will bring about an interrupt Set this bit to indicate that Card Presence IT will appear if CPRES is at high level. Clear this bit to indicate that Card Presence IT will appear if CPRES is at low level.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	PRESIT	**Card presence detection interrupt flag** Set by hardware Must be cleared by software
4	RXIT	**Received data interrupt flag** Set by hardware Must be cleared by software
3	OELEV	**OE/INT1 signal active level** Set this bit to indicate that high level is active. Clear this bit to indicate that low level is active.
2	OEEN	**OE/INT1 Interrupt Disable bit** Clear to disable INT1 interrupt Set to enable INT1 interrupt
1	PRESEN	**Card presence detection Interrupt Enable bit** Clear to disable the card presence detection interrupt coming from SCIB. Set to enable the card presence detection interrupt coming from SCIB.
0	RXEN	**Received data Interrupt Enable bit** Clear to disable the RxD interrupt. Set to enable the RxD interrupt (a minimal bit width of 0.1 ms is required to wake up from Power-Down).

Reset Value = 0000 0100b

Table 36. IPL0 Register

7	6	5	4	3	2	1	0
-	-	-	PSL	PT1L	PX1L	PT0L	PX0L

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	PSL	**Serial port Priority bit** Refer to PSH for priority level.
3	PT1L	**Timer 1 overflow interrupt Priority bit** Refer to PT1H for priority level.
2	PX1L	**External interrupt 1 Priority bit** Refer to PX1H for priority level.
1	PT0L	**Timer 0 overflow interrupt Priority bit** Refer to PT0H for priority level.
0	PX0L	**External interrupt 0 Priority bit** Refer to PX0H for priority level.

Reset Value = XXX0 0000b
Bit addressable

Table 37. IPL1 Register

7	6	5	4	3	2	1	0
-	-	-	-	PSCIL	-	-	-

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	PSCIL	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.

Reset Value = XXXX 0XXXb
Bit addressable

Table 38. IPH0 Register

7	6	5	4	3	2	1	0
-	-	-	PSH	PT1H	PX1H	PT0H	PX0H

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	PSH	**Serial port Priority High bit** PSH PS Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
3	PT1H	**Timer 1 overflow interrupt Priority High bit** PT1H PT1 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
2	PX1H	**External interrupt 1 Priority High bit** PX1H PX1 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
1	PT0H	**Timer 0 overflow interrupt Priority High bit** PT0H PT0 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
0	PX0H	**External interrupt 0 Priority High bit** PX0 HPX0 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest

Reset Value = XXX0 0000b

Table 39. IPH1 Register

7	6	5	4	3	2	1	0
-	-	-	-	PSCIH	-	-	-

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	PSCIH	**SCI Interrupt Priority level most significant bit** PSCIH PSCIL Priority level 0 0 Lowest 0 1 1 0 1 1 Highest priority
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.

Reset Value = XXXX 0XXXb

LED Ports Configuration

The current source of the LED Ports can be adjusted to 3 different values: 2, 4 or 10 mA. The LED output is an alternate function of P3.6 an P3.7 and cannot be used while the alternate card function is used.

The control register LEDCON is detailed below.

Registers Definition

Table 40. LEDCON Register

7	6	5	4	3	2	1	0
-	-	-	-	LED1[1]	LED1[0]	LED0[1]	LED0[0]

Bit Number	Bit Mnemonic	Description
7 - 4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3 - 2	LED1[1,0]	**Port LED1 configuration:** LED1[1] LED1[0] Configuration 0 0 Standard C51 port 0 1 2 mA current source when P3.7 is at Low Level 1 0 4 mA current source when P3.7 is at Low Level 1 1 10 mA current source when P3.7 is at Low Level
1 - 0	LED0[1,0]	**Port LED0 configuration:** LED0[1] LED0[0] Configuration 0 0 standard C51 port 0 1 2 mA current source when P3.6 is at Low Level 1 0 4 mA current source when P3.6 is at Low Level 1 1 10 mA current source when P3.6 is at Low Level

Reset Value = XXXX 0000b

Dual Data Pointer

T8xC5121 contains a Dual Data Pointer accelerating data memory block moves. The Standard 80C52 Data Pointer is a 16-bit value that is used to address off-chip data RAM or peripherals. In T8xC5121, the standard 16-bit data pointer is called DPTR and located at SFR location 82H and 83H. The second Data Pointer named DPTR1 is located at the same address than the previous one. The DPTR select bit (DPS / bit0) chooses the active pointer and it is located into the AUXR1 register. It should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.
The user switches between data pointers by toggling the LSB of the AUXR1. The increment (INC) is a solution for this. All DPTR-related instructions use the currently selected DPTR for any activity. Therefore only one instruction is required to switch from a source to a destination address. Using the Dual Data Pointer saves code and resources when moves of blocks need to be accomplished.

The second Data Pointer can be used to address the on-chip XRAM.

Table 41. DPL Register

DPL - Low Byte of DPTR1 (82h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Reset value = 0000 0000b

Table 42. DPH Register

DPH - High Byte of DPTR1 (83h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Reset value = 0000 0000b

Table 43. AUXR1 Register

AUXR1 - Dual Pointer Selection Register (A2h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	DPS

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	DPS	**Data pointer 1** Clear to select DPTR0 as Data Pointer. Set to select DPTR1 as Data Pointer.

Reset value = XXXX XXX0b

Memory Management

Program Memory

Introduction

All the T8xC5121 versions implement 16 Kbytes of ROM memory, 256 Bytes RAM and 256 Bytes XRAM.

The hardware configuration byte and the split of internal memory spaces depends on the product and is detailed below.

ROM Configuration Byte

Table 44. ROM Configuration Byte Hardware Register

7	6	5	4	3	2	1	0
-	BLJRB	-	-	-	-	-	

Bit Number	Bit Mnemonic	Description
7		**Reserved**
6	BLJRB	**Bootloader Jump RAM Bit** Set to configure User Code in ROM Clear to configure Bootlader in ROM
5-0		**Reserved**

The BLJRB depends of the product version:

- 1: ROM mask version
- 0: EEPROM/CRAM versions

This bit defines if, after reset, either the Customer ROM program or the Bootloader program is executed (for In System programming).

Program ROM Lock Bits

The program Lock system protects the on-chip program against software piracy.

The T8xC5121 products are delivered with the highest protection level.

Table 45. T8xC5121 Products Protection Level

Program Lock Bits			Protection Description
Security Level	LB1	LB2	
3	P	P	**SSOP24 version:** Read function is disabled.But checksum control is still enabled **PLCC52 version:** MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset. But checksum control is still enabled. External execution is possible.

P = Programmed

Memory Mapping

In the products versions, the following internal spaces are defined:

- RAM
- XRAM
- CRAM: 16 KBytes Program RAM Memory
- ROM

The specific accesses from/to these memories are:

- XRAM: if the bit RPS in RCON (described below) is reset, MOVX instructions address the XRAM space.
- CRAM: if the bit RPS in RCON is set, MOVX instructions address the CRAM space.

Table 46. RCON Register

7	6	5	4	3	2	1	0
	-	-		**RPS**			

Bit Number	Bit Mnemonic	Description
7-4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	RPS	**CRAM space map bit** Set to map the CRAM space during MOVX instructions Clear to map the Data space during MOVX. This bit has priority over the EXTRAM bit.
2-0	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.

Reset Value = XXXX 0XXXb

T89C5121 Flash ROM Version

Three memory blocks are implemented

- An internal serial EEPROM can be loaded from external with the application program.
- The ROM memory contains the Bootloader program. The entry point is located at address F800h. The lower 14K Bytes between address C000h and F7FFh is, also, used for the Bootloader program.
- The CRAM is the application program memory. This memory is mapped in the External RAM space. The bit RPS in RCON (SFR address 0D1h) is set to map the CRAM space during MOVX instructions

For first programming or an update, the program can be downloaded in the internal EEPROM (and in the CRAM) from an external device:

- Either an external EEPROM if detected
- or from a host through RS232 serial communication.

For this purpose, an In-System Programming (ISP) is supplied in a Bootloader. This Bootloader is program masked in ROM space.

The Hardware Byte BLJRB value is 0.

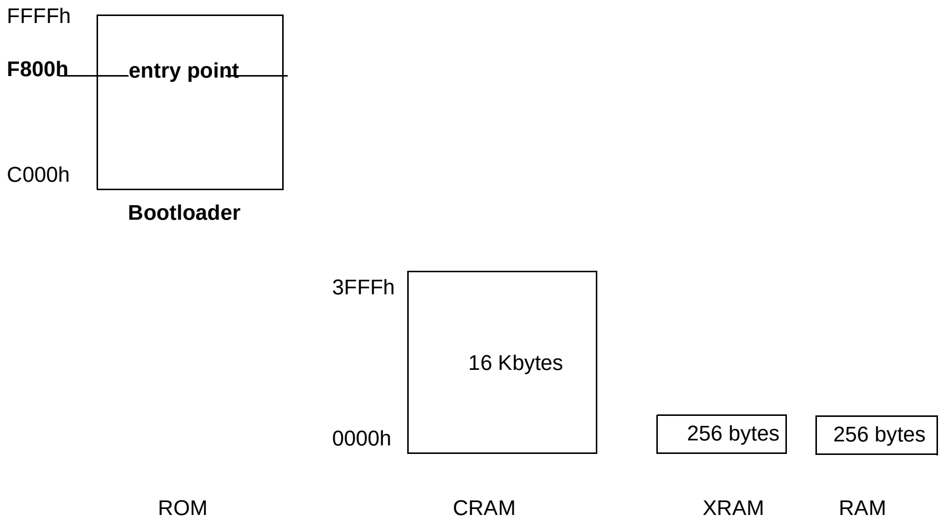
As described on page 7, after Reset, the Bootloader program is executed.

If a serial communication device (as described above: TWI or RS232) is detected, the program download its content in the internal EEPROM and in CRAM.

Else, the program is internally downloaded from the internal EEPROM into the program CRAM memory (16 Kbytes)

Then, in the two cases, the Bootloader executes a Long Jump at address 0000h which initializes the Program counter at the lower address (0000h) of the executable CRAM.

Figure 23. CRAM with ROM and EEPROM Memory Mappings



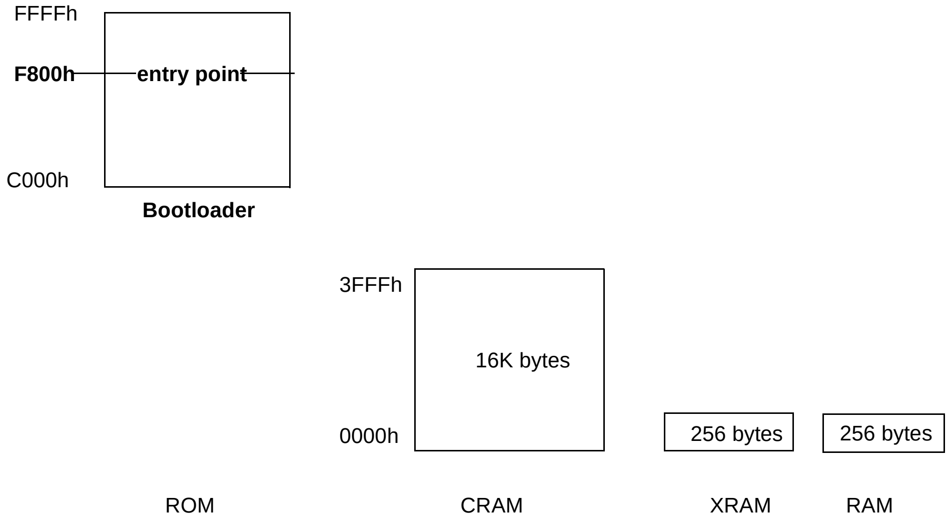
T85C121 Code RAM Version

Two memory blocks are implemented:

- The ROM memory contains the Bootloader program.
- The CRAM is the Application program memory.

After Reset, the program is downloaded, as described in last paragraph, from either an external EEPROM or from an host connected on RS232 serial link into the program CRAM memory of 16 Kbytes. Then the Program Counter is set at address 0000h of the CRAM space and the program is executed.

Figure 24. CRAM and ROM Mappings



T83C5121 with Mask ROM Version

In this version, the customer program is masked in 16 Kbytes ROM.

- The customer program is masked in ROM during the final production phase. The ROM size will be determined at mask generation process depending of the program size.

In-System Programming

The In-System Programming (ISP) mode is only implemented in the following product versions:

- EEPROM version
- CRAM version

(The ROM product version is masked with the customer program and does not need ISP mode)

The ISP is used to download an Application program in the device and to run it.

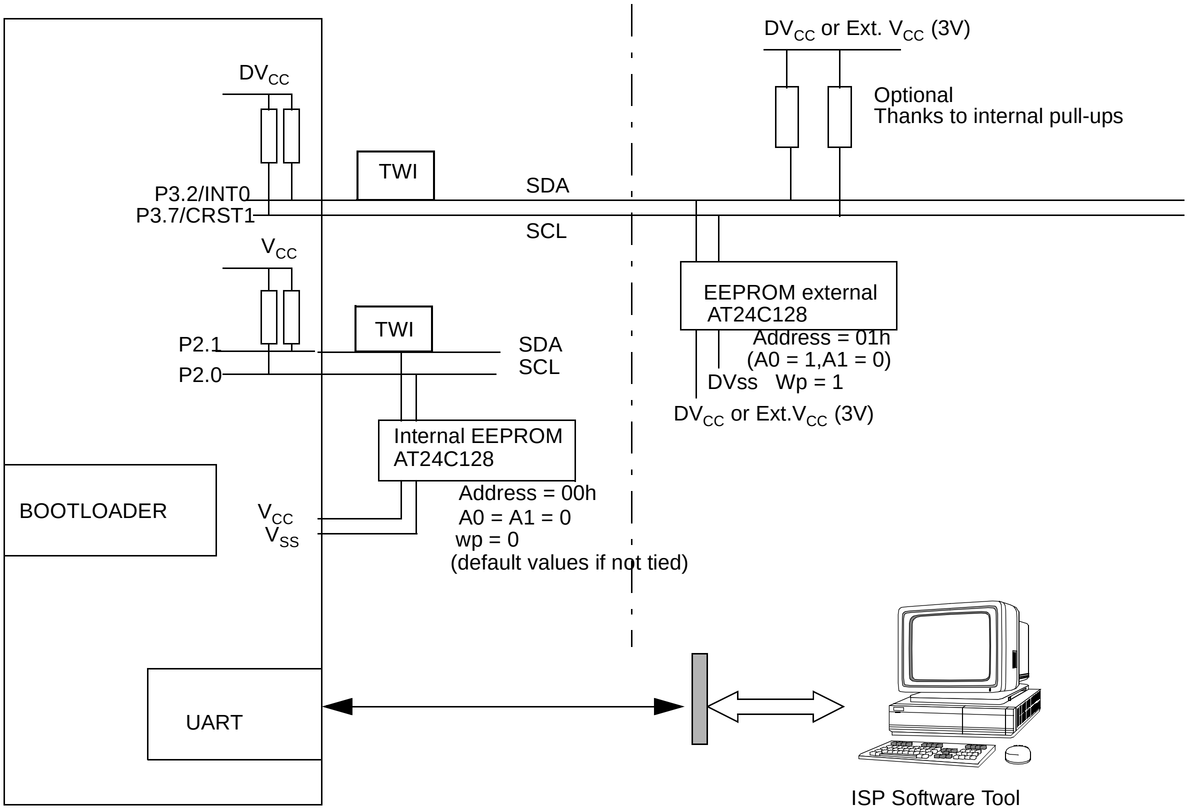
The communication protocols which are implemented are: UART and TWI.

Hardware Interface

The hardware in relation with the two communication protocols is detailed below:

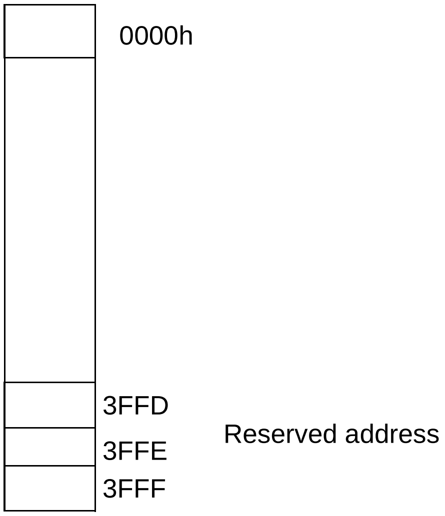
- TWI protocol
- Serial protocol

Figure 25. Hardware in Relation with the Two Communication Protocols



EEPROM Mapping

The 16K Bytes EEPROM mapping is the following:



The three last bytes are reserved respectively:

- Software Security Byte: address 3FFDh
- CRC Bytes: address 3FFEh and 3FFFh

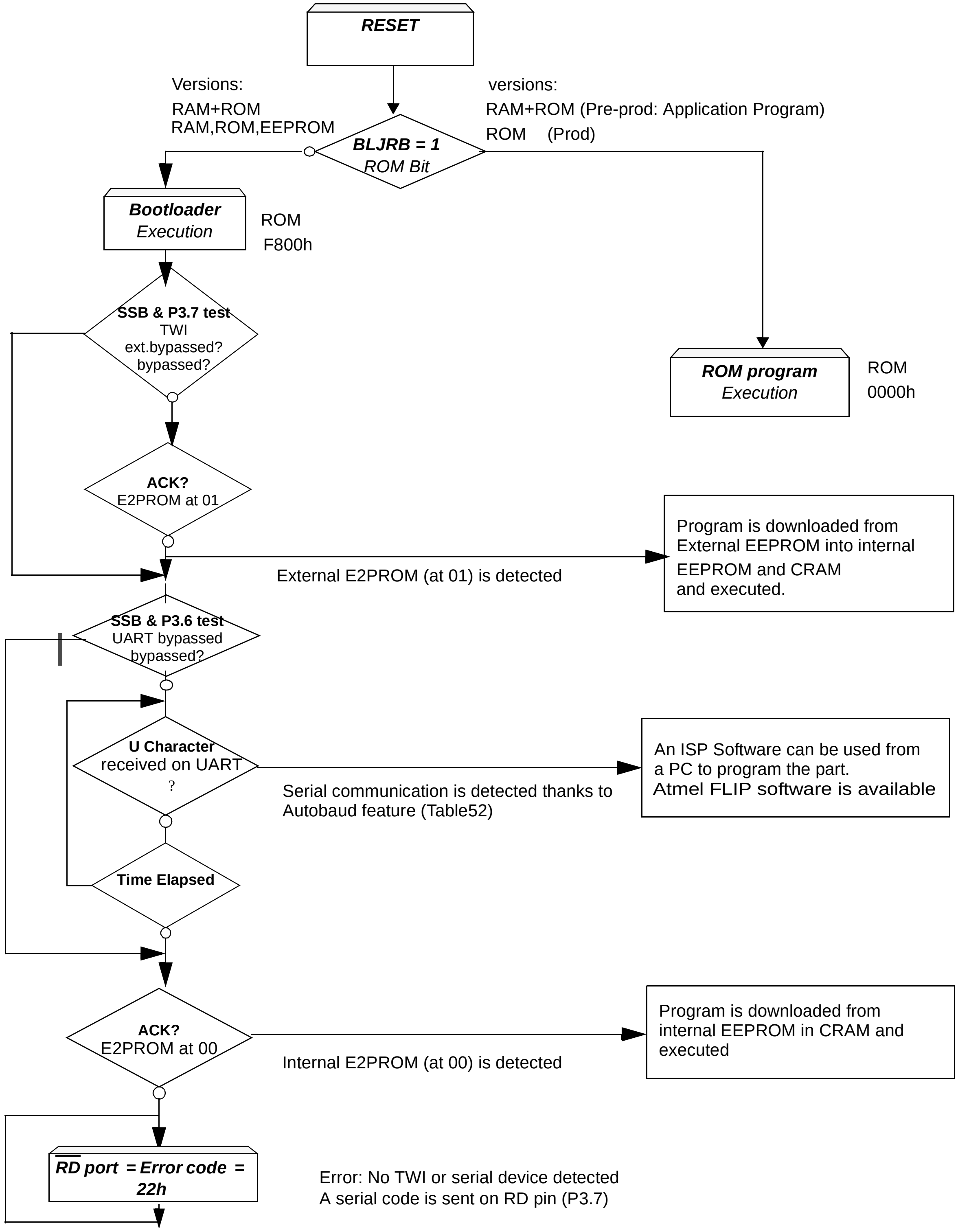
The use of these bytes is described in the following paragraphs.

Therefore, the User Program must be mapped from 0000h to 3FFCh address.

Bootloader Functional Diagram

As described in Section “ROM Configuration Byte”, page 58a ROM bit BLJRB (Boot Loader Jump ROM Bit) defines which product version is. The Bootloader program is mapped in ROM space from address C000h up to FFFFh and the entry point is located at address F800h.

Figure 26. Bootloader Flowchart



In-System Programming Timings

The download from the internal EEPROM to CRAM is executed after 4 seconds when operating at 12 MHz frequency.

Protection Mechanisms

Transfer Checks

In order to verify that the transfers are free of errors, a CRC check is implemented during the download of the program in CRAM.

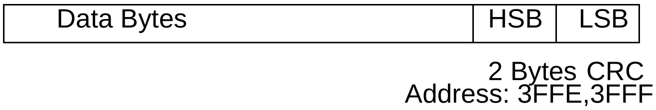
This test is done at the end of the 16K space programming.

As detailed in the next algorithms:

- in ISP mode, if CRC test pass, a character Y is returned before the CRLF characters else a character Z is retuned.
- in download mode, a serial data AA is sent on P3.7 port and CRAM is not executed.

For this purpose, the user program must include in the two last upper bytes (address 3FFEh and 3FFFh) the CRC of the previous bytes (calculated from the address 0000h to 3FFFDh).

The following frames are examples including the CRC in the two last upper bytes:



- FF 03 C0 21 04 00 00 08 07 02 08 02 2D DB (CRC = 2DDBh)
- FF 03 80 21 02 04 00 0A 03 06 C0 A8 70 01 E3 3D (CRC = E33Dh)
- FF 03 C0 21 02 01 00 10 02 06 00 00 00 00 05 06 00 00 76 55 49 AC (CRC = 49ACh)

Table 47. Synthesis of Transfer Protection Mechanisms

Source	Target	Check
MCU	CRAM	CRC computed during CRAM Write operation: if error an error code is applied on P3.7 and Code execution by LJMP000 is not done.
Intern. EEP	MCU	This Read operation is secured by the Write sequence described above
MCU	Intern. EEP	Same protection as in first row above because CRAM is written in sequence after each page programming of EEP
Ext. EEP	MCU	Same as above as data are transferred to EEP INT and then to CRAM

Notes:

1. The transfer of SSB Byte is also secured by CRC as the CRC is computed on all the 16K data.
2. If a Bad transfer has occurred in the Internal EEPROM (CRC is bad), as the CRC check is finally done at the end of CRAM programming, application program will NOT be executed after any Reset.

Read/Write Protection

Lock Byte

In order to protect the content of the internal EEPROM, a Software Security Byte (SSB) defines two security levels:

- level 0: SSB = 0xFF: Write and Read are allowed
- level 1: SSB = 0xFE: Write is disabled
- level 2: SSB = 0xFC: Write and Read are disabled

This SSB Byte is located at address 3FFDh.

When the level 2 is set, the command to set level 1 is disabled. The security levels can only be increased.

The only mean to remove the security level 2 is to send a Full Chip Erase command.

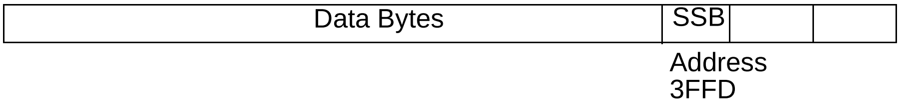


Table 48. Synthesis of Security Mechanisms

Source	Function	Protection
Internal EEPROM	Write	The first protection level of the SSB Byte IN the internal EEPROM protects against ISP Write command
Internal EEPROM	Read	The second protection level of the SSB Byte IN the internal EEPROM protects against ISP Read commands
CRAM	Write	The first protection level of the SSB Byte IN the internal EEPROM protects against ISP Write command in CRAM
CRAM	Read	The second protection level of the SSB Byte IN the CRAM protects against ISP Read commands

Configuration Bits

The Bootloader tests that TWI components are connected as slave components on the TWI external bus and later in the algorithm if characters are received on the UART input. This default configuration can be changed, after a first programming, in order:

- to disable new programming in download mode from external serial EEPROM to disable ISP programming using UART and
- to avoid any conflict with the target hardware on external TWI bus or UART.

This can be configured with the two higher bits of the SSB Byte detailed in the previous paragraph.

The bit 7 is used to bypass (if 0) the External TWI Acknowledge test.

The bit 6 is used to bypass (if 0) the UART receipt test.

These two bypass modes can be disabled if a level 0 is applied on, respectively, P3.5 and P3.6 pins. This allows to force and use ISP even if the device has been configured as programmed device.

Table 49. Valid Software Security Byte Values

SSB Values	Functions
FE	No bypass and level1 security
FC	No bypass and level2 security
BF,BE,BC	UART bypass and security levels
7F,7E,7C	External TWI bypass and security levels
3F,3E,3C	UART and Ext. TWI bypass

UART Protocol

Overview

The serial protocol used is described below.

Physical Layer

The UART is used to transmit information with the following configuration:

- Character: 8-bit data
- Parity: none
- Stop: 1 bit
- Flow control: none
- Baudrate: autobaud is performed by the bootloader to compute the baudrate chosen by the host.

Datas and Limits

As described in Section “Transfer Checks”, the downloaded program include the CRC values in the last two upper bytes of the 16K bytes space.

An update of a part of the 16K program cannot be done because the CRC value would have to be updated with a value which depends of the actual value of the rest of the program.

So the Program function of the PC Software Tool include the individual program commands (with 64 data bytes) from address 0000h to address 3FFFh.

Frame Description

The Serial Protocol is based on the Intel Hex-type records.

Intel Hex records consist of ASCII characters used to represent hexadecimal values and are summarized below:

Table 50. Intel Hex Type Frame

Record Mark ‘:’	Reclen	Load Offset	Record Type	Data or Info	Checksum
1-byte	1-byte = 40h	2-byte	1-byte	64-byte	1-byte

- Record Mark:
  - Record Mark is the start of frame. This field must contain’:’.
- Reclen:
  - Reclen specifies that the number of bytes of information or data that follow the Record Type field of the record.
- Load Offset:
  - Load Offset specifies the 16-bit starting load offset of the data bytes, therefore this field is used only for Program Data Record (see Table 51).

- Record Type:
  - Record Type specifies the command type. This field is used to interpret the remaining information within the frame. The encoding for all the current record types are described in Table 51.
- Data/Info:
  - Data/Info is a 64 bytes length field. It consists of 64 bytes encoded as pairs of hexadecimal digits. The meaning of data depends on the Record Type.
- Checksum:
  - The two's complement of the 8-bit bytes that result from converting each pair of ASCII hexadecimal digits to one byte of binary, and including the Reclen field to and including the last byte of the Data/Info field. Therefore, the sum of all the ASCII pairs in a record after converting to binary, from the Reclen field to and including the Checksum field, is zero.

Notes:
1. A data byte is represented by two ASCII characters.
2. When the field Load Offset is not used, it should be coded as 2 bytes (00h 00h).

Command Description

Table 51. Frame Description

Command	Command Name	data[0]	data[1]	Command Effect
00h	Program Data			Program 64 Data Bytes
01h	End Of File	-	-	End of File
03h	Write Function	07h		Full Chip Erase
		05h	00h	Program SSB level1
		05h	01h	Program SSB level2
		03h	01h	LJMP(data[2],data[3]) (LJMP0000h)
04h	Display Function	Data[0:1] = start address Data [2:3] = end address Data[4] = 00h -> Display data Data[4] = 01h -> Blank check Data[4] = 03h -> Display CRAM		Display Data
05h	Read Function	07h	00h	Read SSB
		0Fh	00h	Read Bootloader Version
06h	Direct Load of Baud Rate	HSB	LSB	Not implemented

Autobaud

The ISP feature allows a wide range of baud rates in the user application. It is also adaptable to a wide range of oscillator frequencies. This is accomplished by measuring the bit-time of a single bit in a received character. This information is then used to program the baud rate in terms of timer counts based on the oscillator frequency. The ISP feature requires that an initial character (an uppercase U) be sent to the T8xC5121 to establish the baud rate. Table show the autobaud capability.

Table 52. Autobaud performances

Frequency (MHz) **Baudrate (kHz)**	**6.176**	**8**	**11.0592**	**12**	**14.3**	**14.7456**	**16**
9600	OK	OK	OK	OK	OK	OK	-
19200	OK	-	OK	OK	Ok	OK	OK
38400	-		OK	OK	OK	OK	OK
57600	-	-	OK	-	OK	OK	-
115200	-	-	-	-	-	OK	-

Protection Mechanisms

Transfer Checks

Table 53. Synthesis of the Communication Protection Mechanisms

Source	**Target**	**Check**
UART ISP	MCU	Checksum included in commands is tested with calculated checksum: if bad, X echo returned to ISP
MCU	CRAM	CRC computed during CRAM Write operation: if error an error code is applied on P3.7. Error code'Z' is returned to ISP.
MCU	Intern. EEP	Same protection as above because CRAM is written in sequence after each page programming of EEP

Notes:
1. The transfer of SSB Byte is also secured by CRC as the CRC is computed on all the 16K data.
2. If a bad transfer has occurred in the Internal EEPROM (CRC is bad), as the CRC check is finally done at the end of CRAM programming, application program will NOT be executed after any Reset.

Security

Table 54. Synthesis of the Security Mechanisms

Source	**Target**	**Case**	**Protection**
UART ISP	Intern. EEP	Read access	SSB level 2 must be set (done, if selected, at ISP Programming or Ext EEP Download)
UART ISP	CRAM	Read access	SSB level 2 IN CRAM must be set (SSB is downloaded from Int EEP after Reset)

Source	Target	Case	Protection
UART ISP	Intern. EEP	Partial Programming which would not fit with old CRC	SSB level 1 must be set (done, if selected, at ISP Programming or Ext EEP Download) Then the EEP must be, first, erased before reprogramming. Programming is done on all the memory space
UART ISP	Intern. EEP	Programming	SSB level 1 must be set (done, if selected, at ISP Programming or Ext EEP Donwload)
UART ISP	CRAM	Program access	SSB level 1 IN Int EEP protects as, first, the Int EEP is programmed before CRAM
UART ISP	SSB in EEP and CRAM	level 2 to level 1	Protected by Bootloader
UART ISP	SSB in EEP and CRAM	level 1 to level 0	Protected by Bootloader

Timers/Counters

Introduction

The T8xC5121 implements two general-purpose, 16-bit Timer 0s/Counters. Although they are identified as Timer 0, Timer 1, you can independently configure each to operate in a variety of modes as a Timer 0 or as an event Counter. When operating as a Timer 0, a Timer 0/Counter runs for a programmed length of time, then issues an interrupt request. When operating as a Counter, a Timer 0/Counter counts negative transitions on an external pin. After a preset number of counts, the Counter issues an interrupt request.

The Timer 0 registers and associated control registers are implemented as addressable Special Function Registers (SFRs). Two of the SFRs provide programmable control of the Timer 0s as follows:

- Timer 0/Counter mode control register (TMOD) and Timer 0/Counter control register (TCON) control respectively Timer 0 and Timer 1.

The various operating modes of each Timer 0/Counter are described below.

Timer 0/Counter Operations

For example, a basic operation is Timer 0 registers THx and TLx (x = 0, 1) connected in cascade to form a 16-bit Timer 0. Setting the run control bit (TRx) in the TCON register (see Figure 55) turns the Timer 0 on by allowing the selected input to increment TLx. When TLx overflows it increments THx and when THx overflows it sets the Timer 0 overflow flag (TFx) in the TCON register. Setting the TRx does not clear the THx and TLx Timer 0 registers. Timer 0 registers can be accessed to obtain the current count or to enter preset values. They can be read at any time but the TRx bit must be cleared to preset their values, otherwise the behavior of the Timer 0/Counter is unpredictable.

The C/Tx# control bit selects Timer 0 operation or Counter operation by selecting the divided-down system clock or the external pin Tx as the source for the counted signal. The TRx bit must be cleared when changing the operating mode, otherwise the behavior of the Timer 0/Counter is unpredictable.
For Timer 0 operation (C/Tx# = 0), the Timer 0 register counts the divided-down system clock. The Timer 0 register incremented once every peripheral cycle.

Exceptions are the Timer 0 2 Baud Rate and Clock-out modes in which the Timer 0 register is incremented by the system clock divided by two.

For Counter operation (C/Tx# = 1), the Timer 0 register counts the negative transitions on the Tx external input pin. The external input is sampled during every S5P2 state. The Programmer’s Guide describes the notation for the states in a peripheral cycle. When the sample is high in one cycle and low in the next one, the Counter is incremented. The new count value appears in the register during the next S3P1 state after the transition has been detected. Since it takes 12 states (24 oscillator periods) to recognize a negative transition, the maximum count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full peripheral cycle.

Timer 0

Timer 0 functions as either a Timer 0 or an event Counter in four operating modes. Figure 27 through Figure 30 show the logic configuration of each mode.

Timer 0 is controlled by the four lower bits of the TMOD register (see Figure 56) and bits 0, 1, 4 and 5 of the TCON register (see Figure 55). The TMOD register selects the method of Timer 0 gating (GATE0), Timer 0 or Counter operation (T/C0#) and the operating mode (M10 and M00). The TCON register provides Timer 0 control functions: overflow flag (TF0), run control bit (TR0), interrupt flag (IE0) and interrupt type control bit (IT0).
For normal Timer 0 operation (GATE0 = 0), setting TR0 allows TL0 to be incremented by the selected input. Setting GATE0 and TR0 allows external pin $\overline{\text{INT0}}$ to control Timer 0 operation.

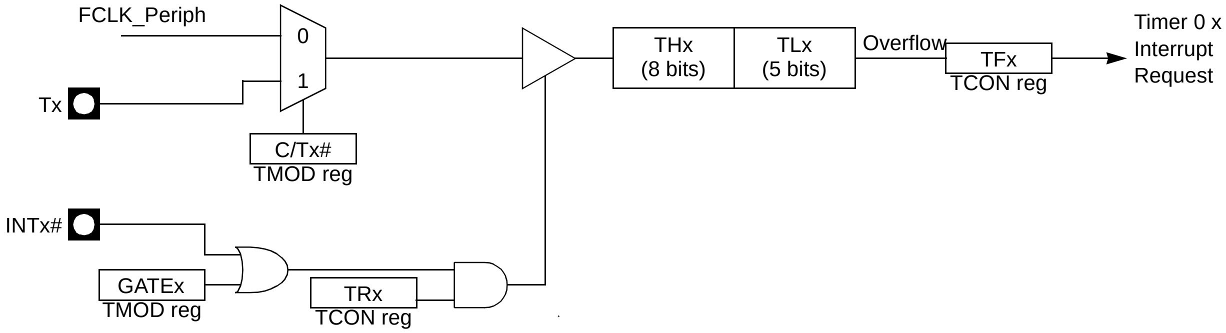
Timer 0 overflow (count rolls over from all 1s to all 0s) sets the TF0 flag and generates an interrupt request.

It is important to stop the Timer 0/Counter before changing modes.

Mode 0 (13-bit Timer 0)

Mode 0 configures Timer 0 as a 13-bit Timer 0 which is set up as an 8-bit Timer 0 (TH0 register) with a module-32 prescaler implemented with the lower five bits of the TL0 register (see Figure 27). The upper three bits of the TL0 register are indeterminate and should be ignored. Prescaler overflow increments the TH0 register.

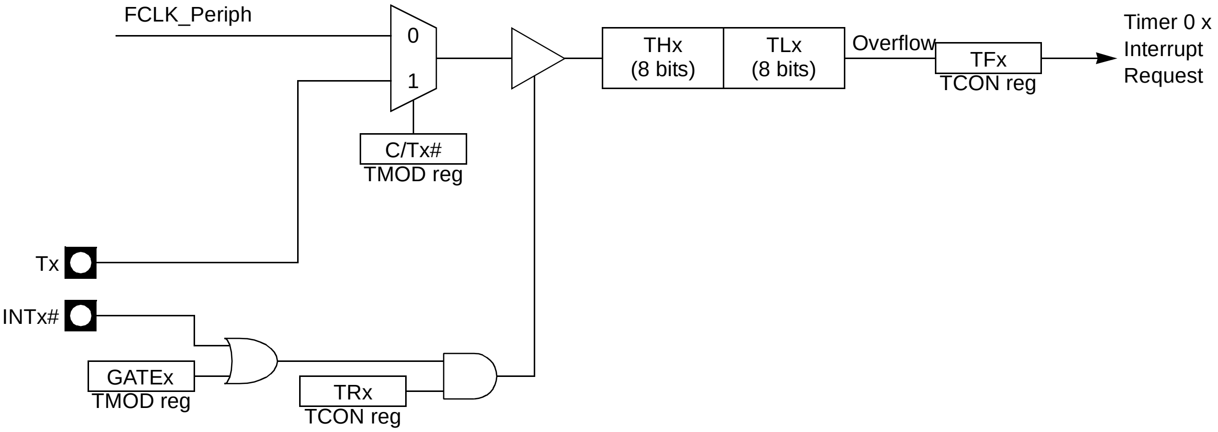
Figure 27. Timer 0/Counter x (x = 0 or 1) in Mode 0



Mode 1 (16-bit Timer 0)

Mode 1 configures Timer 0 as a 16-bit Timer 0 with the TH0 and TL0 registers connected in a cascade (see Figure 28). The selected input increments the TL0 register.

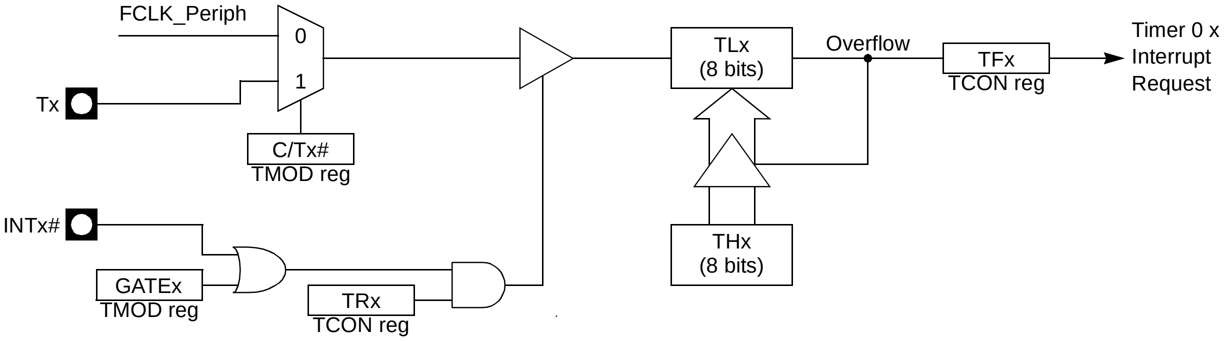
Figure 28. Timer 0/Counter x (x = 0 or 1) in Mode 1



Mode 2 (8-bit Timer 0 with Auto-Reload)

Mode 2 configures Timer 0 as an 8-bit Timer 0 (TL0 register) that automatically reloads from the TH0 register (see Figure 29). TL0 overflow sets the TF0 flag in the TCON register and reloads TL0 with the contents of TH0, which is preset by the software. When the interrupt request is serviced, the hardware clears TF0. The reload leaves TH0 unchanged. The next reload value may be changed at any time by writing it to the TH0 register.

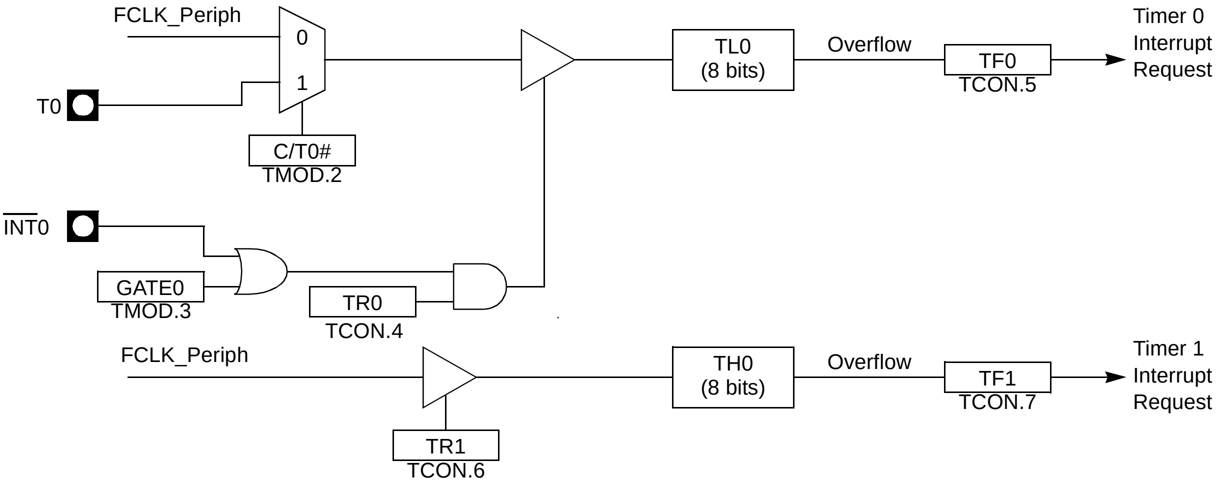
Figure 29. Timer 0/Counter x (x = 0 or 1) in Mode 2



Mode 3 (Two 8-bit Timer 0s)

Mode 3 configures Timer 0 so that registers TL0 and TH0 operate as 8-bit Timer 0s (see Figure 30). This mode is provided for applications requiring an additional 8-bit Timer 0 or Counter. TL0 uses the Timer 0 control bits C/T0# and GATE0 in the TMOD register, and TR0 and TF0 in the TCON register in the normal manner. TH0 is locked into a Timer 0 function (counting F_{UART}) and takes over use of the Timer 1 interrupt (TF1) and run control (TR1) bits. Thus, operation of Timer 1 is restricted when Timer 0 is in mode 3.

Figure 30. Timer 0/Counter 0 in Mode 3: Two 8-bit Counters



Timer 1

Timer 1 is identical to Timer 0 except for Mode 3 which is a hold-count mode. The following comments help to understand the differences:

- Timer 1 functions as either a Timer 0 or an event Counter in the three operating modes. Figure 27 through Figure 29 show the logical configuration for modes 0, 1, and 2. Mode 3 of Timer 1 is a hold-count mode.
- Timer 1 is controlled by the four high-order bits of the TMOD register (see Figure 56) and bits 2, 3, 6 and 7 of the TCON register (see Figure 55). The TMOD register selects the method of Timer 0 gating (GATE1), Timer 0 or Counter operation (C/T1#) and the operating mode (M11 and M01). The TCON register provides Timer 1 control functions: overflow flag (TF1), run control bit (TR1), interrupt flag (IE1) and the interrupt type control bit (IT1).
- Timer 1 can serve as the Baud Rate Generator for the Serial Port. Mode 2 is best suited for this purpose.
- For normal Timer 0 operation (GATE1 = 0), setting TR1 allows TL1 to be incremented by the selected input. Setting GATE1 and TR1 allows external pin $\overline{\text{INT1}}$ to control Timer 0 operation.
- Timer 1 overflow (count rolls over from all 1s to all 0s) sets the TF1 flag and generates an interrupt request.
- When Timer 0 is in mode 3, it uses Timer 1's overflow flag (TF1) and run control bit (TR1). For this situation, use Timer 1 only for applications that do not require an interrupt (such as a Baud Rate Generator for the Serial Port) and switch Timer 1 in and out of mode 3 to turn it off and on.
- It is important to stop the Timer 0/Counter before changing modes.

Mode 0 (13-bit Timer 0)

Mode 0 configures Timer 1 as a 13-bit Timer 0, which is set up as an 8-bit Timer 0 (TH1 register) with a modulo-32 prescaler implemented with the lower 5 bits of the TL1 register (see Figure 27). The upper 3 bits of TL1 register are ignored. Prescaler overflow increments the TH1 register.

Mode 1 (16-bit Timer 0)

Mode 1 configures Timer 1 as a 16-bit Timer 0 with TH1 and TL1 registers connected in cascade (see Figure 28). The selected input increments the TL1 register.

Mode 2 (8-bit Timer 0 with Auto-Reload)

Mode 2 configures Timer 1 as an 8-bit Timer 0 (TL1 register) with automatic reload from the TH1 register on overflow (see Figure 29). TL1 overflow sets the TF1 flag in the TCON register and reloads TL1 with the contents of TH1, which is preset by the software. The reload leaves TH1 unchanged.

Mode 3 (Halt)

Placing Timer 1 in mode 3 causes it to halt and hold its count. This can be used to halt Timer 1 when the TR1 run control bit is not available i.e., when Timer 0 is in mode 3.

Registers

Table 55. TCON Register
TCON (S:88h) - Timer 0/Counter Control Register

7	6	5	4	3	2	1	0
TF1	**TR1**	**TF0**	**TR0**	**IE1**	**IT1**	**IE0**	**IT0**

Bit Number	Bit Mnemonic	Description
7	TF1	**Timer 1 Overflow flag** Cleared by the hardware when processor vectors to interrupt routine. Set by the hardware on Timer 0/Counter overflow when Timer 1 register overflows.
6	TR1	**Timer 1 Run Control bit** Clear to turn off Timer 0/Counter 1. Set to turn on Timer 0/Counter 1.
5	TF0	**Timer 0 Overflow flag** Cleared by the hardware when processor vectors to interrupt routine. Set by the hardware on Timer 0/Counter overflow when Timer 0 register overflows.
4	TR0	**Timer 0 Run Control bit** Clear to turn off Timer 0/Counter 0. Set to turn on Timer 0/Counter 0.
3	IE1	**Interrupt 1 Edge flag** Cleared by the hardware when interrupt is processed if edge-triggered (see IT1). Set by the hardware when external interrupt is detected on the INT1 pin.
2	IT1	**Interrupt 1 Type Control bit** Clear to select low level active (level triggered) for external interrupt 1 ($\overline{\text{INT1}}$). Set to select falling edge active (edge triggered) for external interrupt 1.
1	IE0	**Interrupt 0 Edge flag** Cleared by the hardware when interrupt is processed if edge-triggered (see IT0). Set by the hardware when external interrupt is detected on INT0 pin.
0	IT0	**Interrupt 0 Type Control bit** Clear to select low level active (level triggered) for external interrupt 0 ($\overline{\text{INT0}}$). Set to select falling edge active (edge triggered) for external interrupt 0.

Reset Value = 0000 0000b

Table 56. TMOD Register

TMOD (S:89h) - Timer 0/Counter Mode Control Registers

7	6	5	4	3	2	1	0
GATE1	**C/T1#**	**M11**	**M01**	**GATE0**	**C/T0#**	**M10**	**M00**

Bit Number	Bit Mnemonic	Description
7	GATE1	**Timer 1 Gating Control bit** Clear to enable Timer 1 whenever TR1 bit is set. Set to enable Timer 1 only while $\overline{\text{INT1}}$ pin is high and TR1 bit is set.
6	C/T1#	**Timer 1 Counter/Timer 0 Select bit** Clear for Timer 0 operation: Timer 1 counts the divided-down system clock. Set for Counter operation: Timer 1 counts negative transitions on external pin T1.
5	M11	**Timer 1 Mode Select bits** M11 M01 Operating mode 0 0 Mode 0:8-bit Timer 0/Counter (TH1) with 5-bit prescaler (TL1). 0 1 Mode 1:16-bit Timer 0/Counter. 1 0 Mode 2:8-bit auto-reload Timer 0/Counter (TL1). Reloaded from TH1 at overflow. 1 1 Mode 3:Timer 1 halted. Retains count.
4	M01	
3	GATE0	**Timer 0 Gating Control bit** Clear to enable Timer 0 whenever TR0 bit is set. Set to enable Timer 0/Counter 0 only while $\overline{\text{INT0}}$ pin is high and TR0 bit is set.
2	C/T0#	**Timer 0 Counter/Timer 0 Select bit** Clear for Timer 0 operation: Timer 0 counts the divided-down system clock. Set for Counter operation: Timer 0 counts negative transitions on external pin T0.
1	M10	**Timer 0 Mode Select bit** M10 M00 Operating mode 0 0 Mode 0:8-bit Timer 0/Counter (TH0) with 5-bit prescaler (TL0). 0 1 Mode 1:16-bit Timer 0/Counter 1 0 Mode 2:8-bit auto-reload Timer 0/Counter (TL0). Reloaded from TH0 at overflow. 1 1 Mode 3:TL0 is an 8-bit Timer 0/Counter. TH0 is an 8-bit Timer 0 using Timer 1's TR0 and TF0 bits.
0	M00	

Reset Value = 0000 0000b

Table 57. TH0 Register

TH0 (S:8Ch) - Timer 0 High Byte Register.

7	6	5	4	3	2	1	0

Bit Number	Bit Mnemonic	Description
7:0		**High Byte of Timer 0**

Reset Value = 0000 0000b

Table 58. TL0 Register

TL0 (S:8Ah) - Timer 0 Low Byte Register.

7	6	5	4	3	2	1	0

Bit Number	Bit Mnemonic	Description
7:0		**Low Byte of Timer 0**

Reset Value = 0000 0000b

Table 59. TH1 Register

TH1 (S:8Dh) - Timer 1 High Byte Register.

7	6	5	4	3	2	1	0

Bit Number	Bit Mnemonic	Description
7:0		**High Byte of Timer 1**

Reset Value = 0000 0000b

Table 60. TL1 Register

TL1 (S:8Bh) - Timer 1 Low Byte Register.

7	6	5	4	3	2	1	0

Bit Number	Bit Mnemonic	Description
7:0		**Low Byte of Timer 1**

Reset Value = 0000 0000b

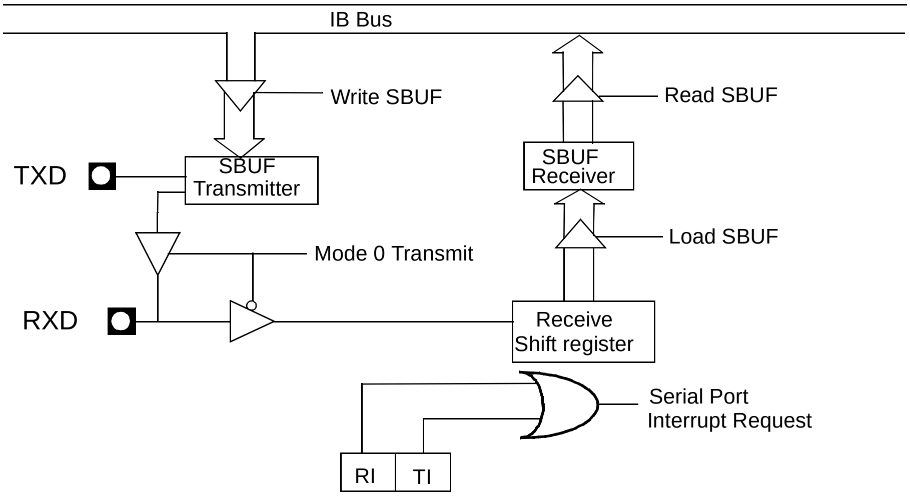
Serial I/O Port

The serial I/O port is entirely compatible with the serial I/O port in the 80C52.
It provides both synchronous and asynchronous communication modes. It operates as an Universal Asynchronous Receiver and Transmitter (UART) in three full-duplex modes (Modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates.

Serial I/O port includes the following enhancements:

- Framing error detection and Automatic Address Recognition
- Internal Baud Rate Generator

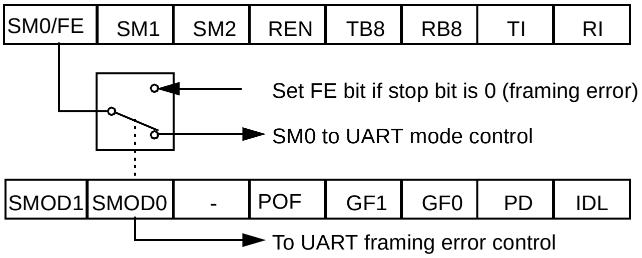
Figure 31. Serial I/O UART Port Block Diagram



Framing Error Detection

Framing bit error detection is provided for the three asynchronous modes. To enable the framing bit error detection feature, set SMOD0 bit in PCON register.

Figure 32. Framing Error Block Diagram



When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two CPUs. If a valid stop bit is not found, the Framing Error bit (FE) in SCON register bit is set.

Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 33 and Figure 34).

Figure 33. UART Timings in Mode 1

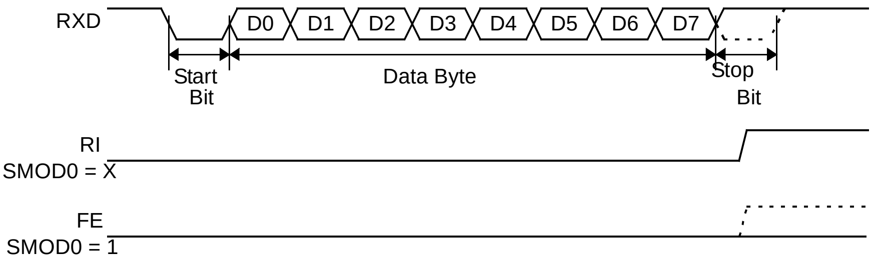
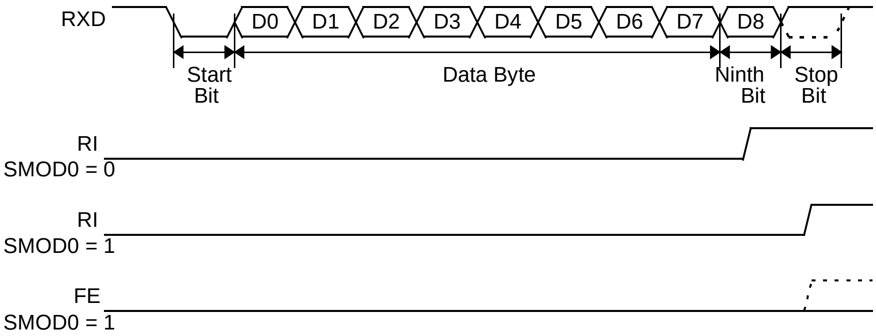


Figure 34. UART Timings in Modes 2 and 3



Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.

To support automatic address recognition, a device is identified by a given address and a broadcast address.

Note: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e., setting SM2 bit in SCON register in mode 0 has no effect).

Given Address

Each device has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don't care bits (defined by zeros) to form the device's given address. The don't care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed.

To address a device by its individual address, the SADEN mask byte must be `1111 1111b`.
For example:

SADDR0101 0110b
SADEN1111 1100b

Given0101 01XXb

The following is an example of how to use given addresses to address different slaves:

Slave A:SADDR1111 0001b
SADEN1111 1010b

Given1111 0X0Xb

Slave B:SADDR1111 0011b
SADEN1111 1001b

Given1111 0XX1b

Slave C:SADDR1111 0010b
SADEN1111 1101b

Given1111 00X1b

The SADEN byte is selected so that each slave may be addressed separately.
For slave A, bit 0 (the LSB) is a don't care bit; for slaves B and C, bit 0 is a 1. To communicate with slave A only, the master must send an address where bit 0 is clear (e.g. `1111 0000b`).
For slave A, bit 1 is a 0; for slaves B and C, bit 1 is a don't care bit. To communicate with slaves A and B, but not slave C, the master must send an address with bits 0 and 1 both set (e.g. `1111 0011b`).
To communicate with slaves A, B and C, the master must send an address with bit 0 set, bit 1 clear, and bit 2 clear (e.g. `1111 0001b`).

Broadcast Address

A broadcast address is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't care bits, e.g.:

SADDR0101 0110b
SADEN1111 1100b

SADDR OR SADEN1111 111Xb

The use of don't care bits provides flexibility in defining the broadcast address, however in most applications, a broadcast address is FFh. The following is an example of using broadcast addresses:

Slave A:SADDR1111 0001b
SADEN1111 1010b

Given1111 1X11b,

Slave B:SADDR1111 0011b
SADEN1111 1001b

Given1111 1X11B,

Slave C:SADDR = 1111 0010b
SADEN1111 1101b

Given1111 1111b

For slaves A and B, bit 2 is a don't care bit; for slave C, bit 2 is set. To communicate with all of the slaves, the master must send an address FFh. To communicate with slaves A and B, but not slave C, the master can send and address FBh.

Reset Addresses

On reset, the SADDR, SADEN register are initialized to 00h, i.e. the given and broadcast addresses are `XXXX XXXXb` (all don't care bits). This ensures that the serial port is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition.

UART Output Configuration

Voltage Level

The I/O Ports of UART are powered by the EV_{CC} Regulator. The voltage of this regulator can be:

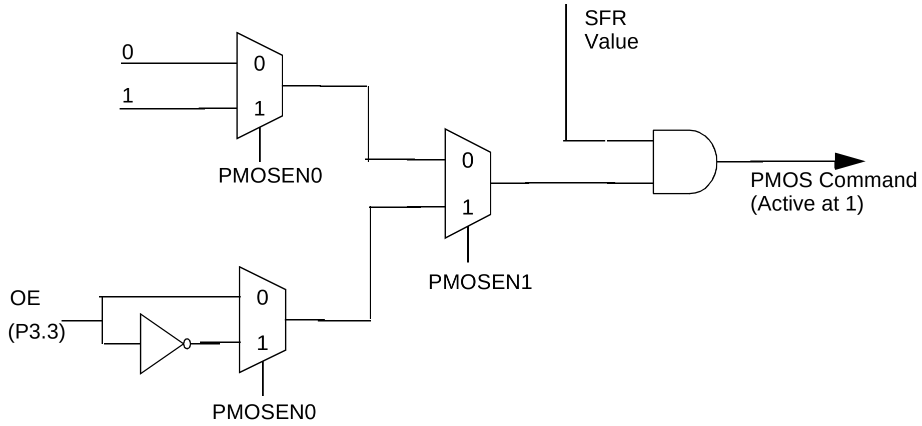
- Automatically controlled by the microcontroller which adapt the power supply level versus the OE input voltage level.
- Set at three defined levels (1.8V, 2.3V or 2.8V)

These configurations are defined with the EVAUTO and VEXT0,VEXT1 Bits of SIOCON Register.

Output Enable Function

The UART outputs (Tx, T0) can be controlled by the Output Enable input.

The Bits PMOSEN0 and PMOSEN1 in SIOCON Register are used to control this output.



UART Control Registers

Table 61. SADEN Register

SADEN
Slave Address Mask Register (B9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

Table 62. SADDR Register

SADDR
Slave Address Register (A9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

Table 63. SBUF Register

SBUF
Serial Buffer Register (99h)

7	6	5	4	3	2	1	0

Reset Value = XXXX XXXXb

UART Timings

The following description will be included in L version:

Mode Selection

SM0 and SM1 bits in SCON register (see Table 67) are used to select a mode among the single synchronous and the three asynchronous modes according to Table 64.

Table 64. Serial I/O Port Mode Selection

SM0	SM1	Mode	Description	Baud Rate
0	0	0	Synchronous Shift Register	Fixed / Variable
0	1	1	8-bit UART	Variable
1	0	2	9-bit UART	Fixed
1	1	3	9-bit UART	Variable

Baud Rate Generator

Depending on the mode and the source selection, the baud rate can be generated from either the Timer 1 or the Internal Baud Rate Generator. The Timer 1 can be used in Modes 1 and 3 while the Internal Baud Rate Generator can be used in Modes 0, 1 and 3.

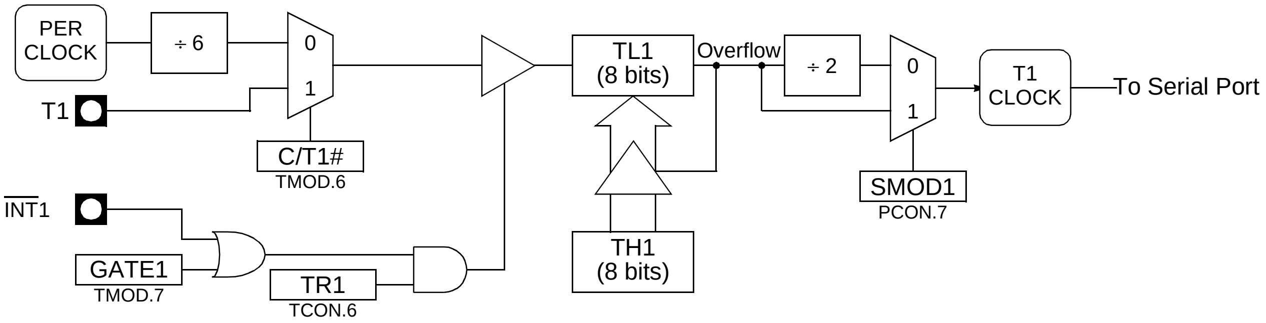
The addition of the Internal Baud Rate Generator allows freeing of the Timer 1 for other purposes in the application. It is highly recommended to use the Internal Baud Rate Generator as it allows higher and more accurate baud rates than with Timer 1.

Baud rate formulas depend on the modes selected and are given in the following mode sections.

Timer 1

When using the Timer 1, the Baud Rate is derived from the overflow of the timer. As shown in Figure 35 the Timer 1 is used in its 8-bit auto-reload mode (detailed in Section "Timer 0/Counter Operations", page 70). SMOD1 bit in PCON register allows doubling of the generated baud rate.

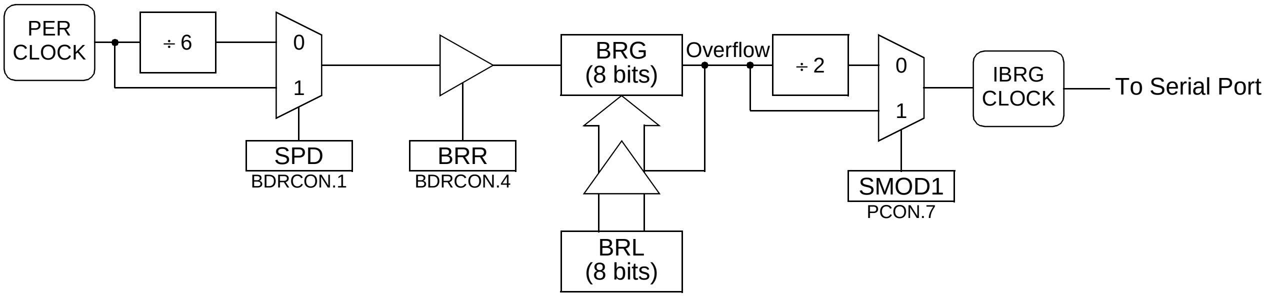
Figure 35. Timer 1 Baud Rate Generator Block Diagram



Internal Baud Rate Generator

When using the Internal Baud Rate Generator, the Baud Rate is derived from the overflow of the timer. As shown in Figure 36, the Internal Baud Rate Generator is an 8-bit auto-reload timer feed by the peripheral clock or by the peripheral clock divided by 6 depending on the SPD bit in BDRCON register (see Table 68). The Internal Baud Rate Generator is enabled by setting BBR bit in BDRCON register. SMOD1 bit in PCON register allows doubling of the generated baud rate.

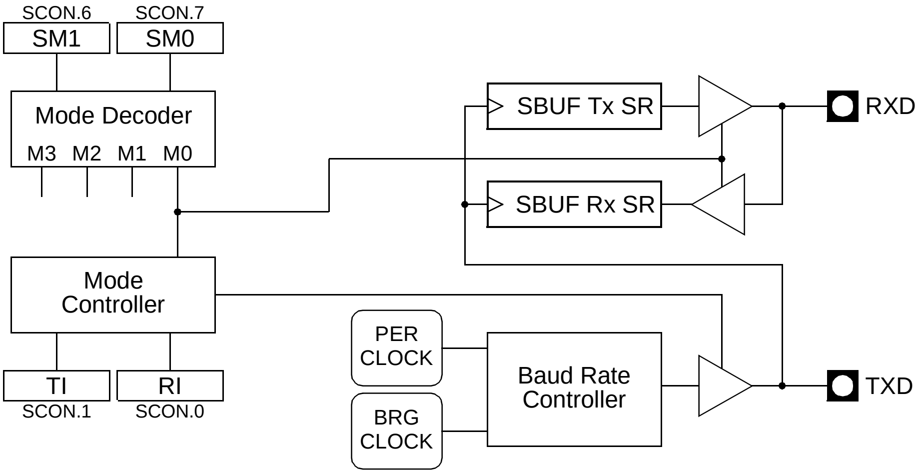
Figure 36. Internal Baud Rate Generator Block Diagram



Synchronous Mode (Mode 0)

Mode 0 is a half-duplex, synchronous mode, which is commonly used to expand the I/0 capabilities of a device with shift registers. The transmit data (TXD) pin outputs a set of eight clock pulses while the receive data (RXD) pin transmits or receives a byte of data. The 8-bit data are transmitted and received least-significant bit (LSB) first. Shifts occur at a fixed Baud Rate. Figure 37 shows the serial port block diagram in Mode 0.

Figure 37. Serial I/O Port Block Diagram (Mode 0)

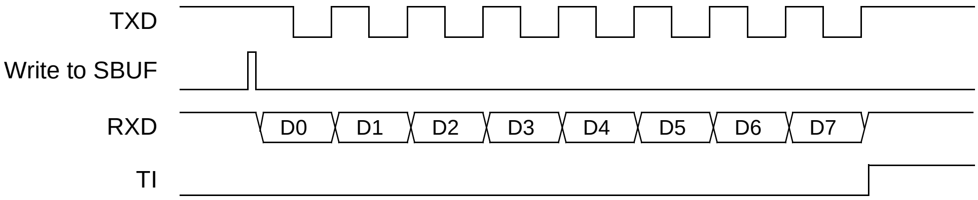


Transmission (Mode 0)

To start a transmission mode 0, write to SCON register clearing bits SM0, SM1.

As shown in Figure 38, writing the byte to transmit to SBUF register starts the transmission. Hardware shifts the LSB (D0) onto the RXD pin during the first clock cycle composed of a high level then low level signal on TXD. During the eighth clock cycle the MSB (D7) is on the RXD pin. Then, hardware drives the RXD pin high and asserts TI to indicate the end of the transmission.

Figure 38. Transmission Waveforms (Mode 0)

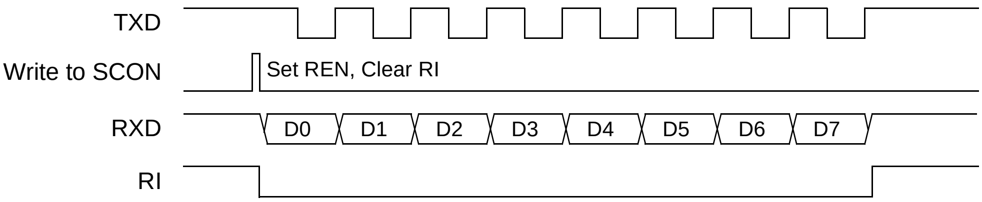


Reception (Mode 0)

To start a reception in mode 0, write to SCON register clearing SM0, SM1 and RI bits and setting the REN bit.

As shown in Figure 39, Clock is pulsed and the LSB (D0) is sampled on the RXD pin. The D0 bit is then shifted into the shift register. After eight sampling, the MSB (D7) is shifted into the shift register, and hardware asserts RI bit to indicate a completed reception. Software can then read the received byte from SBUF register.

Figure 39. Reception Waveforms (Mode 0)



Baud Rate Selection (Mode 0)

In mode 0, baud rate can be either fixed or variable.

As shown in Figure 40, the selection is done using M0SRC bit in BDRCON register. Figure 41 gives the baud rate calculation formulas for each baud rate source.

Figure 40. Baud Rate Source Selection (Mode 0)

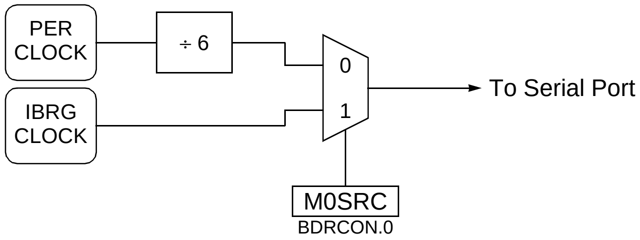


Figure 41. Baud Rate Formulas (Mode 0)

$$\text{Baud\_Rate} = \frac{F_{PER}}{6}$$

a. Fixed Formula

$$\text{Baud\_Rate} = \frac{2^{SMOD1} \cdot F_{PER}}{6^{(1-SPD)} \cdot 32 \cdot (256 - BRL)}$$

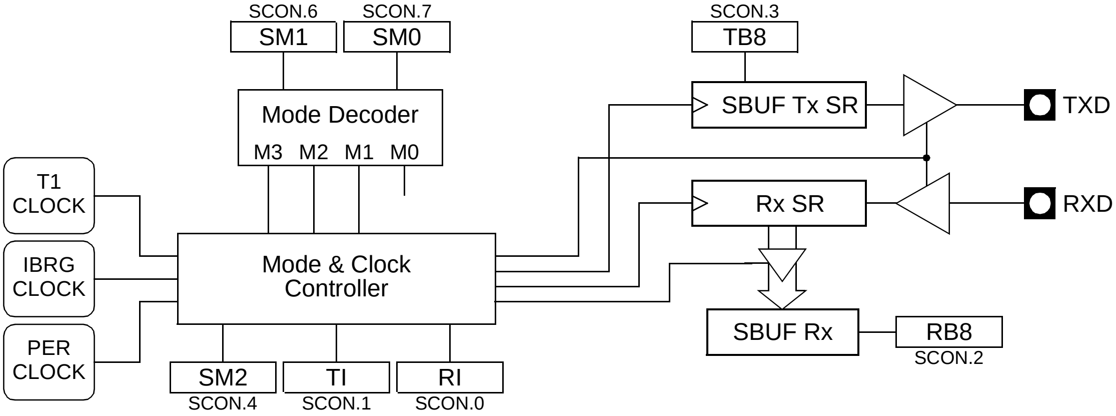
$$BRL = 256 - \frac{2^{SMOD1} \cdot F_{PER}}{6^{(1-SPD)} \cdot 32 \cdot \text{Baud\_Rate}}$$

b. Variable Formula

Asynchronous Modes (Modes 1, 2 and 3)

The Serial Port has one 8-bit and two 9-bit asynchronous modes of operation. Figure 42 shows the Serial Port block diagram in such asynchronous modes.

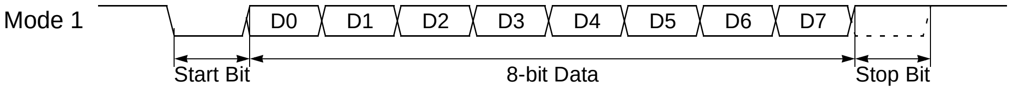
Figure 42. Serial I/O Port Block Diagram (Modes 1, 2 and 3)



Mode 1

Mode 1 is a full-duplex, asynchronous mode. The data frame (see Figure 43) consists of 10 bits: one start, eight data bits and one stop bit. Serial data is transmitted on the TXD pin and received on the RXD pin. When a data is received, the stop bit is read in the RB8 bit in SCON register.

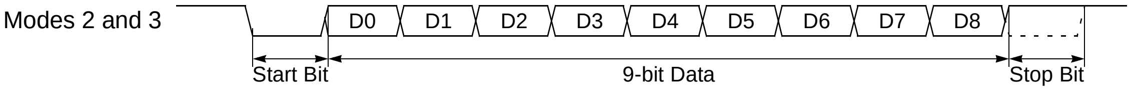
Figure 43. Data Frame Format (Mode 1)



Modes 2 and 3

Modes 2 and 3 are full-duplex, asynchronous modes. The data frame (see Figure 44) consists of 11 bits: one start bit, eight data bits (transmitted and received LSB first), one programmable ninth data bit and one stop bit. Serial data is transmitted on the TXD pin and received on the RXD pin. On receive, the ninth bit is read from RB8 bit in SCON register. On transmit, the ninth data bit is written to TB8 bit in SCON register. Alternatively, you can use the ninth bit as a command/data flag.

Figure 44. Data Frame Format (Modes 2 and 3)



Transmission (Modes 1, 2 and 3)

To initiate a transmission, write to SCON register, setting SM0 and SM1 bits according to Table 64, and setting the ninth bit by writing to TB8 bit. Then, writing the byte to be transmitted to SBUF register starts the transmission.

Reception (Modes 1, 2 and 3)

To prepare for a reception, write to SCON register, setting SM0 and SM1 bits according to Table 64, and setting REN bit. The actual reception is then initiated by a detected high-to-low transition on the RXD pin.

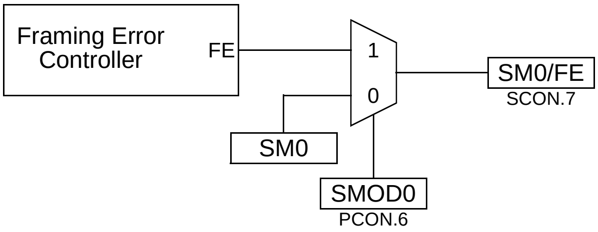
Framing Error Detection (Modes 1, 2 and 3)

Framing error detection is provided for the three asynchronous modes. To enable the framing bit error detection feature, set SMOD0 bit in PCON register as shown in Figure 45.

When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two devices. If a valid stop bit is not found, the software sets FE bit in SCON register.

Software may examine FE bit after each reception to check for data errors. Once set, only software or a chip reset clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When the framing error detection feature is enabled, RI rises on stop bit instead of the last data bit as detailed in Figure 35.

Figure 45. Framing Error Block Diagram



Baud Rate Selection (Modes 1 and 3)

In modes 1 and 3, the Baud Rate is derived either from the Timer 1 or the Internal Baud Rate Generator and allows different baud rate in reception and transmission.

As shown in Figure 46 the selection is done using RBCK and TBCK bits in BDRCON register.

Figure 47 gives the baud rate calculation formulas for each baud rate source while Table 65 details Internal Baud Rate Generator configuration for different peripheral clock frequencies and giving baud rates closer to the standard baud rates.

Figure 46. Baud Rate Source Selection (Modes 1 and 3)

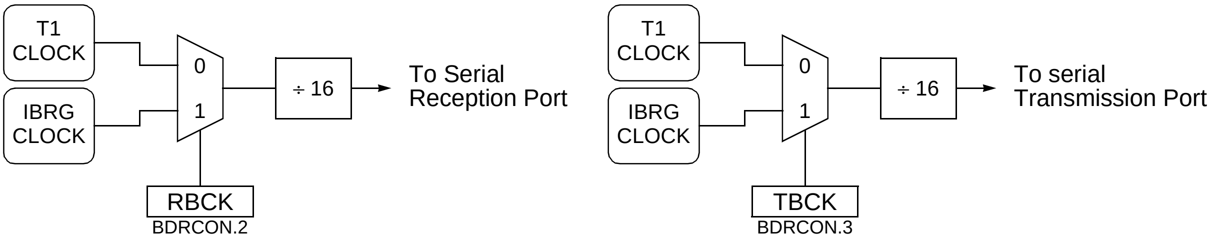


Figure 47. Baud Rate Formulas (Modes 1 and 3)

$$\mathrm{Baud\_Rate} = \frac{2^{\mathrm{SMOD1}} \cdot F_{\mathrm{PER}}}{6^{(1-\mathrm{SPD})} \cdot 32 \cdot (256 - \mathrm{BRL})}$$

$$\mathrm{BRL} = 256 - \frac{2^{\mathrm{SMOD1}} \cdot F_{\mathrm{PER}}}{6^{(1-\mathrm{SPD})} \cdot 32 \cdot \mathrm{Baud\_Rate}}$$

a. BRG Formula

$$\mathrm{Baud\_Rate} = \frac{2^{\mathrm{SMOD1}} \cdot F_{\mathrm{PER}}}{6 \cdot 32 \cdot (256 - \mathrm{TH1})}$$

$$\mathrm{TH1} = 256 - \frac{2^{\mathrm{SMOD1}} \cdot F_{\mathrm{PER}}}{192 \cdot \mathrm{Baud\_Rate}}$$

b. T1 Formula

Table 65. Internal Baud Rate Generator Value

	F_{PER} = 6 MHz[1]				F_{PER} = 8 MHz[1]			
Baud Rate	**SPD**	**SMOD1**	**BRL**	**Error %**	**SPD**	**SMOD1**	**BRL**	**Error %**
115200	-	-	-	-	-	-	-	-
57600	-	-	-	-	1	1	247	3.55
38400	1	1	246	2.34	1	1	243	0.16
19200	1	1	236	2.34	1	1	230	0.16
9600	1	1	217	0.16	1	1	204	0.16
4800	1	1	178	0.16	1	1	152	0.16

	F_{PER} = 12 MHz[2]				F_{PER} = 16 MHz[2]			
Baud Rate	**SPD**	**SMOD1**	**BRL**	**Error %**	**SPD**	**SMOD1**	**BRL**	**Error %**
115200	-	-	-	-	1	1	247	3.55
57600	1	1	243	0.16	1	1	239	2.12
38400	1	1	236	2.34	1	1	230	0.16
19200	1	1	217	0.16	1	1	204	0.16
9600	1	1	178	0.16	1	1	152	0.16
4800	1	1	100	0.16	1	1	48	0.16

Notes: 1. These frequencies are achieved in X1 mode, $F_{PER} = F_{OSC} \div 2$.

2. These frequencies are achieved in X2 mode, $F_{PER} = F_{OSC}$.

Baud Rate Selection (Mode 2)

In mode 2, the baud rate can only be programmed to two fixed values: 1/16 or 1/32 of the peripheral clock frequency.

As shown in Figure 48, the selection is done using SMOD1 bit in PCON register.

Figure 49 gives the baud rate calculation formula depending on the selection.

Figure 48. Baud Rate Generator Selection (Mode 2)

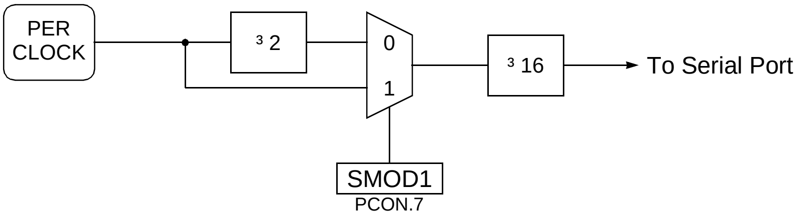


Figure 49. Baud Rate Formula (Mode 2)

$$\text{Baud\_Rate} = \frac{2SMOD1 \cdot FPER}{32}$$

Table 66. BRL (S:91h)
BRL Register
Baud Rate Generator Reload Register

7	6	5	4	3	2	1	0
BRL7	BRL6	BRL5	BRL4	BRL3	BRL2	BRL1	BRL0

Bit Number	Bit Mnemonic	Description
7 - 0	BRL7:0	Baud Rate Reload Value.

Reset Value = 0000 0000b

Table 67. SCON Register
SCON (S:98h)
Serial Control Registe

7	6	5	4	3	2	1	0
FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Bit Number	Bit Mnemonic	Description
7	FE	**Framing Error bit** To select this function, set SMOD0 bit in PCON register. Set by hardware to indicate an invalid stop bit. Must be cleared by software.
	SM0	**Serial Port Mode bit 0** To select this function, clear SMOD0 bit in PCON register. Software writes to bits SM0 and SM1 to select the Serial Port operating mode. Refer to SM1 bit for the mode selections.
6	SM1	**Serial Port Mode bit 1** To select this function, set SMOD0 bit in PCON register. Software writes to bits SM1 and SM0 to select the Serial Port operating mode. SM0 SM1 Mode Description Baud Rate 0 0 0 Shift Register $F_{OSC}/12$ or variable if SRC bit in BDRCON is set 0 1 1 8-bit UART Variable 1 0 2 9-bit UART $F_{OSC}/32$ or $F_{OSC}/64$ 1 1 3 9-bit UART Variable
5	SM2	**Serial Port Mode bit 2** Software writes to bit SM2 to enable and disable the multiprocessor communication and automatic address recognition features. This allows the Serial Port to differentiate between data and command frames and to recognize slave and broadcast addresses.
4	REN	**Receiver Enable bit** Clear to disable reception in mode 1, 2 and 3, and to enable transmission in mode 0. Set to enable reception in all modes.
3	TB8	**Transmit bit 8** Modes 0 and 1: Not used. Modes 2 and 3: Software writes the ninth data bit to be transmitted to TB8.
2	RB8	**Receiver bit 8** Mode 0: Not used. Mode 1 (SM2 cleared): Set or cleared by hardware to reflect the stop bit received. Modes 2 and 3 (SM2 set): Set or cleared by hardware to reflect the ninth bit received.
1	TI	**Transmit Interrupt flag** Set by the transmitter after the last data bit is transmitted. Must be cleared by software.
0	RI	**Receive Interrupt flag** Set by the receiver after the stop bit of a frame has been received. Must be cleared by software.

Reset Value = XXX0 0000b

Table 68. BDRCON Register

BDRCON
Baud Rate Control Register (9Bh)

7	6	5	4	3	2	1	0
-	-	-	BRR	TBCK	RBCK	SPD	SRC

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	BRR	**Baud Rate Run Control bit** Clear to stop the Baud Rate. Set to start the Baud Rate.
3	TBCK	**Transmission Baud rate Generator Selection bit for first UART** Clear to select Timer 1 for the Baud Rate Generator. Set to select internal Baud Rate Generator.
2	RBCK	**Reception Baud Rate Generator Selection bit for first UART** Clear to select Timer 1 for the Baud Rate Generator. Set to select internal Baud Rate Generator.
1	SPD	**Baud Rate Speed Control bit for first UART** Clear to select the SLOW Baud Rate Generator when SRC = 1. Set to select the FAST Baud Rate Generator when SRC = 1.
0	SRC	**Baud Rate Source select bit in Mode 0 for first UART** Clear to select $F_{OSC}/12$ as the Baud Rate Generator. Set to select the internal Baud Rate Generator.

Reset Value = XXX0 0000b

Table 69. SIOCON Register
Serial Input Output Configuration Register
Register (91h)

7	6	5	4	3	2	1	0
PMSOEN1	**PMSOEN0**	**-**	**-**	**CPRES RES**	**EVAUTO**	**VEXT0**	**VEXT1**

Bit Number	Bit Mnemonic	Description
7 - 6	PMOSEN1 PMOSEN0	**Output Enable function on Txd/P3.1 and T0/P3.4:** PMSOEN1 PMSOEN0 0 0 PMOS is always off (reset value) 0 1 PMOS is always driven according to P3.1 or P3.4 value 1 0 PMOS is driven only when OE is high 1 1 PMOS is driven only when OE is low
5 - 4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	CPRES RES	**Card Presence pull-up resistor** 0 Internal pull-up is connected 1 Internal pull-up is disconnected
2	EVAUTO	**EVCC Auto setup** Set to enable the Automatic mode of EV_{CC}regulator Clear to disable the Automatic mode of EV_{CC} regulator
1 - 0	VEXT0 VEXT1	**EVCC voltage configuration:** VEXT0 VEXT1 0 0 Power-down, EV_{CC} is external (reset value) 0 1 EV_{CC} = 1.8V 1 0 EV_{CC} = 2.3V 1 1 EV_{CC} = 2.7V

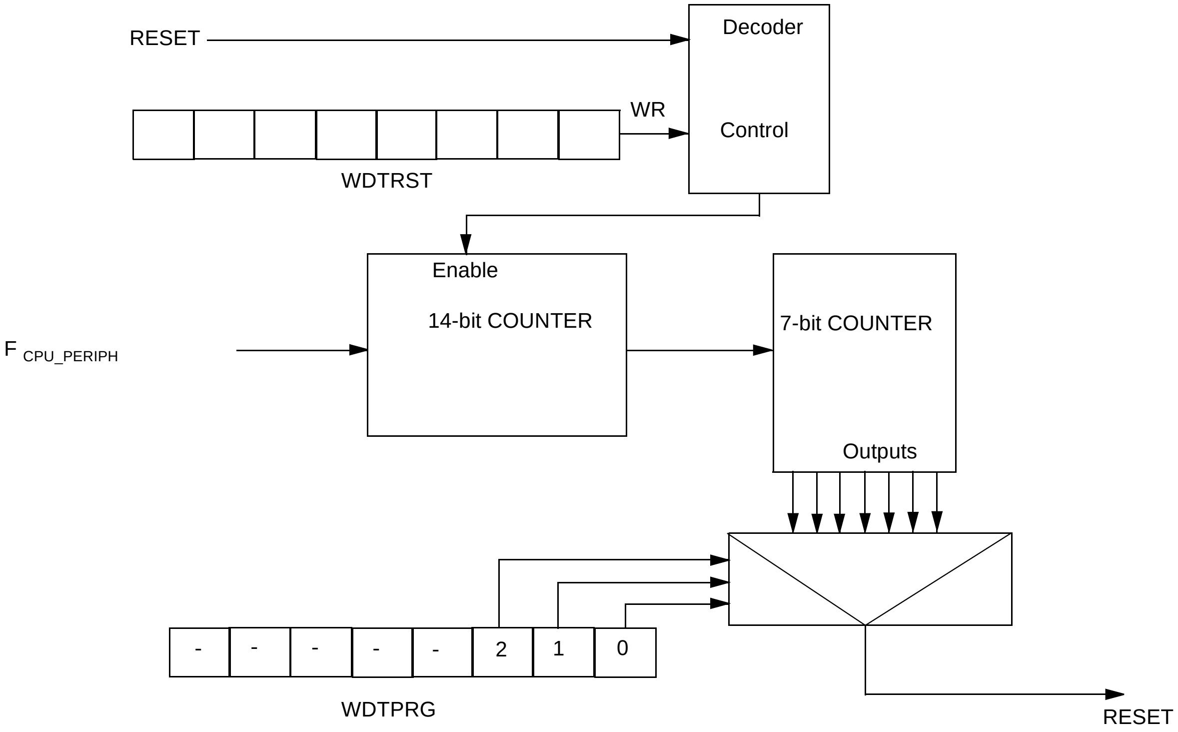
Reset Value = 00XX 0000b

Watchdog Timer

T8xC5121 contains a powerful programmable hardware Watchdog Timer (WDT) that automatically resets the chip if its software fails to reset the WDT before the selected time interval has elapsed. It permits large Timeout ranking from 16ms to 2s at F_{OSC} = 12 MHz.

This WDT consist of a 14-bit counter plus a 7-bit programmable counter, a Watchdog Timer reset register (WDTRST) and a Watchdog Timer programmation (WDTPRG) register. When exiting reset, the WDT is -by default- disable. To enable the WDT, the user has to write the sequence 1EH and E1H into WDRST register. When the Watchdog Timer is enabled, it will increment every machine cycle while the oscillator is running and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is $96xT_{OSC}$, where $T_{OSC} = 1/F_{OSC}$. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

Figure 50. Watchdog Timer



The WDT is controlled by two registers (WDTRST and WDTPRG).

Table 70. WDT Registers

7	6	5	4	3	2	1	0
-	-	-	-	-	S2	S1	S0

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	S2	**Watchdog Timer Duration selection bit 2** Work in conjunction with bit 1 and bit 0.
1	S1	**Watchdog Timer Duration selection bit 1** Work in conjunction with bit 2 and bit 0.
0	S0	**Watchdog Timer Duration selection bit 0** Work in conjunction with bit 1 and bit 2.

Reset Value = XXXX X000b
The three lower bits (S0, S1, S2) located into WDTPRG register permits to program the WDT duration.

Table 71. Machine Cycle Count

S2	S1	S0	Machine Cycle Count
0	0	0	$2^{14} - 1$
0	0	1	$2^{15} - 1$
0	1	0	$2^{16} - 1$
0	1	1	$2^{17} - 1$
1	0	0	$2^{18} - 1$
1	0	1	$2^{19} - 1$
1	1	0	$2^{20} - 1$
1	1	1	$2^{21} - 1$

To compute WD Timeout, the following formula is applied:

$$\text{Time Out} = 6 * (2^{14} * 2^{\text{Svalue}} - 1) / F_{CPU\_PERIPH}$$

Note: Svalue represents the decimal value of (S2 S1 S0)/CKRL represents the Prescaler.

The following describes computed Timeout value for F_{OSC} = 12 MHz

Table 72. Timeout Computation at 12 MHz

S2	S1	S0	Timeout for F_{OSC} = 12 MHz
0	0	0	16.38 ms
0	0	1	32.77 ms
0	1	0	65.54 ms
0	1	1	131.07 ms
1	0	0	262.14 ms
1	0	1	524.29 ms
1	1	0	1.05 s
1	1	1	2.10 s

Table 73. Watchdog Timer Enable Register

WDTRST - Watchdog Timer Enable register (Write Only) (A6h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-

Reset Value = XXXX XXXXb

The WDTRST register is used to reset/enable the WDT by writing 1EH then E1H in sequence.

Watchdog Timer during Power-down Mode and Idle

In Power-Down mode the oscillator stops, which means the WDT also stops. While in Power-Down mode the user does not need to service the WDT. There are 2 methods of exiting Power-Down mode: by a hardware reset or via a level activated external interrupt which is enabled prior to entering Power-Down mode. When Power-Down is exited with hardware reset, servicing the WDT should occur as it normally does whenever PAROS is reset. Exiting Power-Down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-Down.

To ensure that the WDT does not overflow within a few states of exiting of power-down, it is best to reset the WDT just before entering power-down.

In the Idle mode, the oscillator continues to run. To prevent the WDT from resetting while in Idle mode, the user should always set up a timer that will periodically exit Idle, service the WDT, and re-enter Idle mode.

Electrical Characteristics

Absolute Maximum Ratings

Ambiant Temperature Under Bias ....-25°C to 85°C

Storage Temperature .... -65°C to + 150°C

Voltage on V_{CC} to V_{SS}..-0.5V to + 6.0V

Voltage on Any Pin to V_{SS}.......................... -0.5V to V_{CC} + 0.5V

Note: Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

DC Parameters

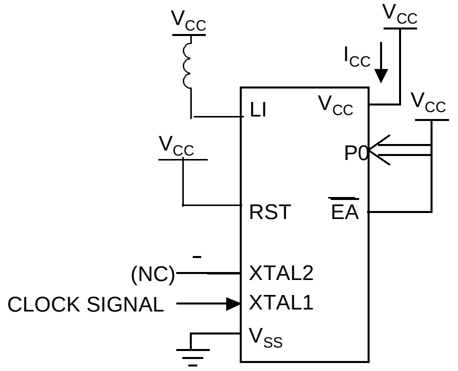
T_A = -40°C to +85°C; V_{SS} = 0 V; V_{CC} = 2.85V to 5.4V; F = 7.36 to 16 MHz

Table 74. Core DC Parameters (XTAL, $\overline{RST}$, P0, P2, ALE, $\overline{PSEN}$, $\overline{EA}$)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5		0.2 V_{CC} - 0.1	V	
V_{IH}	Input High Voltage except XTAL1, $\overline{RST}$	.2 V_{CC} + .9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage, XTAL1, $\overline{RST}$	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage, Port 0 and 2			0.45	V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage, Port 0 and 2	0.9 x V_{CC}			V	I_{OH} = -40 µA
DI_{CC}	Digital Supply Output Current		6	10	mA	C_L = 100 nF
DV_{CC}	Digital Supply Voltage	2.65	2 .9	3.0	V	C_L = 100 nF DIcc=10mA
Icc	Normal Power Down mode		80	100	µA	25°C
Icc	Pulsed Power Down mode		20	30	µA	50°C Vcc=3V
Iccop	Power Supply current	I_{ccop} = 0.25 Freq (MHz) +4 mA I_{ccIDLE} = 0.03 Freq (MHz) +5 mA				V_{CC} = 5.4V and Bootloader execution
V_{PFDP}	Power-fail high level threshold		2 .55		V	
V_{PFDM}	Power-fail low level threshold		2 .45		V	
t_G	Power Fail glitch time			50	ns	
t_{rise}, t_{fall}	V_{DD} rise and fall time	1 µs		600	sec.	

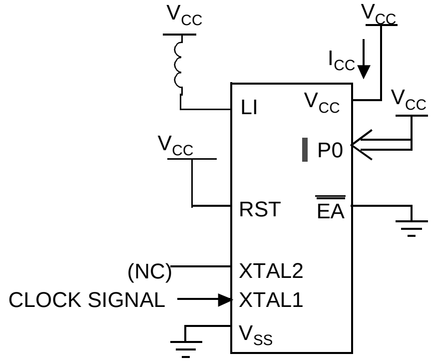
The operating conditions for I_{CC} Tests are the following:

Figure 51. **I_{CC} Test Condition, Active Mode**



PLCC52 configuration
All other pins are disconnected.

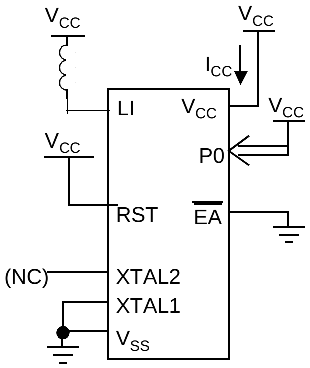
Figure 52. I_{CC} Test Condition, Idle Mode



PLCC52 configuration

All other pins are disconnected.

Figure 53. I_{CC} Test Condition, Power-down Mode



PLCC52 configuration

All other pins are disconnected.

Table 75. Serial Interface DC parameters (P3.0, P3.1, P3.3 and P3.4)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5		0.4	V	EV_{CC} = 1.8V
		-0.5		0.5	V	EV_{CC} = 2.3V
		-0.5		0.5	V	EV_{CC} = 2.8V
						External EVcc
						Automatic EVcc
V_{IH}	Input High Voltage	1.4		2.3	V	EV_{CC} = 1.8V
		1.6		2.8	V	EV_{CC} = 2.3V
		2.0		3.3	V	EV_{CC} = 2.8V
		0.7 x EV_{CC}	EV_{CC}	EV_{CC} + 0.5	V	External EV_{CC}
						Automatic EVcc
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 1.2 mA
V_{OH}	Output High Voltage	1.6		1.8	V	EV_{CC} = 1.8V I_{OH} = 1 µA
		1.8		2.3	V	EV_{CC} = 2.3V
		2.2		2.7	V	EV_{CC} = 2.8V I_{OH} = 10µA
		0.8 x EV_{CC}		EV_{CC}	V	External EV_{CC}
EI_{CC}	Extra Supply Current			+3	mA	C_L = 100 nF
EV_{CC}	Extra Supply Voltage	1.6	1.7	1.8	V	C_L = 100 nF, 1.8V
		2.1	2.2	2.3	V	C_L = 100 nF, 2.3V
		2.6	2.7	2.8	V	C_L = 100 nF, 2.8V
		1.6		V_{CC}	V	External EV_{CC}
						Automatic EVcc
Ts	Sampling time					Automatic EVcc

Table 76. LED outputs DC Parameters (P3.6 and P3.7)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{OL}	Output Low Current, P3.6 and P3.7 LED modes	1	2	4	mA	2 mA configuration
		2	4	8	mA	4 mA configuration
		5	10	20	mA	10 mA configuration
						(T_A = -20°C to +50°C, V_{CC} - V_{OL} = 2V ± 20%)

Table 77. Smart Card 5V Interface DC Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
CI_{CC}	Card Supply Current	60		121 105 102	mA	V_{CC} = 5.4V V_{CC} = 4V V_{CC} = 2.85V
CV_{CC}	Card Supply Voltage	4.6		5.4	V	CIcc = 60 mA
CV_{CC}	Ripple on CVcc			200	mV	0<CIcc<60 mA
CV_{CC}	Spikes on CVcc	4.6		5.4	V	Maxi. charge 20 nA.s Max. duration 400 ns Max. variation CIcc 100 mA (1)
T_{VHLI}	CVcc to 0			750	µs	CIcc = 0 CVcc = 5V to 0.4V (1)

Note: 1. Capacitor = 10 µF, X7R type. Maximum ESR value is 250 mohm, Inductor = 4.7 µH.

Table 78. Smart Card 3V Interface DC Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
CI_{CC}	Card Supply Current	60		110 89 110	mA	V_{CC} = 5.4V V_{CC} = 4V V_{CC} = 2.85V
CV_{CC}	Card Supply Voltage	2.76		3.24	V	CIcc = 60 mA
CV_{CC}	Ripple on CVcc			200	mV	0<CIcc<60 mA
CV_{CC}	Spikes on CVcc	2.76		3.24	V	Max. charge 10 ns Max. duration 400 ns Max. variation CIcc 50 mA
T_{VHLI}	CVcc to 0			750	µs	CIcc = 0 CVcc = 5V to 0.4V (1)

Note: 1. Capacitor = 10 µF, X7R type. Maximum ESR value is 250 mohm, Inductor = 4.7 µH.

Table 79. Smart Card 1.8V Interface DC Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
CI_{CC}	Card Supply Current	20		109 100 82	mA	V_{CC} = 5.4V V_{CC} = 4V V_{CC} = 2.85V
CV_{CC}	Card Supply Voltage	1.68		1.92	V	CIcc = 20 mA
CV_{CC}	Spikes on CVcc	1.68		1.92	V	
T_{VHLI}	CVcc to 0			750	µs	CIcc = 0 CVcc = 5V to 0.4V (1)

Note: 1. Capacitor = 10 µF, X7R type. Maximum ESR value is 250 mohm, Inductor = 4.7 µH.

Table 80. Smart Card Clock DC Parameters (Port P1.4)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL}	Output Low Voltage	0(1) 0(1)		0.2 x CV_{CC} 0.4	V	I_{OL} = 20 µA (1.8,3 V) I_{OL} = 50 µA (5V)
I_{OL}	Output Low Current			15	mA	
V_{OH}	Output High Voltage	0.7 x CV_{CC} 0.7 x CV_{CC} CV_{CC} - 0.5		CV_{CC} CV_{CC} CV_{CC}	V V V	I_{OH} = 20 µA (1.8V) I_{OH} = 20 µA (3V) I_{OH} = 50 µA (5V)
I_{OH}	Output High Current			15	mA	
t_R t_F	Rise and Fall time			16 22.5 50	ns	C_{IN} = 30 pF(5V) C_{IN} = 30 pF(3V) C_{IN} = 30 pF(1.8V)
	Voltage Stability	-0.25 CV_{CC}-0.5		0.4 x CV_{CC} CV_{CC} + 0.25	V	Low level High level

Note: 1. The voltage on CLK should remain between -0.3V and CV_{CC} + 0.3V during dynamic operation.

Table 81. Alternate Card Clock DC parameters (Port P3.6)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL}	Output Low Voltage	0 (1) 0(1)		0.2 x DV_{CC} 0.5	V	I_{OL} = 20 µA I_{OL} = -200 µA
V_{OH}	Output High Voltage	0.7 x DV_{CC}		DV_{CC} (1)	V	I_{OH} = 20 µA
t_R t_F	Rise and Fall times			18	ns	C_{IN} = 30 pF

Note: 1. The voltage on CLK should remain between -0.3V and V_{CC} + 0.3V during dynamic operation.

Table 82. Smart Card I/O DC Parameters (P1.0)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	0(1) 0(1)		0.5 0.15 x CV_{CC}	V	I_{IL} = 500 µA I_{IL} = 20 µA
I_{IL}	Input Low Current			500	µA	
V_{IH}	Input High Voltage	0.7 x CV_{CC}		CV_{CC}	V	I_{IH} = -20 µA
I_{IH}	Input High Current			-20 / +20	µA	
V_{OL}	Output Low Voltage	0(1)		0.4 0.4 0.3	V	I_{OL} = 1µA (5V) I_{OL} = 1 mA (3V) I_{OL} = 1 mA (1.8V)
I_{OL}	Output Low Current			15	mA	
V_{OH}	Output High Voltage	0.8 x CV_{CC}		CV_{CC} (1)	V	I_{OH} = 20 µA (5V,3V,1.8V)
I_{OH}	Output High Current			15	mA	
t_R t_F	Rise and Fall times			0.8	µs	C_{IN} = 30 pF Output

Note: 1. The voltage on RST should remain between -0.3V and CV_{CC} + 0.3V during dynamic operation.

Table 83. Alternate Card I/O DC Parameters (P3.5)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.3		0.2 x DV_{CC}	V	I_{IL} = 1 mA
V_{IH}	Input High Voltage	0.7 x DV_{CC}		DV_{CC} + 0.3	V	I_{IH} = -20 µA
V_{OL}	Output Low Voltage	0(1)		0.3	V	I_{OL} = 1000 µA
V_{OH}	Output High Voltage	0.7 x DV_{CC}		DV_{CC} (1)	V	I_{OH} = 20 µA
t_R t_F	Rise and Fall delays			1	µs	C_{IN} = 30 pF

Note: 1. The voltage on I/O should remain between -0.3V and DV_{CC} + 0.3V during dynamic operation.

Table 84. Smart Card RST, CC4, CC8, DC Parameters (Port P1.5, P1.3, P1.1)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL}	Output Low Voltage	0(1) 0(1)		0.12 x CV_{CC} 0.4	V	I_{OL} = 20 µA I_{OL} = 50 µA
I_{OL}	Output Low Current			15	mA	
V_{OH}	Output High Voltage	CV_{CC} - 0.5 0.8 x CV_{CC}		CV_{CC} CV_{CC} (1)	V	I_{OH} = 50 µA I_{OH} = 20 µA
I_{OH}	Output High Current			15	mA	
t_R t_F	Rise and Fall delays			0.8	µs	C_{IN} = 30 pF
	Voltage stability	-0.25 CV_{CC}-0.5		0.4 x CV_{CC} CV_{CC} + 0.25		Low level High level

Note: 1. The voltage on RST should remain between -0.3V and CV_{CC} + 0.3V during dynamic operation.

Table 85. Alternate Card RST DC Parameters (Port P3.7)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL}	Output Low Voltage	0 (1)		0.2 x DV_{CC}	V	I_{OL} = 200 µA
V_{OH}	Output High Voltage	0.8 x DV_{CC} 0.8 x DV_{CC}		DV_{CC} (1) DV_{CC}	V	I_{OH} = 20 µA (1.8V) I_{OH} = 200 µA (3V)
t_R t_F	Rise and Fall delays			400	µs	C_{IN} = 30 pF

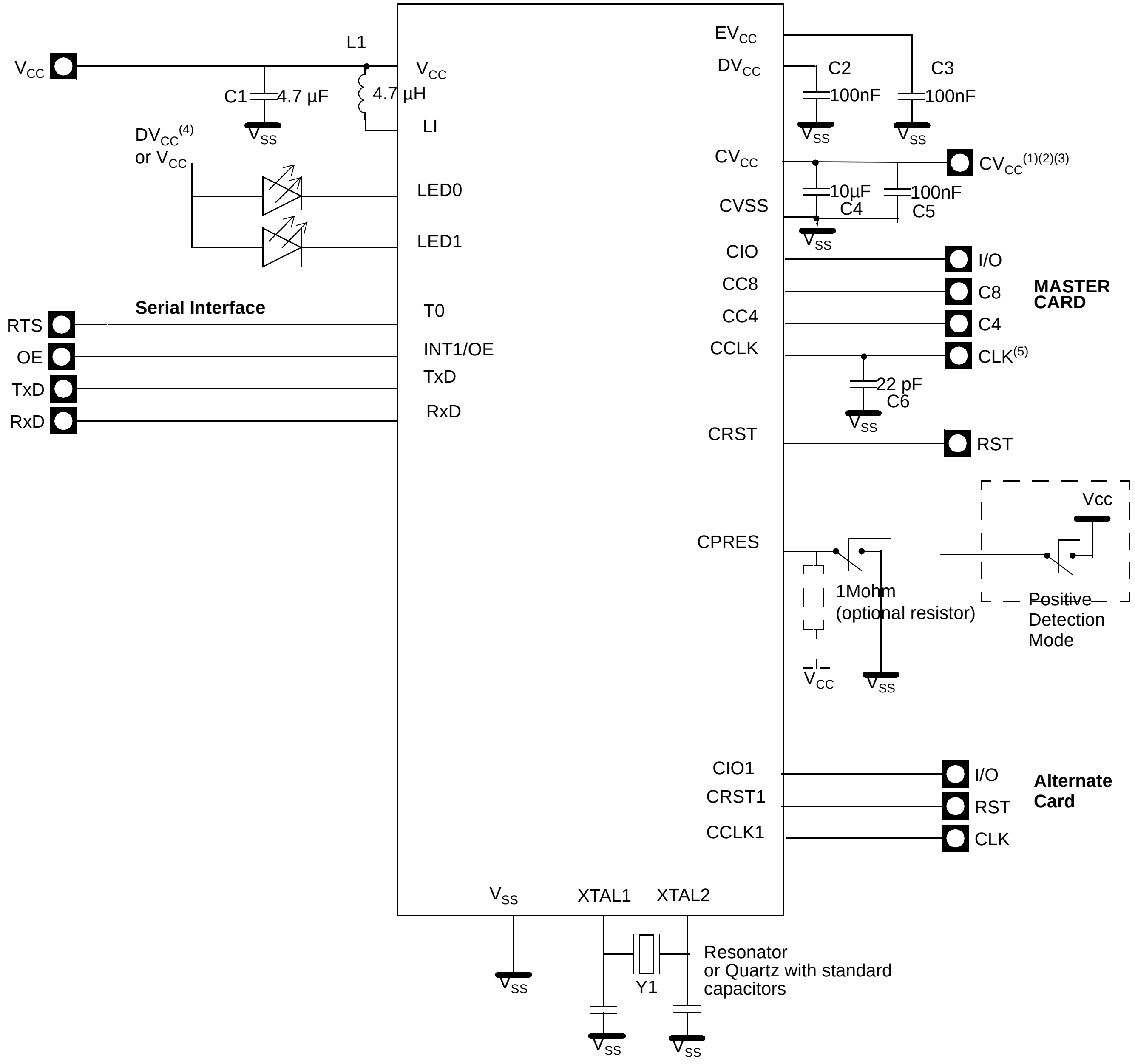
Note: 1. The voltage on RST should remain between -0.3V and DV_{CC} + 0.3V during dynamic operation.

Table 86. Card Presence DC Parameters (P1.2)

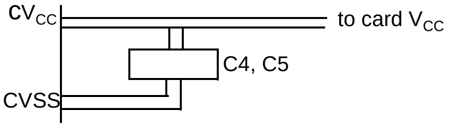
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{OL1}	CPRES weak pull-up output current	3	10	25	µA	P1.2 = 1, short to V_{SS} (internal pull-up enabled)

Typical Application

Figure 54. Typical Application Diagram



Notes:
1. C4 and C5 must be placed near IC and have low ESR (<250mΩ)
2. Straight and short connections avoid any loop between:
   - CVSS and V_{SS}
   - CV_{CC} and C4, C5
3. V_{CC} connection of the master card must be placed as follows:



4. Current is limited to 10 mA.
5. CCLK should be routed far from CRST, CIO, CC4, CC8 and surrounded with ground tracks.

Ordering Information

Part Number	Code Memory Size (Bytes)	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
T83C5121xxx-ICSIL	16K ROM	2.85 - 5.4V	Industrial	16 MHz	SSOP24	Stick
T83C5121xxx-ICRIL	16K ROM	2.85 - 5.4V	Industrial	16 MHz	SSOP24	Tape & Reel
T83C5121xxx-S3SIL	16K ROM	2.85 - 5.4V	Industrial	16 MHz	PLCC52(1)	Stick
T83C5121xxx-S3RIL	16K ROM	2.85 - 5.4V	Industrial	16 MHz	PLCC52(1)	Tape & Reel
T85C5121-ICSIL	16K RAM	2.85 - 5.4V	Industrial	16 MHz	SSOP24	Stick
T85C5121-ICRIL	16K RAM	2.85 - 5.4V	Industrial	16 MHz	SSOP24	Tape & Reel
T85C5121-S3SIL	16K RAM	2.85 - 5.4V	Industrial	16 MHz	PLCC52	Stick
T85C5121-S3RIL	16K RAM	2.85 - 5.4V	Industrial	16 MHz	PLCC52	Tape & Reel
T89C5121-ICSIL	16K Flash RAM	2.85 - 5.4V	Industrial	16 MHz	SSOP24	Stick
T89C5121-ICRIL	16K Flash RAM	2.85 - 5.4V	Industrial	16 MHz	SSOP24	Tape & Reel

Note: 1. Contact Atmel for availability.

Datasheet Change Log for T8xC5121

Changes from 4164B - 06/02 to 4164C - 07/03

1. Ports description update.
2. Added Bootloader Autobaud table.
3. Modified I_{CC} test conditions Figure 51.
4. Added I_{CCOP} power supply current characteristics.
5. Added I_{CCO} pulsed power down mode current characteristics.
6. Modified Smart card characteristics : V_{CC}/CV_{CC} mixed.

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