

R2021
Brief Sheet
FAST ETHERNET RISC PROCESSOR

1. Features

I CPU Core

- RDC's proprietary RISC architecture
- Five-stage pipeline
- Operation frequency: 125 MHz
- Supports an 8K-byte Uniform cache
- Supports CPU ID
- Supports 40 PIO pins

I Bus Interface

- Supports non-multiplexed address bus A[21:0]
- With 8-bit or 16-bit Boot ROM bus size
- 8-bit or 16-bit external bus dynamic access
- Supports an independent data/address bus for external I/O device

I PCMCIA Bus Interface

- Supports a glueless and simplified 16-bit PCMCIA bus interface

I ROM/RAM/SDRAM Controller and Addressing Space

- Supports 16-bit data bus [15:0]
- 16M-byte memory address space Address[23:0]
- SDRAM control Interface
- 64K-byte I/O space

I Compatible UART Channels

- Supports two compatible UART serial channels with 16-byte FIFO and hardware flow-control

I Two Independent DMA Channels

I Fast Ethernet MAC Ports

- 2-Port Fast Ethernet MAC with MII interface
- The MAC packet buffer is cacheble with snooping function

I Interrupt Controller

- The Interrupt controller with five maskable external interrupts and one non-maskable external interrupt

I Programmable Chip-select Logic

- Programmable chip-select logic for Memory or I/O bus cycle decoder

I Programmable wait-state generator

I Counter/Timers

- Three independent 16-bit timers and one independent programmable watchdog timer

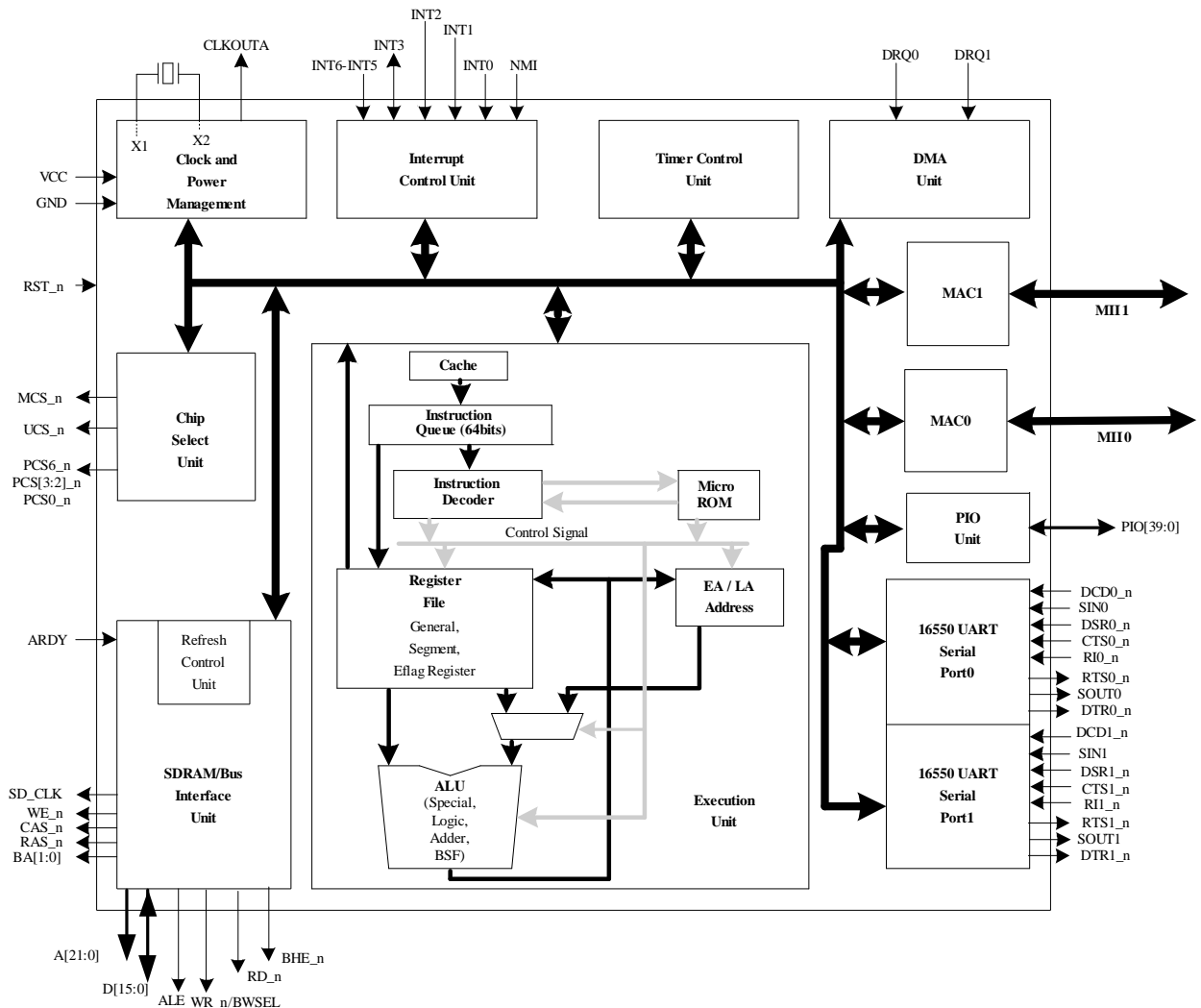
I Operating Voltage Range

- Core voltage: 2.5V \pm 5%
- I/O voltage: 3.3V \pm 10%

I Package Type

128-pin PQFP

2. Block Diagram



3. Package Information

PQFP 128 pins

