

# M62421SP/FP

# Tone and Volume Controller with 2 Line Control

REJ03F0208-0201 Rev.2.01 Mar 31, 2008

#### **Outline**

M62421SP/FP is the tone and volume controller with 2 line control.

This IC can apply the broad application because of low noise and distortion.

#### **Feature**

- Tone (Bass/Treble) control and 1 dB step volume control are enabled.
- Low noise and low distortion.  $V_{NO} = 4.5 \mu Vrms$ , THD = 0.1% max
- Controlling by 2 Line serial data.

#### **Application**

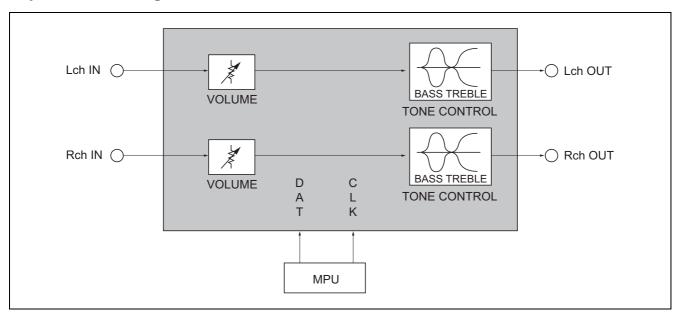
• Mini-Stereo, etc

#### **Recommended Operating Condition**

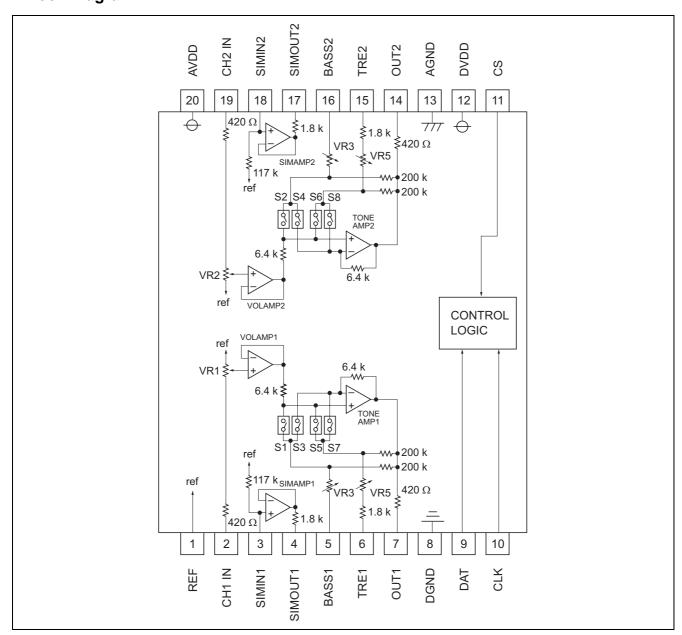
Supply voltage range:  $5.5 \sim 9.5 \text{ V}$  (analog),  $4.5 \sim 5.5 \text{ V}$  (digital)

Rated supply voltage: 9 V (analog), 5 V (digital)

#### **System Block Diagram**



### **Block Diagram**

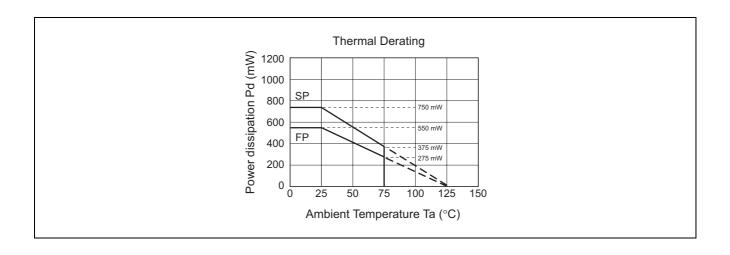


# **Pin Description**

Pin No.	Pin Name	I/O	Description
1	REF	I	Reference voltage terminal for analog
2	CH1 IN	I	Input terminal (ch1)
3	SIMIN1	I	Pin for capacitor of simulated inductor 1
4	SIMOUT1	0	Pin for capacitor of simulated inductor 1
5	BASS1	1	Pin for capacitor of ch1-side bass setting
6	TRE1	I	Pin for capacitor of ch1-side treble setting
7	OUT1	0	Output terminal (ch1)
8	DGND	_	Digital GND
9	DAT	1	I/O terminal of DATA 2 line bus format
10	CLK	1	Input terminal of CLOCK 2 line bus format
11	CS	1	Chip select terminal
12	DVDD		VDD for digital circuit
13	AGND	_	GND for analog circuit
14	OUT2	0	Output terminal (ch2)
15	TRE2	1	Pin for capacitor of ch2-side treble setting
16	BASS2	1	Pin for capacitor of ch2-side bass setting
17	SIMOUT2	0	Pin for capacitor of simulated inductor 2
18	SIMIN2	1	Pin for capacitor of simulated inductor 2
19	CH2 IN	1	Input terminal (ch2)
20	AVDD	_	V <sub>CC</sub> for analog circuit

# **Absolute Maximum Ratings**

Item	Symbol	Limits	Unit	Condition
Analog supply voltage	AVdd	10.0	V	
Digital supply voltage	DVdd	7.0	V	
Power dissipation	Pd	750 (SP)	mW	Ta ≤ 25°C
		550 (FP)		
Thermal derating ratio	Кθ	7.5 (SP)	mW/°C	Ta > 25°C
		5.5 (FP)		
Operating temperature	Topr	<b>−</b> 20 ~ <b>+</b> 75	°C	
Storage temperature	Tstg	<b>−40 ~ +125</b>	°C	



# **Recommended Operating Condition**

 $(Ta = 25^{\circ}C \text{ unless otherwise noted})$ 

Item	Symbol	Min	Тур	Max	Unit
Analog supply voltage	AVDD	5.5	9.0	9.5	V
Digital supply voltage	DVDD	4.5	5.0	5.5	V
H level input voltage (logic circuit)	VIH	0.7 DVDD	_	VDD	V
L level input voltage (logic circuit)	VIL	0	_	0.3 DVDD	V

### **Electric Characteristics**

(Ta = 25°C, AVdd = 9 V, DVdd = 5 V and bass and treble = 0 dB unless otherwise noted)

### (1) Supply Voltage

			Limit			
Item	Symbol	Min	Тур	Max	Unit	Condition
Analog supply current	Icc	_	10	20	mA	• AVdd = 9.0 V
						<ul> <li>measure terminal = 20 pin</li> </ul>
						no signal input
Digital supply current	ldd	_	0	2	μΑ	• DVdd = 5 V
						measure terminal = 12 pin
						no signal input

### (2) I/O Characteristics

			Limit			
Item	Symbol	Min	Тур	Max	Unit	Condition
Maximum input voltage	VIM	2.0	3.2	_	Vrms	2, 19 pin input
						7, 14 pin output
						RL = 10 k $\Omega$ , THD = 1%, f = 1 kHz
						ATT = -6 dB
Output voltage	Vodc	4.35	4.5	4.65	V	7 pin, 14 pin, no signal
Gain	Gv	-2	0	2	dB	Vin = 0 dBm, FLAT, f = 1 kHz
						2 ~ 7 pin, 19 ~ 14 pin gain
Output noise voltage	Vono	_	4.5	10	μVrms	IHF-A filter
						no signal
						Rg = 10 kΩ 7, 14 pin
Total harmonic distortion	THD	_	0.007	0.1	%	7 pin, 14 pin f = 1 kHz
						Vo = 0.5 Vrms, $RL = 10 kΩ$
						LPF = 30 kHz
Channel separation	СТ	_	-100	-70	dB	$RL = 10 \text{ k}\Omega$
						S: Vin = 1 Vrms, f = 1 kHz
						M: Rg = 10 kΩ, IHF-A filter

### (3) Tone Characteristics

		Limit				
Item	Symbol	Min	Тур	Max	Unit	Condition
Tone control gain (bass)	Gbassb	9	12	15	dB	f = 100 Hz
	Gbassc	-15	-12	-9	dB	
Tone control gain (treble)	Gtrebb	9	12	15	dB	f = 10 kHz
	Gtrebc	-15	-12	-9	dB	

### (4) Volume Characteristics

		Limit				
Item	Symbol	Min	Тур	Max	Unit	Condition
Maximum attenuation	ATTmax	-108	-100	-80	dB	f = 1 kHz, Vin = 0 dBm
Minimum attenuation	ATTmin	-1.5	0	1.5	dB	2 pin ~ 7 pin
						19 pin ~ 14 pin gain
						IHF-A-filter

# **Function Explanation**

#### **Equivalent Circuit of Tone Control**

The resonance circuit is able to construct by using built-in amplifier for simulated inductor. (Shows the constant as follow)

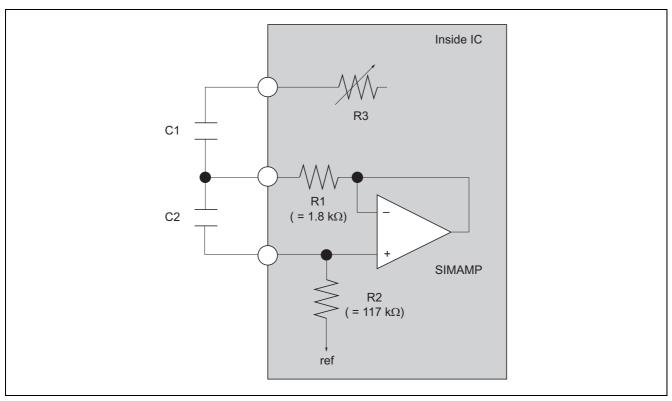


Figure 1 The circuit used simulated inductor

Center frequency:

f0 = 1 / 
$$2\pi$$
  $\sqrt{C1 \cdot C2 \cdot R1 \cdot R2 \text{ [Hz]}}$   
Q =  $\sqrt{(C2 \cdot R2) / (C1 \cdot R1)}$ 

Example: BASS band ( $f \approx 100 \text{ Hz}$ )

$$R1 = 1.8 \text{ k}\Omega, R2 = 117 \text{ k}\Omega$$

$$C1 = 0.47 \mu$$
,  $C2 = 0.022 \mu$ 

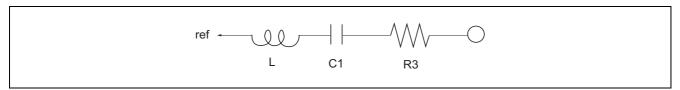
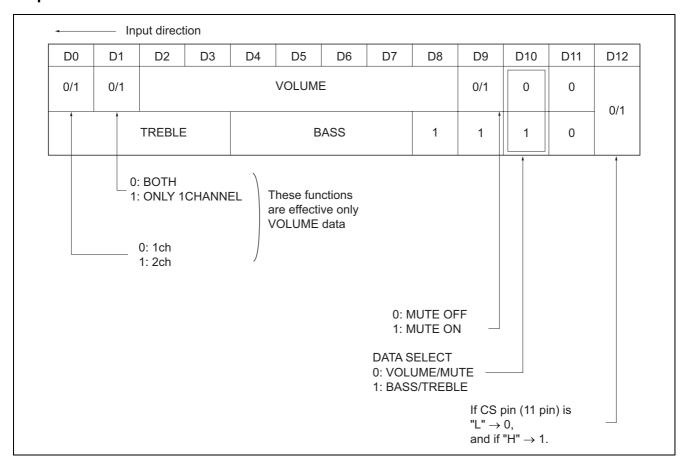


Figure 2 The equivalent circuit used L

Figure 1 is equal to figure 2.

The following relation is concluded.

# **Input Data Format**



#### **Volume Control**

#### **Volume Code**

ATT	D2	D3	D4	D5	D6
0 dB	Н	L	Н	L	Н
–4 dB	L	L	Н	L	Н
–8 dB	Н	Н	L	L	Н
–12 dB	L	Н	L	L	Н
–16 dB	Н	L	L	L	Н
–20 dB	L	L	L	L	Н
–24 dB	Н	Н	Н	Н	L
–28 dB	L	Н	Н	Н	L
–32 dB	Н	L	Н	Н	L
–36 dB	L	L	Н	Н	L
–40 dB	Н	Н	L	Н	L
–44 dB	L	Н	L	Н	L
–48 dB	Н	L	L	Н	L
–52 dB	L	L	L	Н	L
–56 dB	Н	Н	Н	L	L
–60 dB	L	Н	Н	L	L
−64 dB	Н	L	Н	L	L
–68 dB	L	L	Н	L	L
–72 dB	Н	Н	L	L	L
–76 dB	L	Н	L	L	L
-80 dB	Н	L	L	L	L
–∞ dB	L	L	L	L	L

ATT	D7	D8
0 dB	Н	Н
−1 dB	L	Н
−2 dB	Н	L
–3 dB	L	L

#### **Tone Level Control**

#### **Tone Code**

		Ва	ISS			Tre	ble	
	D7	D6	D5	D4	D3	D2	D1	D0
12 dB	L	Н	Н	L	L	Н	Н	L
10 dB	L	Н	L	Н	L	Н	L	Н
8 dB	L	Н	L	L	L	Н	L	L
6 dB	L	L	Н	Н	L	L	Н	Н
4 dB	L	L	Н	L	L	L	Н	L
2 dB	L	L	L	Н	L	L	L	Н
0 dB	L	L	L	L	L	L	L	L
–2 dB	Н	L	L	Н	Н	L	L	Н
−4 dB	Н	L	Н	L	Н	L	Н	L
−6 dB	Н	L	Н	Н	Н	L	Н	Н
–8 dB	Н	Н	L	L	Н	Н	L	L
-10 dB	Н	Н	L	Н	Н	Н	L	Н
–12 dB	Н	Н	Н	L	Н	Н	Н	L

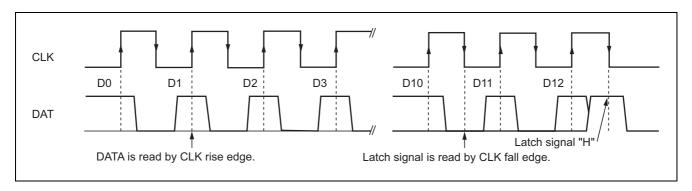
Note: Not used "HHHH", "LHHH", "HLLL"

#### **Mute Control**

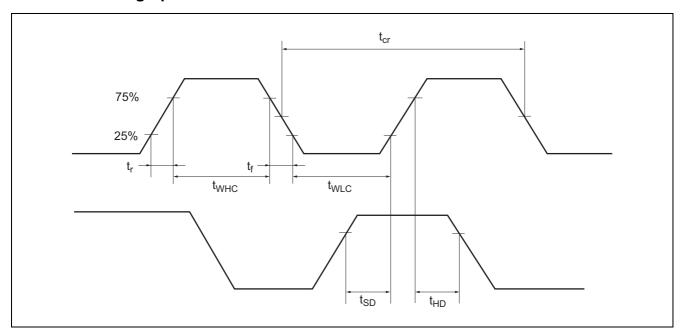
On condition D9 = 1, MUTE can be set up.

In MUTE, VOLUME LEVEL is set up VOL =  $-\infty$  automatically.

### **Data and Clock**

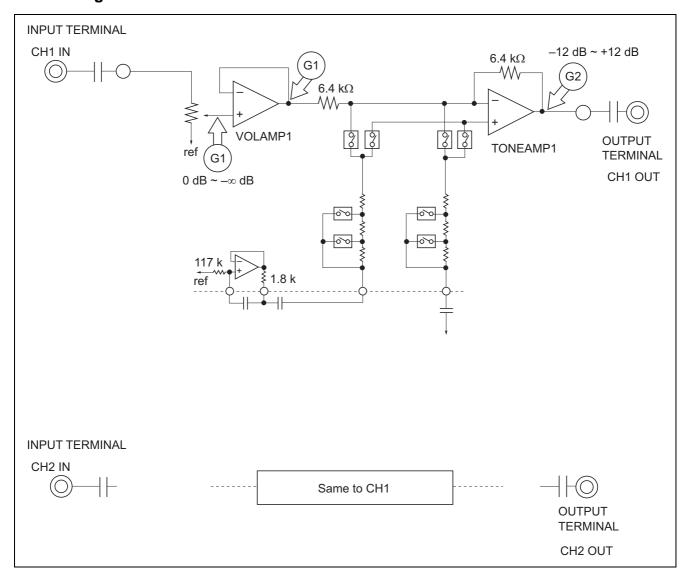


# **Bus Line Timing Specification**

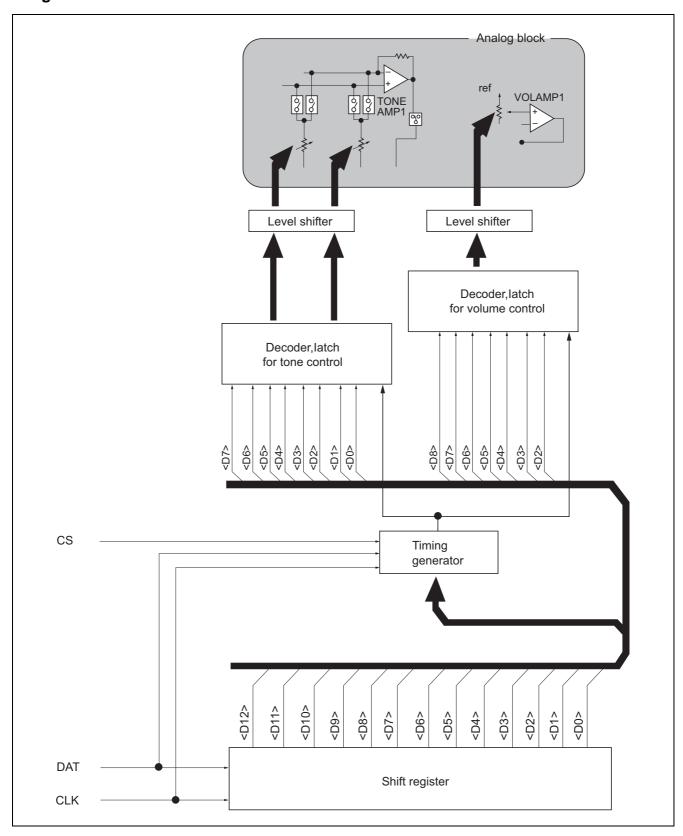


Item	Symbol	Min	Max	Units
CLK clock frequency	t <sub>cr</sub>	4	_	μS
The HIGH period of the clock	t <sub>WHC</sub>	1.6	_	μS
The LOW period of the clock	t <sub>WLC</sub>	1.6	_	μS
Rise time of CLK line	t <sub>r</sub>	_	0.4	μS
Fall time of CLK line	t <sub>f</sub>	_	0.4	μS
Set-up time DATA	t <sub>SD</sub>	0.8	_	μS
Hold time DATA	t <sub>HD</sub>	0.8	_	μS

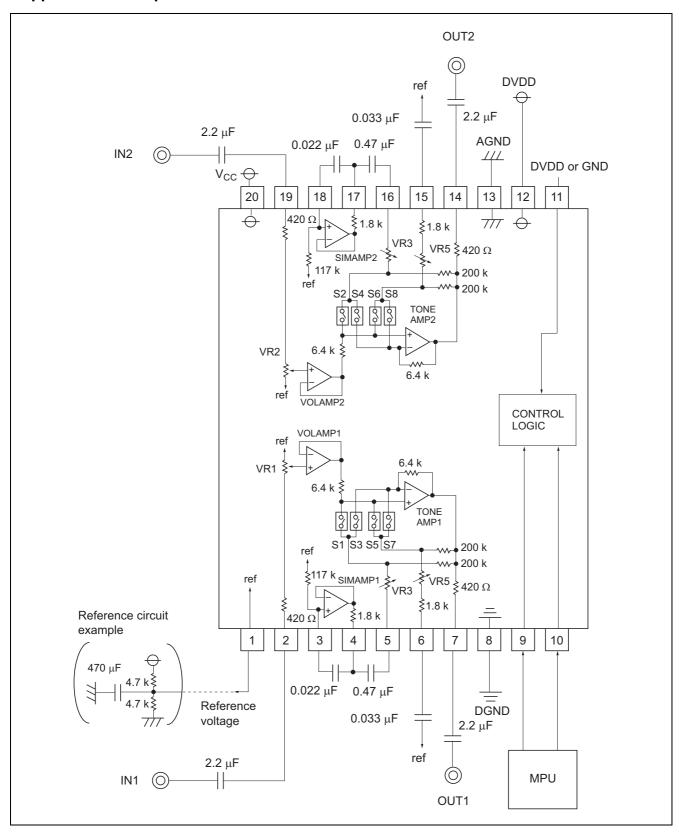
### **Level Diagram**



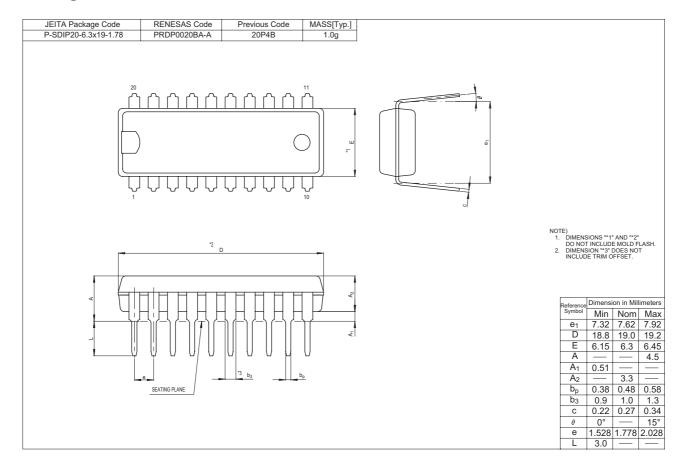
# **Logic Circuit**

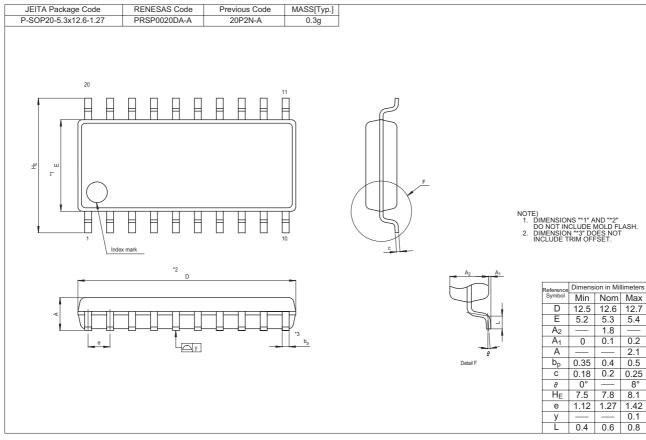


# **Application Example**



#### **Package Dimensions**





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