To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Description

The M30221 group of single-chip microcomputers are built using the high-performance silicon gate CMOS process using a M16C/60 Series CPU core. The M30221 group has LCD controller/driver. M30221 group is packaged in a 120-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, they are capable of executing instructions at high speed.

Features

- Basic machine instructions ..... Compatible with the M16C/60 series
- Memory capacity ..... See Figure 1.1.3 Memory Expansion
- Shortest instruction execution time ..... 100ns (f(X_{IN})=10MHz)
- Supply voltage ..... 4.0 to 5.5V (f(X_{IN})=10MHz)
  2.7 to 5.5V (f(X_{IN})=7MHz with software one-wait)
- Interrupts ..... 24 internal and 8 external interrupt sources, 4 software interrupt sources; 7 levels(including key input interrupt)
- Multifunction 16-bit timer ..... Timer A (output) x 8, timer B (input) x 6
- Real time port outputs ..... 8 bits X 3 lines,6 bits X 1 lines
- Serial I/O ..... 2 channels for UART or clock synchronous
- DMAC ..... 2 channels (trigger: 24 souces)
- A-D converter ..... 10 bits X 7 channels
- D-A converter ..... 8 bits X 2 channels
- Watchdog timer ..... 1 line
- Programmable I/O ..... 83 lines (26 lines are shared with LCD outputs)
- Output port ..... 14 lines (14 lines are shared with LCD outpus)
- Input port ..... 1 line ($P7_7$, shared with NMI pin)
- LCD drive control circuit ..... 1/2, 1/3 bias
  2, 3 and 4 duty
  4 common outputs
  40 segment outputs
  built-in charge pump
- Key input interrupt ..... 20 lines
- Clock generating circuit ..... 2 built-in clock generation circuits
  (built-in feedback resistor, and external ceramic or quartz oscillator)

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error.
Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.

Applications

Camera, Home appliances, Portable equipment, Audio, office equipment, etc.

------Table of Contents------

Pin Configuration

Figures 1.1.1 show the pin configurations (top view).

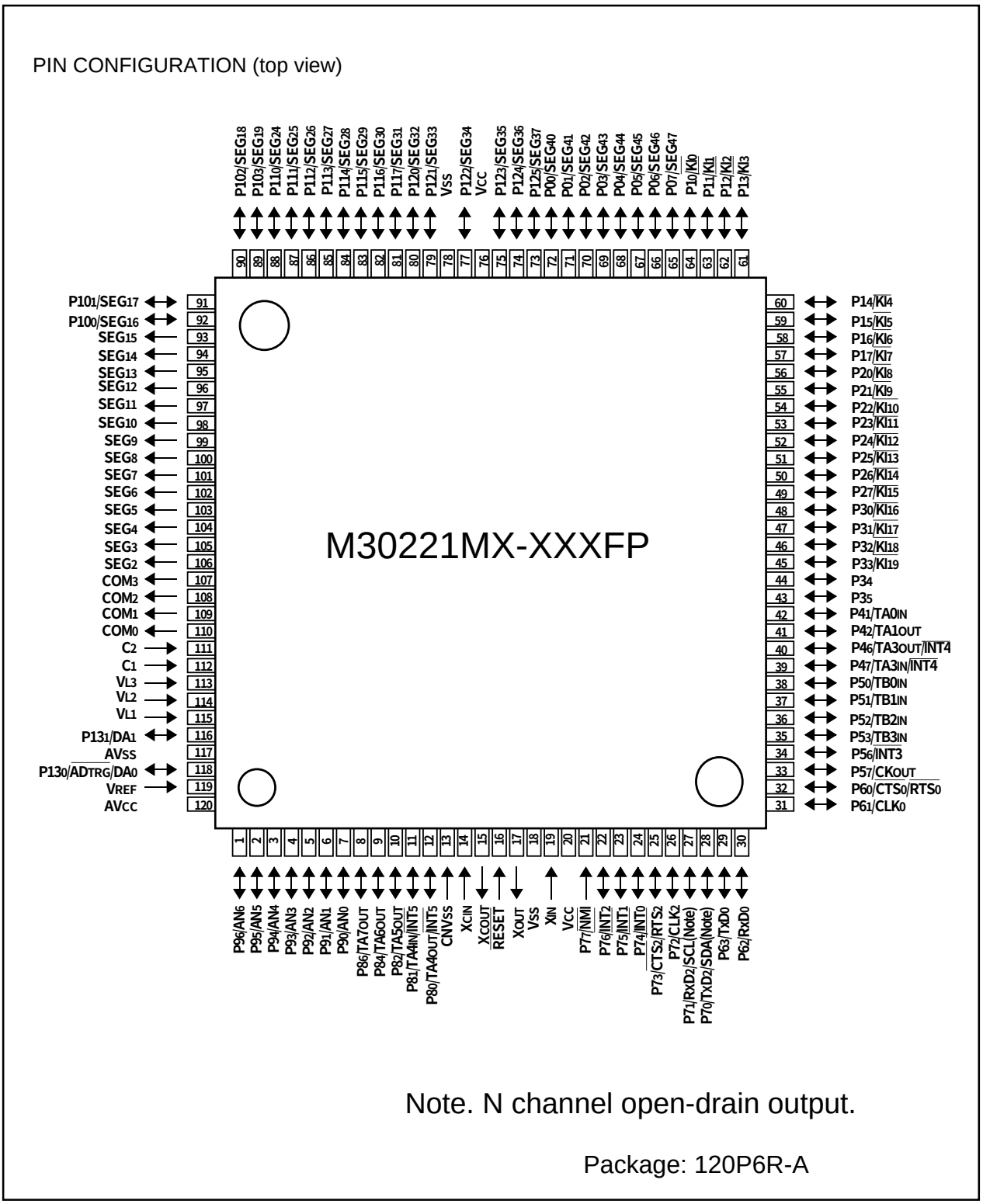


Figure 1.1.1. Pin configuration for the M30221 group (top view)

Block Diagram

Figure 1.1.2 is a block diagram of the M30221 group.

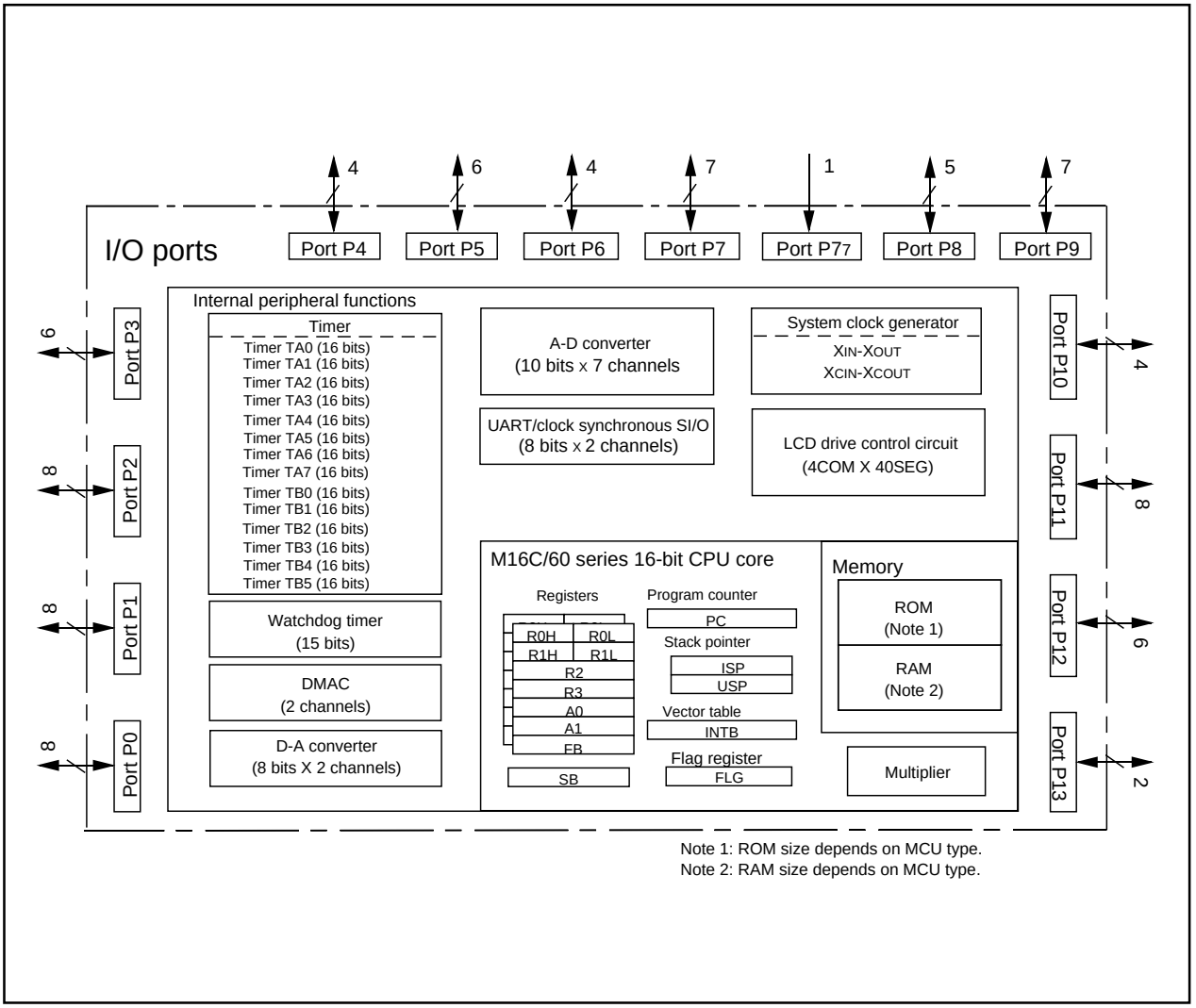


Figure 1.1.2. Block diagram of M30221 group

Performance Outline

Table 1.1.1 is performance outline of M30221 group.

Table 1.1.1. Performance outline of M30221 group

Item			Performance
Number of basic instructions			91 instructions
Shortest instruction execution time			100ns (f(XIN)=10MHz
Memory capacity	ROM		24 Kbytes
	RAM		1.5 Kbytes
I/O port	P0 to P13 (except P77)		8 bits x 4, 2 bits x 1, 6 bits x 3, 7 bits x 2 5 bits x 1, 4 bits x 3
Input port	P77		1 bit x 1
Output port	SEG2 to SEG15		2 bits x 7
Multifunction timer	TA0 to TA7		16 bits x 8
	TB0 to TB5		16 bits x 6
Real time port outputs			8 bits x 3 lines,6 bits x 1 lines
Serial I/O	UART0 , UART2		(UART or clock synchronous) x 2
A-D converter			10 bits x 7 channels
D-A converter			8 bits x 2 channels
DMAC			2 channel(trigger:24 sources)
LCD	COM0 to COM3		4 lines
	SEG2 to SEG47		40 lines (26 lines are shared with I/O ports)
Watchdog timer			15 bits x 1 (with prescaler)
Interrupt			24 internal and 8 external sources, 4 software sources
Clock generating circuit			2 built-in clock generation circuits (built-in feedbackresistor, and external ceramic or quartz oscillator)
Supply voltage			4.0 to 5.5V (f(XIN)=10MHz)
			2.7 to 5.5V (f(XIN)=7MHz with software one-wait)
Power consumption			18 mW (Vcc=3.3V, f(XIN)=7MHz with software one-wait)
I/O characteristics	I/O withstand voltage (P0 to P13)		5 V
	Output current	P1 to P9,P13	5 mA
		P0, P10 to P12	0.1mA("H" output), 2.5mA("L" output)
Device configuration			CMOS silicon gate
Package			120-pin plastic mold QFP

Mitsubishi plans to release the following products in the M30221 group:

(1) Support for mask ROM version, flash memory version

(2) Memory capacity

(3) Package

120P6R-A : Plastic molded QFP (mask ROM and flash memory versions)

Figure 1.1.3 shows the memory expansion and figure 1.1.4 shows the Type No., memory size, and package.

April. 2001

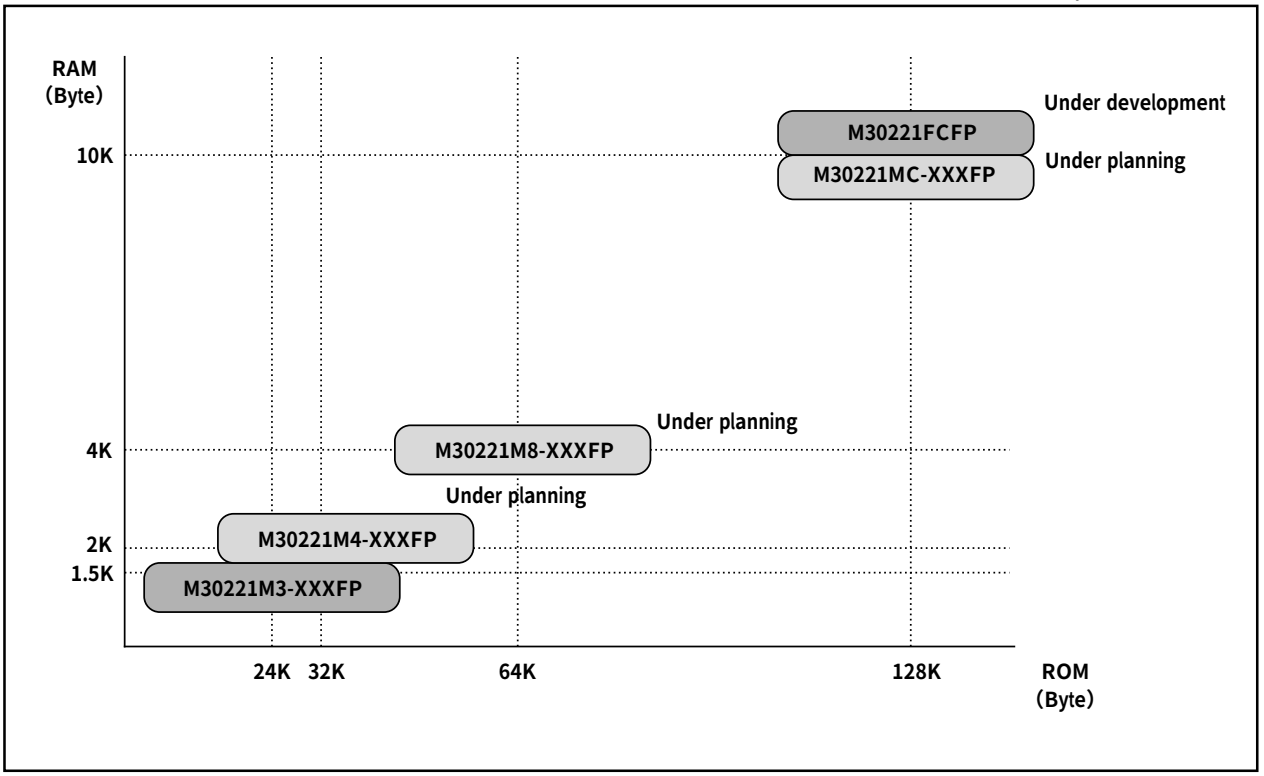


Figure 1.1.3. Memory expansion

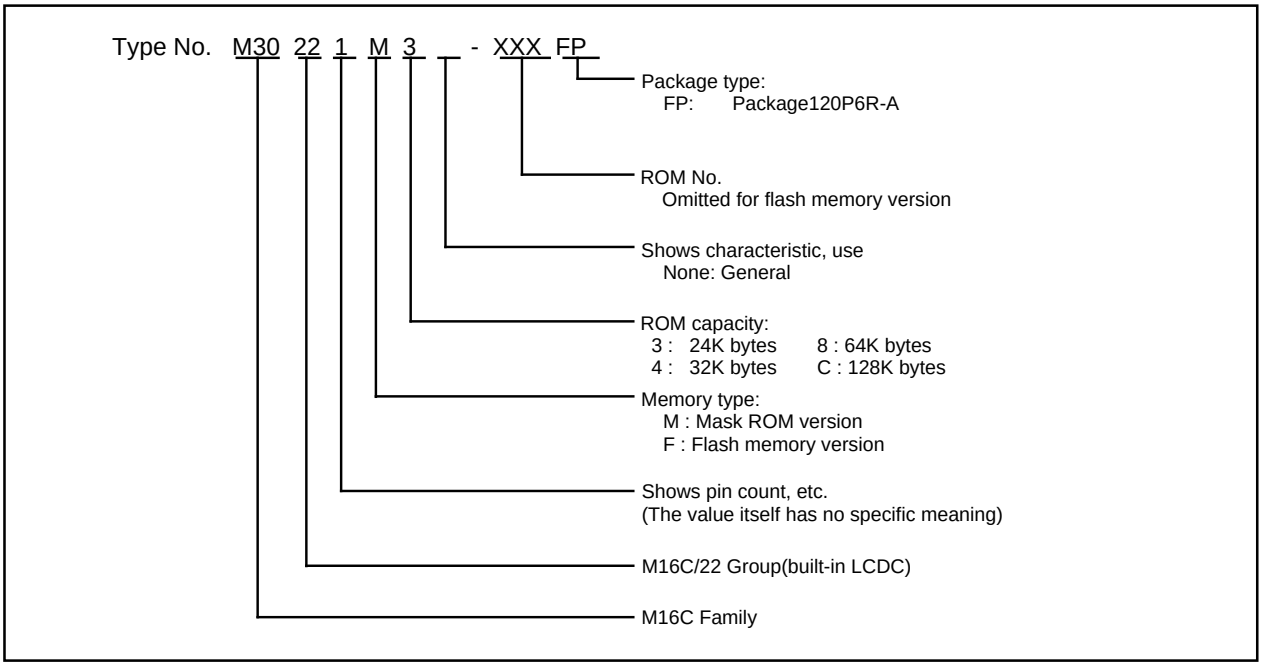


Figure 1.1.4. Type No., memory size, and package

Pin Description

Pin name	Signal name	I/O	Function
V_{CC}, V_{SS}	Power supply input		Supply 2.7 to 5.5 V to the V_{CC} pin. Supply 0 V to the V_{SS} pin.
CNV_{SS}	CNV_{SS}	I	Connect it to the V_{SS} pin.
$\overline{RESET}$	Reset input	I	A “L” on this input resets the microcomputer.
X_{IN} X_{OUT}	Clock input Clock output	I O	These pins are provided for the main clock generating. circuit.Connect a ceramic resonator or crystal between the X_{IN} and the X_{OUT} pins. To use an externally derived clock, input it to the X_{IN} pin and leave the X_{OUT} open.
X_{CIN} X_{COUT}	Clock input Clock output	I O	These pins are provided for the sub clock generating circuit.Connect a ceramic resonator or crystal between the X_{CIN} and the X_{COUT} pins. To use an externally derived clock, input it to the X_{CIN} pin and leave the X_{COUT} open.
AV_{CC}	Analog power supply input		This pin is a power supply input for the A-D converter. Connect it to VCC.
AV_{SS}	Analog power supply input		This pin is a power supply input for the A-D converter. Connect it to VSS.
V_{REF}	Reference voltage input	I	This pin is a reference voltage input for the A-D converter.
$P0_0$ to $P0_7$	I/O port P0	I/O	This is an 8-bit CMOS I/O port. It has an input/output port direction register that allows the user to set each pin for input or output individually. When set for input, the user can specify in units of four bits via software whether or not they are tied to a pull-up resistor. Pins in this port also use as LCD segment output and real time port output.
$P1_0$ to $P1_7$	I/O port P1	I/O	This is an 8-bit I/O port equivalent to P0. Pins in this port also function as input pins for the key input interrupt function and real time port output.
$P2_0$ to $P2_7$	I/O port P2	I/O	This is an 8-bit I/O port equivalent to P0. Pins in this port also function as input pins for the key input interrupt function and real time port output.
$P3_0$ to $P3_5$	I/O port P3	I/O	This is a 6-bit I/O port equivalent to P0. $P3_0$ to $P3_3$ also function as input pins for the key input interrupt function.
$P4_1$, $P4_2$, $P4_6$, $P4_7$	I/O port P4	I/O	This is a 4-bit I/O port equivalent to P0. The $P4_1$ pin is shared with timer A0 input. The $P4_2$ pin is shared with timer A1 output. The $P4_6$ pin is shared with timer A3 output and $\overline{INT4}$. The $P4_7$ pin is shared with timer A3 input and $\overline{INT4}$.
$P5_0$ to $P5_3$, $P5_6$, $P5_7$	I/O port P5	I/O	This is a 6-bit I/O port equivalent to P0. The $P5_0$, $P5_1$, $P5_2$, and $P5_3$ pins are shared with timerB0, B1, B2, and B3 input, respectively. The $P5_6$ pin is shared with $\overline{INT3}$. The $P5_7$ pin is shared with CKOUT output.
$P6_0$ to $P6_3$	I/O port P6	I/O	This is an 4-bit I/O port equivalent to P0. The P60 pin is shared with $\overline{CTS_0}$ and $\overline{RTS_0}$. The $P6_1$, $P6_2$, and $P6_3$ pins are shared with CLK_0, RxD_0, and TxD_0, respectively.

Pin Description

Pin name	Signal name	I/O	Function
$P7_0$ to $P7_6$	I/O port P7	I/O	$P7_0$ to $P7_6$ are I/O ports equivalent to P0 ($P7_0$ and $P7_1$ are N channel open-drain output). The $P7_0$, $P7_1$, and $P7_2$ pins are shared with TxD_2, RxD_2, and CLK_2, respectively. The $P7_3$ is shared with $\overline{CTS_2}$ and $\overline{RTS_2}$. The $P7_4$, $P7_5$ and $P7_6$ pins are shared with $\overline{INT_0}$, $\overline{INT_1}$ and $\overline{INT_2}$, respectively.
$P7_7$		I	$P7_7$ is an input-only port that also functions for $\overline{NMI}$.
$P8_0$ to $P8_2$, $P8_4$, $P8_6$	I/O port P8	I/O	This is a 5-bit I/O port equivalent to P0. The $P8_0$ pin is shared with timer A4 output and $\overline{INT5}$ input . The $P8_1$ pin is shared with timer A4 input and $\overline{INT5}$ input. The $P8_2$ pin is shared with timer A5 output. The $P8_4$ pin is shared with timer A6 output. The $P8_6$ pin is shared with timer A7 output.
$P9_0$ to $P9_6$	I/O port P9	I/O	This is an 7-bit I/O port equivalent to P0. Pins in this port also function as A-D converter input pins.
$P10_0$ to $P10_3$	I/O port P10	I/O	This is an 4-bit I/O port equivalent to P0. Pins in this port also function as SEG output for LCD.
$P11_0$ to $P11_7$	I/O port P11	I/O	This is an 8-bit I/O port equivalent to P0. Pins in this port also function as SEG output for LCD.
$P12_0$ to $P12_5$	I/O port P12	I/O	This is an 6-bit I/O port equivalent to P0. Pins in this port also function as SEG output for LCD and real time port output.
$P13_0$, $P13_1$	I/O port P13	I/O	This is an 2-bit I/O port equivalent to P0. $P13_0$ pins in this port also function as D-A converter output pins or start trigger for A-D input pins. $P13_1$ pins in this port also function as D-A converter output pins.
SEG_2 to SEG_{15}	Segment output	O	Pins in this port function as SEG output for LCD drive circuit.
COM_0 to COM_3	Common output	O	Pins in this port function as common output for LCD drive circuit.
V_{L1} to V_{L3}	Power supply input for LCD		Power supply input for LCD drive circuit.
C_1, C_2	Step-up condenser connect port		Pins in this port function as external pin for LCD step-up condenser. Connect a condenser between C_1 and C_2.

Operation of Functional Blocks

The M30221 group accommodates certain units in a single chip. These units include ROM and RAM to store instructions and data and the central processing unit (CPU) to execute arithmetic/logic operations. Also included are peripheral units such as timers, real time port, serial I/O, LCD drive control circuit, D-A converter, A-D converter, DMAC and I/O ports.

Memory

Figure 1.4.1 is a memory map of the M30221 group. The address space extends the 1M bytes from address 00000_{16} to $FFFFF_{16}$. From $FFFFF_{16}$ down is ROM. For example, in the M30221M3-XXXFP, there is 24K bytes of internal ROM from $FA000_{16}$ to $FFFFF_{16}$. The vector table for fixed interrupts such as the reset and $\overline{NMI}$ are mapped to $FFFDC_{16}$ to $FFFFF_{16}$. The starting address of the interrupt routine is stored here. The address of the vector table for timer interrupts, etc., can be set as desired using the internal register (INTB). See the section on interrupts for details.

From 00400_{16} up is RAM. For example, in the M30221M3-XXXFP, 1.5K bytes of internal RAM is mapped to the space from 00400_{16} to $009FF_6$. In addition to storing data, the RAM also stores the stack used when calling subroutines and when interrupts are generated.

The SFR area is mapped to 00000_{16} to $003FF_{16}$. This area accommodates the control registers for peripheral devices such as I/O ports, A-D converter, serial I/O, timers, and LCD, etc. Figures 1.7.1 to 1.7.3 are location of peripheral unit control registers. Any part of the SFR area that is not occupied is reserved and cannot be used for other purposes.

The special page vector table is mapped to $FFE00_{16}$ to $FFFDB_{16}$. If the starting addresses of subroutines or the destination addresses of jumps are stored here, subroutine call instructions and jump instructions can be used as 2-byte instructions, reducing the number of program steps.

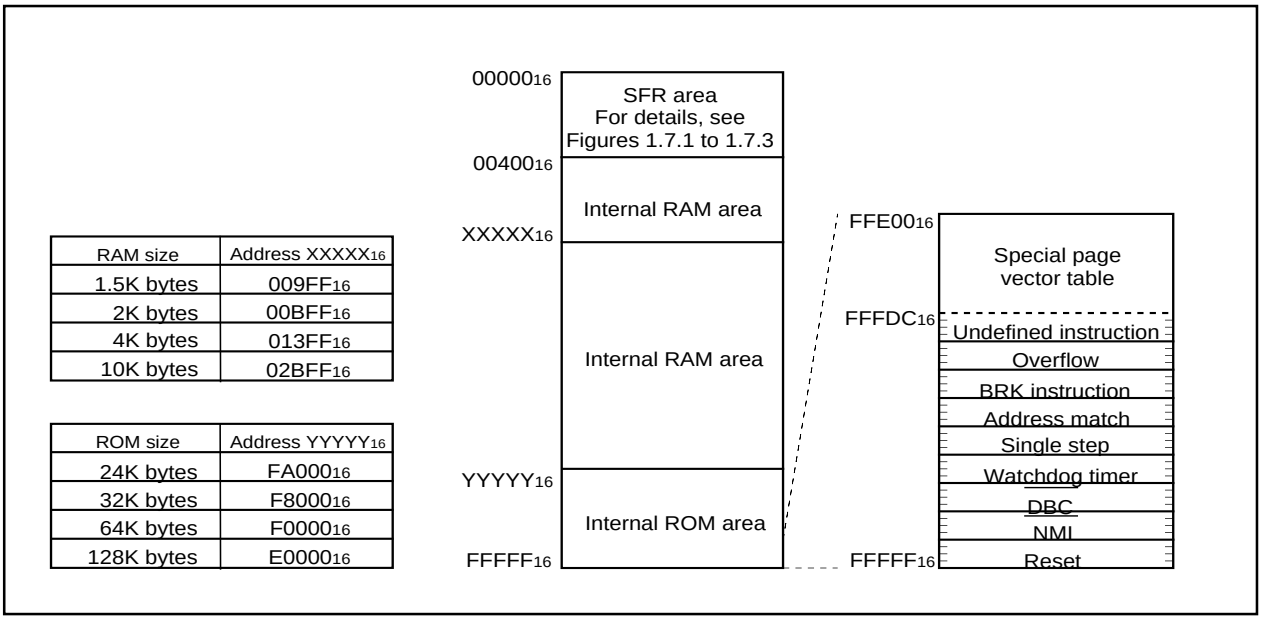


Figure 1.4.1. Memory map

Central Processing Unit (CPU)

The CPU has a total of 13 registers shown in Figure 1.5.1. Seven of these registers (R0, R1, R2, R3, A0, A1, and FB) come in two sets; therefore, these have two register banks.

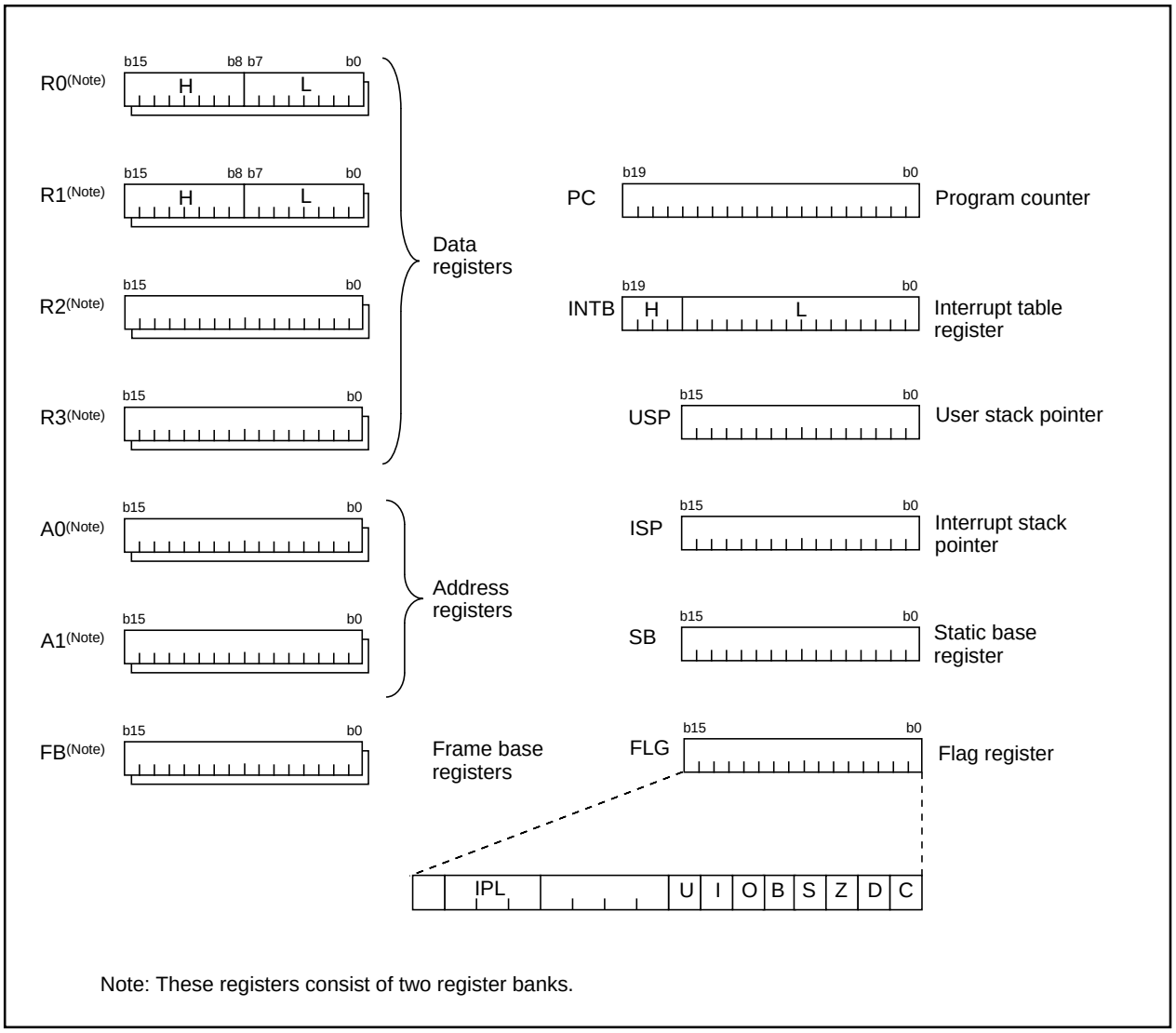


Figure 1.5.1. Central processing unit register

(1) Data registers (R0, R0H, R0L, R1, R1H, R1L, R2, and R3)

Data registers (R0, R1, R2, and R3) are configured with 16 bits, and are used primarily for transfer and arithmetic/logic operations.

Registers R0 and R1 each can be used as separate 8-bit data registers, high-order bits as (R0H/R1H), and low-order bits as (R0L/R1L). In some instructions, registers R2 and R0, as well as R3 and R1 can use as 32-bit data registers (R2R0/R3R1).

(2) Address registers (A0 and A1)

Address registers (A0 and A1) are configured with 16 bits, and have functions equivalent to those of data registers. These registers can also be used for address register indirect addressing and address register relative addressing.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

(3) Frame base register (FB)

Frame base register (FB) is configured with 16 bits, and is used for FB relative addressing.

(4) Program counter (PC)

Program counter (PC) is configured with 20 bits, indicating the address of an instruction to be executed.

(5) Interrupt table register (INTB)

Interrupt table register (INTB) is configured with 20 bits, indicating the start address of an interrupt vector table.

(6) Stack pointer (USP/ISP)

Stack pointer comes in two types: user stack pointer (USP) and interrupt stack pointer (ISP), each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by a stack pointer select flag (U flag). This flag is located at the position of bit 7 in the flag register (FLG).

(7) Static base register (SB)

Static base register (SB) is configured with 16 bits, and is used for SB relative addressing.

(8) Flag register (FLG)

Flag register (FLG) is configured with 11 bits, each bit is used as a flag. Figure 1.5.2 shows the flag register (FLG). The following explains the function of each flag:

- **Bit 0: Carry flag (C flag)**
  This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.
- **Bit 1: Debug flag (D flag)**
  This flag enables a single-step interrupt.
  When this flag is “1”, a single-step interrupt is generated after instruction execution. This flag is cleared to “0” when the interrupt is acknowledged.
- **Bit 2: Zero flag (Z flag)**
  This flag is set to “1” when an arithmetic operation resulted in 0; otherwise, cleared to “0”.
- **Bit 3: Sign flag (S flag)**
  This flag is set to “1” when an arithmetic operation resulted in a negative value; otherwise, cleared to “0”.
- **Bit 4: Register bank select flag (B flag)**
  This flag chooses a register bank. Register bank 0 is selected when this flag is “0” ; register bank 1 is selected when this flag is “1”.
- **Bit 5: Overflow flag (O flag)**
  This flag is set to “1” when an arithmetic operation resulted in overflow; otherwise, cleared to “0”.
- **Bit 6: Interrupt enable flag (I flag)**
  This flag enables a maskable interrupt.
  An interrupt is disabled when this flag is “0”, and is enabled when this flag is “1”. This flag is cleared to “0” when the interrupt is acknowledged.

- **Bit 7: Stack pointer select flag (U flag)**
  Interrupt stack pointer (ISP) is selected when this flag is “0” ; user stack pointer (USP) is selected when this flag is “1”.
  This flag is cleared to “0” when a hardware interrupt is acknowledged or an INT instruction of software interrupt Nos. 0 to 31 is executed.
- **Bits 8 to 11: Reserved area**
- **Bits 12 to 14: Processor interrupt priority level (IPL)**
  Processor interrupt priority level (IPL) is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.
  If a requested interrupt has priority greater than the processor interrupt priority level (IPL), the interrupt is enabled.
- **Bit 15: Reserved area**

The C, Z, S, and O flags are changed when instructions are executed. See the software manual for details.

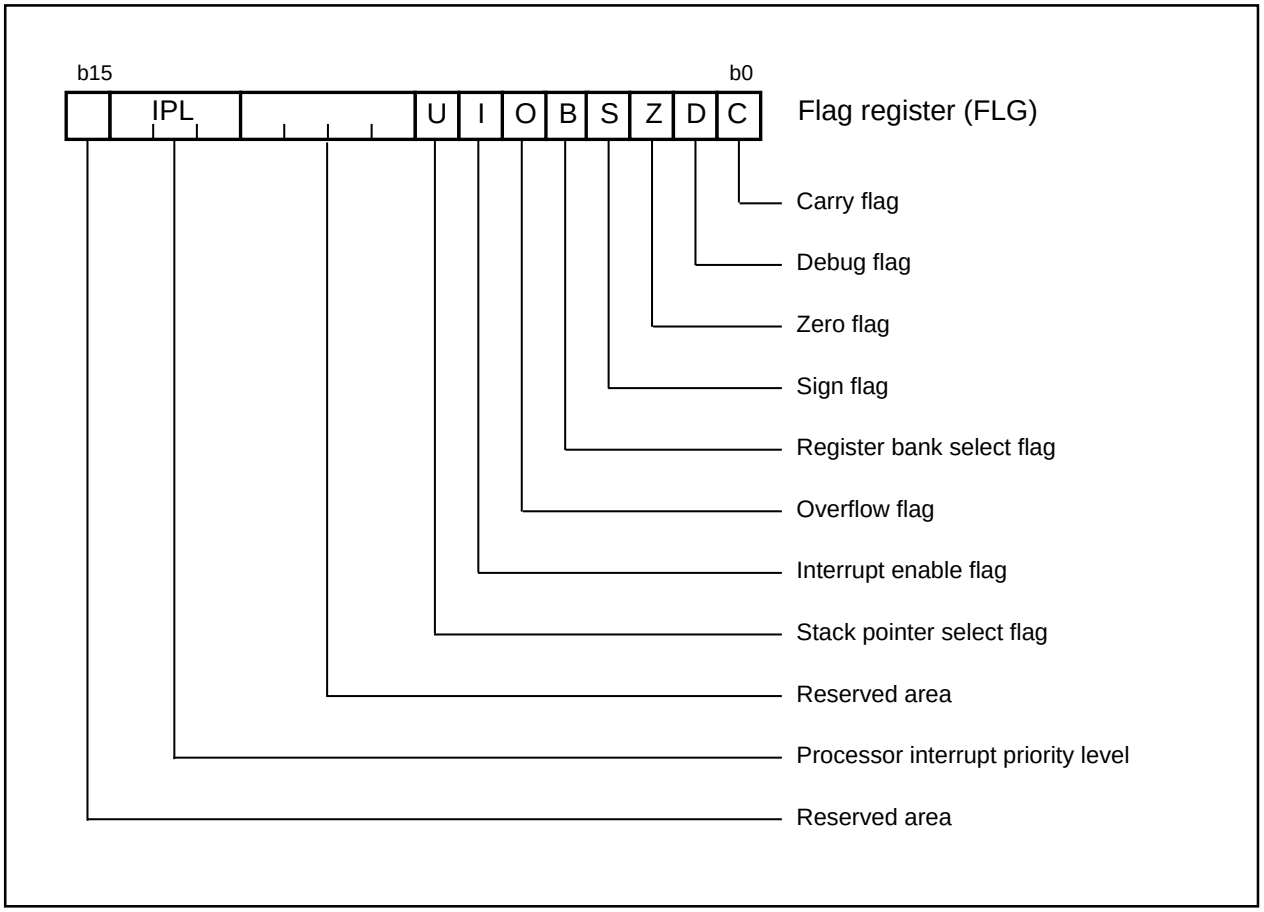


Figure 1.5.2. Flag register (FLG)

Reset

There are two kinds of resets; hardware and software. In both cases, operation is the same after the reset. (See “Software Reset” for details of software resets.) This section explains on hardware resets.

When the supply voltage is in the range where operation is guaranteed, a reset is effected by holding the reset pin level “L” (0.2VCC max.) for at least 20 cycles. When the reset pin level is then returned to the “H” level while main clock is stable, the reset status is cancelled and program execution resumes from the address in the reset vector table.

Figure 1.6.1 shows the example reset circuit. Figure 1.6.2 shows the reset sequence.

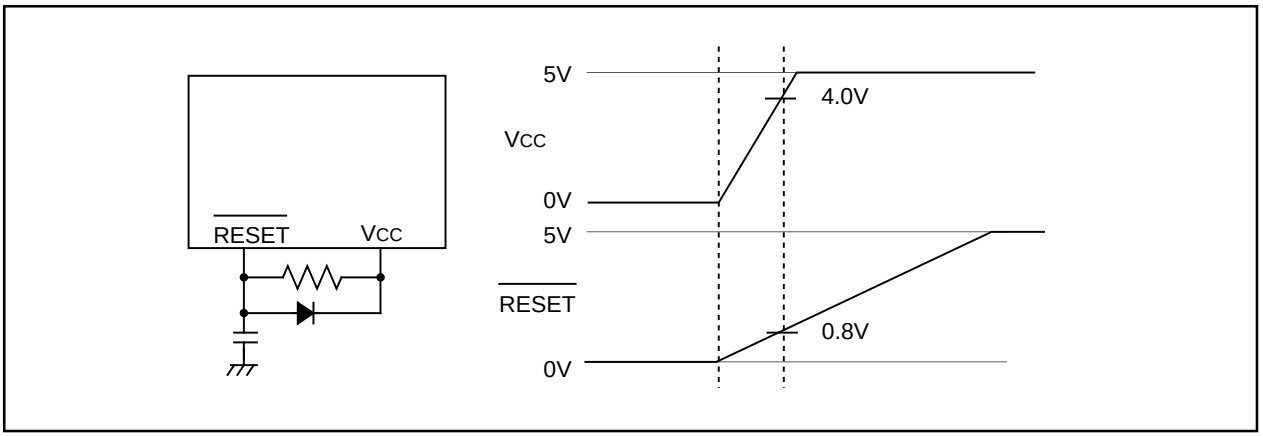


Figure 1.6.1. Example reset circuit

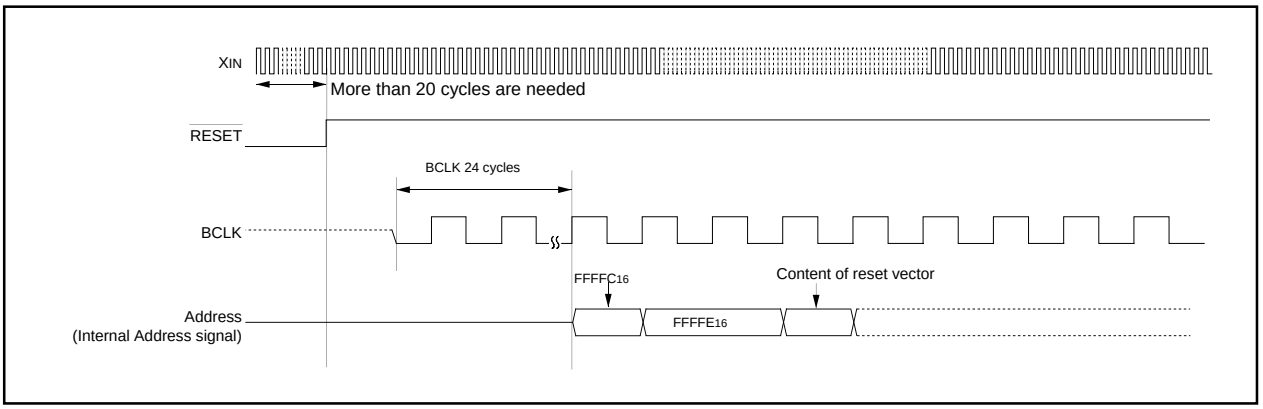
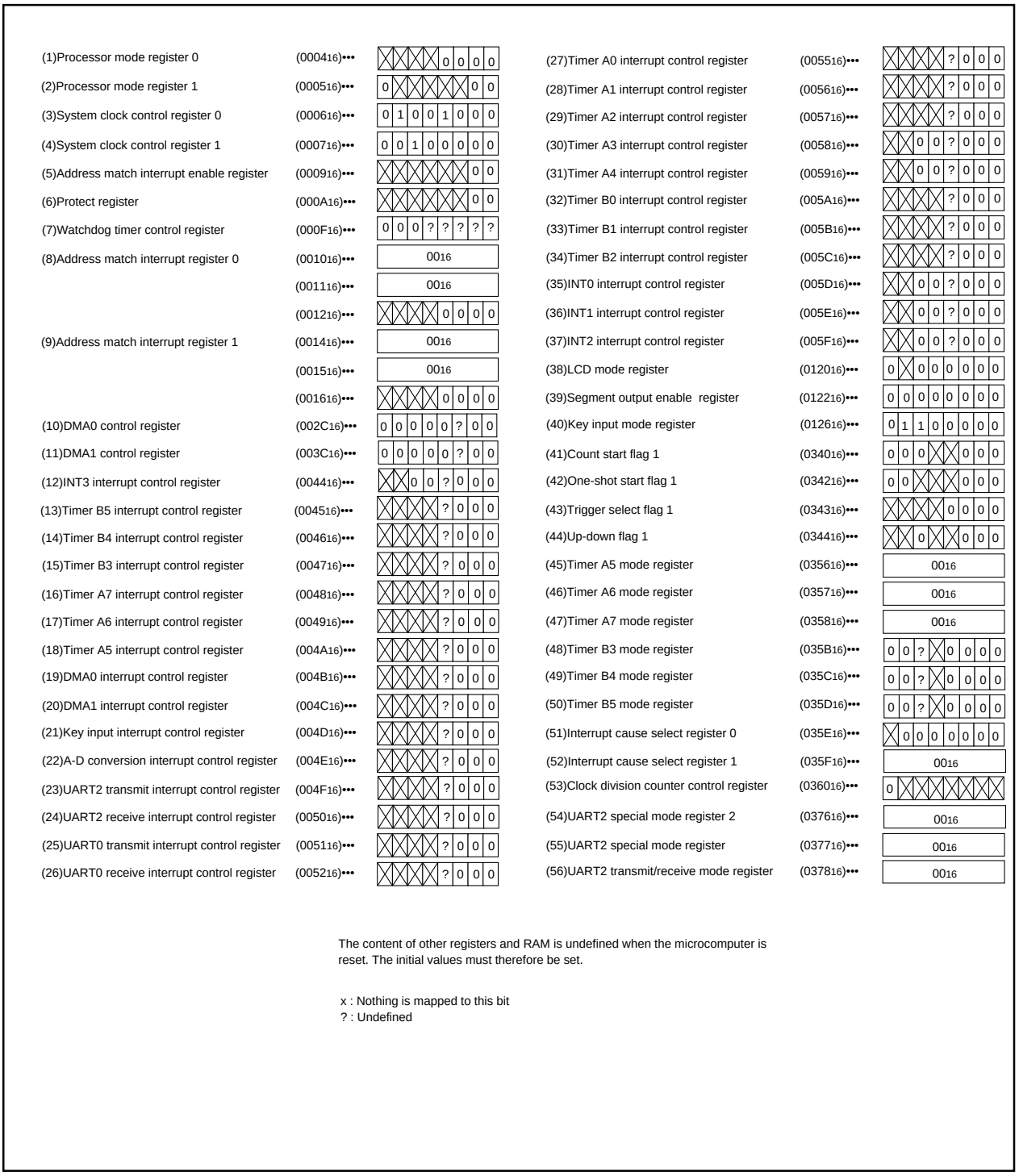


Figure 1.6.2. Reset sequence

Table 1.6.1 shows the statuses of the other pins while the $\overline{\text{RESET}}$ pin level is “L”. Figures 1.6.3 and 1.6.4 show the internal status of the microcomputer immediately after the reset is cancelled.

Table 1.6.1. Pin status when $\overline{\text{RESET}}$ pin level is “L”

Pin name	Status
P0, P10 to P12	Input port(with a pull up resistor)
P1 to P9, P13	Input port (floating)
SEG2 to SEG15	“H” level is output
COM0 to COM3	“H” level is output



The content of other registers and RAM is undefined when the microcomputer is reset. The initial values must therefore be set.

x : Nothing is mapped to this bit
? : Undefined

Figure 1.6.3. Device's internal status after a reset is cleared(1)

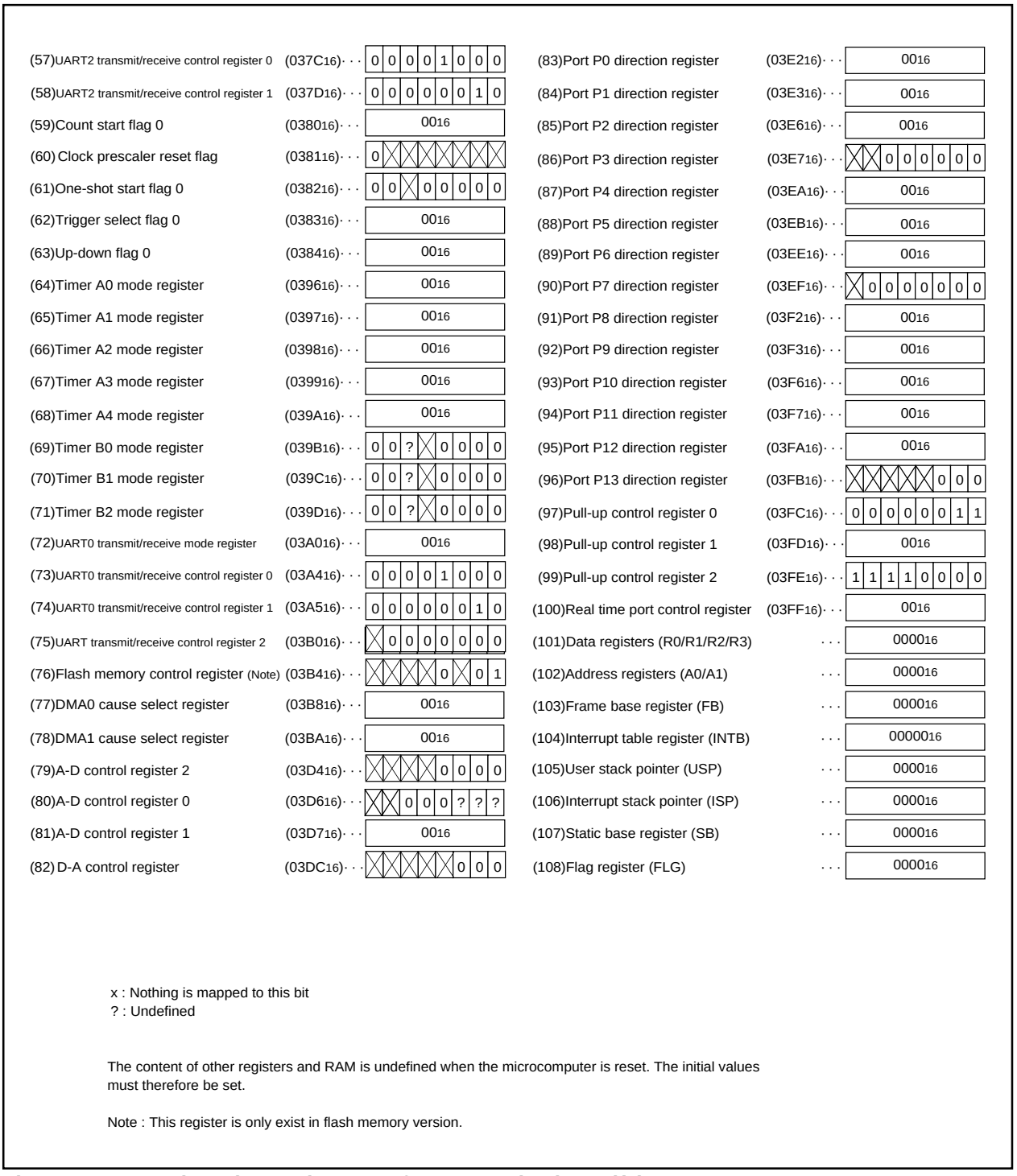


Figure 1.6.4. Device's internal status after a reset is cleared(2)

0000₁₆	
0001₁₆	
0002₁₆	
0003₁₆	
0004₁₆	Processor mode register 0 (PM0)
0005₁₆	Processor mode register 1(PM1)
0006₁₆	System clock control register 0 (CM0)
0007₁₆	System clock control register 1 (CM1)
0008₁₆	
0009₁₆	Address match interrupt enable register (AIER)
000A₁₆	Protect register (PRCR)
000B₁₆	
000C₁₆	
000D₁₆	
000E₁₆	Watchdog timer start register (WDTS)
000F₁₆	Watchdog timer control register (WDC)
0010₁₆	Address match interrupt register 0 (RMAD0)
0011₁₆	
0012₁₆	
0013₁₆	
0014₁₆	Address match interrupt register 1 (RMAD1)
0015₁₆	
0016₁₆	
0017₁₆	
0018₁₆	
0019₁₆	
001A₁₆	
001B₁₆	
001C₁₆	
001D₁₆	
001E₁₆	
001F₁₆	
0020₁₆	DMA0 source pointer (SAR0)
0021₁₆	
0022₁₆	
0023₁₆	
0024₁₆	DMA0 destination pointer (DAR0)
0025₁₆	
0026₁₆	
0027₁₆	
0028₁₆	DMA0 transfer counter (TCR0)
0029₁₆	
002A₁₆	
002B₁₆	
002C₁₆	DMA0 control register (DM0CON)
002D₁₆	
002E₁₆	
002F₁₆	
0030₁₆	DMA1 source pointer (SAR1)
0031₁₆	
0032₁₆	
0033₁₆	
0034₁₆	DMA1 destination pointer (DAR1)
0035₁₆	
0036₁₆	
0037₁₆	
0038₁₆	DMA1 transfer counter (TCR1)
0039₁₆	
003A₁₆	
003B₁₆	
003C₁₆	DMA1 control register (DM1CON)
003D₁₆	
003E₁₆	
003F₁₆	

0040₁₆	
0041₁₆	
0042₁₆	
0043₁₆	
0044₁₆	INT3 interrupt control register (INT3IC)
0045₁₆	Timer B5 interrupt control register (TB5IC)
0046₁₆	Timer B4 interrupt control register (TB4IC)
0047₁₆	Timer B3 interrupt control register (TB3IC)
0048₁₆	Timer A7 interrupt control register (TA7IC)
0049₁₆	Timer A6 interrupt control register (TA6IC)
004A₁₆	Timer A5 interrupt control register (TA5IC) Bus collision detection interrupt control register (BCNIC)
004B₁₆	DMA0 interrupt control register (DM0IC)
004C₁₆	DMA1 interrupt control register (DM1IC)
004D₁₆	Key input interrupt control register (KUPIC)
004E₁₆	A-D conversion interrupt control register (ADIC)
004F₁₆	UART2 transmit interrupt control register (S2TIC)
0050₁₆	UART2 receive interrupt control register (S2RIC)
0051₁₆	UART0 transmit interrupt control register (S0TIC)
0052₁₆	UART0 receive interrupt control register (S0RIC)
0053₁₆	UART1 transmit interrupt control register (S1TIC)
0054₁₆	UART1 receive interrupt control register (S1RIC)
0055₁₆	Timer A0 interrupt control register (TA0IC)
0056₁₆	Timer A1 interrupt control register (TA1IC)
0057₁₆	Timer A2 interrupt control register (TA2IC)
0058₁₆	Timer A3 interrupt control register (TA3IC) INT4 interrupt control register (INT4IC)
0059₁₆	Timer A4 interrupt control register (TA4IC) INT5 interrupt control register (INT5IC)
005A₁₆	Timer B0 interrupt control register (TB0IC)
005B₁₆	Timer B1 interrupt control register (TB1IC)
005C₁₆	Timer B2 interrupt control register (TB2IC)
005D₁₆	INT0 interrupt control register (INT0IC)
005E₁₆	INT1 interrupt control register (INT1IC)
005F₁₆	INT2 interrupt control register (INT2IC)
	≈ ≈
0100₁₆	LCD RAM0(LRAM0)
0101₁₆	LCD RAM1(LRAM1)
0102₁₆	LCD RAM2(LRAM2)
0103₁₆	LCD RAM3(LRAM3)
0104₁₆	LCD RAM4(LRAM4)
0105₁₆	LCD RAM5(LRAM5)
0106₁₆	LCD RAM6(LRAM6)
0107₁₆	LCD RAM7(LRAM7)
0108₁₆	LCD RAM8(LRAM8)
0109₁₆	LCD RAM9(LRAM9)
010A₁₆	
010B₁₆	
010C₁₆	LCD RAM12(LRAM12)
010D₁₆	LCD RAM13(LRAM13)
010E₁₆	LCD RAM14(LRAM14)
010F₁₆	LCD RAM15(LRAM15)
0110₁₆	LCD RAM16(LRAM16)
0111₁₆	LCD RAM17(LRAM17)
0112₁₆	LCD RAM18(LRAM18)
0113₁₆	
0114₁₆	LCD RAM20(LRAM20)
0115₁₆	LCD RAM21(LRAM21)
0116₁₆	LCD RAM22(LRAM22)
0117₁₆	LCD RAM23(LRAM23)
	≈ ≈
0120₁₆	LCD mode register (LCDM)
0121₁₆	
0122₁₆	Segment output enable register (SEG)
0123₁₆	
0124₁₆	LCD frame frequency counter (LCDTIM)
0125₁₆	
0126₁₆	Key input mode register (KUPM)

Note : Locations in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

Figure 1.7.1. Location of peripheral unit control registers (1)

0340₁₆	Count start flag 1 (TABSR1)
0341₁₆	
0342₁₆	One-shot start flag 1 (ONSF1)
0343₁₆	Trigger select register 1 (TRGSR1)
0344₁₆	Up-down flag 1(UDF1)
0345₁₆	
0346₁₆	Timer A5 register (TA5)
0347₁₆	
0348₁₆	Timer A6 register (TA6)
0349₁₆	
034A₁₆	Timer A7 register (TA7)
034B₁₆	
034C₁₆	
034D₁₆	
034E₁₆	
034F₁₆	
0350₁₆	Timer B3 register (TB3)
0351₁₆	
0352₁₆	Timer B4 register (TB4)
0353₁₆	
0354₁₆	Timer B5 register (TB5)
0355₁₆	
0356₁₆	Timer A5 mode register (TA5MR)
0357₁₆	Timer A6 mode register (TA6MR)
0358₁₆	Timer A7 mode register (TA7MR)
0359₁₆	
035A₁₆	
035B₁₆	Timer B3 mode register (TB3MR)
035C₁₆	Timer B4 mode register (TB4MR)
035D₁₆	Timer B5 mode register(TB5MR)
035E₁₆	Interrupt cause select register 0 (IFSR0)
035F₁₆	Interrupt cause select register 1 (IFSR1)
0360₁₆	Clock division counter control register (CDCC)
0361₁₆	
0362₁₆	
0363₁₆	
0364₁₆	
0365₁₆	
0366₁₆	
0367₁₆	
0368₁₆	
0369₁₆	
036A₁₆	
036B₁₆	
036C₁₆	
036D₁₆	
036E₁₆	Clock division counter (CDC)
036F₁₆	
0370₁₆	
0371₁₆	
0372₁₆	
0373₁₆	
0374₁₆	
0375₁₆	
0376₁₆	UART2 special mode register 2(U2SMR2)
0377₁₆	UART2 special mode register (U2SMR)
0378₁₆	UART2 transmit/receive mode register (U2MR)
0379₁₆	UART2 bit rate generator (U2BRG)
037A₁₆	UART2 transmit buffer register (U2TB)
037B₁₆	
037C₁₆	UART2 transmit/receive control register 0 (U2C0)
037D₁₆	UART2 transmit/receive control register 1 (U2C1)
037E₁₆	UART2 receive buffer register (U2RB)
037F₁₆	

0380₁₆	Count start flag 0 (TABSR0)
0381₁₆	Clock prescaler reset flag (CPSRF)
0382₁₆	One-shot start flag 0 (ONSF0)
0383₁₆	Trigger select register 0 (TRGSR0)
0384₁₆	Up-down flag 0 (UDF0)
0385₁₆	
0386₁₆	Timer A0 register (TA0)
0387₁₆	
0388₁₆	Timer A1 register (TA1)
0389₁₆	
038A₁₆	Timer A2 register (TA2)
038B₁₆	
038C₁₆	Timer A3 register (TA3)
038D₁₆	
038E₁₆	Timer A4 register (TA4)
038F₁₆	
0390₁₆	Timer B0 register (TB0)
0391₁₆	
0392₁₆	Timer B1 register (TB1)
0393₁₆	
0394₁₆	Timer B2 register (TB2)
0395₁₆	
0396₁₆	Timer A0 mode register (TA0MR)
0397₁₆	Timer A1 mode register (TA1MR)
0398₁₆	Timer A2 mode register (TA2MR)
0399₁₆	Timer A3 mode register (TA3MR)
039A₁₆	Timer A4 mode register (TA4MR)
039B₁₆	Timer B0 mode register (TB0MR)
039C₁₆	Timer B1 mode register (TB1MR)
039D₁₆	Timer B2 mode register (TB2MR)
039E₁₆	
039F₁₆	
03A0₁₆	UART0 transmit/receive mode register (U0MR)
03A1₁₆	UART0 bit rate generator (U0BRG)
03A2₁₆	UART0 transmit buffer register (U0TB)
03A3₁₆	
03A4₁₆	UART0 transmit/receive control register 0 (U0C0)
03A5₁₆	UART0 transmit/receive control register 1 (U0C1)
03A6₁₆	UART0 receive buffer register (U0RB)
03A7₁₆	
03A8₁₆	
03A9₁₆	
03AA₁₆	
03AB₁₆	
03AC₁₆	
03AD₁₆	
03AE₁₆	
03AF₁₆	
03B0₁₆	UART transmit/receive control register 2 (UCON)
03B1₁₆	
03B2₁₆	
03B3₁₆	
03B4₁₆	Flash memory control register (FMCR)(Note)
03B5₁₆	
03B6₁₆	
03B7₁₆	
03B8₁₆	DMA0 request cause select register (DM0SL)
03B9₁₆	
03BA₁₆	DMA1 request cause select register (DM1SL)
03BB₁₆	
03BC₁₆	
03BD₁₆	
03BE₁₆	
03BF₁₆	

Note1 : This register is only exist in flash memory version.
Note2 : Locations in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

Figure 1.7.2. Location of peripheral unit control registers (2)

03C0₁₆ 03C1₁₆	A-D register 0 (AD0)
03C2₁₆ 03C3₁₆	A-D register 1 (AD1)
03C4₁₆ 03C5₁₆	A-D register 2 (AD2)
03C6₁₆ 03C7₁₆	A-D register 3 (AD3)
03C8₁₆ 03C9₁₆	A-D register 4 (AD4)
03CA₁₆ 03CB₁₆	A-D register 5 (AD5)
03CC₁₆ 03CD₁₆	A-D register 6 (AD6)
03CE₁₆	
03CF₁₆	
03D0₁₆	
03D1₁₆	
03D2₁₆	
03D3₁₆	
03D4₁₆	A-D control register 2 (ADCON2)
03D5₁₆	
03D6₁₆	A-D control register 0 (ADCON0)
03D7₁₆	A-D control register 1 (ADCON1)
03D8₁₆	D-A register 0 (DA0)
03D9₁₆	
03DA₁₆	D-A register 1 (DA1)
03DB₁₆	
03DC₁₆	D-A control register (DACON)
03DD₁₆	
03DE₁₆	
03DF₁₆	
03E0₁₆	Port P0 register (P0)
03E1₁₆	Port P1 register (P1)
03E2₁₆	Port P0 direction register (PD0)
03E3₁₆	Port P1 direction register (PD1)
03E4₁₆	Port P2 register (P2)
03E5₁₆	Port P3 register (P3)
03E6₁₆	Port P2 direction register (PD2)
03E7₁₆	Port P3 direction register (PD3)
03E8₁₆	Port P4 register (P4)
03E9₁₆	Port P5 register (P5)
03EA₁₆	Port P4 direction register (PD4)
03EB₁₆	Port P5 direction register (PD5)
03EC₁₆	Port P6 register (P6)
03ED₁₆	Port P7 register (P7)
03EE₁₆	Port P6 direction register (PD6)
03EF₁₆	Port P7 direction register (PD7)
03F0₁₆	Port P8 register (P8)
03F1₁₆	Port P9 register (P9)
03F2₁₆	Port P8 direction register (PD8)
03F3₁₆	Port P9 direction register (PD9)
03F4₁₆	Port P10 register (P10)
03F5₁₆	Port P11 register (P11)
03F6₁₆	Port P10 direction register (PD10)
03F7₁₆	Port P11 direction register (PD11)
03F8₁₆	Port P12 register (P12)
03F9₁₆	Port P13 register (P13)
03FA₁₆	Port P12 direction register (PD12)
03FB₁₆	Port P13 direction register (PD13)
03FC₁₆	Pull-up control register 0 (PUR0)
03FD₁₆	Pull-up control register 1 (PUR1)
03FE₁₆	Pull-up control register 2 (PUR2)
03FF₁₆	Real time port control register (RTP)

Note : Locations in the SFR area where nothing is allocated are reserved areas.
Do not access these areas for read or write.

Figure 1.7.3. Location of peripheral unit control registers (3)

Programmable I/O Ports

There are 83 programmable I/O ports: P0 to P13 (excluding P7$_7$). Each port can be set independently for input or output using the direction register. A pull-up resistance for each block of 4 ports can be set. P7$_7$ is an input-only port and has no built-in pull-up resistance.

Figures 1.19.1 to 1.19.4 show the programmable I/O ports. Figure 1.19.5 shows the I/O pins.

Each pin functions as a programmable I/O port and as the I/O for the built-in peripheral devices.

To use the pins as the inputs for the built-in peripheral devices, set the direction register of each pin to input mode. When the pins are used as the outputs for the built-in peripheral devices (other than the D-A converter), they function as outputs regardless of the contents of the direction registers. When pins are to be used as the outputs for the D-A converter, do not set the direction registers to output mode.

(1) Direction registers

These registers are used to choose the direction of the programmable I/O ports. Each bit in these registers corresponds one for one to each I/O pin.

Note: There is no direction register bit for P7$_7$.

(2) Port registers

These registers are used to write and read data for input and output to and from an external device. A port register consists of a port latch to hold output data and a circuit to read the status of a pin. Each bit in port registers corresponds one for one to each I/O pin.

(3) Pull-up control registers

The pull-up control register can be set to apply a pull-up resistance to each block of 4 ports. When ports are set to have a pull-up resistance, the pull-up resistance is connected only when the direction register is set for input. The pull-up resistance is not connected for pins that are set for output from peripheral functions, regardless of the setting in the pull-up control register. When pull-up is ON for ports P1 and P2, an intermittent pull-up that pulls up the port for only a set period of time, can be performed from the key input mode register.

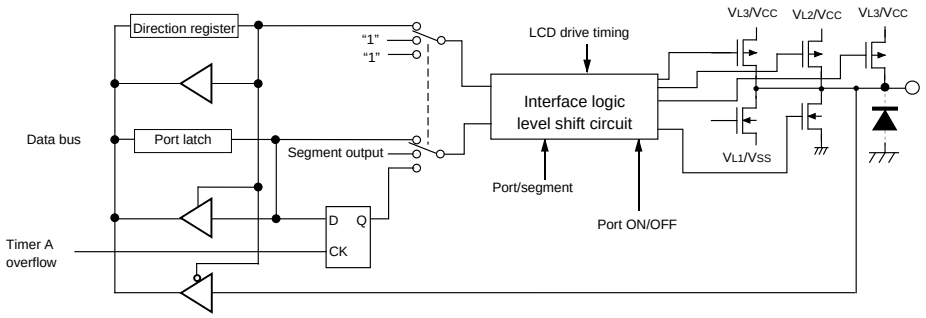
(4) Key input mode register

With bits 0 and 1 of this register, it is possible to select both edges or the fall edge of the key input for P1 and P2. Also, with bit 2, it is possible to make the pull-up for a port (P1 or P2), which is set for pull-up using the pull-up control register, automatically connect as an intermittent pull-up. And, using the significant 3 bits, the pull-up resistance can be connected to and disconnected from ports P12 and P13.

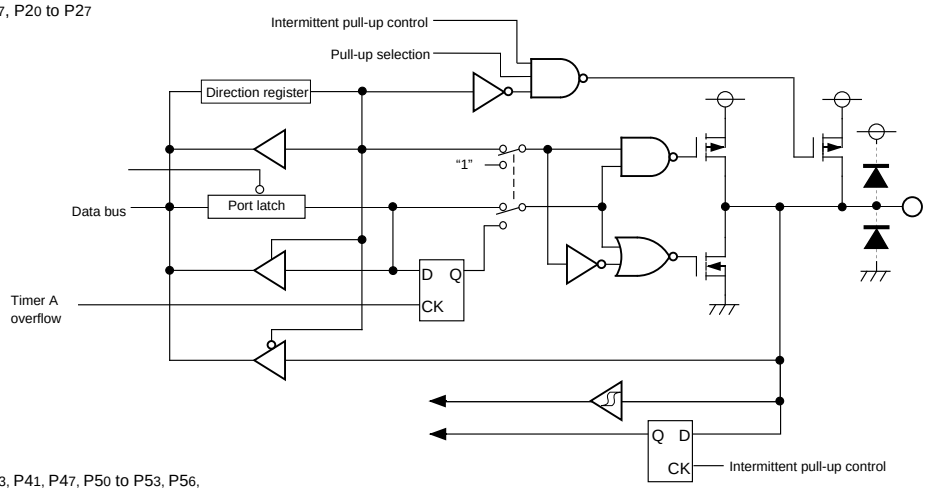
(5) Real-time port control register

The real-time port control register can be used to set the registers of ports P0, P1, P2 and P12 for real-time port output, whereby output is synchronized with timer overflow of timers A0, A1, A5 and A6 in the timer mode.

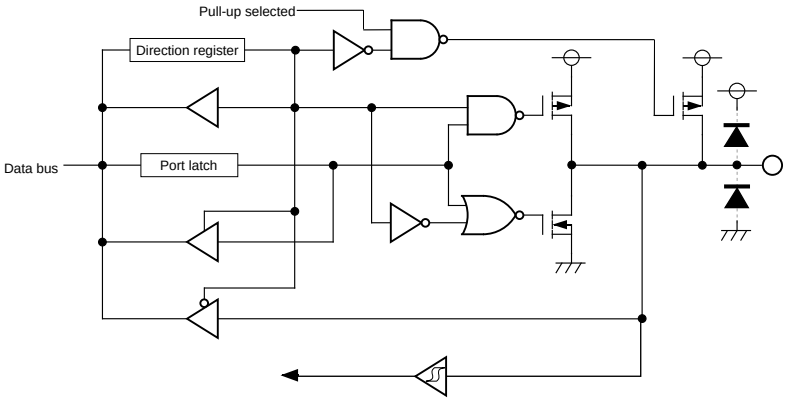
P00 to P07, P120 to P125



P10 to P17, P20 to P27



P30 to P33, P41, P47, P50 to P53, P56,
P62, P74 to P76, P81



P34, P35

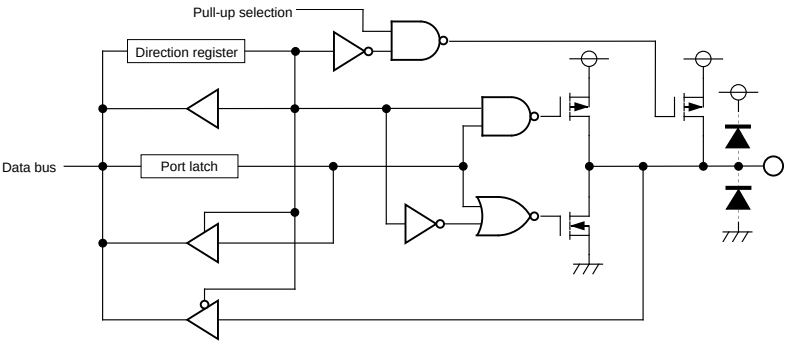


Figure 1.19.1. Programmable I/O ports (1)

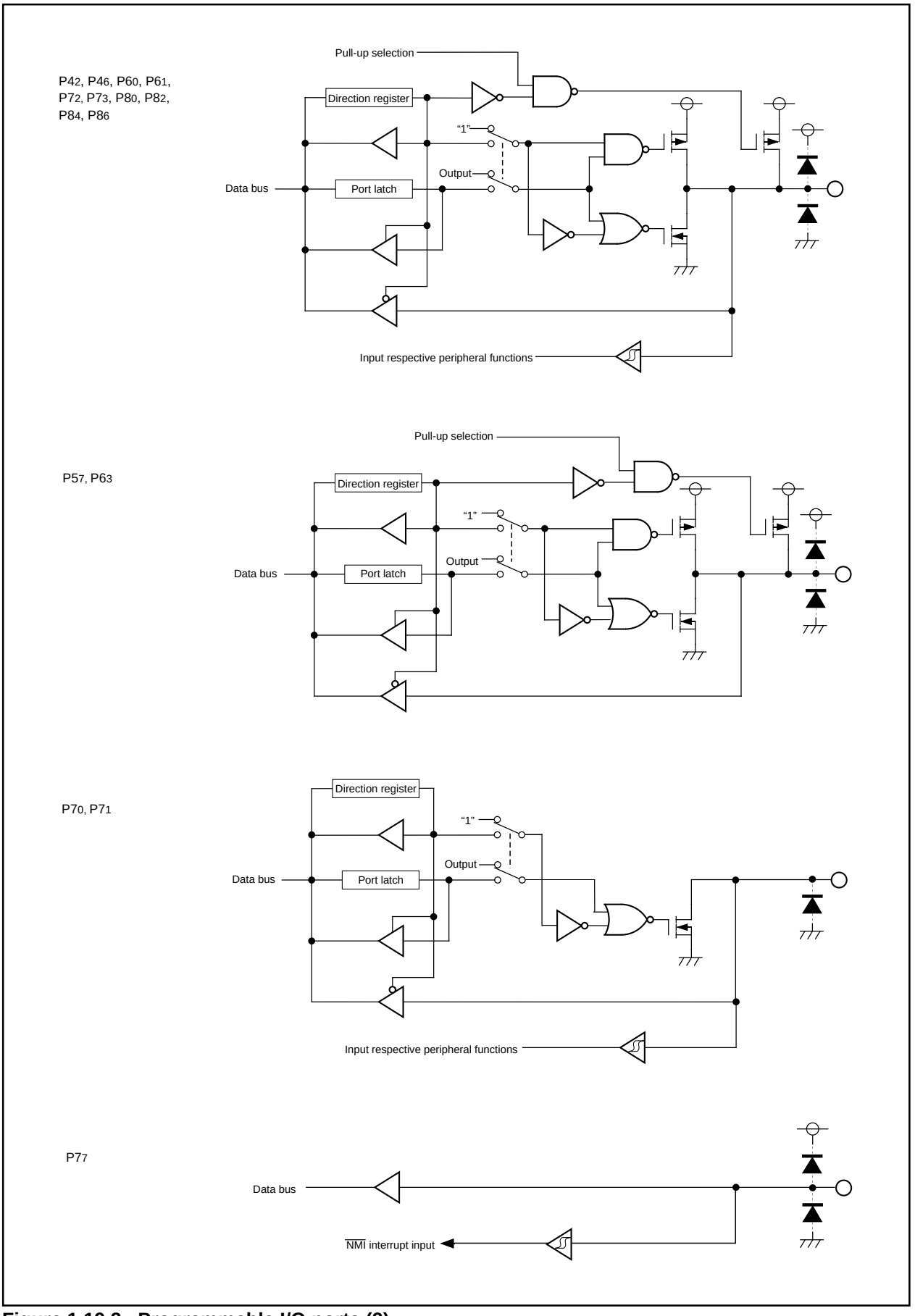
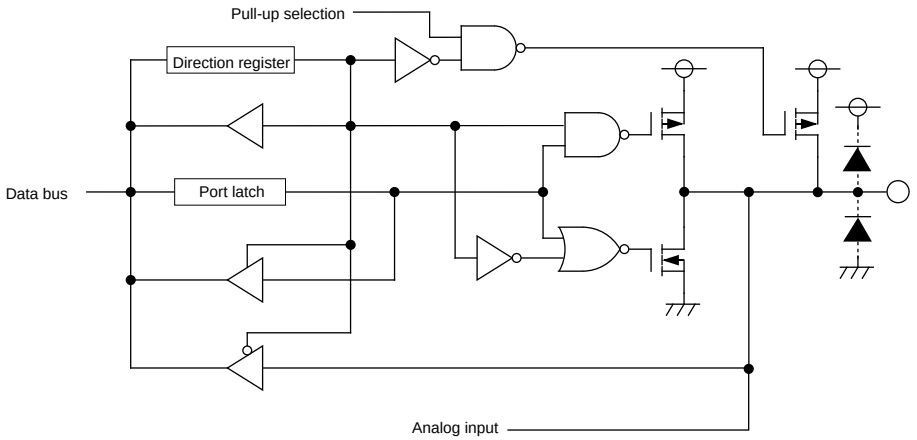
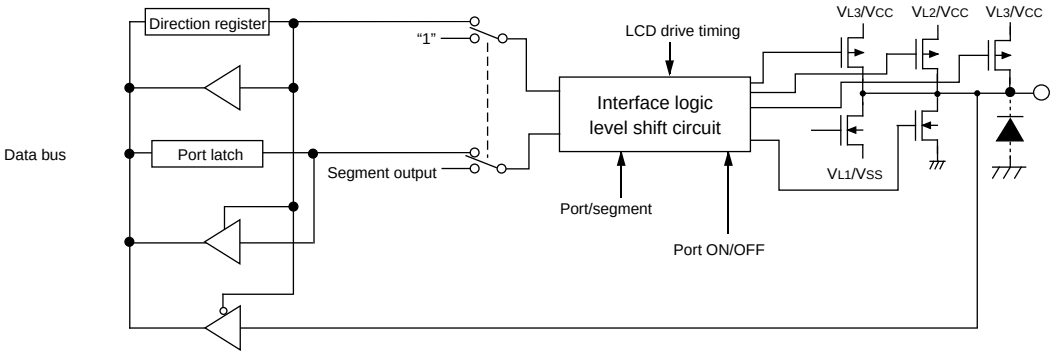


Figure 1.19.2. Programmable I/O ports (2)

P90 to P96



P100 to P103, P110 to P117



P130

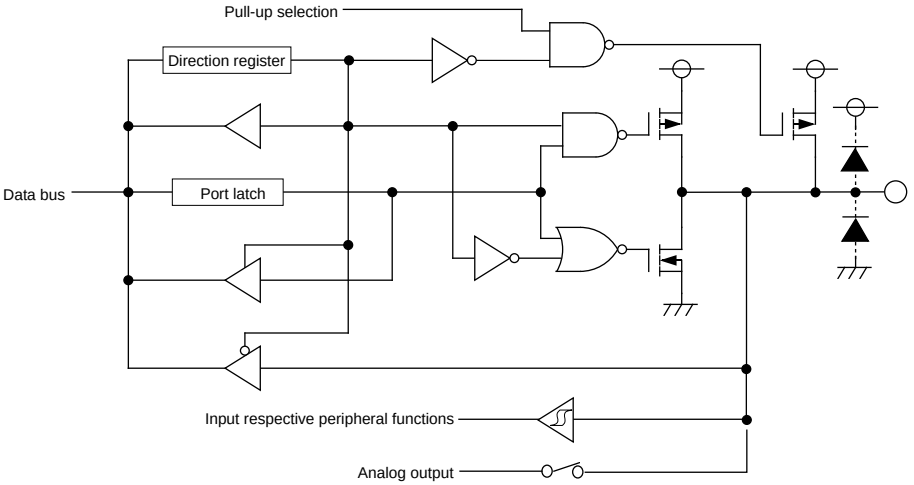


Figure 1.19.3. Programmable I/O ports (3)

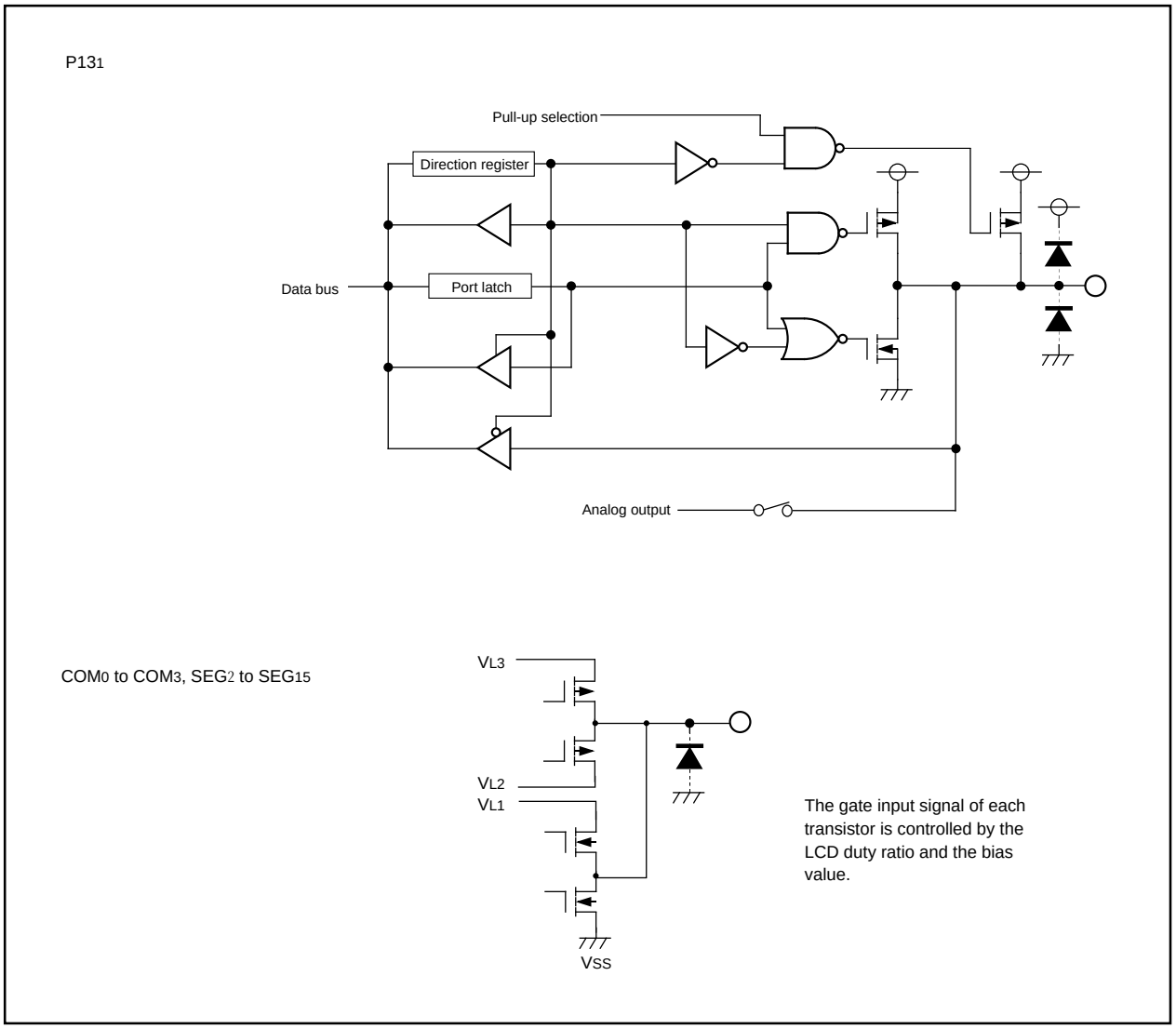


Figure 1.19.4. Programmable I/O ports (4)

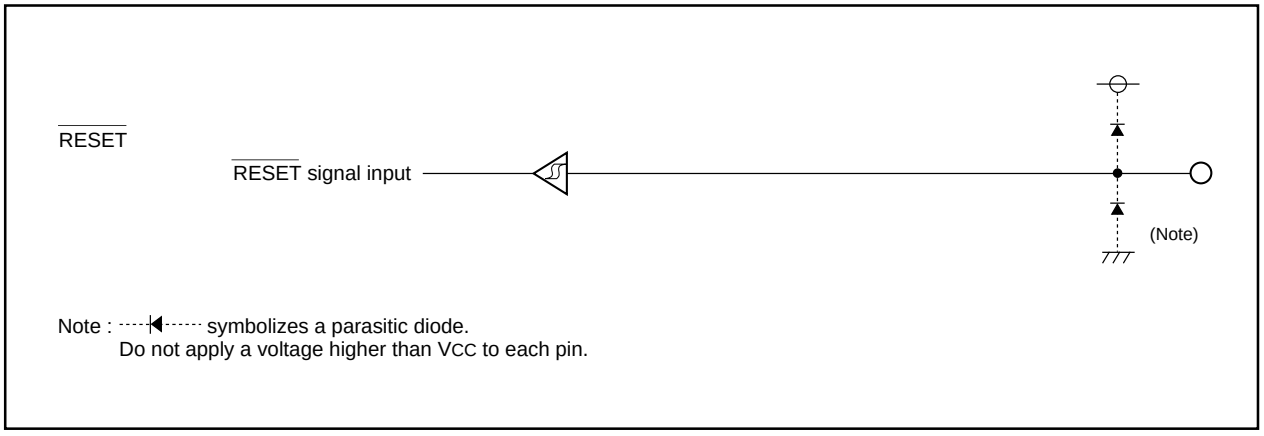


Figure 1.19.5. I/O pins

Table 1.19.1. Example connection of unused pins in single-chip mode

Pin name	Connection
Ports P0 to P13 (excluding P77)	After setting for output mode, leave these pins open; or after setting for input mode, connect every pin to VSS via a resistor.(Note1,Note3)
XOUT (Note 2),XCOUT	Open
XCIN	Connect via resistor to VSS (pull-down)
$\overline{\text{NMI}}$	Connect via resistor to VCC (pull-up)
AVCC	Connect to VCC
AVSS, VREF	Connect to VSS
COM0～COM3	Open
SEG2～SEG15	Open
C1, C2	Open
VL2, VL3	Connect to VCC
VL1	Connect to VSS
CNVSS	Connect via resistor to VSS

Note 1: If setting these pins in output mode and opening them, ports are in input mode untill switched into output mode by use of software after reset. Thus the voltage levels of the pins become unstable, and there can be instances in which the power source current increases while the ports are in input mode. In view of an instance in which the contents of the direction registers change due to a runaway generated by noise or other causes, setting the contents of the direction registers periodically by use of software increases program reliability.

Note 2: With external clock input to XIN pin.

Note 3: Output "L" if port P70 and P71 are set to output mode.Port P70 and P71 are N channel open drain.

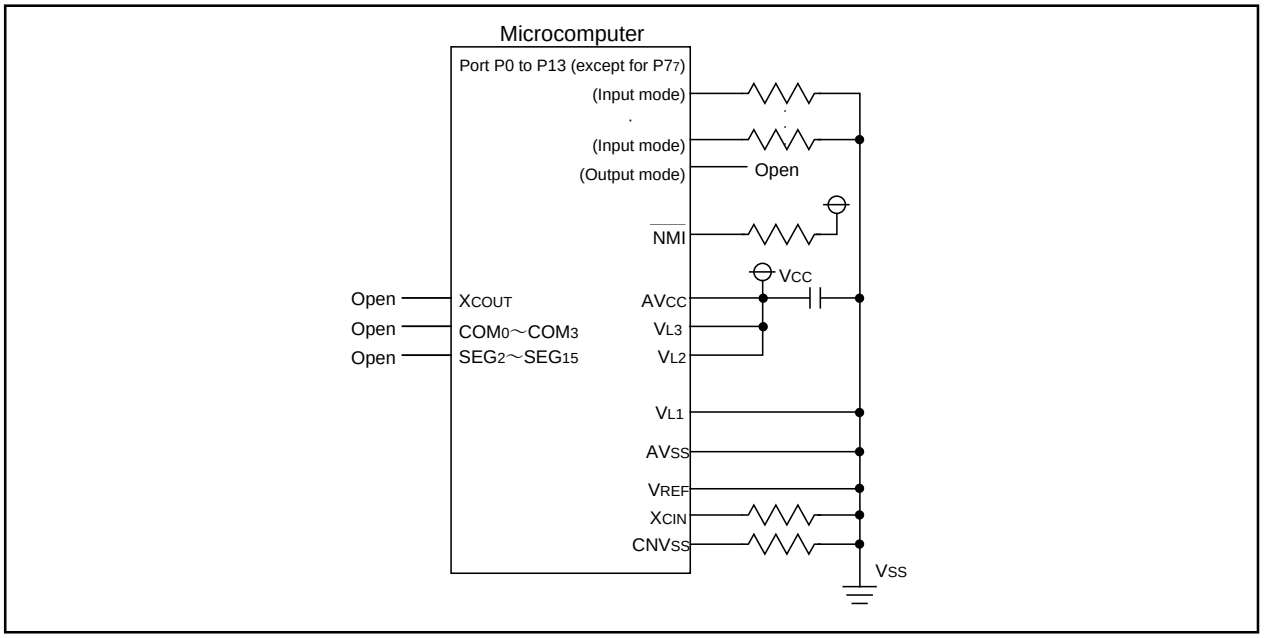


Figure 1.19.13. Example connection of unused pins

Usage Precaution

Timer A (timer mode)

(1) Reading the timer Ai register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the timer Ai register with the reload timing gets "$FFFF_{16}$". Reading the timer Ai register after setting a value in the timer Ai register with a count halted but before the counter starts counting gets a proper value.

Timer A (event counter mode)

(1) Reading the timer Ai register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the timer Ai register with the reload timing gets "$FFFF_{16}$" by underflow or "0000_{16}" by overflow. Reading the timer Ai register after setting a value in the timer Ai register with a count halted but before the counter starts counting gets a proper value.

(2) When stop counting in free run type, set timer again.

Timer A (one-shot timer mode)

(1) Setting the count start flag to "0" while a count is in progress causes as follows:

- The counter stops counting and a content of reload register is reloaded.
- The TAi_{OUT} pin outputs "L" level.
- The interrupt request generated and the timer Ai interrupt request bit goes to "1".

(2) The timer Ai interrupt request bit goes to "1" if the timer's operation mode is set using any of the following procedures:

- Selecting one-shot timer mode after reset.
- Changing operation mode from timer mode to one-shot timer mode.
- Changing operation mode from event counter mode to one-shot timer mode.

Therefore, to use timer Ai interrupt (interrupt request bit), set timer Ai interrupt request bit to "0" after the above listed changes have been made.

Timer A (pulse width modulation mode)

(1) The timer Ai interrupt request bit becomes "1" if setting operation mode of the timer in compliance with any of the following procedures:

- Selecting PWM mode after reset.
- Changing operation mode from timer mode to PWM mode.
- Changing operation mode from event counter mode to PWM mode.

Therefore, to use timer Ai interrupt (interrupt request bit), set timer Ai interrupt request bit to "0" after the above listed changes have been made.

(2) Setting the count start flag to "0" while PWM pulses are being output causes the counter to stop counting. If the TAi_{OUT} pin is outputting an "H" level in this instance, the output level goes to "L", and the timer Ai interrupt request bit goes to "1". If the TAi_{OUT} pin is outputting an "L" level in this instance, the level does not change, and the timer Ai interrupt request bit does not becomes "1".

Timer B (timer mode, event counter mode)

(1) Reading the timer Bi register while a count is in progress allows reading , with arbitrary timing, the value of the counter. Reading the timer Bi register with the reload timing gets "$FFFF_{16}$". Reading the timer Bi register after setting a value in the timer Bi register with a count halted but before the counter starts counting gets a proper value.

Timer B (pulse period/pulse width measurement mode)

(1) If changing the measurement mode select bit is set after a count is started, the timer Bi interrupt request bit goes to “1”.

(2) When the first effective edge is input after a count is started, an indeterminate value is transferred to the reload register. At this time, timer Bi interrupt request is not generated.

Real time port

(1) Make sure timer Ai for real time port output is set for timer mode, and is set to have “no gate function” using the gate function select bit.

(2) Before setting the real time port mode select bit to “1”, temporarily turn off the timer Ai used and write its set value to the timer Ai register.

Sirial I/O

(1) In case IIC mode select bit (bit 0 of address 0377_{16}) is set to "1" with UART2.When setting up port direction P7 (address $03EF_{16}$), write immediate values. If you use Read/Modify/Write instructions (BSET,BCLR,AND,OR,etc..) on the P7 direction register, the value of $P7_1$ direction register may change to unknown data.

(2) MASK ROM version ONRY when IIC mode select bit (bit 0 of address 0377_{16}) and the internal/ external select bit (bit 3 of address 0378_{16}) are both set to "1". The function of "SCL wait output bit 2 (bit 5 of address 0376_{16})" dose not work.

(3) MASK ROM version ONRY when IIC mode select bit (bit 0 of address 0377_{16}) and the internal/ external select bit (bit 3 of address 0378_{16}) are both set to "1". According to the datasheet, when IICM is set to "1", the port terminal is readable by the CPU even though "1" is assigned to $P7_1$ of the direction register. However, the CPU cannot read port $P7_1$ data if the $P7_1$ direction register is set to "1".

A-D Converter

(1) Write to each bit (except bit 6) of A-D control register 0, to each bit of A-D control register 1, and to bit 0 of A-D control register 2 when A-D conversion is stopped (before a trigger occurs).
In particular, when the Vref connection bit is changed from “0” to “1”, start A-D conversion after an elapse of 1 μs or longer.

(2) When changing A-D operation mode, select analog input pin again.

(3) Using one-shot mode or single sweep mode
Read the correspondence A-D register after confirming A-D conversion is finished. (It is known by A-D conversion interrupt request bit.)

(4) Using repeat mode, repeat sweep mode 0 or repeat sweep mode 1
Use the undivided main clock as the internal CPU clock.

Stop Mode and Wait Mode

(1) When returning from stop mode by hardware reset, $\overline{\text{RESET}}$ pin must be set to “L” level until main clock oscillation is stabilized.

(2) When switching to either wait mode or stop mode, instructions occupying four bytes either from the WAIT instruction or from the instruction that sets the every-clock stop bit to “1” within the instruction queue are prefetched and then the program stops. So put at least four NOPs in succession either to the WAIT instruction or to the instruction that sets the every-clock stop bit to “1”.

(3) When the MCU running in low-speed or low power dissipation mode, do not enter WAIT mode with peripheral function clock stop bit (CM02) set to "1".

Interrupts

(1) Reading address 00000_{16}

- When maskable interrupt is occurred, CPU read the interrupt information (the interrupt number and interrupt request level) in the interrupt sequence.
  The interrupt request bit of the certain interrupt written in address 00000_{16} will then be set to “0”.
  Reading address 00000_{16} by software sets enabled highest priority interrupt source request bit to “0”.
  Though the interrupt is generated, the interrupt routine may not be executed.
  Do not read address 00000_{16} by software.

(2) Setting the stack pointer

- The value of the stack pointer immediately after reset is initialized to 0000_{16}. Accepting an interrupt before setting a value in the stack pointer may become a factor of runaway. Be sure to set a value in the stack pointer before accepting an interrupt.
  When using the $\overline{\text{NMI}}$ interrupt, initialize the stack point at the beginning of a program. Concerning the first instruction immediately after reset, generating any interrupts including the $\overline{\text{NMI}}$ interrupt is prohibited.

(3) The $\overline{\text{NMI}}$ interrupt

- The $\overline{\text{NMI}}$ interrupt can not be disabled. Be sure to connect $\overline{\text{NMI}}$ pin to Vcc via a pull-up resistor if unused.
- Do not get either into stop mode with the $\overline{\text{NMI}}$ pin set to “L”.

(4) External interrupt

- When the polarity of the INT0 to INT5 pins is changed, the interrupt request bit is sometimes set to "1". After changing the polarity, set the interrupt request bit to "0".

(5) Rewrite the interrupt control register

• To rewrite the interrupt control register, do so at a point that does not generate the interrupt request for that register. If there is possibility of the interrupt request occur, rewrite the interrupt control register after the interrupt is disabled. The program examples are described as follow:

Example 1:

```
INT_SWITCH1:
    FCLR    I           ; Disable interrupts.
    AND.B   #00h, 0055h ; Clear TA0IC int. priority level and int. request bit.
    NOP                 ; Four NOP instructions are required when using HOLD function.
    NOP
    FSET    I           ; Enable interrupts.
```

Example 2:

```
INT_SWITCH2:
    FCLR    I           ; Disable interrupts.
    AND.B   #00h, 0055h ; Clear TA0IC int. priority level and int. request bit.
    MOV.W   MEM, R0     ; Dummy read.
    FSET    I           ; Enable interrupts.
```

Example 3:

```
INT_SWITCH3:
    PUSHC   FLG         ; Push Flag register onto stack
    FCLR    I           ; Disable interrupts.
    AND.B   #00h, 0055h ; Clear TA0IC int. priority level and int. request bit.
    POPC    FLG         ; Enable interrupts.
```

• When a instruction to rewrite the interrupt control register is executed but the interrupt is disabled, the interrupt request bit is not set sometimes even if the interrupt request for that register has been generated. This will depend on the instruction. If this creates problems, use the below instructions to change the register.
Instructions : AND, OR, BCLR, BSET

Table 1.21.1. Absolute maximum ratings

Symbol	Parameter		Condition	Rated value	Unit
V_{CC}	Supply voltage		V_{CC}=AVcc	– 0.3 to 6.5	V
AVcc	Analog supply voltage		V_{CC}=AVcc	– 0.3 to 6.5	V
V_I	Input voltage	$\overline{RESET}$, V_{REF}, X_{IN} $P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_5$, $P4_1$, $P4_2$, $P4_6$, $P4_7$, $P5_0$ to $P5_3$, $P5_6$, $P5_7$, $P6_0$ to $P6_3$, $P7_2$ to $P7_7$, $P8_0$ to $P8_2$, $P8_4$, $P8_6$, $P9_0$ to $P9_6$, $P10_0$ to $P10_3$, $P11_0$ to $P11_7$, $P12_0$ to $P12_5$, $P13_0$, $P13_1$ (Mask ROM version CNVss)		– 0.3 to Vcc+0.3	V
		VL1		– 0.3 to VL2	
		VL2		VL1 to VL3	
		VL3		VL2 to 6.5	
		$P7_0$, $P7_1$, C1, C2 (flash memory version CNVss)		– 0.3 to 6.5	
V_O	Output voltage	$P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_5$, $P4_1$, $P4_2$, $P4_6$, $P4_7$, $P5_0$ to $P5_3$, $P5_6$, $P5_7$, $P6_0$ to $P6_3$, $P7_2$ to $P7_6$, $P8_0$ to $P8_2$, $P8_4$, $P8_6$, $P9_0$ to $P9_6$, $P13_0$, $P13_1$, X_{OUT}		– 0.3 to Vcc+0.3	V
		$P0_0$ to $P0_7$, $P10_0$ to $P10_3$, $P11_0$ to $P11_7$, $P12_0$ to $P12_5$	When output port	– 0.3 to Vcc	
			When segment output	– 0.3 to VL3	
		$P7_0$, $P7_1$		– 0.3 to 6.5	
P_d	Power dissipation		Ta = 25°C	300	mW
T_{opr}	Operating ambient temperature			– 20 to 85	°C
T_{stg}	Storage temperature			– 40 to 150	°C

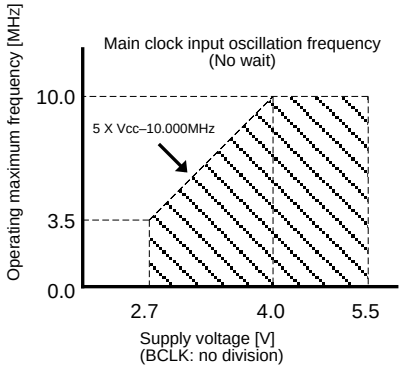
Table 1.21.2. Recommended operating conditions (referenced to Vcc = 2.7V to 5.5V at Ta = – 20 to 85°C unless otherwise specified)

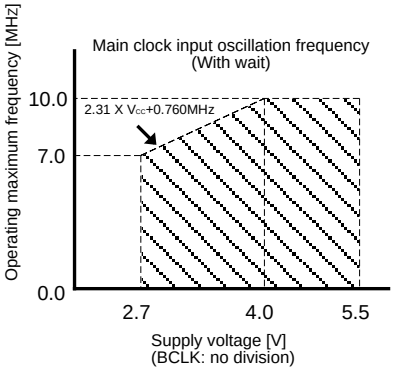
Symbol	Parameter			Standard			Unit
				Min.	Typ.	Max.	
Vcc	Supply voltage			2.7	5.0	5.5	V
AVcc	Analog supply voltage				Vcc		V
Vss	Analog supply voltage				0		V
AVss	Analog supply voltage				0		V
V_{IH}	HIGH input voltage	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_5$, $P4_1$, $P4_2$, $P4_6$, $P4_7$, $P5_0$ to $P5_3$, $P5_6$, $P5_7$, $P6_0$ to $P6_3$, $P7_2$ to $P7_7$, $P8_0$ to $P8_2$, $P8_4$, $P8_6$, $P9_0$ to P9₆, P10₀ to $P10_3$, $P11_0$ to $P11_7$, $P12_0$ to $P12_5$, $P13_0$, $P13_1$, XIN, RESET, CNVSS		0.8Vcc		Vcc	V
		$P7_0$, $P7_1$		0.8Vcc		6.5	
V_{IL}	LOW input voltage	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_5$, $P4_1$, $P4_2$, $P4_6$, $P4_7$, $P5_0$ to $P5_3$, $P5_6$, $P5_7$, $P6_0$ to $P6_3$, $P7_0$ to $P7_7$, $P8_0$ to $P8_2$, $P8_4$, $P8_6$, $P9_0$ to P9₆, P10₀ to $P10_3$, $P11_0$ to $P11_7$, $P12_0$ to $P12_5$, $P13_0$, $P13_1$, XIN, RESET, CNVSS		0		0.2Vcc	V
$I_{OH\ (peak)}$	HIGH peak output current (Note 2)	$P0_0$ to $P0_7$, P10₀ to $P10_3$, $P11_0$ to $P11_7$, $P12_0$ to $P12_5$				–0.5	mA
		$P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_5$, $P4_1$, $P4_2$, $P4_6$, $P4_7$, $P5_0$ to $P5_3$, $P5_6$, $P5_7$, $P6_0$ to $P6_3$, $P7_2$ to $P7_6$, $P8_0$ to $P8_2$, $P8_4$, $P8_6$, $P9_0$ to $P9_6$, $P13_0$, $P13_1$,				–10.0	
$I_{OH\ (avg)}$	HIGH average output current (Note 1)	$P0_0$ to $P0_7$, P10₀ to $P10_3$, $P11_0$ to $P11_7$, $P12_0$ to $P12_5$				–0.1	mA
		$P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_5$, $P4_1$, $P4_2$, $P4_6$, $P4_7$, $P5_0$ to $P5_3$, $P5_6$, $P5_7$, $P6_0$ to $P6_3$, $P7_2$ to $P7_6$, $P8_0$ to $P8_2$, $P8_4$, $P8_6$, $P9_0$ to $P9_6$, $P13_0$, $P13_1$,				–5.0	
$I_{OL\ (peak)}$	LOW peak output current (Note 2)	$P0_0$ to $P0_7$, P10₀ to $P10_3$, $P11_0$ to $P11_7$, $P12_0$ to $P12_5$				5.0	mA
		$P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_5$, $P4_1$, $P4_2$, $P4_6$, $P4_7$, $P5_0$ to $P5_3$, $P5_6$, $P5_7$, $P6_0$ to $P6_3$, $P7_0$ to $P7_6$, $P8_0$ to $P8_2$, $P8_4$, $P8_6$, $P9_0$ to $P9_6$, $P13_0$, $P13_1$,				10.0	
$I_{OL\ (avg)}$	LOW average output current (Note 1)	$P0_0$ to $P0_7$, P10₀ to $P10_3$, $P11_0$ to $P11_7$, $P12_0$ to $P12_5$				2.5	mA
		$P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_5$, $P4_1$, $P4_2$, $P4_6$, $P4_7$, $P5_0$ to $P5_3$, $P5_6$, $P5_7$, $P6_0$ to $P6_3$, $P7_0$ to $P7_6$, $P8_0$ to $P8_2$, $P8_4$, $P8_6$, $P9_0$ to $P9_6$, $P13_0$, $P13_1$,				5.0	
f (XIN)	Main clock input oscillation frequency (Note 3)	No wait	Vcc=4.0V to 5.5V	0		10	MHz
			Vcc=2.7V to 4.0V	0		5 x Vcc –10.000	MHz
		With wait	Vcc=4.0V to 5.5V	0		10	MHz
			Vcc=2.7V to 4.0V	0		2.31 x Vcc +0.760	MHz
f (XCIN)	Subclock oscillation frequency				32.768	50	kHz

Note 1: The mean output current is the mean value within 100ms.

Note 2: The total I_{OL} (peak) for ports P0, P1, P2, $P3_0$ to $P3_5$, P4, P5, P6, $P7_0$ to $P7_6$ and $P12_2$ to $P12_7$ must be 80mA max. The total I_{OH} (peak) for ports P0, P1, P2, $P3_0$ to $P3_5$, P4, P5, P6, $P7_2$ to $P7_6$ and $P12_2$ to $P12_7$ must be 80mA max. The total I_{OL} (peak) for ports P8, P9, P10, P11, $P12_0$, $P12_1$ and $P13_0$ to $P13_2$ must be 80mA max. The total I_{OH} (peak) for ports P8, P9, P10, P11, $P12_0$,$P12_1$ and $P13_0$ to $P13_2$ must be 80mA max.

Note 3: Relationship between main clock oscillation frequency and supply voltage.





Electric characteristics (V_{CC} = 5V)

V_{CC} = 5V

Table 1.21.3. Electrical characteristics (referenced to V_{CC} = 5V, V_{SS} = 0V at Ta = 25°C, f(X_{IN})=10MHz unless otherwise specified)

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	HIGH output voltage	$P0_0$ to $P0_7$, $P10_0$ to $P10_3$, $P11_0$ to $P11_7$, $P12_0$ to $P12_5$	I_{OH}= –0.1mA	3.0			V
V_{OH}	HIGH output voltage	$P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_5$, $P4_1$, $P4_2$, $P4_6$, $P4_7$, $P5_0$ to $P5_3$, $P5_6$, $P5_7$, $P6_0$ to $P6_3$, $P7_2$ to $P7_6$, $P8_0$ to $P8_2$, $P8_4$, $P8_6$, $P9_0$ to $P9_6$, $P13_0$, $P13_1$	I_{OH}= –5mA	3.0			V
			I_{OH}= –200µA	4.7			
V_{OH}	HIGH output voltage	X_{OUT} HIGHPOWER	I_{OH}= –1mA	3.0			V
		X_{OUT} LOWPOWER	I_{OH}= –0.5mA	3.0			
V_{OH}	HIGH output voltage	X_{COUT} HIGHPOWER	With no load applied		3.0		V
		X_{COUT} LOWPOWER	With no load applied		1.6		
V_{OL}	LOW output voltage	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_5$, $P4_1$, $P4_2$, $P4_6$, $P4_7$, $P5_0$ to $P5_3$, $P5_6$, $P5_7$, $P6_0$ to $P6_3$, $P7_0$ to $P7_6$, $P8_0$ to $P8_2$, $P8_4$, $P8_6$, $P9_0$ to $P9_6$, $P10_0$ to $P10_3$, $P11_0$ to $P11_7$, $P12_0$ to $P12_5$, $P13_0$, $P13_1$	I_{OL}=5mA			2.0	V
			I_{OL}=200µA			0.45	
V_{OL}	LOW output voltage	X_{OUT} HIGHPOWER	I_{OH}=1mA			2.0	V
		X_{OUT} LOWPOWER	I_{OH}=0.5mA			2.0	
V_{OL}	LOW output voltage	X_{COUT} HIGHPOWER	With no load applied		0		V
		X_{COUT} LOWPOWER	With no load applied		0		
V_{T+}-V_{T-}	Hysteresis	$\overline{TA0_{IN}}$, $\overline{TA3_{IN}}$, $\overline{TA4_{IN}}$, $\overline{TB0_{IN}}$ to $\overline{TB3_{IN}}$, $\overline{INT0}$ to $\overline{INT5}$, $\overline{ADTRG}$, $\overline{CTS0}$, CLK0, $\overline{NMI}$, $\overline{TA3_{OUT}}$, $\overline{TA4_{OUT}}$, $\overline{TA7_{OUT}}$, $\overline{KI0}$ to $\overline{KI15}$ (Note), $\overline{KI16}$ to $\overline{KI19}$		0.2		0.8	V
V_{T+}-V_{T-}	Hysteresis	$\overline{RESET}$		0.2		1.8	V
I_{IH}	HIGH input current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_5$, $P4_1$, $P4_2$, $P4_6$, $P4_7$, $P5_0$ to $P5_3$, $P5_6$, $P5_7$, $P6_0$ to $P6_3$, $P7_0$ to $P7_7$, $P8_0$ to $P8_2$, $P8_4$, $P8_6$, $P9_0$ to $P9_6$, $P10_0$ to $P10_3$, $P11_0$ to $P11_7$, $P12_0$ to $P12_5$, $P13_0$, $P13_1$, X_{IN}, $\overline{RESET}$, CNV_{SS}	V_I=5V			5.0	µA
I_{IL}	LOW input current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_5$, $P4_1$, $P4_2$, $P4_6$, $P4_7$, $P5_0$ to $P5_3$, $P5_6$, $P5_7$, $P6_0$ to $P6_3$, $P7_0$ to $P7_7$, $P8_0$ to $P8_2$, $P8_4$, $P8_6$, $P9_0$ to $P9_6$, $P10_0$ to $P10_3$, $P11_0$ to $P11_7$, $P12_0$ to $P12_5$, $P13_0$, $P13_1$, X_{IN}, $\overline{RESET}$, CNV_{SS}	V_I=0V			–5.0	µA
R_{PULLUP}	Pull-up resistance	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_5$, $P4_1$, $P4_2$, $P4_6$, $P4_7$, $P5_0$ to $P5_3$, $P5_6$, $P5_7$, $P6_0$ to $P6_3$, $P7_2$ to $P7_6$, $P8_0$ to $P8_2$, $P8_4$, $P8_6$, $P9_0$ to $P9_6$, $P10_0$ to $P10_3$, $P11_0$ to $P11_7$, $P12_0$ to $P12_5$, $P13_0$, $P13_1$,	V_I=0V	30.0	50.0	167.0	k
R_{fXIN}	Feedback resistance	X_{IN}			1.0		M
R_{fXCIN}	Feedback resistance	X_{CIN}			6.0		M
V_{RAM}	RAM retention voltage		When clock is stopped	2.0			V

Note : Has no effect during intermittent pullup operation.

Electric characteristics (VCC = 5V)

VCC = 5V

Table 1.21.4. Electrical characteristics (referenced to VCC = 5V, VSS = 0V at Ta = 25°C, f(XIN)=10MHz unless otherwise specified)

Symbol	Parameter		Measuring condition		Standard Min.	Standard Typ.	Standard Max.	Unit
Icc	Power supply current	I/o pin is no load applied		f(XIN)=10MHz Square wave, no division		19.0	38.0	mA
			Mask ROM version	f(XCIN)=32kHz Square wave		90.0		µA
			Flash memory version	f(XCIN)=32kHz Square wave		200.0		µA
				f(XCIN)=32kHz When a WAIT instruction is executed		4.0		µA
				When clock is stopped Ta=25 °C			1.0	µA
				When clock is stopped Ta=85 °C			20.0	
VL1	Supply voltage (VL1)		When voltage multiplier used		1.3	1.7	2.1	V
IL1	Power supply current (VL1)		VL1=1.7V,f(LCDCK)=200Hz			3.0	6.0	µA

Table 1.21.5. A-D conversion characteristics (referenced to VCC = AVCC = VREF = 5V, Vss = AVSS = 0V at Ta = 25°C, f(XIN) = 10MHz unless otherwise specified)

Symbol	Parameter		Measuring condition	Standard Min.	Standard Typ.	Standard Max.	Unit
–	Resolution		VREF =VCC			10	Bits
–	Absolute accuracy	Sample & hold function not available	VREF =VCC = 5V			±3	LSB
		Sample & hold function available(10bit)	VREF =VCC= 5V			±3	LSB
		Sample & hold function available(8bit)	VREF = VCC = 5V			±2	LSB
RLADDER	Ladder resistance		VREF =VCC	10		40	k
tCONV	Conversion time(10bit)			3.3			µs
tCONV	Conversion time(8bit)			2.8			µs
tSAMP	Sampling time			0.3			µs
VREF	Reference voltage			2		VCC	V
VIA	Analog input voltage			0		VREF	V

Table 1.21.6. D-A conversion characteristics (referenced to VCC = AVCC =VREF =5V, VSS = AVSS = 0V at Ta = 25°C, f(XIN) = 10MHz unless otherwise specified)

Symbol	Parameter	Measuring condition	Standard Min.	Standard Typ.	Standard Max.	Unit
–	Resolution				8	Bits
–	Absolute accuracy				1.0	%
tsu	Setup time				3	µs
RO	Output resistance		4	10	20	k
IVREF	Reference power supply input current	(Note)			1.5	mA

Note: This applies when using one D-A converter, with the D-A register for the unused D-A converter set to "0016".
The A-D converter's ladder resistance is not included.
Also, when the Vref is unconnected at the A-D control register, IVREF is sent.

Timing (V_{CC} = 5V)

V_{CC} = 5V

Timing requirements (referenced to V_{CC} = 5V, V_{SS} = 0V at Ta = 25°C unless otherwise specified)

Table 1.21.7. External clock input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	100		ns
$t_{w(H)}$	External clock input HIGH pulse width	40		ns
$t_{w(L)}$	External clock input LOW pulse width	40		ns
t_r	External clock rise time		15	ns
t_f	External clock fall time		15	ns

Table 1.21.8. Timer A input (counter input in event counter mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	100		ns
$t_{w(TAH)}$	TAi_{IN} input HIGH pulse width	40		ns
$t_{w(TAL)}$	TAi_{IN} input LOW pulse width	40		ns

Table 1.21.9. Timer A input (gating input in timer mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	400		ns
$t_{w(TAH)}$	TAi_{IN} input HIGH pulse width	200		ns
$t_{w(TAL)}$	TAi_{IN} input LOW pulse width	200		ns

Table 1.21.10. Timer A input (external trigger input in one-shot timer mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	200		ns
$t_{w(TAH)}$	TAi_{IN} input HIGH pulse width	100		ns
$t_{w(TAL)}$	TAi_{IN} input LOW pulse width	100		ns

Table 1.21.11. Timer A input (external trigger input in pulse width modulation mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAi_{IN} input HIGH pulse width	100		ns
$t_{w(TAL)}$	TAi_{IN} input LOW pulse width	100		ns

Table 1.21.12. Timer A input (up/down input in event counter mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAi_{OUT} input cycle time	2000		ns
$t_{w(UPH)}$	TAi_{OUT} input HIGH pulse width	1000		ns
$t_{w(UPL)}$	TAi_{OUT} input LOW pulse width	1000		ns
$t_{su(UP-TIN)}$	TAi_{OUT} input setup time	400		ns
$t_{h(TIN-UP)}$	TAi_{OUT} input hold time	400		ns

Timing (V_{CC} = 5V)

V_{CC} = 5V

Timing requirements (referenced to V_{CC} = 5V, V_{SS} = 0V at Ta = 25°C unless otherwise specified)

Table 1.21.13. Timer B input (counter input in event counter mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBi_{IN} input HIGH pulse width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBi_{IN} input LOW pulse width (counted on one edge)	40		ns
$t_{c(TB)}$	TBi_{IN} input cycle time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBi_{IN} input HIGH pulse width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBi_{IN} input LOW pulse width (counted on both edges)	80		ns

Table 1.21.14. Timer B input (pulse period measurement mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time	400		ns
$t_{w(TBH)}$	TBi_{IN} input HIGH pulse width	200		ns
$t_{w(TBL)}$	TBi_{IN} input LOW pulse width	200		ns

Table 1.21.15. Timer B input (pulse width measurement mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time	400		ns
$t_{w(TBH)}$	TBi_{IN} input HIGH pulse width	200		ns
$t_{w(TBL)}$	TBi_{IN} input LOW pulse width	200		ns

Table 1.21.16. A-D trigger input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{ADTRG}$ input cycle time (trigger able minimum)	1000		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ input LOW pulse width	125		ns

Table 1.21.17. Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200		ns
$t_{w(CKH)}$	CLKi input HIGH pulse width	100		ns
$t_{w(CKL)}$	CLKi input LOW pulse width	100		ns
$t_{d(C-Q)}$	TxDi output delay time		80	ns
$t_{h(C-Q)}$	TxDi hold time	0		ns
$t_{su(D-C)}$	RxDi input setup time	30		ns
$t_{h(C-D)}$	RxDi input hold time	90		ns

Table 1.21.18. External interrupt $\overline{INTi}$ inputs

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input HIGH pulse width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ input LOW pulse width	250		ns

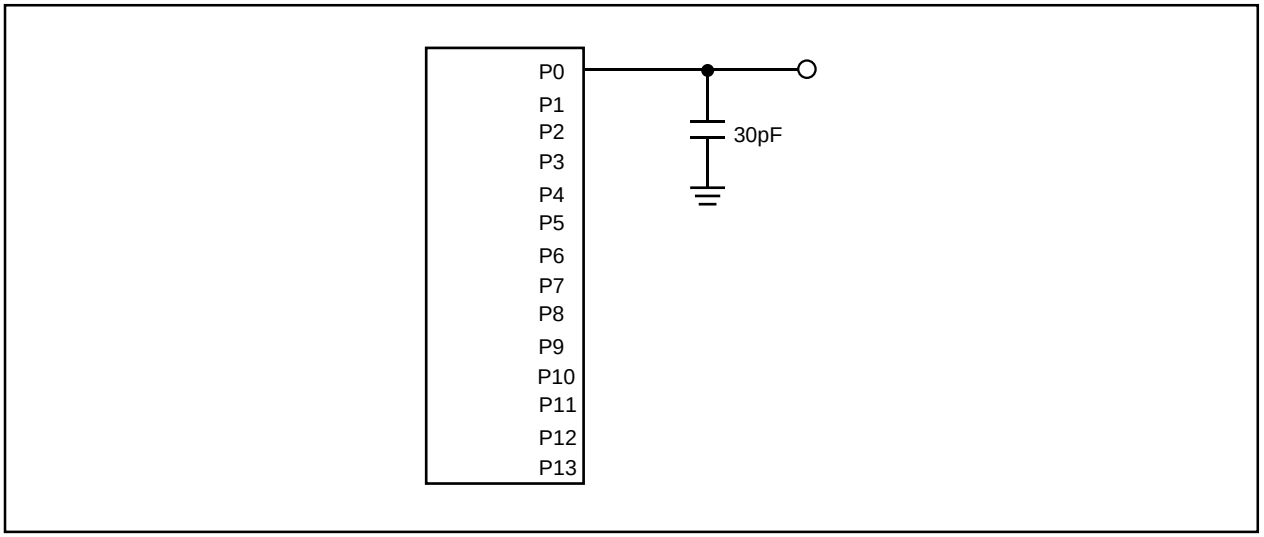
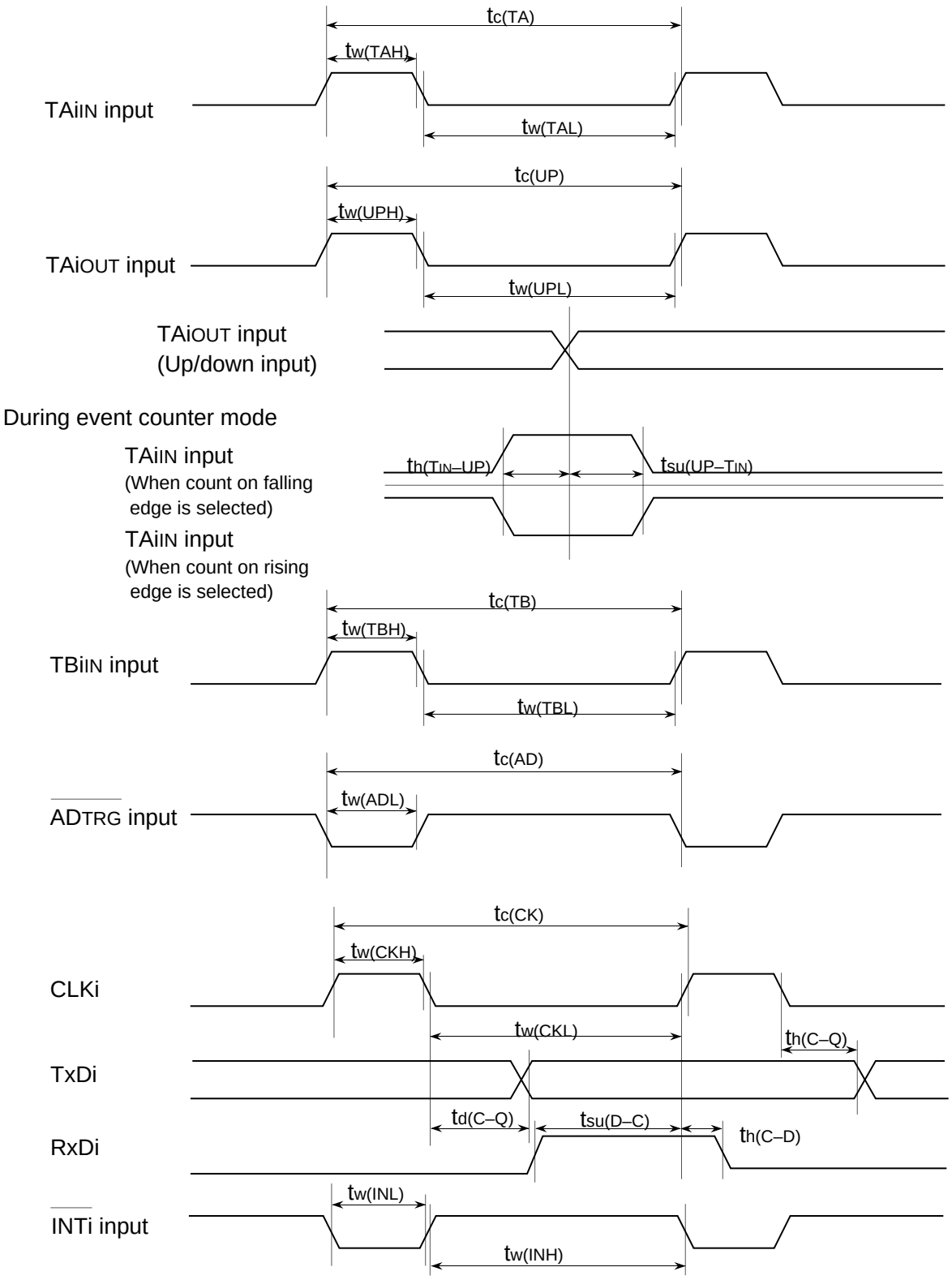


Figure 1.21.1. Port P0 to P13 measurement circuit

Timing (VCC = 5V)

VCC = 5V



Electric characteristics (V_{CC} = 3V)

V_{CC} = 3V

Table 1.21.19. Electrical characteristics (referenced to V_{CC} = 3V, V_{SS} = 0V at Ta = 25°C, f(X_{IN}) = 7MHz, with wait)

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	HIGH output voltage	$P0_0$ to $P0_7$, $P10_0$ to $P10_3$, $P11_0$ to $P11_7$, $P12_0$ to $P12_5$	I_{OH}= –20µA	2.0			V
V_{OH}	HIGH output voltage	$P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_5$, $P4_1$, $P4_2$, $P4_6$, $P4_7$, $P5_0$ to $P5_3$, $P5_6$, $P5_7$, $P6_0$ to $P6_3$, $P7_2$ to $P7_6$, $P8_0$ to $P8_2$, $P8_4$, $P8_6$, $P9_0$ to $P9_6$, $P13_0$, $P13_1$	I_{OH}= –1mA	2.5			V
V_{OH}	HIGH output voltage	X_{OUT} HIGHPOWER	I_{OH}= –0.1mA	2.5			V
		X_{OUT} LOWPOWER	I_{OH}= –50µA	2.5			
V_{OH}	HIGH output voltage	X_{COUT} HIGHPOWER	With no load applied		3.0		V
		X_{COUT} LOWPOWER	With no load applied		1.6		
V_{OL}	LOW output voltage	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_5$, $P4_1$, $P4_2$, $P4_6$, $P4_7$, $P5_0$ to $P5_3$, $P5_6$, $P5_7$, $P6_0$ to $P6_3$, $P7_0$ to $P7_6$, $P8_0$ to $P8_2$, $P8_4$, $P8_6$, $P9_0$ to $P9_6$, $P10_0$ to $P10_3$, $P11_0$ to $P11_7$, $P12_0$ to $P12_5$, $P13_0$, $P13_1$	I_{OL}=1mA			0.5	V
V_{OL}	LOW output voltage	X_{OUT} HIGHPOWER	I_{OH}=0.1mA			0.5	V
		X_{OUT} LOWPOWER	I_{OH}=50µA			0.5	
V_{OL}	LOW output voltage	X_{COUT} HIGHPOWER	With no load applied		0		V
		X_{COUT} LOWPOWER	With no load applied		0		
V_{T+}-V_{T-}	Hysteresis	$\overline{TA0_{IN}}$, $\overline{TA3_{IN}}$, $\overline{TA4_{IN}}$, $\overline{TB0_{IN}}$ to $\overline{TB3_{IN}}$, $\overline{INT_0}$ to $\overline{INT_5}$, $\overline{ADTRG}$, $\overline{CTS_0}$, CLK_0, $\overline{NMI}$, $\overline{TA3_{OUT}}$, $\overline{TA4_{OUT}}$, $\overline{TA7_{OUT}}$, $\overline{KI_0}$ to $\overline{KI_{15}}$ (Note), $\overline{KI_{16}}$ to $\overline{KI_{19}}$		0.2		0.8	V
V_{T+}-V_{T-}	Hysteresis	$\overline{RESET}$		0.2		1.8	V
I_{IH}	HIGH input current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_5$, $P4_1$, $P4_2$, $P4_6$, $P4_7$, $P5_0$ to $P5_3$, $P5_6$, $P5_7$, $P6_0$ to $P6_3$, $P7_0$ to $P7_7$, $P8_0$ to $P8_2$, $P8_4$, $P8_6$, $P9_0$ to $P9_6$, $P10_0$ to $P10_3$, $P11_0$ to $P11_7$, $P12_0$ to $P12_5$, $P13_0$, $P13_1$, X_{IN}, $\overline{RESET}$, CNV_{SS}	V_I=3V			4.0	µA
I_{IL}	LOW input current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_5$, $P4_1$, $P4_2$, $P4_6$, $P4_7$, $P5_0$ to $P5_3$, $P5_6$, $P5_7$, $P6_0$ to $P6_3$, $P7_0$ to $P7_7$, $P8_0$ to $P8_2$, $P8_4$, $P8_6$, $P9_0$ to $P9_6$, $P10_0$ to $P10_3$, $P11_0$ to $P11_7$, $P12_0$ to $P12_5$, $P13_0$, $P13_1$, X_{IN}, $\overline{RESET}$, CNV_{SS}	V_I=0V			–4.0	µA
R_{PULLUP}	Pull-up resistance	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_5$, $P4_1$, $P4_2$, $P4_6$, $P4_7$, $P5_0$ to $P5_3$, $P5_6$, $P5_7$, $P6_0$ to $P6_3$, $P7_2$ to $P7_6$, $P8_0$ to $P8_2$, $P8_4$, $P8_6$, $P9_0$ to $P9_6$, $P10_0$ to $P10_3$, $P11_0$ to $P11_7$, $P12_0$ to $P12_5$, $P13_0$, $P13_1$,	V_I=0V	66.0	120.0	500.0	k
R_{fXIN}	Feedback resistance	X_{IN}			3.0		M
R_{fXCIN}	Feedback resistance	X_{CIN}			10.0		M
V_{RAM}	RAM retention voltage		When clock is stopped	2.0			V

Note : Has no effect during intermittent pullup operation.

Electric characteristics (V_{CC} = 3V)

V_{CC} = 3V

Table 1.21.20. Electrical characteristics (referenced to V_{CC} = 3V, V_{SS} = 0V at Ta = 25°C, f(X_{IN}) = 7MHz, with wait)

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
Icc	Power supply current	I/o pin is no load applied		f(X_{IN})=7MHz Square wave, no division		6.0	15.0	mA
			Mask ROM version	f(X_{CIN})=32kHz Square wave		40.0		µA
			Flash memory version	f(X_{CIN})=32kHz Square wave		150.0		µA
				f(XCIN)=32kHz When a WAIT instruction is executed Oscillation capacity High (Note)		2.8		µA
				f(XCIN)=32kHz When a WAIT instruction is executed Oscillation capacity Low (Note)		0.9		µA
				When clock is stopped Ta=25 ºC			1.0	µA
				When clock is stopped Ta=85 ºC			20.0	
V_{L1}	Supply voltage (VL1)		When voltage multiplier used		1.3	1.7	2.1	V
I_{L1}	Power supply current (VL1)		VL1=1.7V,f($_{LCDCK}$)=200Hz			3.0	6.0	µA

Note: With one timer operated using f_{C32}.

Table 1.21.21. A-D conversion characteristics (referenced to V_{CC} = AV_{CC} = V_{REF} = 3V, V_{SS} = AV_{SS} = 0V at Ta = 25°C, f(X_{IN}) = 7MHz, with wait unless otherwise specified)

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		V_{REF} =V_{CC}			10	Bits
–	Absolute accuracy	Sample & hold function not available(8bit)	V_{REF} =V_{CC} = 3V, ϕ_{AD}=f_{AD}/2			±2	LSB
R_{LADDER}	Ladder resistance		V_{REF} =V_{CC}	10		40	k
t_{CONV}	Conversion time(8bit)			14.0			µs
V_{REF}	Reference voltage			2.7		V_{CC}	V
V_{IA}	Analog input voltage			0		V_{REF}	V

Table 1.21.22. D-A conversion characteristics (referenced to V_{CC} = AV_{CC}= V_{REF}= 3V, V_{SS} = AV_{SS} = 0V, at Ta = 25°C, f(X_{IN}) = 7MHz unless otherwise specified)

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy				1.0	%
t_{su}	Setup time				3	µs
R_O	Output resistance		4	10	20	k
I_{VREF}	Reference power supply input current	(Note)			1.0	mA

Note : This applies when using one D-A converter, with the D-A register for the unused D-A converter set to "00$_{16}$". The A-D converter's ladder resistance is not included.

Also, when the Vref is unconnected at the A-D control register, IV_{REF} is sent.

Timing (V_{CC} = 3V)

V_{CC} = 3V

Timing requirements (referenced to V_{CC} = 3V, V_{SS} = 0V at Ta = 25°C unless otherwise specified)

Table 1.21.23. External clock input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	143		ns
$t_{w(H)}$	External clock input HIGH pulse width	60		ns
$t_{w(L)}$	External clock input LOW pulse width	60		ns
t_r	External clock rise time		18	ns
t_f	External clock fall time		18	ns

Table 1.21.24. Timer A input (counter input in event counter mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	150		ns
$t_{w(TAH)}$	TAi_{IN} input HIGH pulse width	60		ns
$t_{w(TAL)}$	TAi_{IN} input LOW pulse width	60		ns

Table 1.21.25. Timer A input (gating input in timer mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	600		ns
$t_{w(TAH)}$	TAi_{IN} input HIGH pulse width	300		ns
$t_{w(TAL)}$	TAi_{IN} input LOW pulse width	300		ns

Table 1.21.26. Timer A input (external trigger input in one-shot timer mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	300		ns
$t_{w(TAH)}$	TAi_{IN} input HIGH pulse width	150		ns
$t_{w(TAL)}$	TAi_{IN} input LOW pulse width	150		ns

Table 1.21.27. Timer A input (external trigger input in pulse width modulation mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAi_{IN} input HIGH pulse width	150		ns
$t_{w(TAL)}$	TAi_{IN} input LOW pulse width	150		ns

Table 1.21.28. Timer A input (up/down input in event counter mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAi_{OUT} input cycle time	3000		ns
$t_{w(UPH)}$	TAi_{OUT} input HIGH pulse width	1500		ns
$t_{w(UPL)}$	TAi_{OUT} input LOW pulse width	1500		ns
$t_{su(UP-TIN)}$	TAi_{OUT} input setup time	600		ns
$t_{h(TIN-UP)}$	TAi_{OUT} input hold time	600		ns

Timing (V_{CC} = 3V)

V_{CC} = 3V

Timing requirements (referenced to V_{CC} = 3V, V_{SS} = 0V at Ta = 25°C unless otherwise specified)

Table 1.21.29. Timer B input (counter input in event counter mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time (counted on one edge)	150		ns
$t_{w(TBH)}$	TBi_{IN} input HIGH pulse width (counted on one edge)	60		ns
$t_{w(TBL)}$	TBi_{IN} input LOW pulse width (counted on one edge)	60		ns
$t_{c(TB)}$	TBi_{IN} input cycle time (counted on both edges)	300		ns
$t_{w(TBH)}$	TBi_{IN} input HIGH pulse width (counted on both edges)	160		ns
$t_{w(TBL)}$	TBi_{IN} input LOW pulse width (counted on both edges)	160		ns

Table 1.21.30. Timer B input (pulse period measurement mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time	600		ns
$t_{w(TBH)}$	TBi_{IN} input HIGH pulse width	300		ns
$t_{w(TBL)}$	TBi_{IN} input LOW pulse width	300		ns

Table 1.21.31. Timer B input (pulse width measurement mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time	600		ns
$t_{w(TBH)}$	TBi_{IN} input HIGH pulse width	300		ns
$t_{w(TBL)}$	TBi_{IN} input LOW pulse width	300		ns

Table 1.21.32. A-D trigger input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{AD_{TRG}}$ input cycle time (trigger able minimum)	1500		ns
$t_{w(ADL)}$	$\overline{AD_{TRG}}$ input LOW pulse width	200		ns

Table 1.21.33. Serial I/O

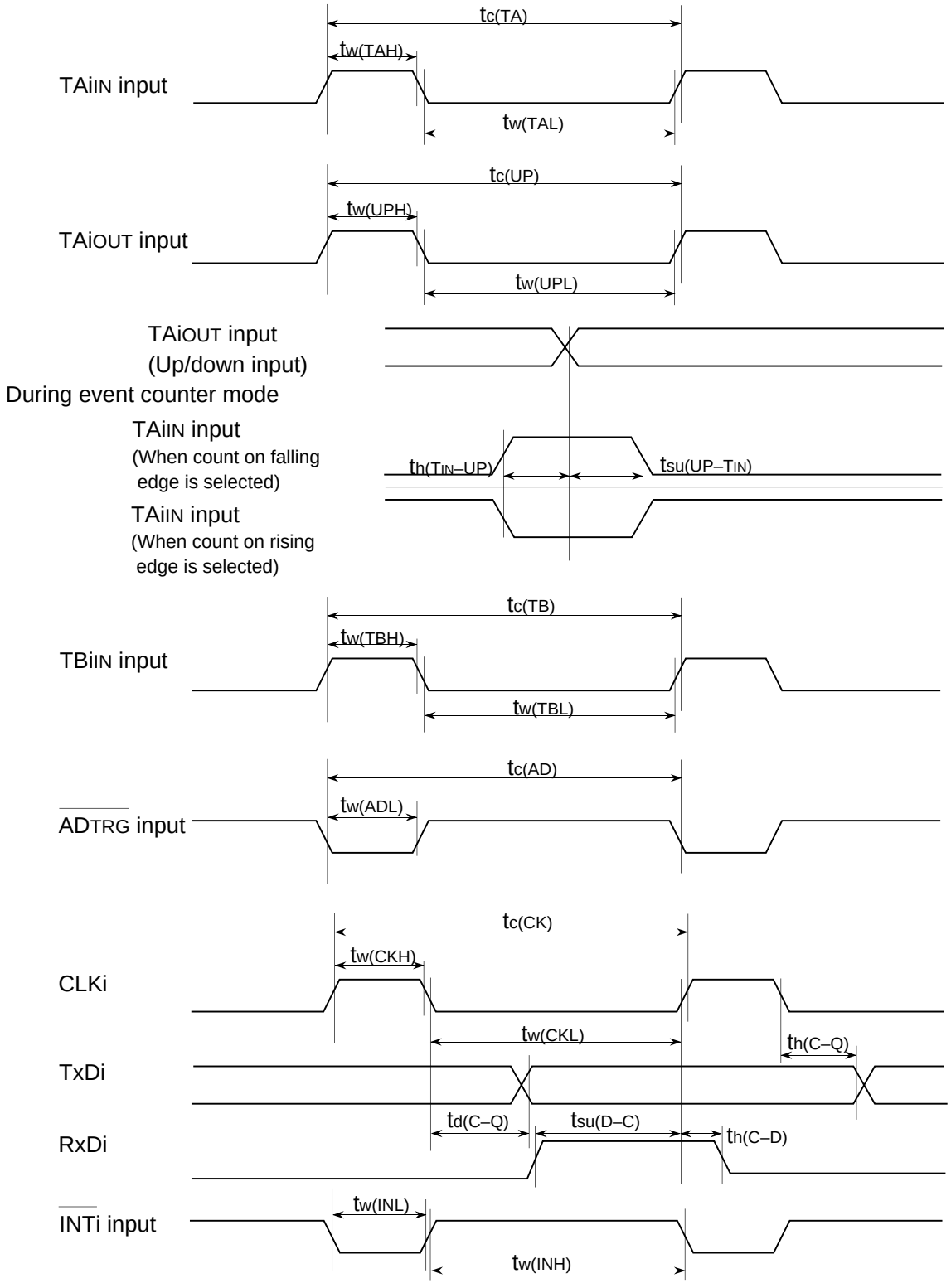
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300		ns
$t_{w(CKH)}$	CLKi input HIGH pulse width	150		ns
$t_{w(CKL)}$	CLKi input LOW pulse width	150		ns
$t_{d(C-Q)}$	TxDi output delay time		160	ns
$t_{h(C-Q)}$	TxDi hold time	0		ns
$t_{su(D-C)}$	RxDi input setup time	50		ns
$t_{h(C-D)}$	RxDi input hold time	90		ns

Table 1.21.34. External interrupt $\overline{INTi}$ inputs

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input HIGH pulse width	380		ns
$t_{w(INL)}$	$\overline{INTi}$ input LOW pulse width	380		ns

Timing (VCC = 3V)

VCC = 3V



Usage precaution against the differences between M30220 Group and M30221 Group

Differences between M30220 Group and M30221 Group

Items		M30220 Group			M30221 Group			
Internal Memory	ROM (Byte)	64K***	96K	128K**	24K	32K***	64K***	128K**
	RAM (Byte)	4K***	6K	10K**	1.5K	2K***	4K***	10K**
I/O Ports	Input only / Output only	Input only : 1 / Output only : 16 (shared with LCD outputs)			Input only : 1 / Output only : 14 (shared with LCD outputs)			
	CMOS I/O	102 (32 lines are shared with LCD outputs)			81 (26 lines are shared with LCD outputs)			
	N-channel open-drain	2						
DMAC (channels)		2						
16-bit timers		8+6						
CRC Operation Circuit		—						
Serial I/O	Clock Sync. / UART	3			2			
	Clock Synchronous	—						
	UART only	—						
A-D Converter (resolution × channels)		10bits×8			10bits×7			
D-A Converter (resolution × channels)		8bits×3			8bits×2			
External Interrupts (source)		8						
Watchdog Timer		Available						
LCD Controller / Driver	Segment (lines)	48			40			
	Common (lines)	4						
	Charge pump	Available						
Real Time Output Ports (bits × ports)		8×4			8×3, 6×1			
Key-on Wake up (lines)		Max.20 (16 lines have Intermittent pull-up operation)						
Sub Clock Generating Circuit		Available						
Packages		144-pin TQFP (144PFB-A) 144-pin LQFP (144P6Q-A)			120-pin LQFP (120P6R-A)			
Power Source Voltage (V)		2.7 to 5.5 (7MHz with 1wait)、 4.0 to 5.5 (10MHz)						
Operating Temperature Range (°C)		-20 to 85、-40 to 85						
Minimum Instruction Excution Time (ns)		100 (10MHz)						
Number of Basic Instructions		91						

★★：Under development ★★★：Under planning (April. 2001)

Deleted pins from M30220 Group

Port	Deleted pin name
P0	—
P1	—
P2	—
P3	—
P4	$P4_0/TA0_{OUT}$、$P4_3/TA1_{IN}$、$P4_4/TA2_{OUT}$、$P4_5/TA2_{IN}$
P5	$P5_4/TB4_{IN}$、$P5_5/TB5_{IN}$
P6	$P6_4/CTS_1/RTS_1/CLKS_1$、$P6_5/CLK_1$、$P6_6/RxD_1$、$P6_7/TxD_1$
P7	—
P8	$P8_3/TA5_{IN}$、$P8_5/TA6_{IN}$、$P8_7/TA7_{IN}$
P9	$P9_7/AN_7$
P10	$P10_4/SEG_{20}$、$P10_5/SEG_{21}$、$P10_6/SEG_{22}$、$P10_7/SEG_{23}$
P11	—
P12	$P12_6/SEG_{38}$、$P12_7/SEG_{39}$
P13	$P13_2/DA_2$
others	SEG_0、SEG_1、VSS(1 pin)

Usage precaution against timer A

Mode	Function	Not available timer Ai
Timer mode	Pulse output	Timer A0 and A2 are not available.
	Gate input	Timer A1 , A2 , and A5 to A7 are not available.
Event counter mode	Pulse output	Timer A0 and A2 are not available.
	Count source input	Timer A1 , A2 , and A5 to A7 are not available.
	Up / down count select input	Timer A0 and A2 are not available.
	Two-phase pulse input	Timer A2 and A7 are not available.(Note 1)
One-shot timer mode	Pulse output	Timer A0 and A2 are not available.
	Trigger input	Timer A1 , A2 , and A5 to A7 are not available.
Pulse width modulation mode		Timer A0 and A2 are not available.
	Trigger input	Timer A1 and A5 to A7 are not available.

Note 1. Timer A3 and A4 are available.

Usage precaution against timer B

Mode	Function	Not available timer Bi
Event counter mode	Count source input	Timer B4 and B5 are not available.
Pulse period / pulse width measurement mode		Timer B4 and B5 are not available.

Usage precaution against real time port outputs

(1) Pins $P12_6$ and $P12_7$ are deleted.

Usage precaution against serial I/O

(1) UART1 is not available.

Usage precaution against LCD controller / driver

(1) Pins SEG_0 , SEG_1 , SEG_{20} to SEG_{23} , SEG_{38} and SEG_{39} are deleted.

(2) Addresses of the designated RAM for the LCD display 0100_{16} , $010A_{16}$, $010B_{16}$ and 0113_{16} are reserved area.

(3) Bit 5 of the segment output enable register (address 0122_{16}) is reserved bit. Must always be clear to "0".

Usage precaution against A-D converter

(1) AN7 pin is deleted.

(2) Do not set the analog input pin select bit (bit 0 to 2 at address 03D616) to "111" in one-shot mode and in repeat mode.

(3) When the A-D sweep pin select bit (bit 0 , 1 at address 03D716) is set to "11" in single sweep mode , the interrupt request generation timing of the A-D conversion is the A-D conversion time of all 8 pins.

(4) The sweep time is the A-D conversion time of all 8 pins in repeat sweep mode 1 and when the A-D sweep pin select bit (bit 0 , 1 at address 03D716) is set to "11" in repeat sweep mode 0.

Usage precaution against D-A converter

(1) DA2 pin is deleted.

(2) Bit 2 of the D-A control register (address 03DC16) is reserved bit. Must always be clear to "0".

(3) Address 03DE16 must always be clear to "0016".

Usage precaution against programmable I/O

(1) Reserved bits of the port Pi direction register and the port Pi register

Register	Bit	Register	Bit
PD0、P0	—	PD7、P7	—
PD1、P1	—	PD8、P8	b3、b5、b7(Note 1)
PD2、P2	—	PD9、P9	b7(Note 1)
PD3、P3	—	PD10、P10	b4～b7(Note 1)
PD4、P4	b0、b3～b5(Note 1)	PD11、P11	—
PD5、P5	b4、b5(Note 1)	PD12、P12	b6、b7(Note 1)
PD6、P6	b4～b7(Note 1)	PD13、P13	b2(Note 1)

Note 1．These are reserved bits. Must always be clear to "0".

(2) Reserved bits of the pull-up control register

Bit 5 of the pull-up control register 1 (address 03FD16) and bit 5 of the pull-up control register 2 (address 03FE16) are reserved bits. Must always be clear to "0".

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